FS1525 µPOL™

DATASHEET

25A Stackable µPOL™ Regulator with Integrated Inductor and Digital Power System Management

Features

- µPOL™ package with output inductor included
- Small size: **6.80mm x 7.65mm x 3.82mm**
- Continuous 25A load capability
- Stackable up to **200A** (eight devices)
- Plug and play: no external compensation required
- True differential remote sensing
- Programmable operation using I^2C and PMBus™
- Wide input voltage range: 4.5V–16V
- Adjustable output voltage up to 1.8V
- Enabled input, programmable under-voltage lock-out (UVLO) circuit
- Open-drain power-good indicator
- Built-in protection features
- Operating junction temperature from -40°C to +125°C
- Lead-free and halogen-free
- Compliant with EU Directives REACH and RoHS 6

Applications

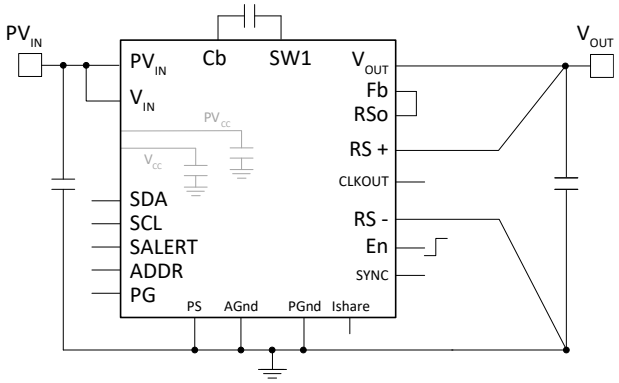
- Telecom and networking applications
- Data center applications
- Storage applications
- Industrial applications
- Distributed point-of-load power architectures
- Computing peripheral voltage regulation

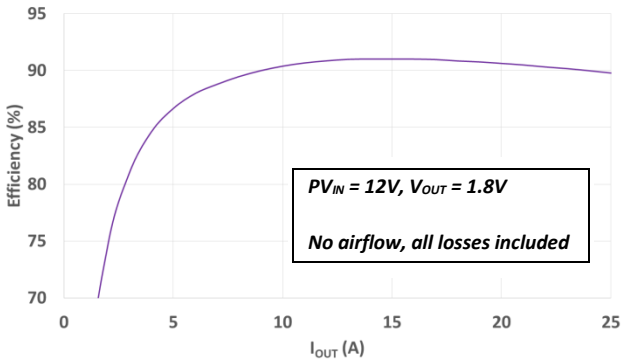
Description

The FS1525 is an easy-to-use, fully integrated and highly efficient micro-point-of-load (µPOL™) voltage regulator. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

Developed by a cross-functional engineering team, the design exemplifies best practice and uses class-leading technologies. From early in the integrated circuit design phase, designers worked with application and packaging engineers to select compatible technologies and implement them in ways that reduce compromise. The ability to program aspects of the FS1525's operation using the I^2C and PMBus™ protocols is unique in this class of product. Developing and optimizing all these elements together has yielded the smallest, most efficient and fully featured 25A to 200A µPOL™ currently available.

The built-in protection features include pre-biased start-up, soft-start protection, over-voltage protection, thermally compensated over-current protection with hiccup mode, thermal shut-down with auto-recovery.





Pin Configuration

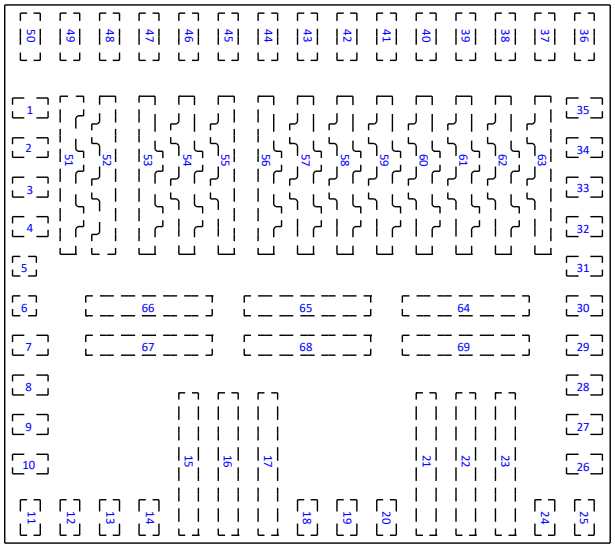


Figure 1 Pin layout (top view)

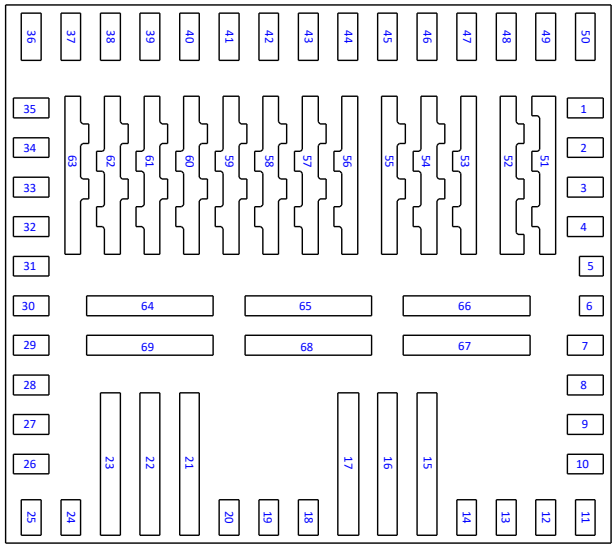


Figure 2 Pin layout (bottom view)

Pin Functions

Pin Numbers	Pin Name	Pin Description
44	NC	Test pin for Sync FET of phase 2.
8	V_{IN}	Input supply to the internal LDO. Connect to PV_{IN} through a 2.7Ω resistor OR to V_{CC} when external 5V (Figure 6) is used to supply V_{CC} (recommended for best performance).
25	En	Enable pin to turn the device ON and OFF. It can be used to set an external UVLO by using two external resistors.
9	PV_{CC}	Input supply for the drivers. Connect to V_{CC} on the application board.
10	V_{CC}	Input bias for an external V_{CC} voltage / Output of the internal LDO. Connect to V_{IN} when using external 5V supply (recommended for best performance).
13	V_{FB}	Feedback voltage to the device. Connect to V_{OUT} on the application board if remote sensing is not used, or to RSo if remote sensing is used.
64–69	AGnd	Signal ground for the internal reference and control circuitry. Connect to power ground plane through vias.
21, 22, 23	V_{OUT1}	Power output from regulator. V_{OUT1} and V_{OUT2} should be shorted by V_{OUT} plane on PCB. Place output capacitors between V_{OUT} and PGnd.
15, 16, 17	V_{OUT2}	Power output from regulator. V_{OUT1} and V_{OUT2} should be shorted by V_{OUT} plane on PCB. Place output capacitors between V_{OUT} and PGnd.
30	PG	Power Good status pin. Output is an open drain. Connect a pull-up resistor (4.99kΩ) between this pin and V_{CC} or to an external bias voltage.

Pin Numbers	Pin Name	Pin Description
12	ADDR	Program device address by connecting a resistor from this pin to ground; up to 16 address offsets may be programmed (see page 19).
5	Boot1	Boot pin for phase 1 driver.
6	Boot2	Boot pin for phase 2 driver.
7	SYNC	Synchronizes device with external clock. If not used, it is recommended to ground this pin.
29	Clkout	Phase shifted clock out. Connect to sync of next slave in daisy chain.
27	SDA	I^2C /PMBus™ Data Serial Input/Output line. Pull up to bus voltage with 4.99kΩ resistor.
26	SCL	I^2C /PMBus™ Clock line. Pull up to bus voltage with 4.99kΩ resistor.
28	ALERT	SMBAlert# line. Pull up to bus voltage with 4.99kΩ resistor.
36–43	SW1	Drain of Sync FET of phase 1. External fly capacitors (2 x 4.7µF) should be connected between this pin and Cb.
31-35, 56–63	PGnd	Power Ground. Serves as a separate ground for the MOSFETs and should be connected to the system's power ground plane.
45-50, 53, 54, 55	Cb	Connection for external fly capacitors (2 X 4.7µF). The capacitor connects between this pin and V_{SW1} and should be connected as close as possible to these pins.
18	RS+	Input of differential remote sense amplifier. Connect to V_{OUT}.
19	RS-	Input of differential remote sense amplifier. Connect to remote or local ground.
14	RSo	Output of remote sensing amplifier.
11	PS	Phase setting pin. Connect resistor to AGnd to set Master/Slave, as well as number of devices in parallel to determine relative phasing (see page 21).
24	Fault#	Tied together with Fault pins of other paralleled devices to share fault information. Pull up to V_{CC} or 5V supply with a 4.99kΩ resistor. Active low.
20	Ishare	Current share. The Ishare pins of all paralleled devices need to be tied together.
1–4, 51, 52	PV_{IN}	Input supply for the power MOSFETs.

Block Diagram

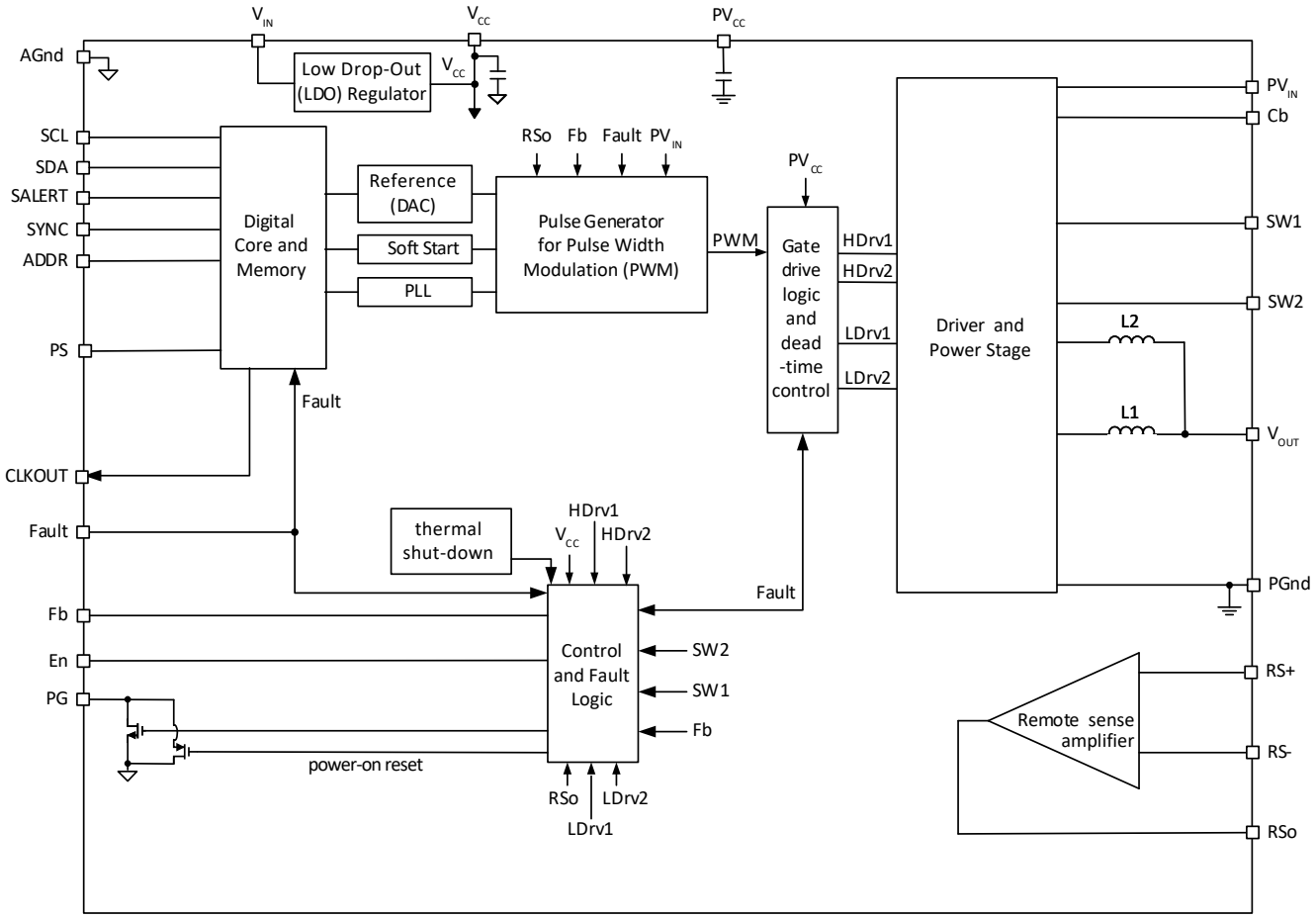


Figure 3 FS1525 µPOL™

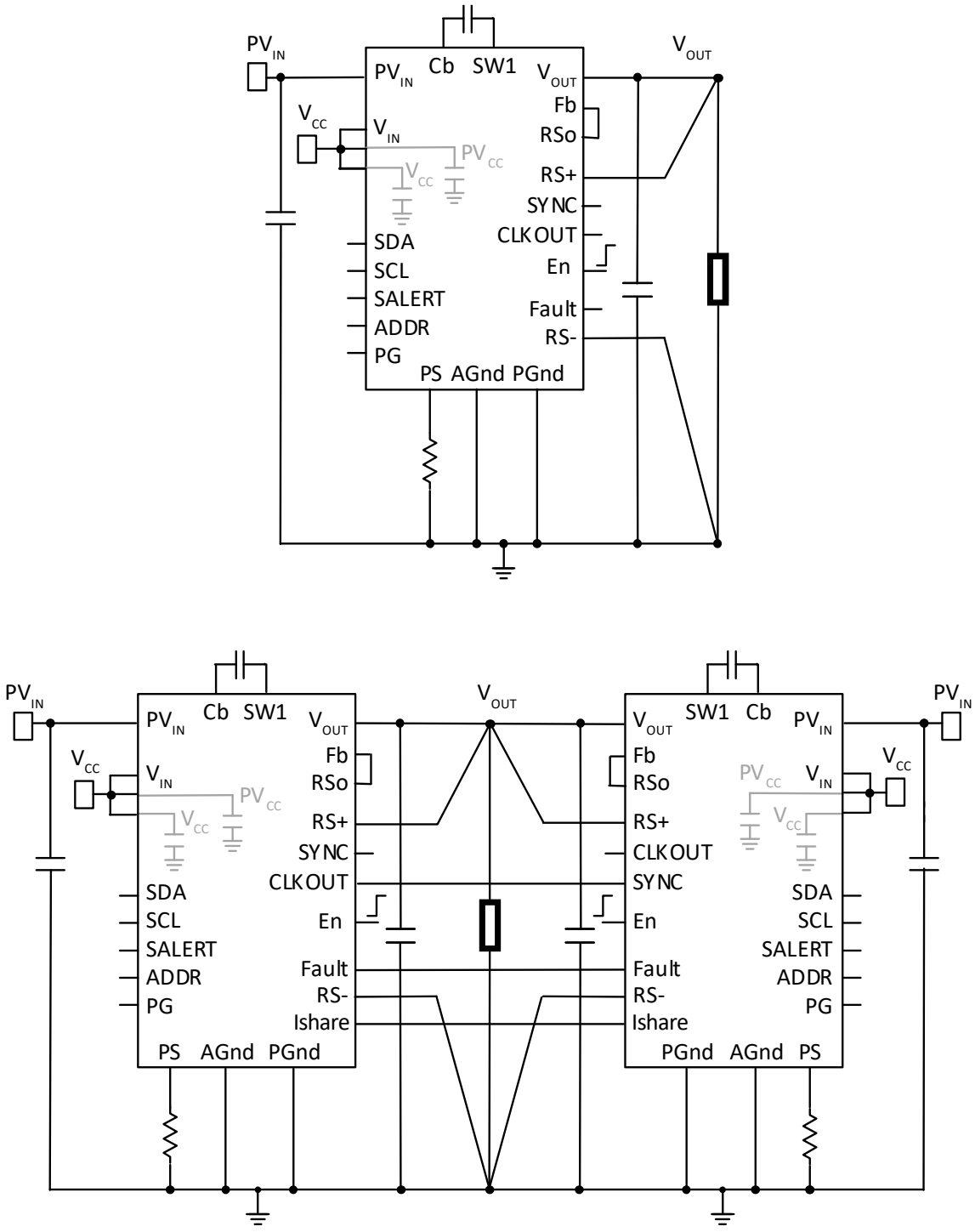


Figure 4 ***Applications circuits for single-phase and two-phase configuration***

Note: The Fault pin needs to be pulled up to 5V through 4.99kΩ resistor for both single- and multi-phase applications.

Absolute Maximum Ratings

Warning: Stresses beyond those shown may cause permanent damage to the FS1525.

Note: Functional operation of the FS1525 is not implied under these or any other conditions beyond those stated in the FS1525 specification.

Reference	Range
PV_{IN}, V_{IN}, En to PGnd, Cb to SW1	-0.3V to 18V
V_{CC} to PGnd (Note 1)	-0.3V to 6V
SW1, SW2	-0.3V to 15V
Fb and other I/Os to AGnd (Note1)	-0.3V to V_{CC}
PG to AGnd (Note 1)	-0.3V to V_{CC}
PGnd to AGnd	-0.3V to +0.3V
ESD Classification (HBM JESD22-A114)	1.5kV
Moisture Sensitivity Level	MSL 3 (per JEDEC J-STD-020D)

Thermal Information	Range
Junction-to-Ambient Thermal Resistance Θ_{JA}	10.5°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$	1.4°C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C
Note: Θ_{JA} : FS1525 evaluation board and JEDEC specifications JESD 51-2A $\Theta_{J\text{-}c\ (bottom)}$: JEDEC specification JESD 51-8	

Order Information

Package Details

The FS1525 uses a µPOL™ 6.80mm x 7.65mm package delivered in tape-and-reel format, with 1250 devices on a reel.

Standard Part Number

V_{OUT}	Part number
0.60	FS1525-0600-AL

Recommended Operating Conditions

Definition	Symbol	Min	Max	Units
Input Voltage Range with External V_{CC} (Note 3, Note 5)	PV_{IN}	6*V_{OUT}	16	V
Input Voltage Range with Internal LDO (Note 4, Note 5)	PV_{IN}, V_{IN}	6*V_{OUT}	16	
Supply Voltage Range (Note 2)	V_{CC}	4.5	5.5	
Output Voltage Range	V_{OUT}	0.6	1.8	
Continuous Output Current Range	I_O	0	25	A
Operating Junction Temperature	T_J	-40	125	°C

Electrical Characteristics

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 6*V_{OUT} <PV_{IN} <16V, 4.5V < V_{IN} < 16V, 0°C < T < 125°C **Typical values are specified at T_A = 25°C**						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Supply Current						
V_{IN} Supply Current (Standby)	$I_{IN\ (STANDBY)}$	Enable low	7	8.2	9.5	mA
V_{IN} Supply Current (Static)	$I_{IN\ (STATIC)}$	No switching, En = 2V	8.8	10.5	12.2	
V_{IN} Supply Current (Dynamic)	$I_{IN\ (DYN)}$	En high, V_{IN} = 12V, F_{SW} =625kHz, Vcc=PVcc	45.5	50	54.5	
Soft-Start						
Soft-Start time	T_{ON_RISE}	Default (Note 7), V_{OUT} = 0.6V	2.3	3	3.7	ms
Output Voltage						
Output Voltage Range	V_{OUT} (default)			0.6		V
	range		0.6		1.8	V
	Resolution			5		mV
Accuracy		T_J = 25°C, V_{OUT} = 0.6V (Note 8)		±0.7		%
		-40°C ≤ T_J ≤ 105°C, V_{OUT} = 0.6V (Note 6, 8)	-1.5		1.5	
		T_J = 25°C, 0.7V ≤ V_{OUT} ≤ 1.8V (Note 7, 8)	-1		1	
On-Time Timer Control						
On-Time	T_{ON}	V_{IN} = 12V, V_{OUT} = 0.6V, F_{SW} = 625kHz	155	180	205	ns
Minimum On-Time	$T_{ON(MIN)}$	(Note 7)		50		
Minimum Off-Time	$T_{OFF(MIN)}$	T_J = 25°C, F_{SW} = 625kHz, V_{IN} = V_{CC} = PV_{CC} = 4.5V PV_{IN} = 6V	395	430	465	
Internal Low Drop-Out (LDO) Regulator						
LDO Regulator Output Voltage	V_{CC}	5.5V ≤ V_{IN} = 16V, 0 – 75mA	4.9	5.2	5.5	V
		4.5V ≤ V_{IN} < 5.5V, 0 – 55mA	4			
Line Regulation	V_{LN}	5.5V < V_{IN} = 16V, 0 – 75mA	0	40	110	mV

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 6*V_{OUT} <PV_{IN} <16V, 4.5V < V_{IN} < 16V, 0°C < T < 125°C Typical values are specified at T_A = 25°C						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Load Regulation	V_{LD}	0 – 75mA	0	110	140	
Short Circuit Current	I_{SHORT}	(Note 7)	130	151	172	mA
Thermal Shut-Down						
Thermal Shut-Down	Default			145		°C
Hysteresis				25		
Under-Voltage Lock-Out						
V_{CC} Start Threshold	V_{CC}_$UVLO_{(START)}$	V_{CC} Rising Trip Level	4.0	4.2	4.4	V
V_{CC} Stop Threshold	V_{CC}_$UVLO_{(STOP)}$	V_{CC} Falling Trip Level	3.6	3.8	4.1	
Enable Threshold	$En_{(HIGH)}$	Ramping Up	1.14	1.20	1.36	
	$En_{(LOW)}$	Ramping Down	0.90	1.00	1.06	
Input Impedance	R_{EN}		500	1000	1500	kΩ
Current Limit						
Current Limit Threshold	I_{OC} (default)	T_J = 25°C, V_{OUT} = 0.6V	30.5	33	35.5	A
Hiccup Blanking Time	$T_{BLK(HICCUP)}$			20		ms
Over-Voltage Protection						
Output Over-Voltage Protection Threshold	V_{OVP} (default)	OVP Detect (Note 7)	110	120	130	Fb%
Output Over-voltage Protection Delay	T_{OVPDEL}			5		µs
Remote Sense Differential Amplifier						
Differential Gain	Adiff			1		V/V
Input Offset Voltage	V_{OS}	RSo=0.6V, No Load		0		mV
Output Source Current	I_{SRC}	RS+ = 2.3V, RS- = 0V, RSo = 1.8V		5.5		mA
Output Sink Current	I_{SNK}	RS+ = 0V, RS- = 0.5V, RSo = 0.5V		0.55		mA
Power Good (PG)						
Power Good Upper Threshold	$V_{PG(UPPER)}$ (default)	V_{OUT} Rising	75	85	95	Fb%
Power Good Hysteresis	$V_{PG(LOWER)}$	V_{OUT} Falling		5		
Power Good Sink Current	I_{PG}	PG = 0.6V, En = 2V	6.6	8.8	11	mA
Telemetry						
Input voltage reporting accuracy	PV_{IN}_report_pc	PV_{IN}=12V, T_J = 25°C	-0.8		0.8	%
		PV_{IN} =12V, -40°C ≤T_J ≤125°C (Note 6)	-1		1	
Output voltage reporting accuracy	V_{OUT}_report_pc	V_{OUT} = V_{FB} = 0.6V, T_J = 25°C	-2.5		2.5	%
		V_{OUT} = V_{FB} = 0.6V, -40°C ≤T_J ≤125°C (Note 6)	-3.2		3.2	
		0.7 ≤ V_{OUT} =V_{FB} ≤1.8V, T_J = 25°C (Note 7)	-2		2	
		0.7 ≤ V_{OUT} =V_{FB} ≤1.8V, -40°C ≤T_J ≤125°C (Note 6)	-2.5		2.5	
Output current reporting accuracy	I_{OUT}_report_acc	PV_{IN} = 12V, T_J = 25°C, V_{OUT} = 0.6V, I_{OUT} = 0A	0		2	A

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 6*V_{OUT} <PV_{IN} <16V, 4.5V < V_{IN} < 16V, 0°C < T < 125°C **Typical values are specified at T_A = 25°C**						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
		PV_{IN} = 12V, -40°C ≤T_J ≤125°C, V_{OUT} = 0.6V, I_{OUT} = 0A (Note 6)	0		2.5	
Temperature reporting accuracy	T_report_acc	-40°C ≤ T_J ≤125°C (Note 7)	-10		10	°C

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: 6*V_{OUT} < PV_{IN} = V_{IN} < 16V, 0°C < T < 125°C **Typical values are specified at T_A = 25°C**							
Parameter	**Symbol**	**Conditions**	**Fast-mode**		**Fast-mode Plus**		**Unit**
I^2C parameters		**(Note 7 for all parameters)**	**Min**	**Max**	**Min**	**Max**	
I^2C bus voltage	V_{BUS}		1.8	5.5	1.8	5.5	V
LOW-level input voltage	V_{IL}		−0.5	0.3V_{BUS}	−0.5	0.3V_{BUS}	
HIGH-level input voltage	V_{IH}		0.7V_{BUS}		0.7V_{BUS}		
Hysteresis	V_{HYS}		0.05V_{BUS}		0.05V_{BUS}		
LOW-level output voltage 1	V_{OL1}	(open-drain or open-collector) at 3mA sink current; V_{DD} > 2V	0	0.4	0	0.4	
LOW-level output voltage 2	V_{OL2}	(open-drain or open-collector) at 2mA sink current; V_{DD} ≤ 2V	0	0.2V_{BUS}	0	0.2V_{BUS}	
LOW-level output current	I_{OL}	V_{OL} = 0.4V	3	-	3	-	mA
		V_{OL} = 0.6V	6	-	6	-	
Output fall time	T_{OF}	From V_{IHmin} to V_{ILmax}	20 × (V_{BUS}/5.5V)	250	20 × (V_{BUS}/5.5V)	125	ns
Pulse width of spikes that must be suppressed by the input filter	T_{SP}		0	50	0	50	
Input current each I/O pin	I_I		−10	10	−10	10	µA
Capacitance for each I/O pin	C_I		-	10	-	10	pF
SCL clock frequency	F_{SCL}		0	400	0	1000	kHz
Hold time (repeated) START condition	$T_{HD;STA}$	After this time, the first clock pulse is generated	0.6	-	0.26	-	µs
LOW period of the SCL clock	T_{LOW}		1.3	-	0.5	-	
HIGH period of the SCL clock	T_{HIGH}		0.6	-	0.26	-	
Set-up time for a repeated START condition	$T_{SU;STA}$		0.6	-	0.26	-	
Data hold time	$T_{HD;DAT}$	I^2C-bus devices	0	-	0	-	
Data set-up time	$T_{SU;DAT}$		100	-	50	-	ns
Rise time of SDA and SCL signals	T_R		20	300	-	120	
Fall time of SDA and SCL signals	T_F		20 × (V_{CC}/5.5V)	300	20 × (V_{CC}/5.5V)	120	

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: 6*V_{OUT} < PV_{IN} = V_{IN} < 16V, 0°C < T < 125°C Typical values are specified at T_A = 25°C							
Parameter	**Symbol**	**Conditions**	**Fast-mode**		**Fast-mode Plus**		**Unit**
I^2C parameters		**(Note 7 for all parameters)**	**Min**	**Max**	**Min**	**Max**	
Set-up time for STOP condition	$T_{SU;STO}$		0.6	-	0.26	-	µs
Bus free time between a STOP and START condition	T_{BUF}		1.3	-	0.5	-	
Capacitive load for each bus line	C_B		-	400	-	550	pF
Data valid time	$T_{VD;DAT}$		-	0.9	-	0.45	µs
Data valid acknowledge time	$T_{VD;ACK}$		-	0.9	-	0.45	
Noise margin at the LOW level	V_{NL}	For each connected device, including hysteresis	0.1V_{CC}	-	0.1V_{CC}	-	V
Noise margin at the HIGH level	V_{NH}		0.2V_{CC}	-	0.2V_{CC}	-	
SDA timeout	T_{TO}		200		200		µs

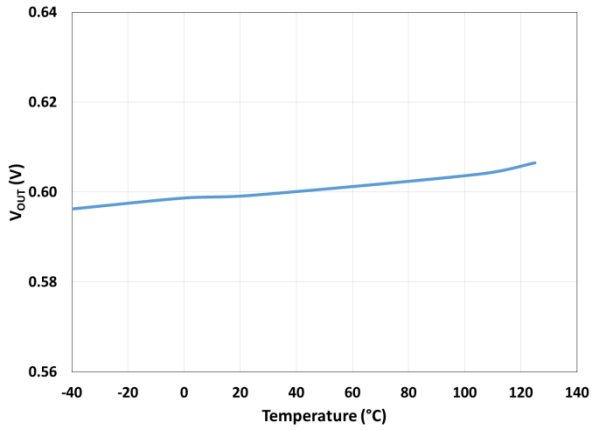
For supported PMBus™ commands, see page 40.

Notes

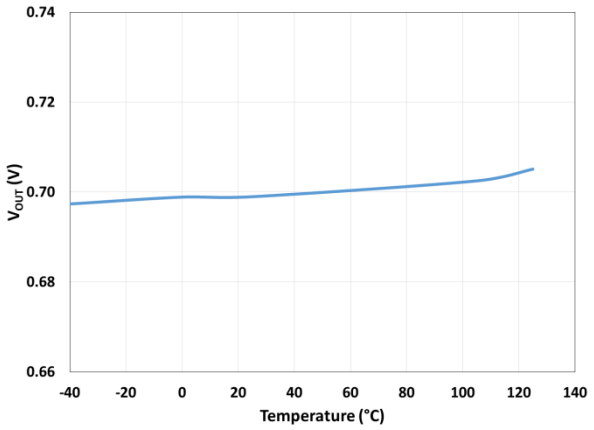
1 PGnd pin and AGnd pin are connected together
2 Must not exceed 6V
3 V_{IN} is connected to V_{CC} to bypass the internal Low Drop-Out (LDO) regulator
4 V_{IN} is connected to PV_{IN} (for single-rail applications with PV_{IN}=V_{IN}=4.5V-16V)
5 Maximum switch node voltage should not exceed 15V
6 Performance over temperature guaranteed by correlation using statistical quality control but not tested in production
7 Guaranteed by design but not tested in production
8 Closed loop V_{OUT} measurement that includes all tolerances (reference, offsets, remote sense, switching ripple)

Temperature Characteristics

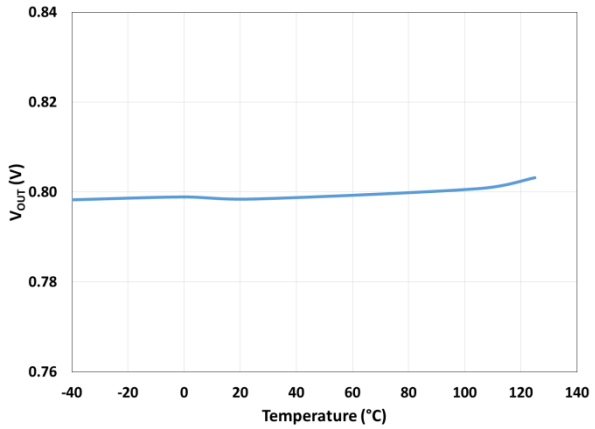
Output Voltage: 0.6V



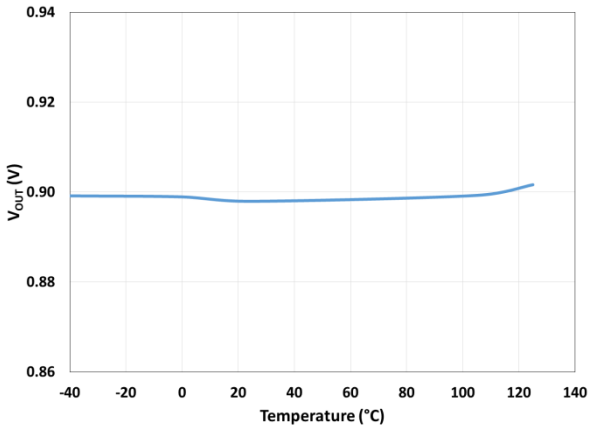
Output Voltage: 0.7V



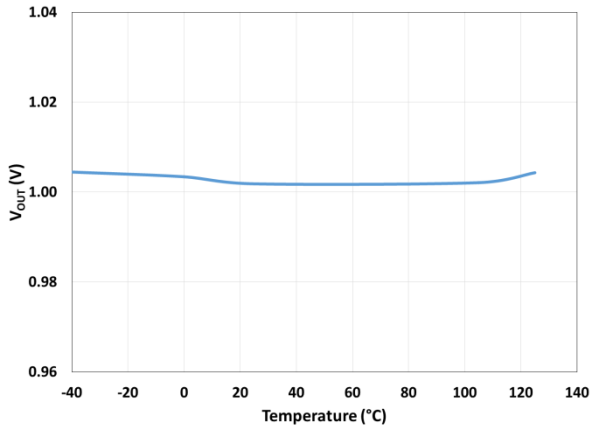
Output Voltage: 0.8V



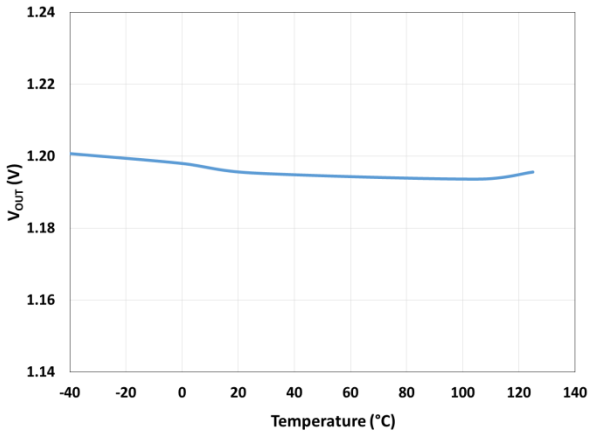
Output Voltage: 0.9V



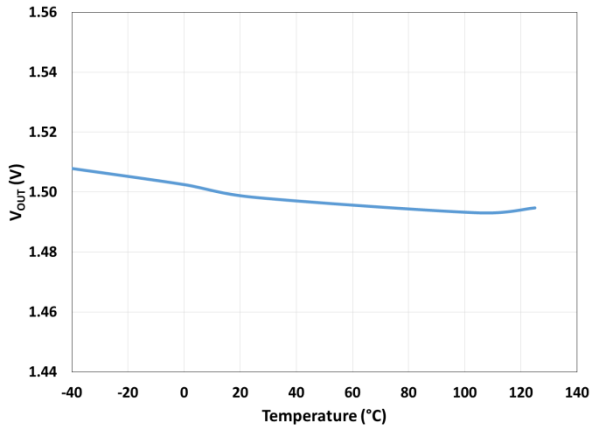
Output Voltage: 1.0V



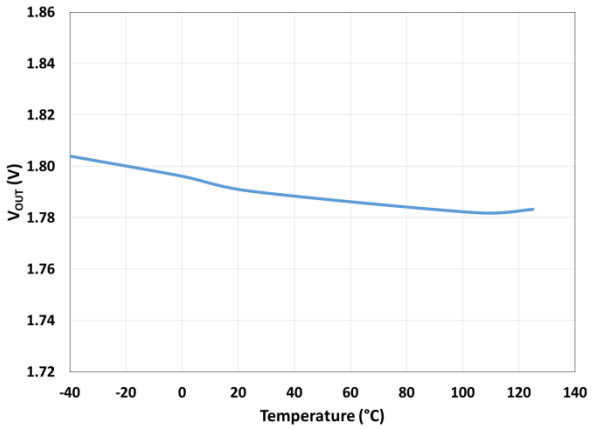
Output Voltage: 1.2V



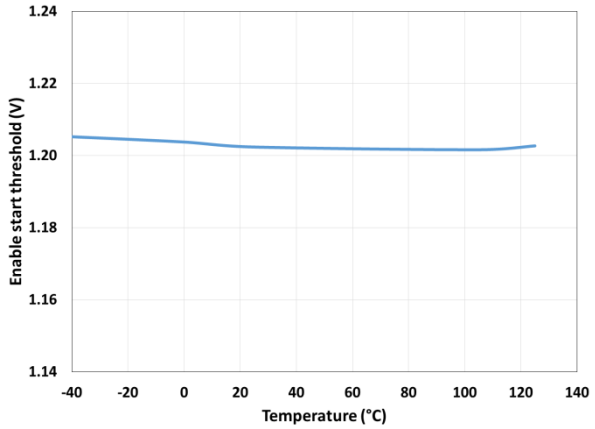
Output Voltage: 1.5V



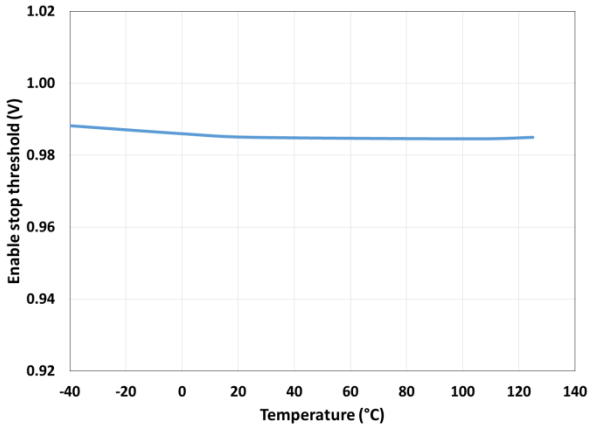
Output Voltage: 1.8V



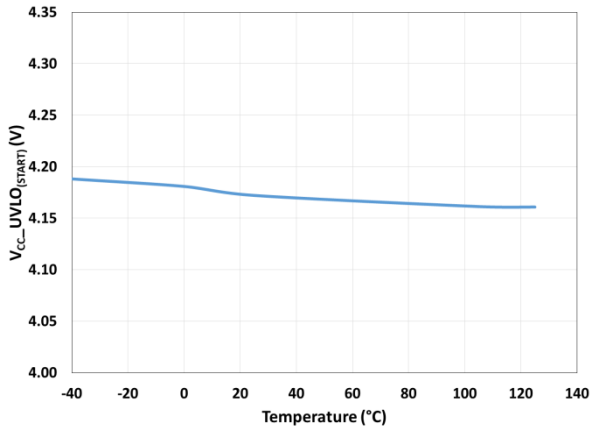
Enable Start Threshold



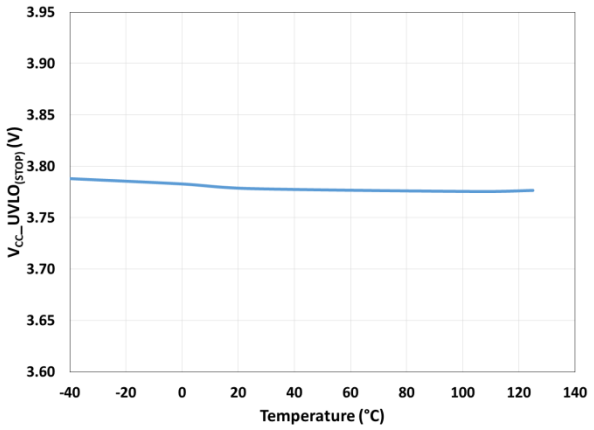
Enable Stop Threshold



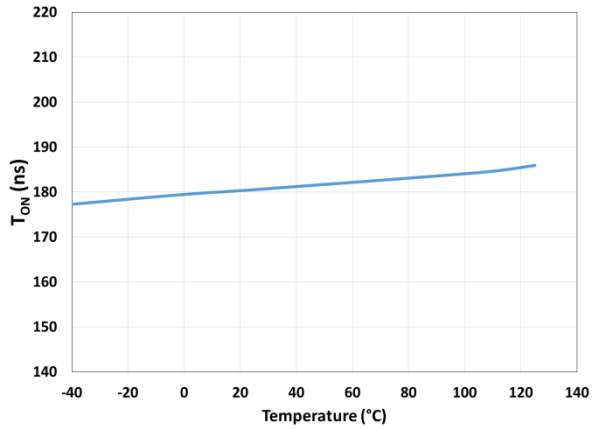
V_{CC} Start Threshold



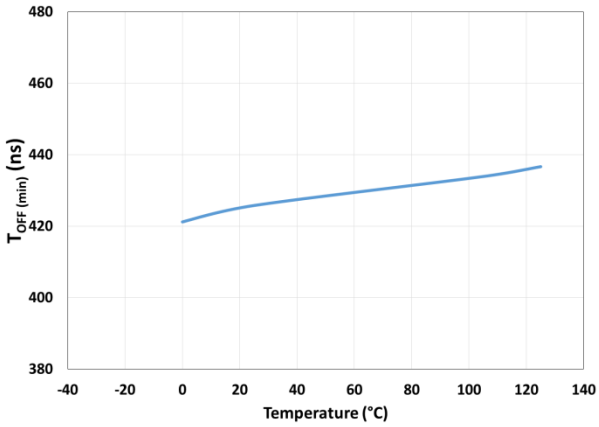
V_{CC} Stop Threshold



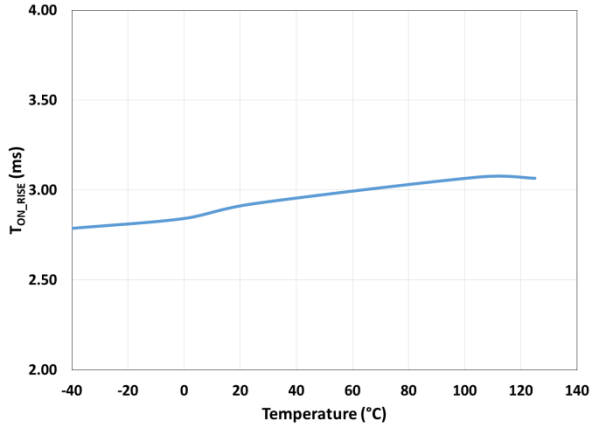
On Time



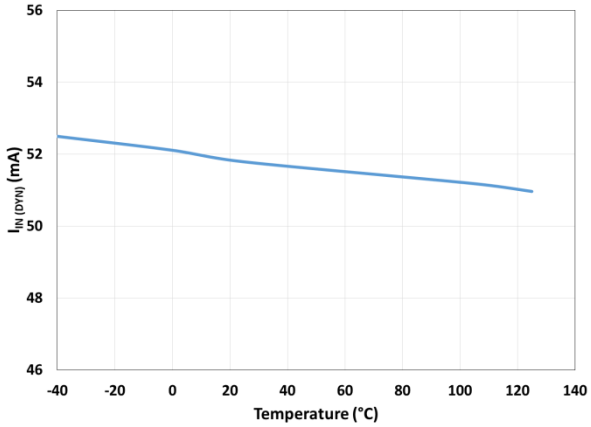
Off Time



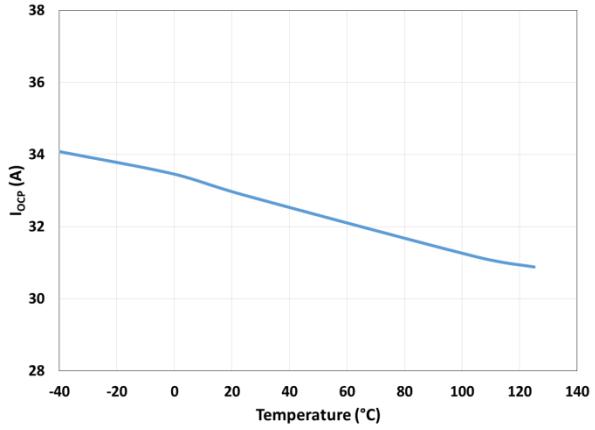
Soft-Start Time



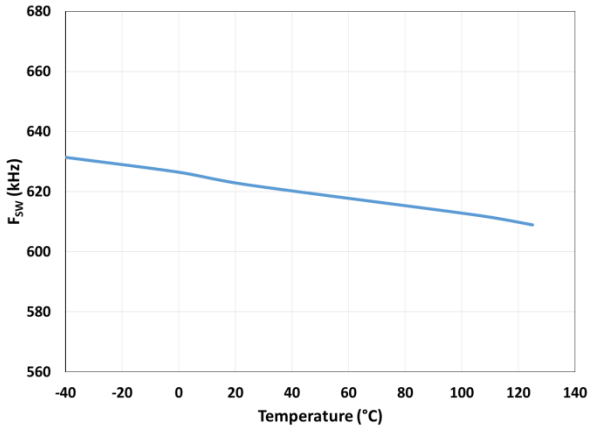
V_{IN} Supply Current (Dynamic)



Over-Current Protection



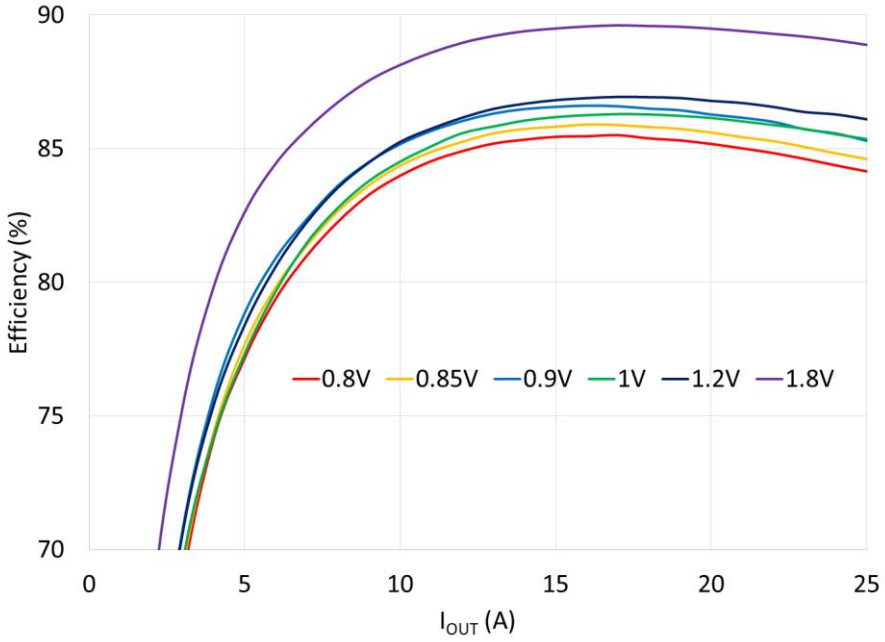
Switching Frequency

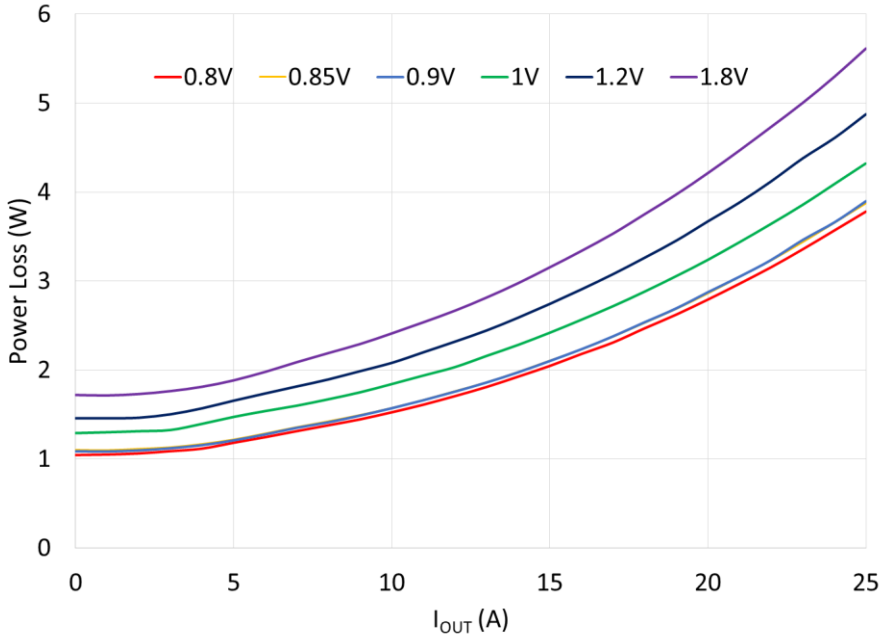


Efficiency Characteristics

Typical efficiency and power loss at PV_{IN} = 12V

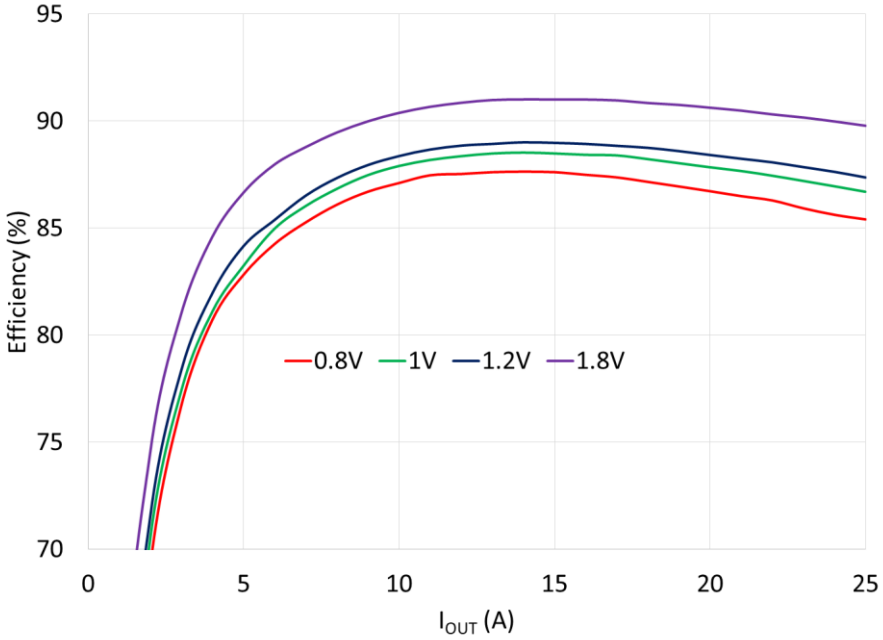
PV_{IN} = 12V, internal LDO used, I_{OUT} = 0A–25A, room temperature, no air flow, all losses included

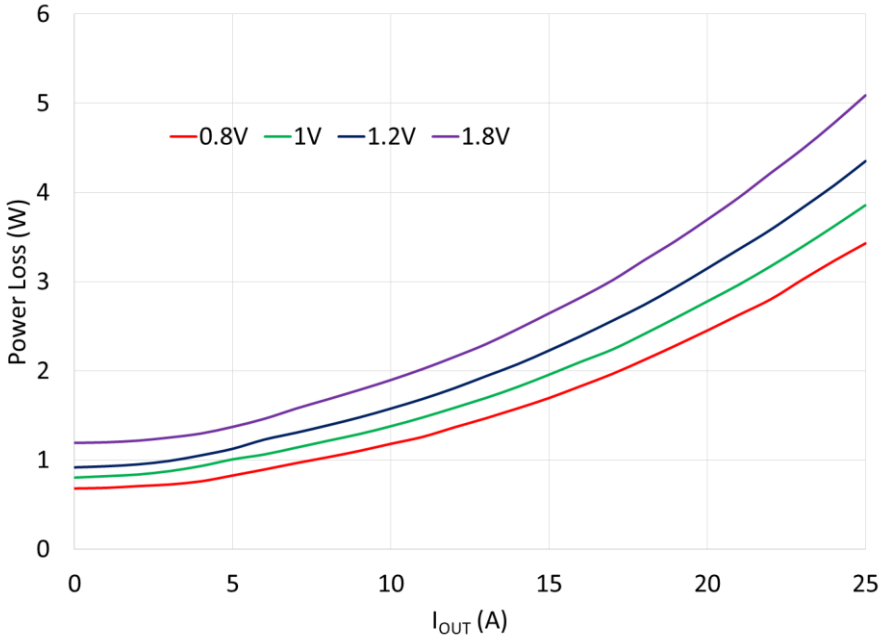




Typical efficiency and power loss at PV_{IN} = 12V

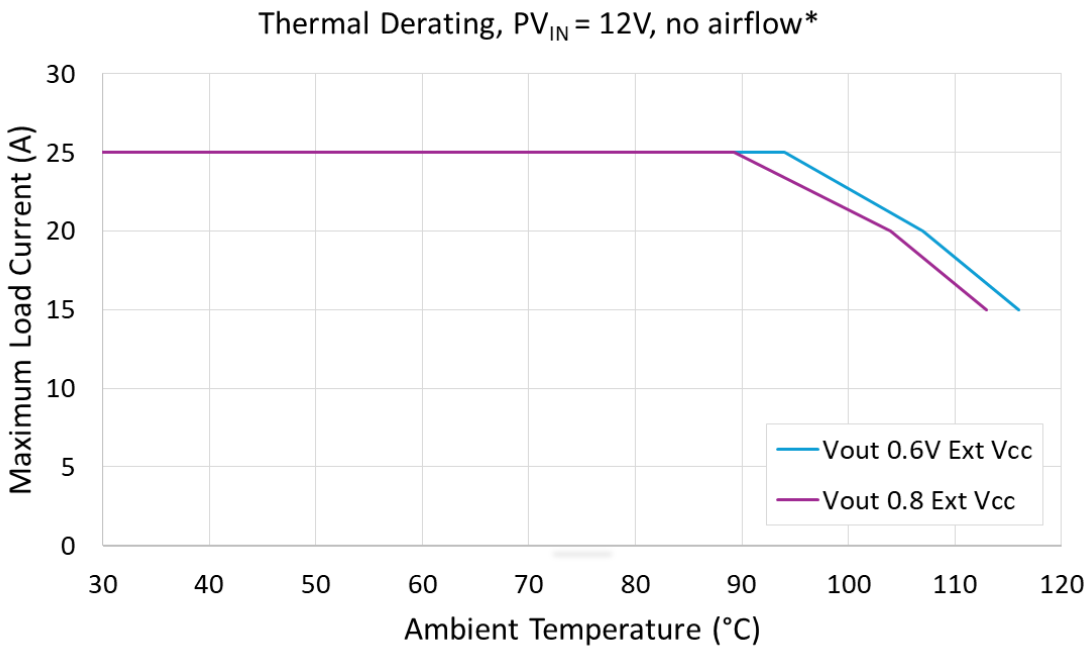
PV_{IN} = 12V, external V_{CC} =5V, I_{OUT} = 0A–25A, room temperature, no air flow, all losses included





Thermal Derating Curve

PV_{IN} = 12V, no airflow, with external V_{CC} = 5V, on FS1525 standard evaluation board



Applications Information

Overview

The FS1525 is an easy-to-use, fully integrated and highly efficient DC/DC regulator. Aspects of its operation, including output voltage and system optimization parameters, can be programmed using the I²C/PMBus™ protocol. It uses a proprietary modulator to deliver fast transient responses. The modulator has internal stability compensation so that it can be used in a wide range of applications, with various types of output capacitors, without loop stability issues.

The FS1525 is a versatile device offering great flexibility for configuration and system monitoring using the I²C/PMBus™ interface. It allows standalone operation without any digital interface by making it easy for the designer to configure output voltages using simple resistor divider changes and to monitor the system using the Power Good output.

Operation And Topology

The FS1525 uses a modified interleaved buck converter topology, employing a coupling capacitor (Cb) in the power path. These modifications reduce voltage stresses on the internal power devices, resulting in smaller size and switching losses comparable to an equivalently rated conventional interleaved buck converter. Other advantages include a higher on-time (2x) compared to an equivalent voltage conversion ratio in a conventional buck converter, and a natural current-sharing mechanism between the two phases provided by the coupling capacitor.

Bias Voltage

The FS1525 has an integrated Low Drop-Out (LDO) regulator providing the DC bias voltage for the internal circuitry. The typical LDO regulator output voltage is 5.2V. For internally biased single-rail operation, the V_{IN} pin should be connected to the PV_{IN} pin (Figure 5). If an external bias voltage is used, the V_{IN} pin should be connected to the V_{CC} pin to bypass the internal LDO regulator (Figure 6). There is a separate pin to provide bias for the drivers (PV_{CC}); this should be connected to V_{CC} in the application circuit. It is recommended that V_{IN} should have a minimum slew rate of 0.06V/ms. Note that PV_{IN} has internal undervoltage detection that latches the device if PV_{IN} drops below 4.2V.

The supply voltage (internal or external) rises with V_{IN} and does not need to be enabled using the En pin. Consequently, I²C/PMBus™ communication can begin as soon as:

- V_{CC}_UVLO start threshold is exceeded
- Memory contents are loaded
- Initialization is complete
- Address offset is read

The I²C bus may be pulled up either to V_{CC} or to a system I²C bus voltage. The FS1525 offers two ranges for the I²C bus voltage, defined by the user register bit **Bus_voltage_sel**.

Register	Bits	Name/Description
0x91	[2]	**Bus_voltage_sel** 0:1.8–2.5V, 1: 3.3–5V

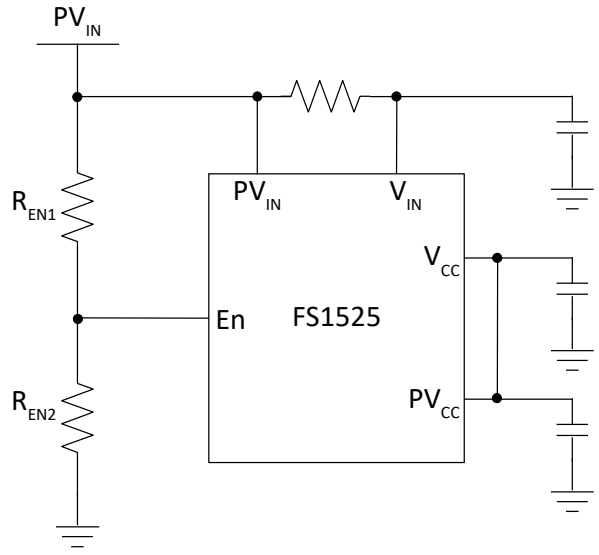


Figure 5 Single supply configuration: internal LDO regulator, adjustable PV_{IN}_UVLO

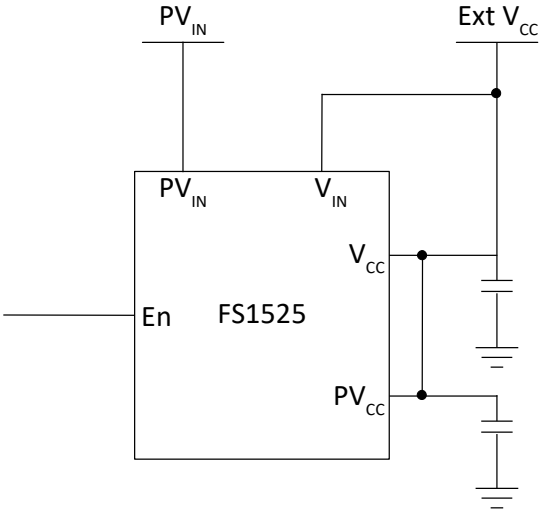


Figure 6 Using an external bias voltage

I²C Base Address and Offsets

The FS1525 has user registers to set its I²C base address and PMBus™ base address. The default I²C base address is 0x10, and the default PMBus™ base address is 0x70. An offset of 0–15 is then defined by connecting the ADDR pin to the AGnd pin, either directly or through a resistor. An address detector reads the resistance of the connection at startup and uses it to set the offset, which is added to the base I²C address to set the address at which the I²C master device will communicate with the FS1525. The same offset is added to the base PMBus™ address to determine the PMBus™ address at which PMBus™ communication will be established.

To select offsets of 0–15, connect the pins as follows:

- **0** – 0Ω (short ADDR to AGnd)
- **+1** – 1.13kΩ
- **+2** – 1.87kΩ
- **+3** – 2.61kΩ
- **+4** – 3.4kΩ
- **+5** – 4.12kΩ
- **+6** – 4.87kΩ
- **+7** – 5.62kΩ
- **+8** – 6.34kΩ
- **+9** – 7.15kΩ
- **+10** – 7.87kΩ
- **+11** – 8.66kΩ
- **+12** – 9.31kΩ
- **+13** – 10.2kΩ
- **+14** – 11kΩ
- **+15** – 12.1kΩ

Note: Do not use the 7-bit address 0x0C; this corresponds to the Alert Response Address in the SMBus™ protocol.

Soft-Start and Target Output Voltage

The FS1525 has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When V_{CC} exceeds its start threshold (V_{CC}_UVLO$_{(START)}$), the FS1525 exits reset mode. This initiates loading of the contents of the non-volatile memory into the working registers and calculates the address offset as described above.

Once initialization is complete, the internal soft start begins to ramp towards the set reference voltage at a rate determined by the TON_RISE registers (corresponding to the TON_RISE command), provided these conditions are met:

a) A valid enable signal is recognized (as defined by the Enable pin, Operation register, ON_OFF_CONFIG register, input voltage PV_{IN}, and PV_{IN} UVLO threshold corresponding to the VIN_ON and VIN_OFF registers).

b) The flying capacitor Cb has been charged to $PV_{IN}/2$ by the internal pre-charge circuit. This is necessary to ensure that when the device starts to switch, it does so with balanced $PV_{IN}/2$ voltages across all FETs.

During initial start-up, the FS1525 operates with a minimum of high-drive (HDrv) pulses until the output voltage increases (see Minimum Values for On-time, Off-time on page 22). On-time is increased until V_{OUT} reaches the target value defined by the VOUT_COMMAND registers. For proper start-up operation of the FS1525, fitting a 100Ω resistor in parallel with the output capacitors (C_{OUT}) is recommended (not mandatory).

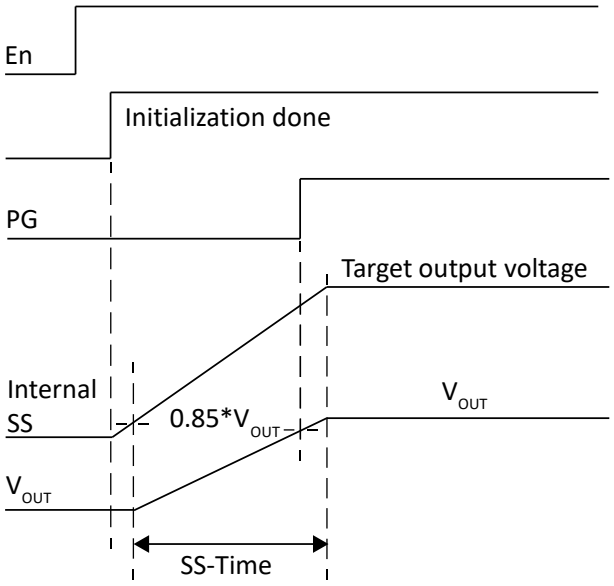


Figure 7 Theoretical operational waveforms during soft-start

Over-current protection (OCP) and over-voltage protection (OVP) are enabled during soft-start to protect the FS1525 from short circuits and excess voltages respectively.

A resistor divider may be used with a standard FS1525-0600 device to set the desired output voltage (Figure 8). This gives system designers the flexibility to design all the power rails in the system across the entire output voltage range (0.6–1.8V) using a single part.

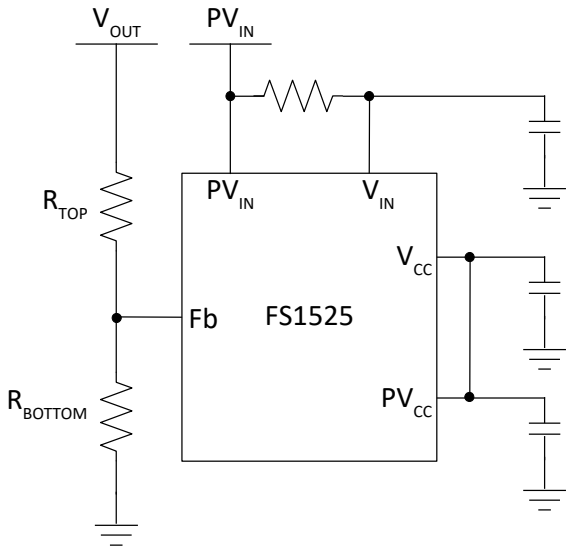


Figure 8 Setting the output voltage with an external resistor divider

The following equation may be used to set the output voltage, where R_{TOP} and R_{BOTTOM} are in kΩ:

$$R_{\text{bottom}} = \frac{R_{\text{top}}}{\left(\frac{V_{\text{out}}}{V_{\text{FB}}} - 1 - \frac{R_{\text{top}}}{47.5}\right)}$$

Recommendations: R_{TOP} should be 1kΩ, with a feedforward capacitor of 2.7nF fitted in parallel.

Instead of an external resistor divider, the output voltage can be set using PMBus™ commands (see page 40) or the corresponding user registers. The FS1525 supports this command with a resolution of 1/1024V. Alternatively, the initial output voltage may be set using a resistor on the PS pin to select from a pre-programmed setting in one of eight user register pairs (see page 22).

Shut-down Mechanisms

The FS1525 has two shut-down mechanisms:

- *Hard shut-down or decay according to load*
  A valid hard-disable is recognized (as defined by the Enable pin, Operation register, ON_OFF_CONFIG register, input voltage PV_{IN}, and PV_{IN} UVLO threshold corresponding to the VIN_OFF registers). Both drivers switch off and soft-start is pulled down instantaneously.
- *Soft-Stop or controlled ramp down*
  A valid soft-off request is recognized (as defined by the Enable pin, Operation register and ON_OFF_CONFIG register). Then, following a delay corresponding to the TOFF_DELAY registers, the SS signal falls to 0 in a time defined by the TOFF_FALL registers; the drivers are disabled only when it reaches 0. The output voltage follows the SS signal down to 0.

By default, the device is configured for hard shut-down. Shut-down with PV_{IN} is always a hard shut-down.

Phase Setting Pin (PS)

The PS pin on the FS1525 is a multi-function pin.

a) In applications requiring multiple FS1525 devices to operate in parallel, the phase between adjacent devices (and hence the number of devices) may be selected by connecting an appropriate resistor from PS to AGnd (R_{PS}). In such applications, this pin can also be used to assign "master" status to one of the parallel devices.

b) Certain values of R_{PS} can be used to set the desired switching frequency of operation as shown in the table below. It is recommended that the switching frequency be set dependent on the output voltage such that

$$700\,kHz \times V_{OUT} \leq F_{sw} \leq 1.1MHz \times V_{OUT}$$

An exception to this is for output voltages of 1.5V and 1.8V. A switching frequency of 1MHz is recommended for these two applications.

c) Certain values of R_{PS} can be used to set the initial output voltage at startup as shown in the table below. Any subsequent PMBus™ commands that set the output voltage will then override this. Note that this refers to the feedback pin voltage. If a resistor divider is used from V_{OUT} to the Fb pin, the voltages in the table must be scaled by the corresponding divider ratio.

R_{PS} (kΩ)	Master/ Slave	Phase (°)	V_{OUT} (V)	F_{SW} (MHz)
0	Master	0	0.6	FSW table
1.13	Slave	180	0.6	Sync to master
1.87	Slave	120	0.6	
2.61	Slave	90	0.6	
3.4	Slave	72	0.6	
4.12	Slave	60	0.6	
4.87	Slave	51.4	0.6	
5.62	Slave	45	0.6	
6.34	Master	0	0.6	1.5
7.15	Master	0	1.2	1.25
7.87	Master	0	0.6	1.04
8.66	Master	0	0.6	0.892
9.31	Master	0	0.9	0.781
10.2	Master	0	0.85	0.694
11	Master	0	0.8	0.625
12.1	Master	0	0.7	0.568

d) If R_{PS} is 0Ω, the switching frequency depends on output voltage as shown in the table below (set by the VOUT_COMMAND PMBus™ command or the corresponding registers).

V_{OUT} set range (V)	F_{SW} (MHz)
$V_{OUT} \leq 0.85$	0.625
$0.85 < V_{OUT} \leq 1.1$	0.781
$1.1 < V_{OUT} < 2.1$	1.25

Minimum Values for On-time, Off-time and PV_{IN}

When input voltage is high relative to target output voltage, the Control MOSFETs are switched on for shorter periods. The shortest period for which it can reliably be switched on is defined by minimum on-time ($T_{ON(MIN)}$). During start-up, when the output voltage is very small, the FS1525 operates with minimum on-time.

The maximum conversion ratio is determined by two factors:

a) When input voltage is low relative to target output voltage, the Control MOSFET is switched on for longer periods. The shortest period for which it can be switched off is defined by minimum off-time ($T_{OFF(MIN)}$). The Synchronous MOSFET stays on during this period and its current is detected for over-current protection. The minimum off-time dictates the minimum input voltage that can still allow the device to regulate its output at the target voltage.

b) To maintain balanced switching amplitudes in both phases (or to maintain the voltage on the Cb pin at $0.5*PV_{IN}$), this topology requires there to be no overlap between the high sides of the two phases (unlike a conventional buck topology). This effectively imposes theoretical maximums of 50% on the duty cycle of each phase and 25% on the conversion ratio; in practice, allowing for circuit delays and dead-times, the conversion ratio must not exceed 16% at full load.

The maximum conversion ratio is affected by both system efficiency and load transient requirements. It is recommended that system designers validate the values in their own applications.

Enable (En) Pin

The Enable (En) pin has several functions:

- In the default setting of the ON_OFF_CONFIG command, it is used to switch the FS1525 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If it is left floating, an internal 1MΩ resistor pulls it down to prevent the FS1525 being switched on unintentionally.
- It can be used to implement a precise input voltage UVLO. The input of the En pin is derived from the PV_{IN} voltage by a set of resistive dividers, R_{EN1} and R_{EN2} (Figure 5). Users can program the UVLO threshold voltage by selecting different ratios. A useful feature that stops the FS1525 regulating when PV_{IN} is lower than the desired voltage, this may be used for finer control over the PV_{IN} UVLO voltage levels than is provided by the VIN_ON/VIN_OFF commands.
- It can be used to monitor other rails for a specific power sequencing scheme (Figure 9).

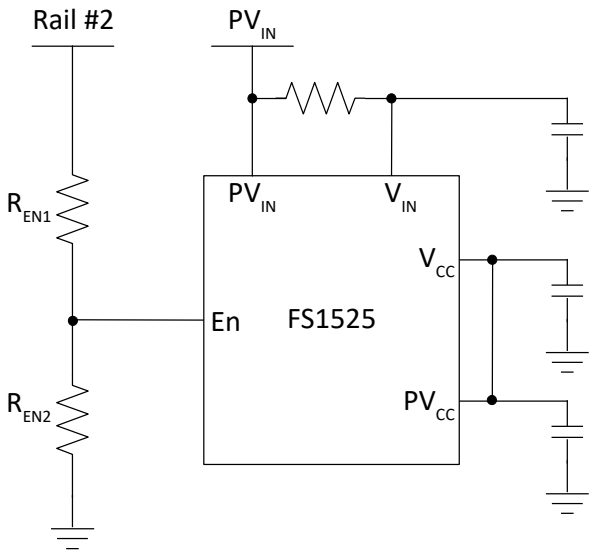


Figure 9 ***En pin used to monitor other rails for sequencing purposes***

Over-current Protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the $R_{DS(on)}$ of the Synchronous MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

- Provides accurate over-current protection without reducing converter efficiency (the current sensing is lossless)
- Reduces cost by eliminating a current-sense resistor
- Reduces any layout-related noise issues.

The OCP threshold is defined by the IOUT_OC_FAULT_LIMIT command (or the corresponding user registers). The over-current limit may be programmed in 0.5A steps, up to a maximum of 37.5A. The default setting is 33A.

The OCP threshold is internally compensated so that it remains almost constant at different ambient temperatures.

When the current exceeds the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET remains on until the current falls to 0, then the FS1525 enters hiccup mode (Figure 10). Both the Control MOSFET and the Synchronous MOSFET remain off for the hiccup-blanking time. After this time, the FS1525 tries to restart. If an over-current fault is still detected, the preceding actions are repeated. The FS1525 remains in hiccup mode until the over-current fault is remedied. Alternatively, the FS1525 can be re-programmed to enter a latched shut-down mode in response to an over-current fault.

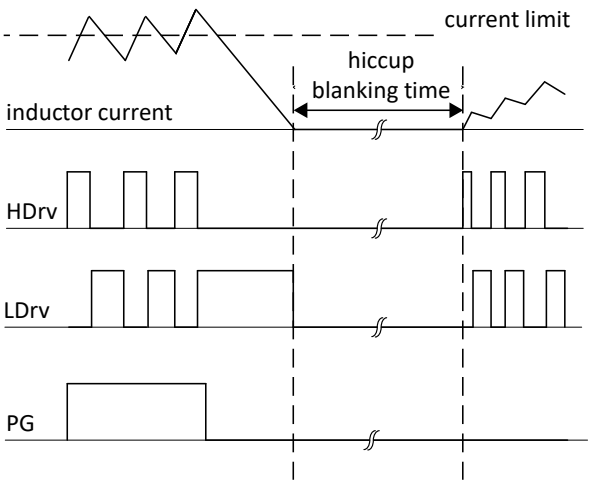


Figure 10 Illustration of OCP in hiccup mode

Over-voltage Protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the FB pin. When FB exceeds the output OVP threshold for longer than the output OVP delay (typically 5µs), a fault condition is generated.

The OVP threshold is defined by the VOUT_OV_FAULT_LIMIT command (or the corresponding user registers). This command allows the over-voltage level to be set relative to the output voltage, with a resolution of 1/1024V. However, internally, these are rounded to one of four settings as shown in the table below.

VOUT_OV_FAULT_LIMIT (% of VOUT_COMMAND)	Actual OVP Threshold (% of VOUT_COMMAND)
100.0 < setting ≤ 105.4	105
105.4 < setting ≤ 110.1	110
110.1 < setting ≤ 114.8	115
setting ≤ 100; setting > 114.8	**120**

The default setting is 120%. All the MOSFETs are switched off immediately and the PG pin is pulled low.

The MOSFETs remain latched off until reset by cycling either V_{CC} or En. Figure 11 shows a timing diagram for over-voltage protection.

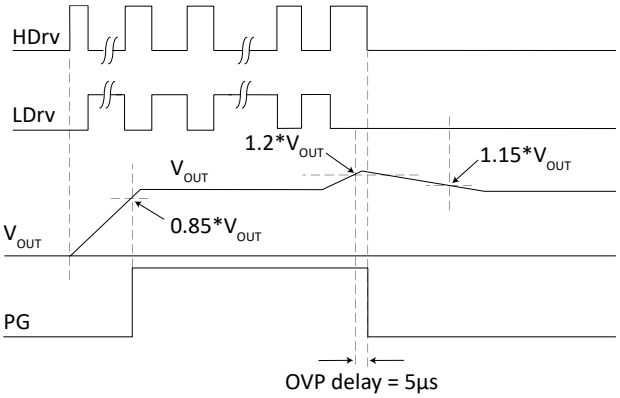


Figure 11 Illustration of latched OVP

The FS1525 provides output over-voltage and under-voltage warnings, as well as output under-voltage fault protection. These are set by three commands, respectively: VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT and VOUT_UV_FAULT_LIMIT (or the corresponding user registers). The mechanism for these thresholds is different from the over-voltage protection mechanism: the former rely on a digital comparison of the digitized and processed V_{OUT} telemetry to the thresholds, whereas the latter relies on an all-analog signal path and an internal high-speed comparator.

Over-temperature Protection (OTP)

Temperature sensing is provided inside the FS1525. A programmable threshold set to a resolution of 1°C using the OT_FAULT_LIMIT command (or the corresponding user registers). When set lower than the fixed analog threshold (145°C), the programmable threshold determines the temperature at which the device trips, making a digital comparison of reported temperature (READ_TEMPERATURE) and OT_FAULT_LIMIT. When the reported temperature exceeds the programmable threshold, the device either continues power conversion (default) or goes into a latched shutdown, a behavior selected by reprogramming the OT_FAULT_RESPONSE PMBus™ command (or corresponding registers). Recovery requires either cycling Enable or the Operation command.

An over-temperature warning threshold may also be set using the OT_WARN_LIMIT command. It is typically set below the over-temperature fault threshold and may be used to provide an alarm through the PMBus™ SALERT# pin and the STATUS_TEMPERATURE register.

Power Good (PG)

Power Good (PG) behavior is defined by the user register bit PGControl **and** by the POWER_GOOD_ON command. When the PGControl bit is set, the PMBus™ command may be used to set the upper power good threshold relative to the output voltage, with a resolution of 1/1024V. However, internally, these are rounded to one of four settings as shown in the table below.

POWER_GOOD_ON (% of VOUT_COMMAND)	Actual PG Threshold (% of VOUT_COMMAND)
setting ≤ 79.6; setting > 95.1	80
79.6 < setting ≤ 85.1	**85**
85.1 < setting ≤ 89.8	90
89.81 < setting ≤ 95.1	95

The default is 85%, so the PG signal will be asserted when the voltage at the Fb pin exceeds 85% of the VOUT_COMMAND setting (default 0.51V).

Hysteresis of 5% is applied to this, giving a lower threshold. When the voltage at the Fb pin drops below this lower threshold, the PG signal is pulled low.

PGControl bit set to 1 (default)

Figure 12 shows PG behavior in this situation.

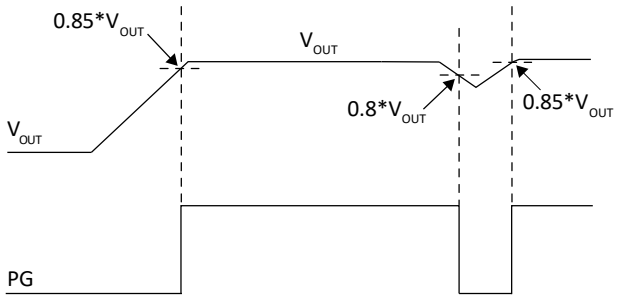


Figure 12 PG signal when PGControl bit=1

The behavior is the same at start-up and during normal operation. The PG signal is asserted when:

- En and V_{CC} are both above their thresholds
- No fault has occurred (including over-current, over-voltage and over-temperature)
- V_{OUT} is within the target range (determined by continuously monitoring whether FB is above the PG threshold)

PGControl bit set to 0

Figure 13 shows PG behavior in this situation.

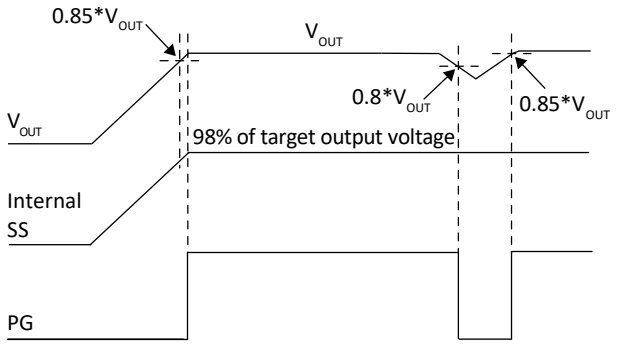


Figure 13 PG signal when PGControl bit=0

In normal operation, the PG signal behaves in the same way as when the **PGControl** bit is 1.

At start-up, however, the PG signal is asserted after Fb is within 2% of target output voltage, not when Fb exceeds the upper PG threshold.

The FS1525 also integrates an additional PMOS in parallel to the NMOS internally connected to the PG pin (Figure 3). This PMOS allows the PG signal to stay at logic low, even if V_{CC} is low and the PG pin is pulled up to an external voltage not V_{CC}.

Remote Sensing (RS)

The FS1525 offers high-performance true-differential remote sensing, which ensures output voltage accuracy by sensing across the actual load to compensate for any voltage drop due to high current. The remote sense amplifier is designed to have a fast slew rate with a source and sink current capability to respond to any transient event at the output. The output of the remote sense amplifier is monitored internally by an analog-to-digital converter (ADC) and can be read using the READ_VOUT PMBus™ command or by reading the registers 0xD6 (vout_report_lower[7:0]) and 0xD7 (vout_report_higher[7:0]). The reporting resolution is 1/1024V.

Parallel Operation

FS1525 devices can operate in a parallel mode, with all devices connected to the output voltage. All devices, including slave devices, should have their RS+ pin connected to the output voltage and their RS- pin connected to the ground reference. For the master device, the RS+ and RS- inputs of the remote sense amplifier must be directly connected to the output voltage at the specific point of regulation. This ensures precise feedback and optimal circuit performance by compensating for voltage drops along the distribution path.

Slave devices primarily focus on current sharing, with the voltage loop playing a secondary role. As a result, there is more flexibility in the placement of their RS+ and RS- connections. While connecting these pins to the same remote sense point as the master device is ideal for consistency, it can be impractical due to the need for excessive board traces from the sense point. In such cases, connecting the RS+ and RS- pins of slave devices to the local output capacitors is the preferred alternative.

The Sync and Clkout pins are used to synchronize the devices, while the Ishare pin ensures current sharing between devices. The PS pin is used on the master device to set the switching frequency and on the slave devices to set the phase relationship between the Sync signal and the PWM clock, based on the number of devices operating in parallel. This allows interleaved operation with correct phase relationships between the parallel devices for optimum system-level performance.

If the master device is also synchronized to an external clock, the thresholds of the sync signal are $0.775*V_{CC}$ (high) and $0.45*V_{CC}$ (low). The clock frequency applied to the Sync pin must be twice the target PWM frequency, which should be from 568kHz to 1.5MHz.

The Fault pin on the FS1525 is both an input and output. It must be pulled up to V_{CC} (or another 5V supply) for correct operation, even with a single device. In parallel operation, it plays a critical role in ensuring that any fault that shuts down one device is communicated to the other devices and shuts down those as well.

Design Example

Let us now consider a simple design example, using the FS1525 for the following design parameters:

- PV_{IN} = V_{IN} = 12V
- V_{OUT} = 0.8V
- F_{SW} = 625kHz
- C_{OUT} = 10 x 47µF
- C_{IN} = 4 x 22µF
- Ripple Voltage = ± 1% * V_{OUT}
- $\Delta V_{OUT(MAX)}$ = ±3% * V_{OUT}
  (for 6A load transient @ 4A/µs)

Input Capacitor

The input capacitor selected for this design must:

- Handle the peak and root mean square (RMS) input currents required by the FS1525
- Have low equivalent series resistance and inductance (ESR and ESL) to reduce input voltage ripple

MLCCs (multi-layer ceramic capacitors) are ideal. Typically, in 0805 case size, they can handle 2A RMS current with less than 5°C temperature rise.

For the FS1525 converter topology operating at duty cycle D and output current I_O, the RMS value of the input current is:

$$I_{RMS} = 0.5 \times Io\sqrt{D(1-D)}$$

In this application, I_O = 25A and $D = \frac{2 \times V_{OUT}}{PV_{IN}} = 0.133$, so I_{RMS} = 4.25A.

Therefore, at least three 22µF 25V ceramic input capacitors are required. In our design, we use four C2012X5R1E226M125AC from TDK.

If the FS1525 is not located close to the 12V power supply, a bulk capacitor (68–330µF) may be used in addition to the ceramic capacitors.

For V_{IN}, which is the input to the LDO, it is recommended to use a 1µF capacitor very close to the pin. The V_{IN} pin should be connected to PV_{IN} through a 2.7Ω resistor. Together, the 2.7Ω resistor and 1µF capacitor filter noise on PV_{IN}.

Output Voltage and Output Capacitor

The FS1525 is trimmed at the factory to provide a 0.6V output in closed loop. When using a resistor divider instead of I²C/PMBus™ commands, as in this design example, we select the values in accordance with the discussion on page 21. Therefore, R_{TOP} = 1kΩ, R_{BOTTOM} = 3.24kΩ and C_{FF} = 2.7nF.

The design requires minimal output capacitance to meet the target output voltage ripple and target maximum output voltage deviation under load transient conditions. We use ten C2012X5R0J476M125AC from TDK (a 47µF MLCC, 0805 case size, rated at 6.3V). At 0.8V, accounting for DC bias and AC ripple derating, it has an equivalent capacitance of 33µF, with equivalent series resistance of 3mΩ and equivalent series inductance of 0.44nH. A 100Ω resistor should be added in parallel with the output capacitors.

Figure 14 to Figure 16 show the measured peak-to-peak output voltage deviations for various load slew rates and step sizes for three different output voltages (0.8V, 1.0V and 1.2V) with 10x47µF output capacitors as described above.

V_{CC} and PV_{CC} Capacitor Selection

FS1525 uses on-package capacitors for V_{CC} as well as PV_{CC} to ensure effective high-frequency bypassing. However, especially for applications that use an external V_{CC} supply, it is recommended that system designers place 2.2µF/0603/X7R/10V capacitors on the application board as close as possible to the V_{CC} and PV_{CC} pins (Figure 17).

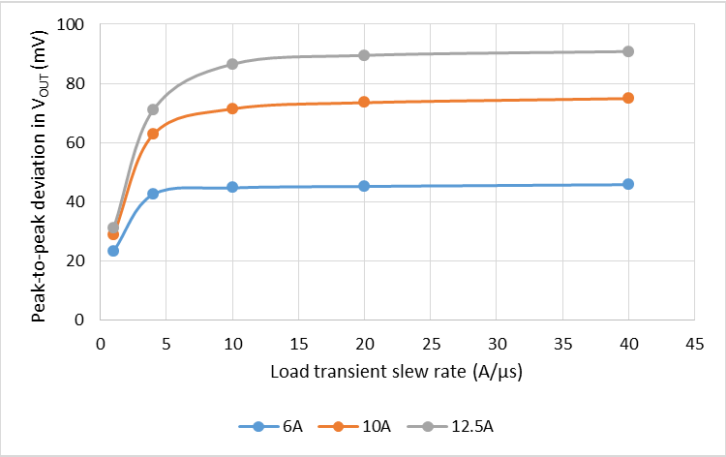


Figure 14 Peak-to-peak voltage deviation (V_{OUT} = 0.8V)

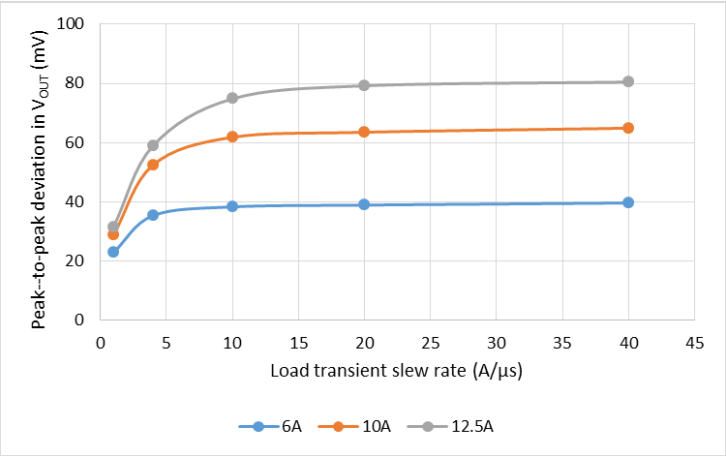


Figure 15 Peak-to-peak voltage deviation (V_{OUT} = 1.0V)

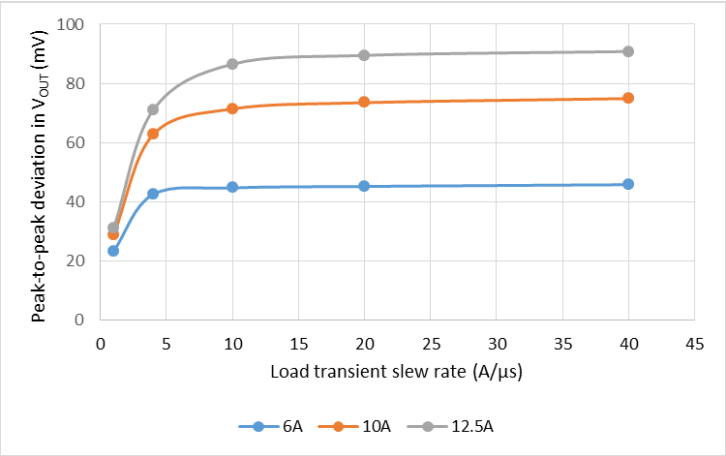
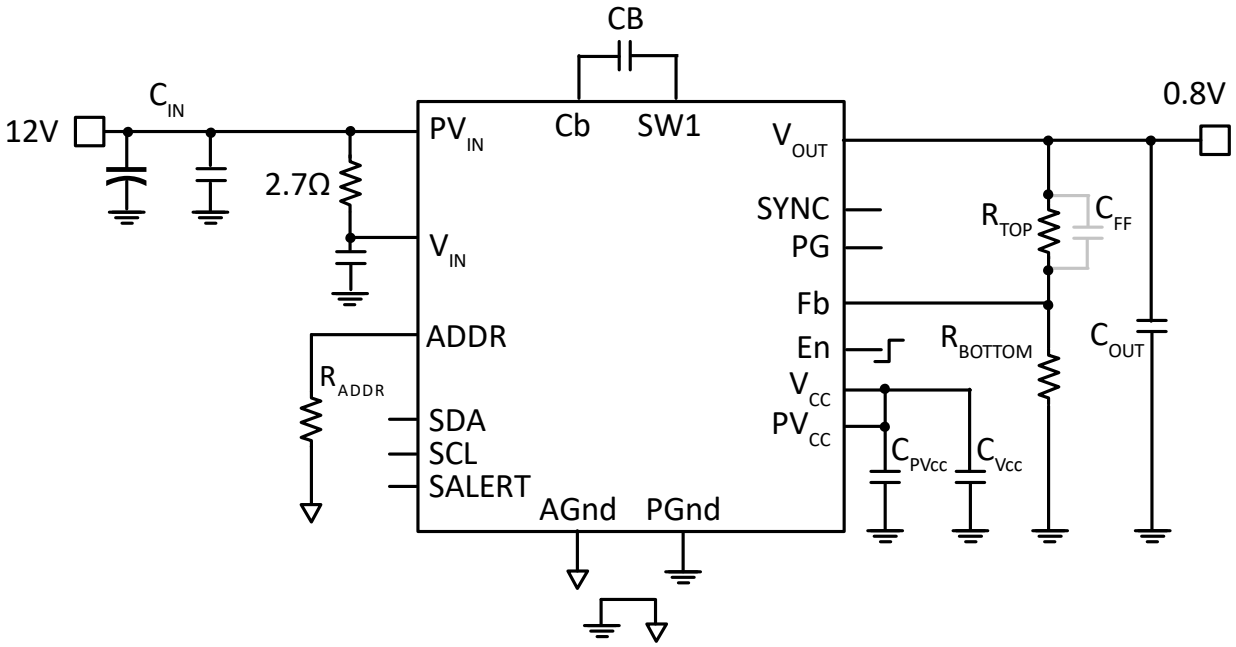


Figure 16 Peak-to-peak voltage deviation (V_{OUT} = 1.2V)



Values:

C_{IN}	4 x 22µF/0805/16V
C_{OUT}	10 x 47µF/0805/6.3V
C_{Vcc} = C_{PVcc}	2.2µF for external V_{CC} configuration (do not place for internal LDO configuration)
CB	2 x 4.7µF/0805/16V
C_{FF}	2.7nF
R_{TOP}	1kΩ
R_{BOTTOM}	3.24kΩ
R_{ADDR}	0Ω (short ADDR to AGnd) for 0 address, I^2C address 0x10, PMBus address 0x70

Notes:

SCL, SDA, SALERT and PG require pull-up resistors when used.
For external V_{CC} configuration, short V_{IN} to V_{CC}.
Connect AGnd to power ground plane through vias.

Figure 17 Application circuit for a single supply (PV_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 25A)

Typical Performance

Figure 18 to Figure 28 show typical operating waveforms for the evaluation board, while Figure 29 and Figure 30 show thermal images of the board in operation. In all cases, the board is operating at room temperature with no airflow; PV_{IN} is 12V, V_{OUT} is 0.8V and I_O is 0–25A.

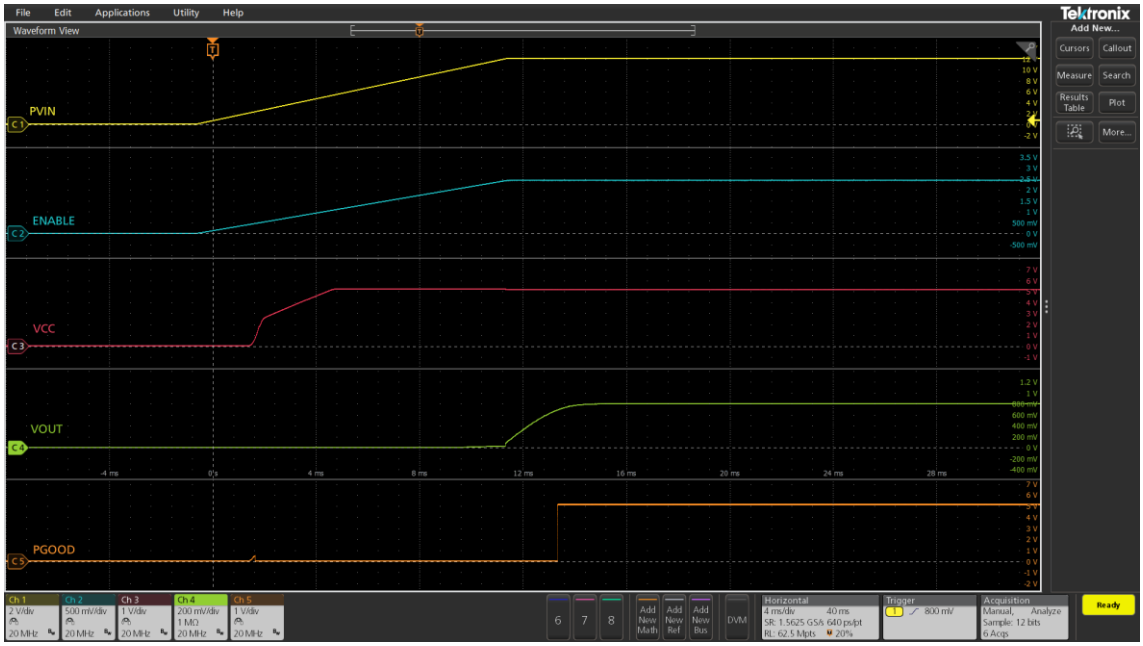


Figure 18 Startup with no load (Ch1: PV_{IN}, Ch2: Enable, Ch3: V_{CC}, Ch4: V_{OUT}, Ch5: PGood)

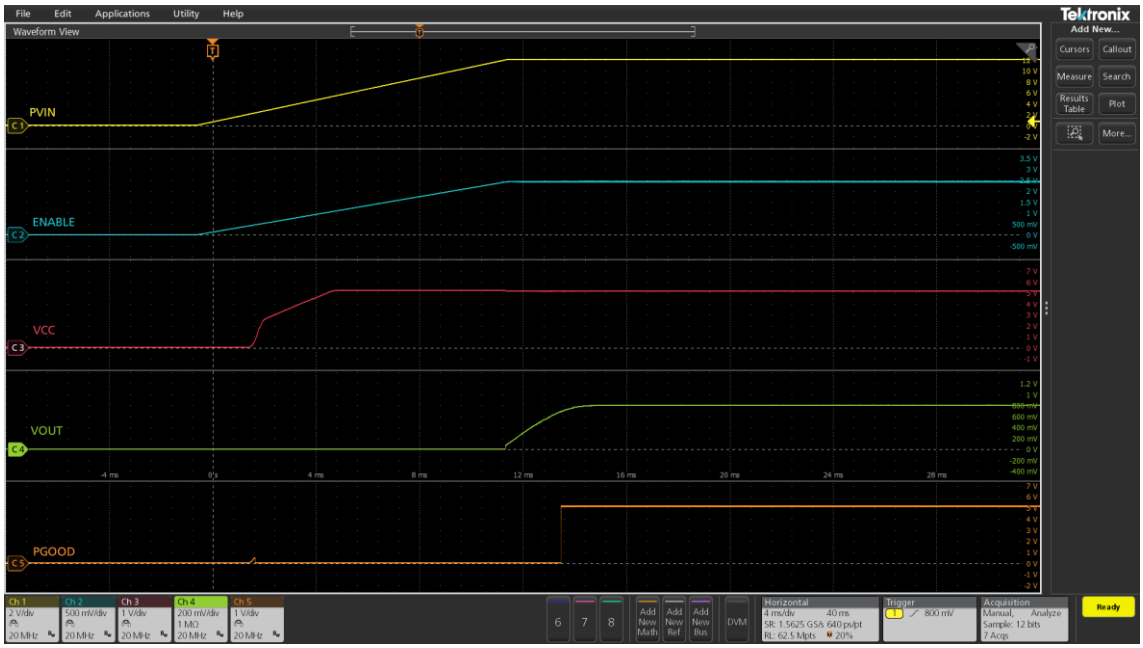


Figure 19 Startup with 25A load (Ch1: PV_{IN}, Ch2: Enable, Ch3: V_{CC}, Ch4: V_{OUT}, Ch5: PGood)

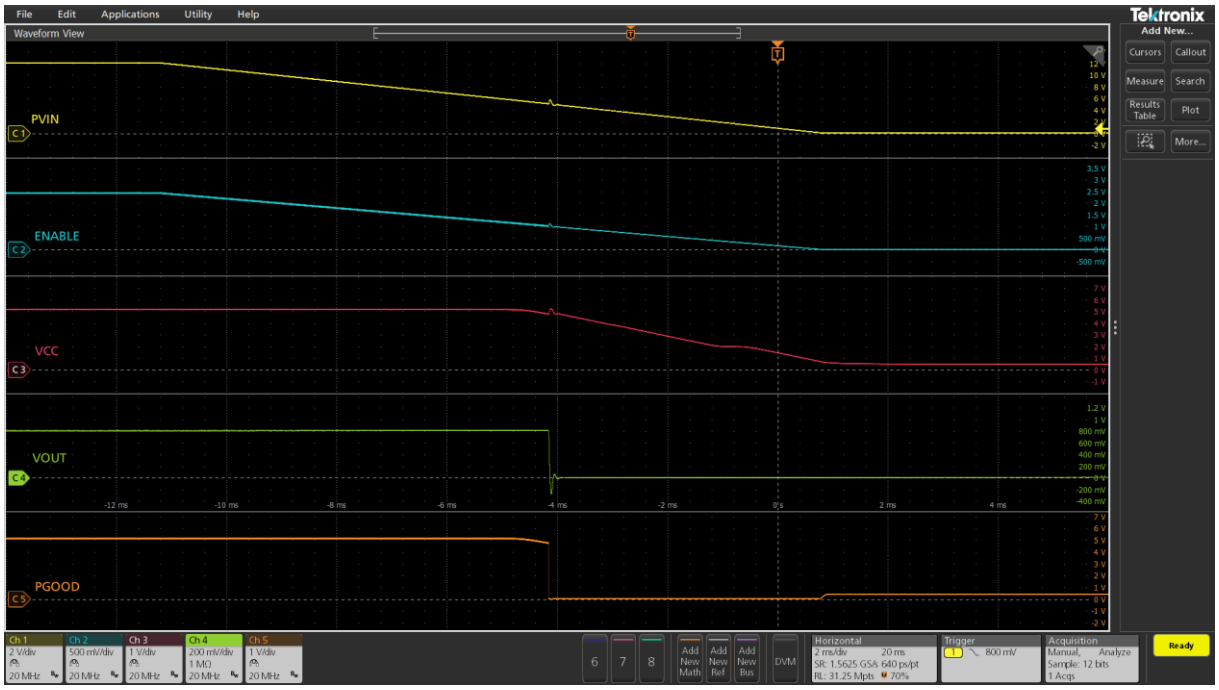


Figure 20 Shutdown with Enable de-assertion at 25A load
(Ch1: PV_{IN}, Ch2: Enable, Ch3: V_{CC}, Ch4: V_{OUT}, Ch5: PGood)

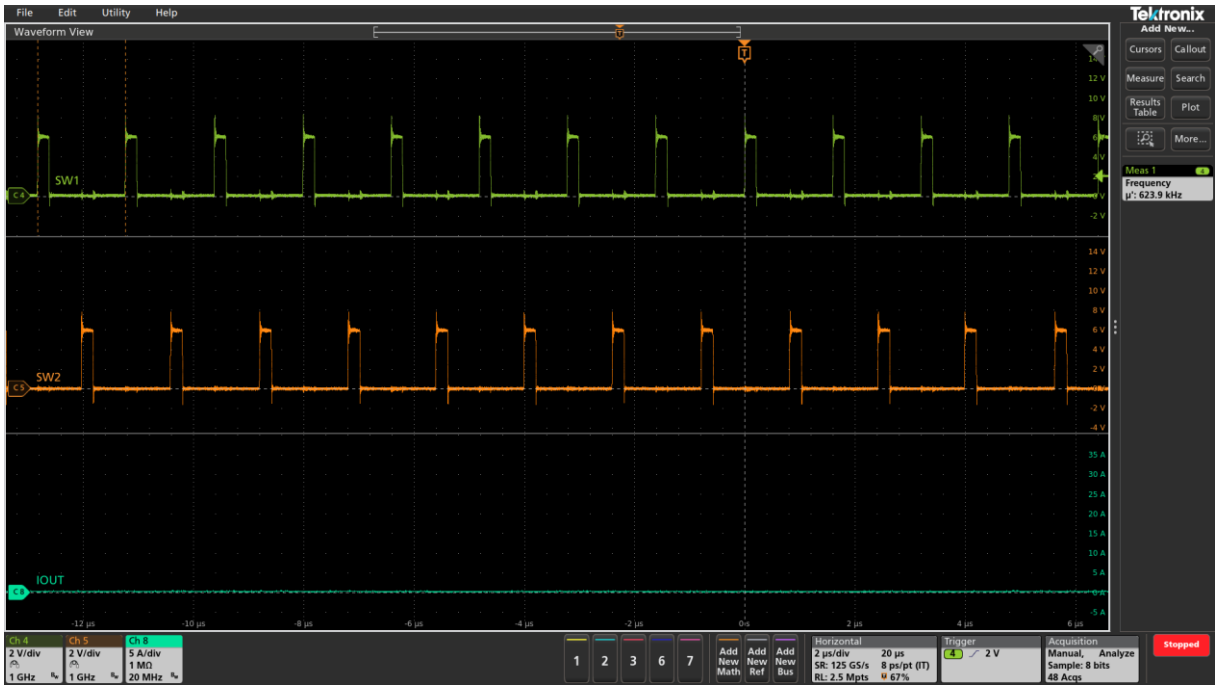


Figure 21 Switch node waveforms at no load

Figure 22 Switch node waveforms at 25A

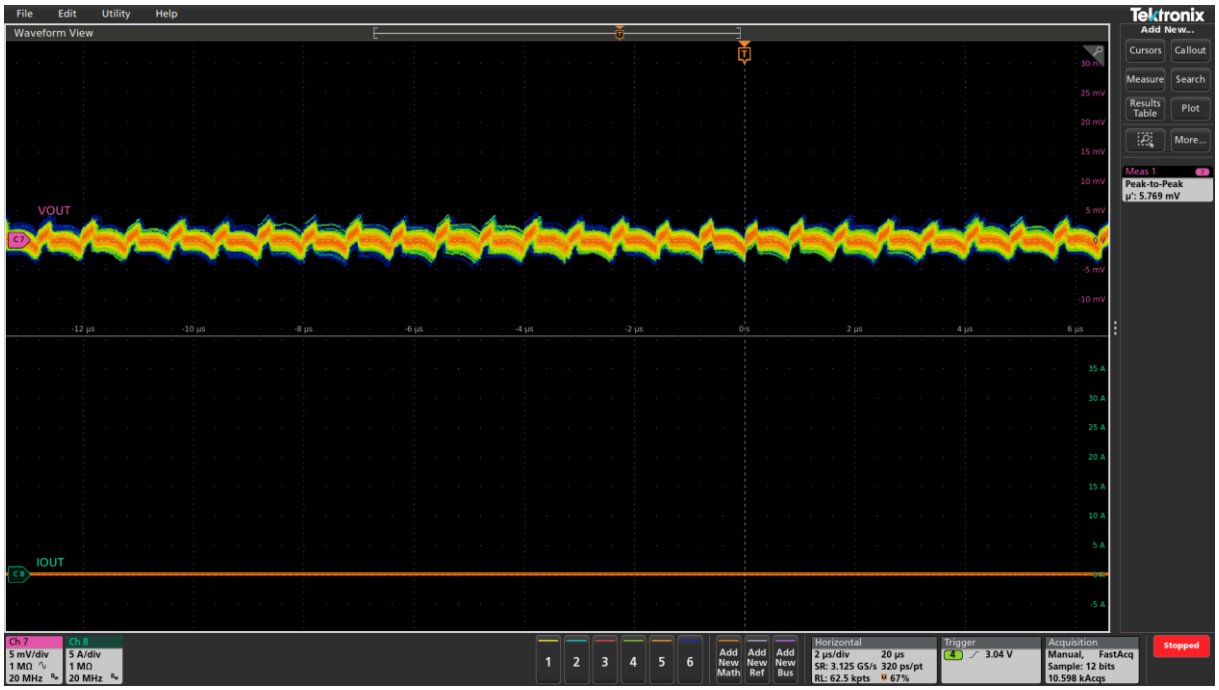


Figure 23 V_{OUT} ripple at 0A (Ch7: V_{OUT}, Ch8: I_O), peak-peak V_{OUT} ripple = 5.8mV

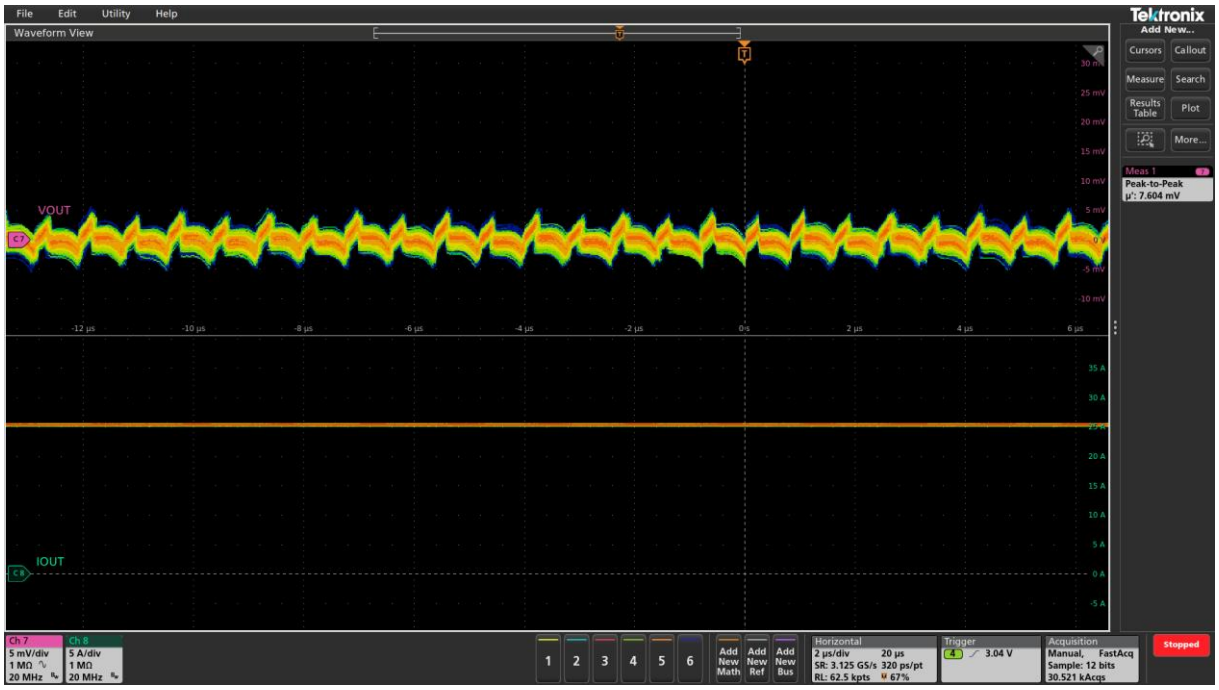


Figure 24 V_{OUT} ripple at 25A (Ch7: V_{OUT}, Ch8: I_O), peak-peak V_{OUT} ripple = 7.6mV

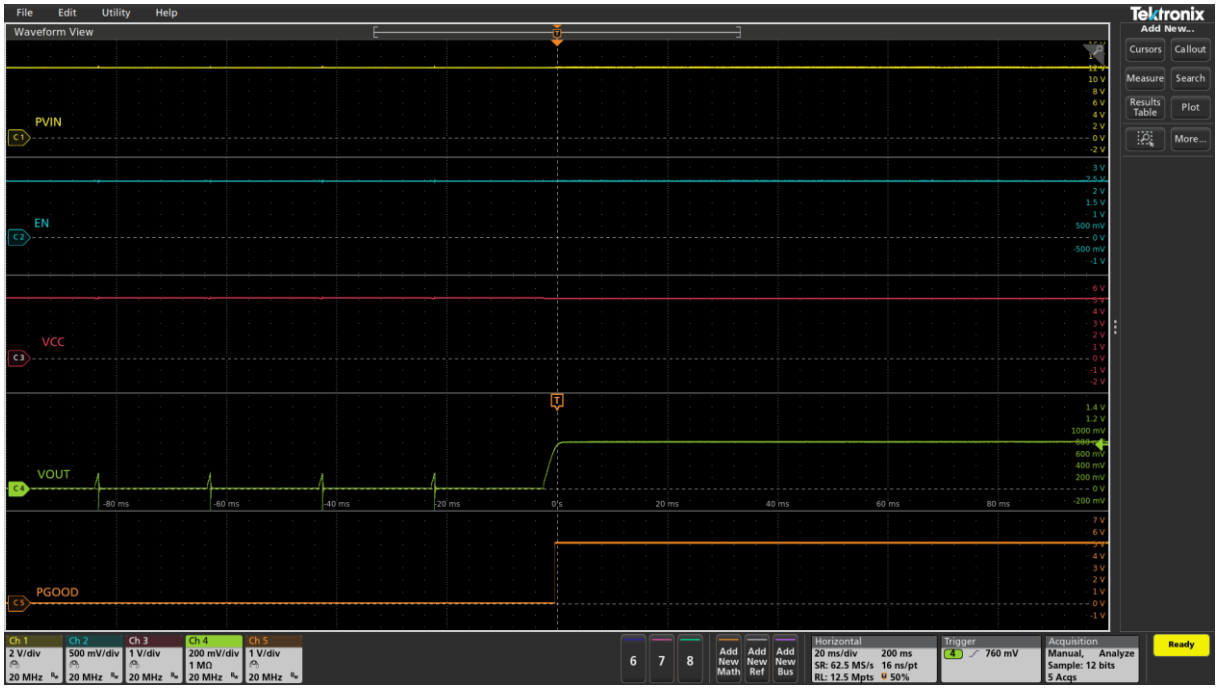


Figure 25 OCP Recovery to 25A (Ch1: PV_{IN}, Ch2: Enable, Ch3: V_{CC}, Ch4: V_{OUT}, Ch5: PGood)

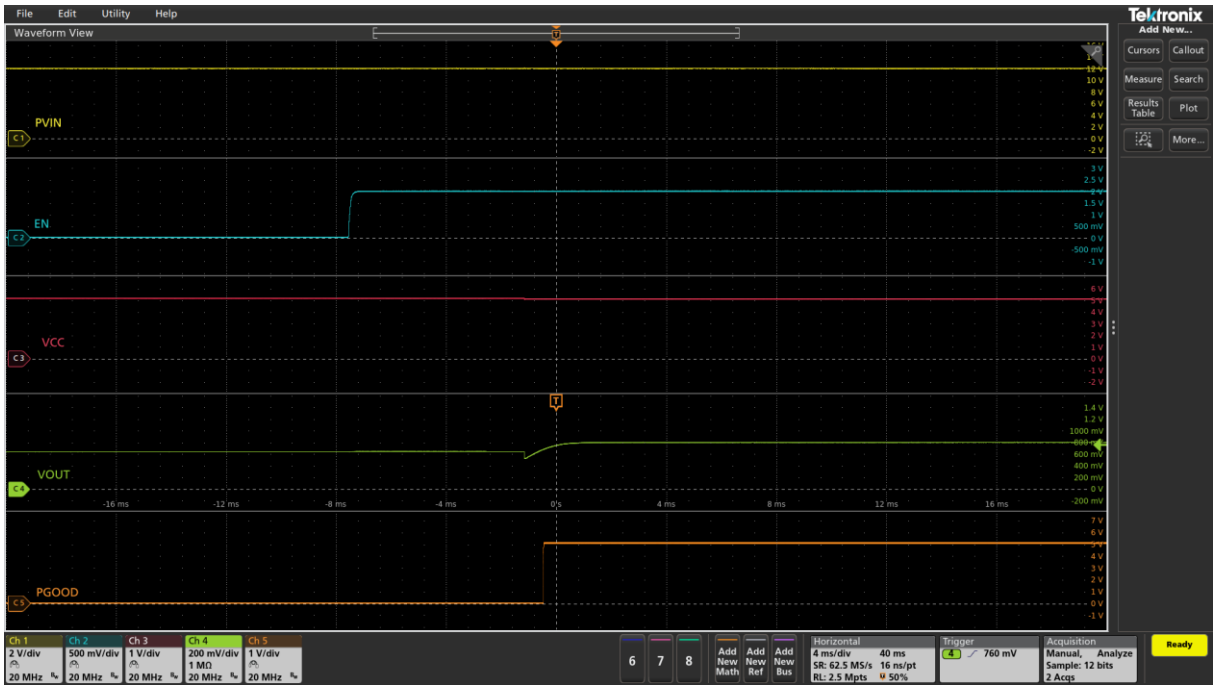


Figure 26 Startup into 80% Prebias (Ch1: PV_{IN}, Ch2: Enable, Ch3: V_{CC}, Ch4: V_{OUT}, Ch5: PGood)

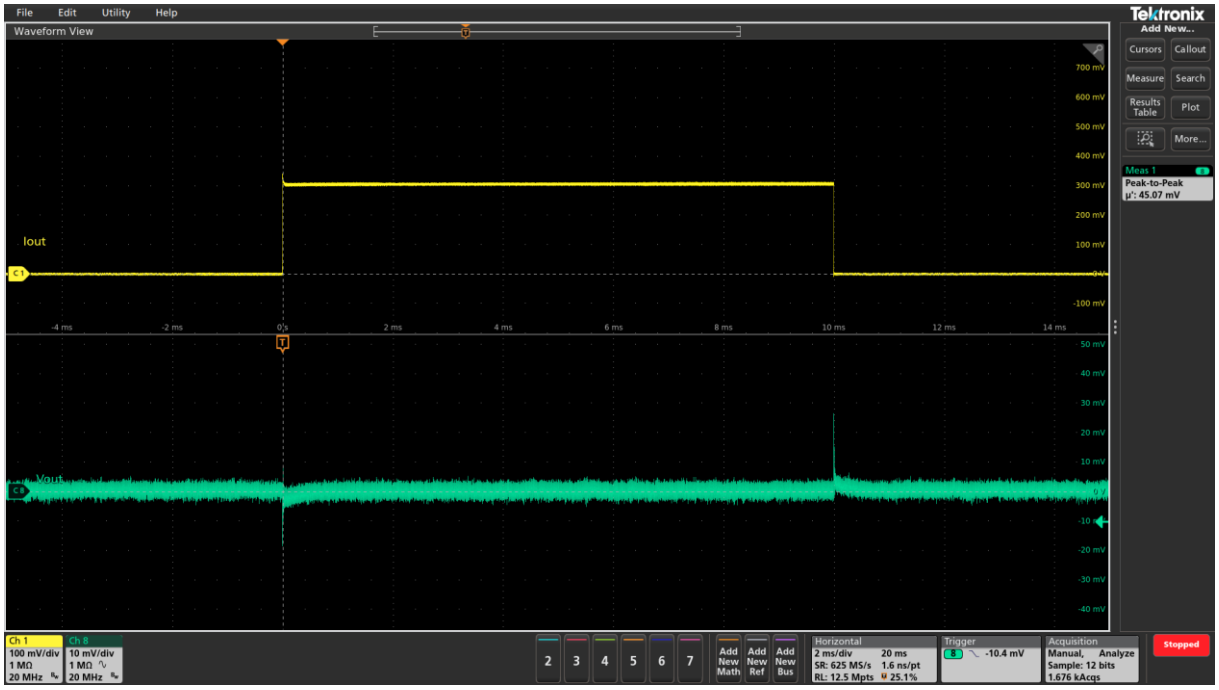


Figure 27 Transient response 10–16A (Ch1: I_{OUT}, Ch8: V_{OUT}), peak-peak deviation = 45mV, load slew rate = 4A/µs

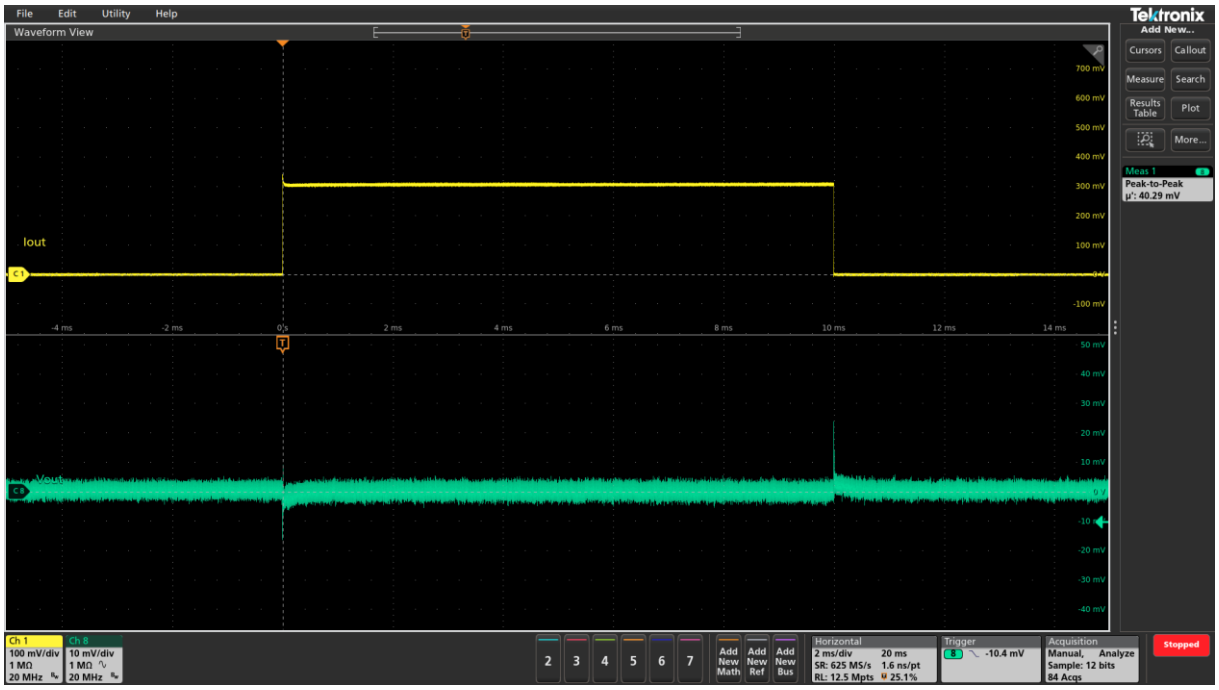


Figure 28 Transient response 19–25A (Ch1: I_{OUT}, Ch8: V_{OUT}), peak-peak deviation = 40.3mV, load slew rate = 4A/µs

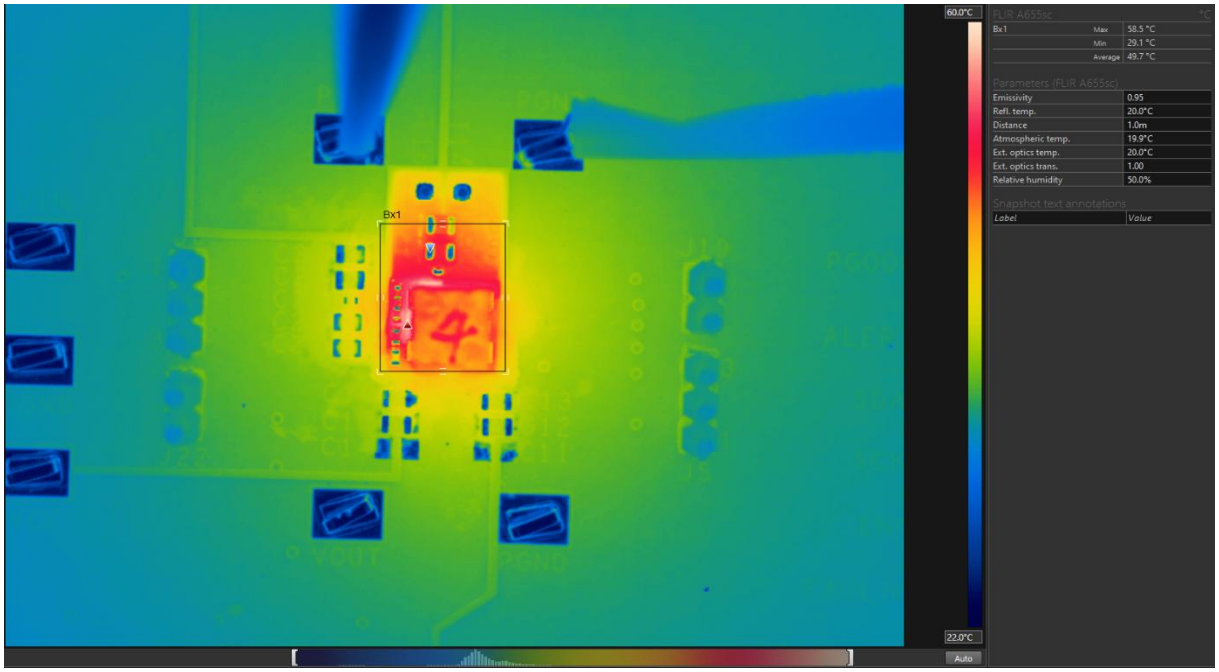


Figure 29 Thermal image at PV_{IN} = 12V, V_{OUT} = 0.8V, I_O = 25A, room temperature, no airflow, using Internal LDO, FS1525 maximum temperature rise = 36.5°C

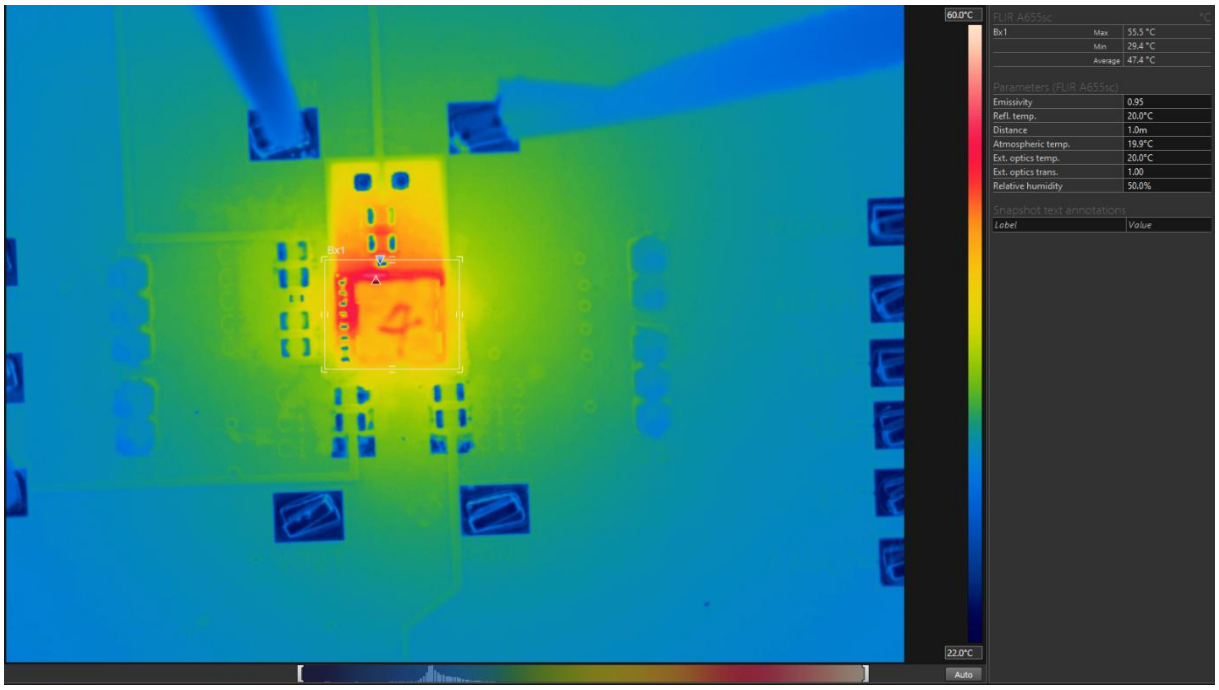


Figure 30 Thermal image at PV_{IN} = 12V, V_{OUT} = 0.8V, I_O = 25A, room temperature, no airflow, using external V_{CC} (5V), FS1525 maximum temperature rise = 33.5°C

Layout Recommendations

FS1525 is a highly integrated device with very few external components, which simplifies PCB layout. However, to achieve the best performance, these general PCB design guidelines should be followed:

- Place capacitors and feedback sensing components as close as possible to the relevant pins on the FS1525.
- Place at least two input capacitors on the top layer and the others on the bottom layer.
- Place at least two output capacitors on the top layer and the others on the top or bottom layer.
- Place coupling capacitors between the Cb and SW1 pins on the top layer and make sure the metal connections to them are adequate.
- Place coupling capacitors next to the V_{IN}, V_{CC} and PV_{CC} pins, on the top or bottom layer.
- Place as many vias as possible on the PV_{IN}, V_{OUT}, PGnd and AGnd pins, using vias in pads plated over (VIPPO).
- Place at least two vias next to the PGnd and V_{OUT} terminals of each input and output coupling capacitor.
- Place V_{OUT} remote sensing traces away from noisy signals.
- Make SCL and SDA traces at least 10mil wide with 20–30mil spacing.

For more detailed guidance, refer to the FS1525 Layout Checklist.

Thermal Considerations

The FS1525 has been thermally tested and modeled in accordance with JEDEC specifications JESD 51-2A and JESD 51-8. It has been tested using a 4-layer application PCB, with thermal vias under the device to assist cooling (for details of the PCB, refer to the application notes).

The FS1525 has two significant sources of heat:

- The power MOSFET section of the IC
- The inductor

The IC is well coupled to the PCB, which provides its primary cooling path. Although the inductor is also connected to the PCB, its primary cooling path is through convection. The cooling process for both heat sources is ultimately through convection. The PCB can be seen as a heat-spreader or, to some degree, a heat-sink.

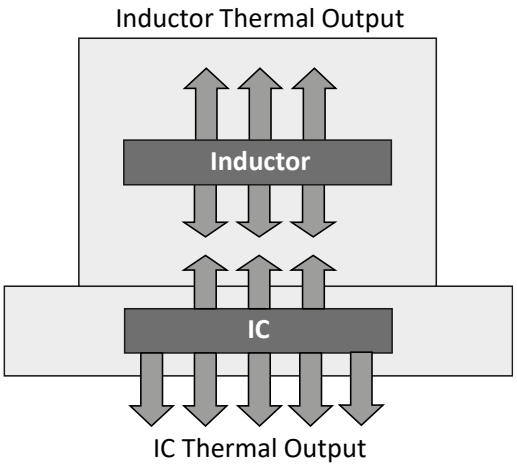


Figure 31 Heat sources in the FS1525

Figure 32 shows the thermal resistances in the FS1525, where:

- Θ_{JA} is the measure of natural convection from the assembled test sample within a confined enclosure of approximately 30x30x30cm. The air is passive within this environment and the only air movement is due to convection from the device on test.
- $\Theta_{JCbottom}$ is the heat flow from the IC to the bottom of the package, to which it is well coupled. The testing method adopts the method outlined in JESD 51-8, where the test PCB is clamped between cold plates at defined distances from the device.
- Θ_{JCtop} is theoretically the heat flow from the IC to the top of the package. This is not representative for the FS1525 for two reasons: firstly, it is not the primary conduction path of the IC and, more importantly, the inductor is positioned directly over the IC. As the inductor is a heat source, generating a similar amount of heat to the IC, a meaningful value for junction-to-case (top) cannot be derived.

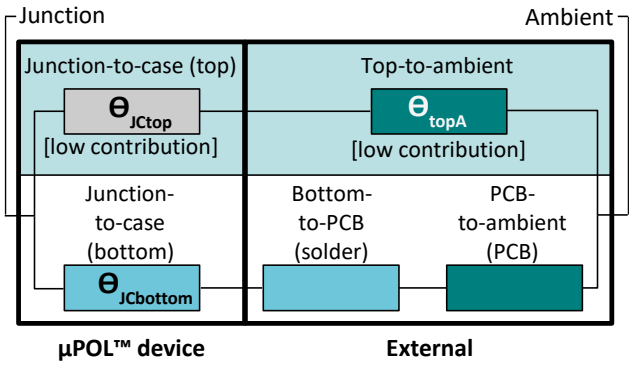


Figure 32 Thermal resistances of the FS1525

The values of the thermal resistances are:

- Θ_{JA} = 10.5°C/W
- $\Theta_{JCbottom}$ = 1.4°C/W

Although these values indicate how the FS1525 compares with similar point-of-load products tested using the same conditions and specifications, they cannot be used to predict overall thermal performance. For accurate modeling of the µPOL™'s interaction with its environment, computational fluid dynamics (CFD) simulation software is needed to calculate combined routes of conduction and convection simultaneously.

Note: In all tests, airflow has been considered as passive or static; applications using forced air may achieve a greater cooling effect.

Protocols

S	=	Start bit	W	=	Write bit (‘0’)	White bits	=	Issued by master
P	=	Stop bit	R	=	Read (‘1’)	Grey bits	=	Sent by slave (FS1525)
A	=	Ack	Sr	=	Repeated start			
N	=	Nack						

I²C

Write transaction

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Register Address	A	Data Byte	A	P

Read transaction

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	W	A	Register Address	A	Sr	Slave Address	R	A	Data Byte	N	P

SMBus™/PMBus™

Send byte

1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	P

Write byte

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte	A	P

Write word

1	7	1	1	8	1	8	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte Low	A	P	Data Byte High	A	P

Read byte

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	Sr	Slave Address	R	A	Data Byte	A	P

Read word

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Sr	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P

Supported PMBus™ Commands

Code	Name	# bytes	R/W	Format	Resolution	Range
01	OPERATION	1	R/W			
02	ON_OFF_CONFIG	1	R/W			
03	CLEAR_FAULTS					
10	WRITE_PROTECT		R/W			00, 20, 40, 80
15	STORE_USER_ALL					
16	RESTORE_USER_ALL					
19	CAPABILITY	1	Read	Return 30		
1B	SMBALERT_MASK		Write word / Block read process call			
20	VOUT_MODE	1	R	Return 96		
21	VOUT_COMMAND	2	R/W	L16	1/1024	
24	VOUT_MAX	2	R/W	L16	1/1024	
25	VOUT_MARGIN_HIGH	2	R/W	L16, 1.3 relative format	1/1024	
26	VOUT_MARGIN_LOW	2	R/W	L16, 1.3 relative format	1/1024	
27	VOUT_TRANSITION_RATE	2	R/W	L11	0.25 mV/µs	0–31.75 mV/µs
29	VOUT_SCALE_LOOP	2	R/W	L11	1, 0.5, 0.25 (default)	
35	VIN_ON	2	R/W	L11	0.5V	0–15.5V
36	VIN_OFF	2	R/W	L11	0.5V	0–15.5V
39	IOUT_CAL_OFFSET	2	R/W	L11	1/16A	
40	VOUT_OV_FAULT_LIMIT	2	R/W	L16, 1.3 relative format	5%	105–120%
41	VOUT_OV_FAULT_RESPONSE	1	R/W			00, 80, C0
42	VOUT_OV_WARN_LIMIT	2	R/W	L16, 1.3 relative format	1/1024	
43	VOUT_UV_WARN_LIMIT	2	R/W	L16, 1.3 relative format	1/1024	
44	VOUT_UV_FAULT_LIMIT	2	R/W	L16, 1.3 relative format	1/1024	
45	VOUT_UV_FAULT_RESPONSE	1	R/W	L16		00, 80
46	IOUT_OC_FAULT_LIMIT	2	R/W	L11	0.5A	22–37.5A
47	IOUT_OC_FAULT_RESPONSE	1	R/W			C0, F8
4A	IOUT_OC_WARN_LIMIT	2	R/W	L11	0.5A	
4F	OT_FAULT_LIMIT	2	R/W	L11	1°C	149°C max
50	OT_FAULT_RESPONSE	1	R/W			00, 80, C0
51	OT_WARN_LIMIT	2	R/W	L11	1°C	149°C max
55	VIN_OV_FAULT_LIMIT	2	R/W	L11	1V	18V max
56	VIN_OV_FAULT_RESPONSE	1	R/W			00, 80
58	VIN_UV_WARN_LIMIT	2	R/W	L11	0.5V	0–15.5V

Code	Name	# bytes	R/W	Format	Resolution	Range
5E	POWER_GOOD_ON	2	R/W	L16, 1.3 relative format	1/1024	-80% to -95%
60	TON_DELAY	2	R/W	L11	0.5ms	0–127.50ms
61	TON_RISE	2	R/W	L11	0.25ms	0–127.75ms
62	TON_MAX_FAULT_LIMIT	2	R/W	L11	0.25ms	0–127.75ms
63	TON_MAX_FAULT_RESPONSE	1	R/W	L16		00, 80
64	TOFF_DELAY	2	R/W	L11	0.5ms	0–127.50ms
65	TOFF_FALL	2	R/W	L11	0.25ms	0–127.75ms
78	STATUS_BYTE	1	R			
79	STATUS_WORD	2	R			
7A	STATUS_VOUT	1	R/W			
7B	STATUS_IOUT	1	R/W			
7C	STATUS_INPUT	1	R/W			
7D	STATUS_TEMPERATURE	1	R/W			
7E	STATUS_CML	1	R/W			
88	READ_VIN	2	R	L11	1/16	
8B	READ_VOUT	2	R	L16	1/1024	
8C	READ_IOUT	2	R	L11	1/16A or 1/4A	
8D	READ_TEMPERATURE	2	R	L11	1°C	
98	PMBUS_REVISION	1	R			
99	MFR_ID	4	Block R/W			
9A	MFR_MODEL	2	Block R/W			
9B	MFR_REVISION	2	Block R/W			
AD	IC_DEVICE_ID	2	Block R/W			
AE	IC_DEVICE_REV	2	Block R/W			

Package Description

The FS1525 is designed for use with standard surface-mount technology (SMT) population techniques. It has a positive (raised) footprint, with the pads being higher than the surrounding substrate. The finish on the pads is ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold).

The footprint design is the first of a new generation for µPOL® called Stiletto™. It has been extensively researched and delivers many benefits for products of this type and class. As a result, the package works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

Note: The symbol, footprint and 3D model for this device is available from ultralibrarian.com

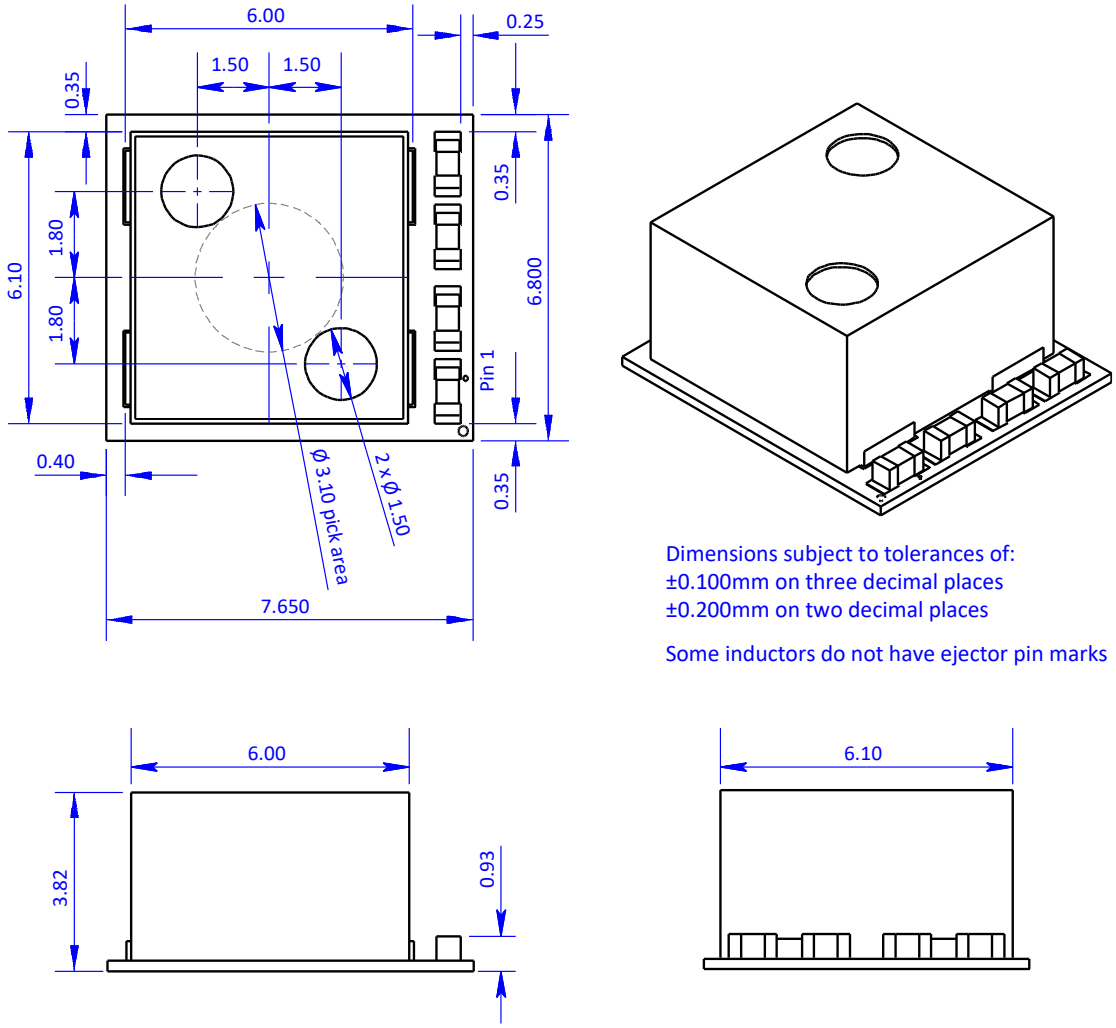


Figure 33 Dimensioned drawings

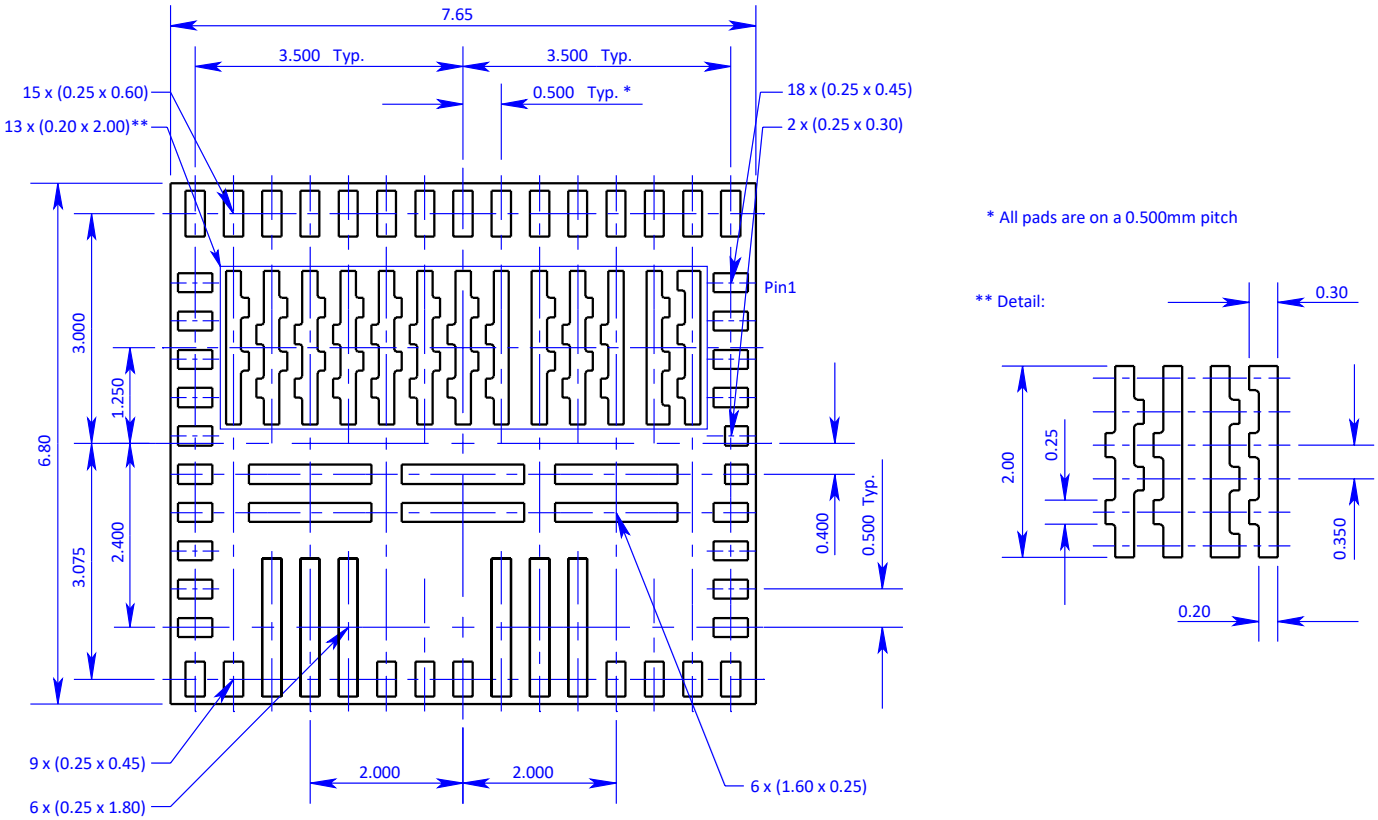


Figure 34 Package footprint

Board Layout

Solder Mask

The recommended design (Figure 35) uses mainly non-solder-mask-defined pads, with some exceptions. As the design has been tested with good results, deviations from it should be considered carefully. However, the solder mask may need some adjustments to comply with PCB design rules.

In particular, there are solder mask dams between the perimeter pads and the inner pads (Figure 36). Removing these dams can allow solder to migrate around the pads and result in some pads being incorrectly soldered (Figure 37).

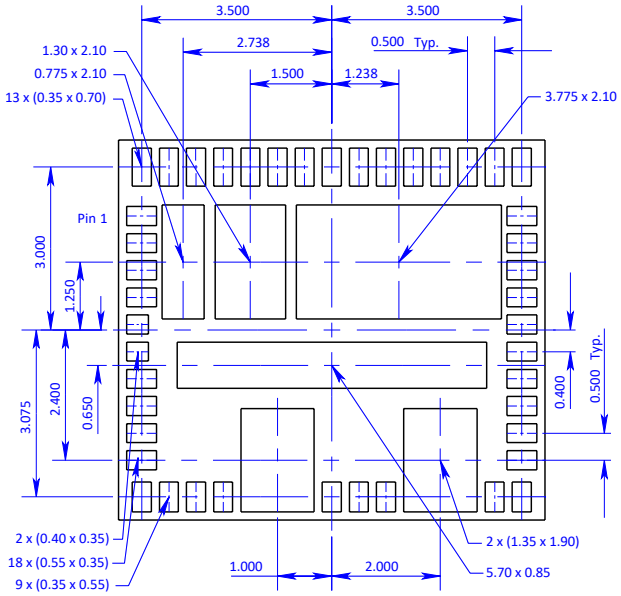


Figure 35 Solder mask

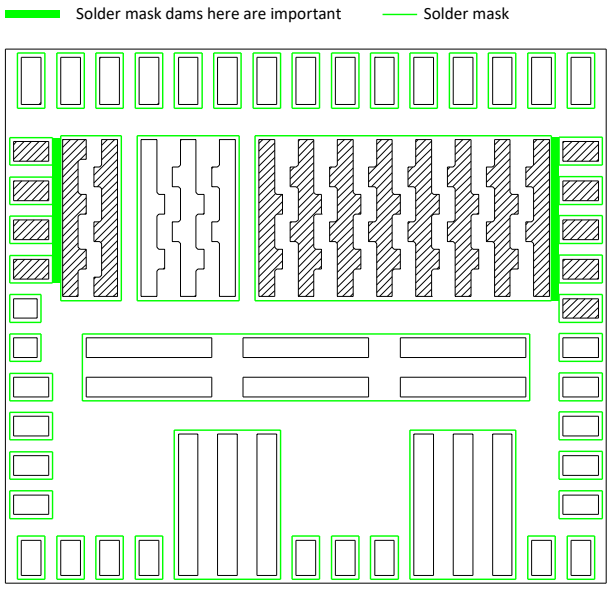


Figure 36 Solder mask dams

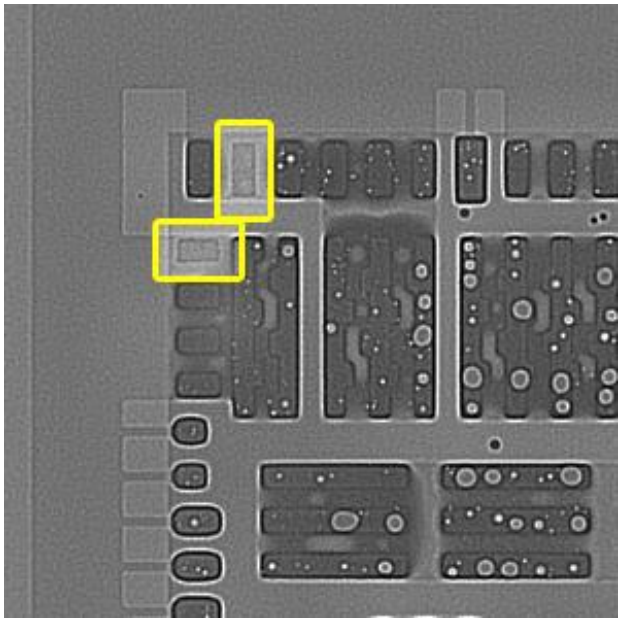


Figure 37 X-ray showing incorrectly soldered pads

Copper Pads and Tracks

The copper areas on the top surface of the board should be the same size as the device footprint (Figure 38). The PV_{IN} pads and PGnd pads should be grouped into single areas of copper as shown (Figure 39). They are not connected in the package.

For best results, the grouped PGnd pads and the adjacent grouped PV_{IN}* pads should be connected through to the inner layers of the PCB using filled-via technology, µVia technology or intrusive reflow technology. Using the PCB to dissipate the thermal energy from the device is extremely effective.

* Effective thermal use of PV_{IN} requires the PV_{IN} pad to be connected to one or more of the inner layers.

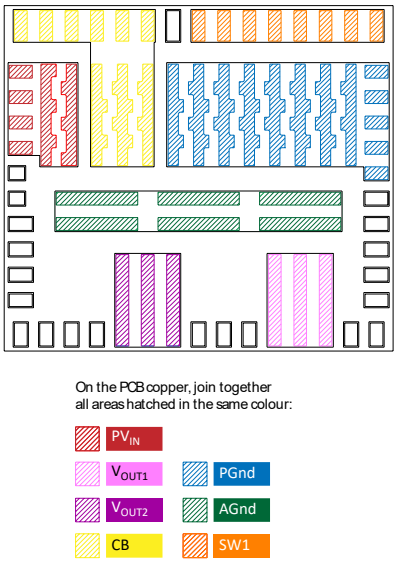


Figure 39 Pad groupings

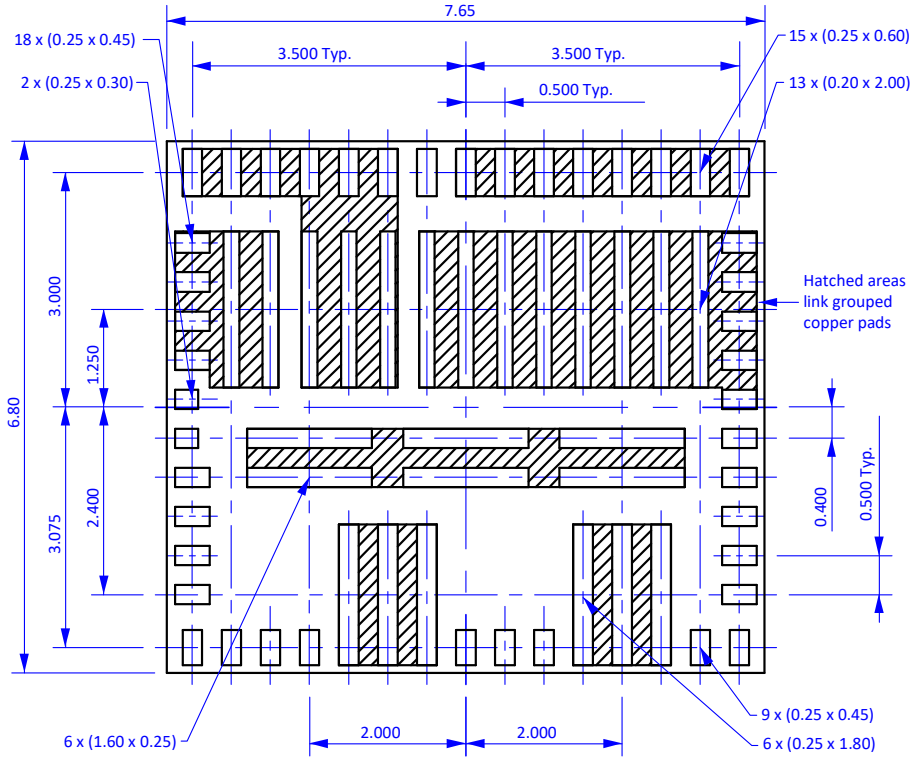


Figure 38 Copper pads and tracks

Solder Stencil

The design shown in Figure 40 is based on a stencil thickness of 0.100mm; it should also work adequately for a thickness of 0.125mm.

As many factors affect soldering performance, experimentation with solder volume may be required to achieve perfect results.

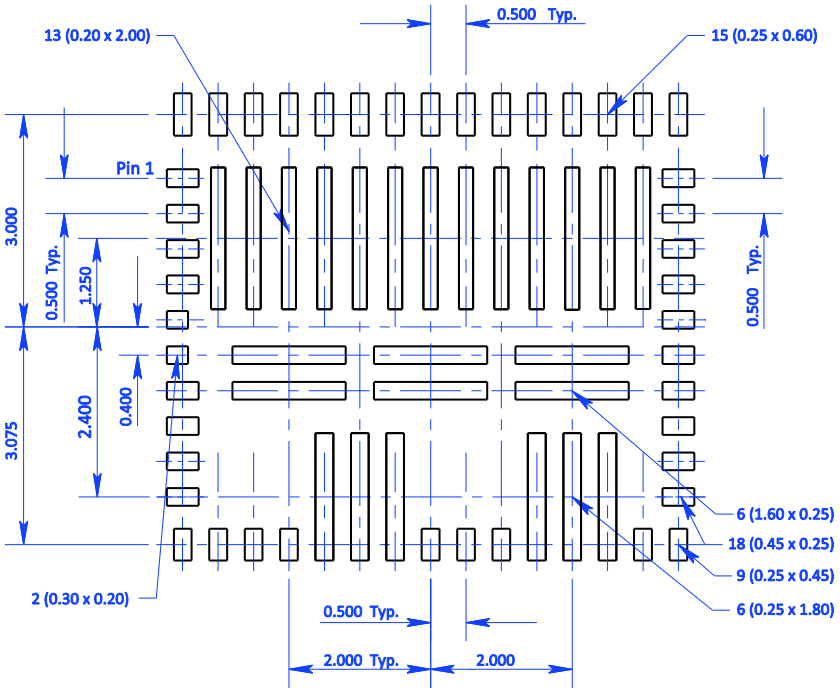
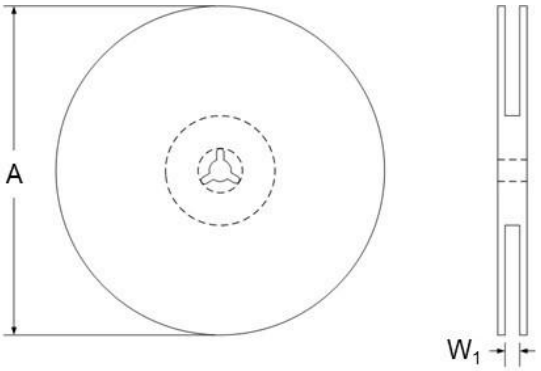


Figure 40 Solder stencil

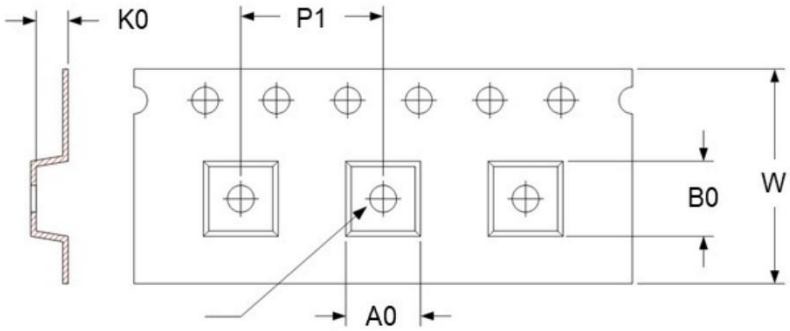
Tape and Reel Information

Reel Dimensions



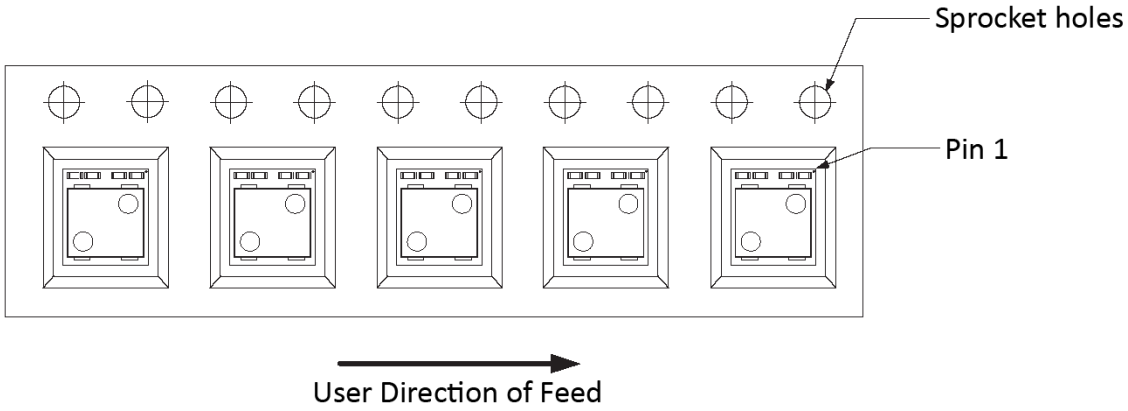
Reel Diameter A (mm)	Reel Width W_1 (mm)
330	12.8

Tape Dimensions



Dimension	(mm)
P1	12.00
W	16.00
A0	7.10
B0	7.95
K0	4.20

Pin 1 Orientation in Carrier Tape



REMINDERS FOR USING THESE PRODUCTS

Before using these products, be sure to request the delivery specifications.

SAFETY REMINDERS

Please pay sufficient attention to the warnings for safe designing when using these products.

REMINDER

The products listed on this specification sheet are intended for use in general electric equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal condition and use condition.

The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to sociality, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet.

1. Aerospace/Aviation equipment
2. Transportation equipment (cars, electric trains, ships, etc.)
3. Medical equipment
4. Power-generation control equipment
5. Atomic energy related equipment
6. Seabed equipment
7. Transportation control equipment
8. Public Information-processing equipment
9. Military equipment
10. Electric heating apparatus, burning equipment
11. Disaster prevention/crime prevention equipment
12. Safety equipment
13. Other applications that are not considered general-purpose applications

When using this product in general-purpose application, you are kindly requested to take into consideration securing protection circuit/ equipment or providing backup circuits, etc., to ensure higher safety.