

500mA Variable/Fixed Output LDO Regulators



BDxxKA5 Series BDxxKA5W Series **BD00KA5W Series**

General Description

The BDxxKA5 series are low-saturation regulators that are available for output currents up to 500mA. The output voltage precision is ±1%. These LDO regulators are offered in several output voltages and package lineups with or without ON/OFF switches (that set the circuit current to 0µA at shutdown). This series can be used for a broad spectrum of applications ranging from TVs and car audio systems to HDDs, PCs, and DVDs. There regulators have a built-in overcurrent protection circuit that prevents the destruction of the IC, due to output short circuits and a thermal shutdown circuit.

Features

- Output voltage precision: ±1%
- Low-saturation voltage with PMOS output: 0.12V Typ.(Io=200mA)
- Built-in over-current protection circuit
- Built-in thermal shutdown circuit
- Shutdown switch (BDxxKA5WFP and BDxxKA5WF series)
- Ceramic capacitor compatible (recommended capacitance: 1µF or greater)

Key Specifications

- Input Power Supply Voltage:
- Output voltage type: BA00KA5
 - BAxxKA5 Fixed

Output current:

500mA (Max.) Operating temperature range: -40°C to +105°C

Applications

Microcontrollers and all electronic devices that use logic circuit



Lineup matrix

Part Number			Package						
	1.0	1.2	1.5	1.8	2.5	3.0	3.3	Variable	rachage
BDxxKA5WFP	0	0	0	0	0	0	0	0	TO252-5
BDxxKA5WF	0	0	0	0	0	0	0	0	SOP8
BDxxKA5FP	0	0	0	0	0	0	0	_	TO252-3

5.5V (Max.)

Variable

Ordering Information

В	D	Х	Х	Κ	А	5	W	Х	Х	-	E 2	
Part I		Output 00:Varia Other: F	able	Curren KA5: 5	t capacity 00mA	W: I	tdown Switch nclude le:without	FP : TC)252-3)252-5		Packaging and fo E2: Embossed tap	rming specification be and reel

OProduct structure : Silicon monolithic integrated circuit OThis product is not designed protection against radioactive rays.

BDxxKA5 Series BDxxKA5W Series BD00KA5W Series

Maximum output current (Max.)	Shutdown Switch	Pac	kage	Output voltage (Typ.)	Orderable Part Number
				1.0V	BD10KA5WFP-E2
				1.2V	BD12KA5WFP-E2
				1.5V	BD15KA5WFP-E2
		TOOLO	Deal of 2000	1.8V	BD18KA5WFP-E2
		TO252-5	Reel of 2000	2.5V	BD25KA5WFP-E2
				3.0V	BD30KA5WFP-E2
				3.3V	BD33KA5WFP-E2
	With Switch			Variable	BD00KA5WFP-E2
		SOP8	Reel of 2500	1.0V	BD10KA5WF-E2
				1.2V	BD12KA5WF-E2
				1.5V	BD15KA5WF-E2
500mA				1.8V	BD18KA5WF-E2
				2.5V	BD25KA5WF-E2
				3.0V	BD30KA5WF-E2
				3.3V	BD33KA5WF-E2
				Variable	BD00KA5WF-E2
				1.0V	BD10KA5FP-E2
				1.2V	BD12KA5FP-E2
				1.5V	BD15KA5FP-E2
	No Switch	TO252-3	Reel of 2000	1.8V	BD18KA5FP-E2
				2.5V	BD25KA5FP-E2
				3.0V	BD30KA5FP-E2
				3.3V	BD33KA5FP-E2

Block Diagrams / Standard Example Application Circuits / Pin Configurations / Pin Descriptions



Absolute Maximum Ratings (Ta=25°C)

Param	eter	Symbol	Limits	Unit.
Power Supply Voltage		Vcc	-0.3 to +7.0 ^{*1}	V
Output Control Tern	ninal Voltage	VCTL	-0.3 to Vcc ^{*1}	V
	TO252-3		1200 ^{*2}	
Power Dissipation	TO252-5	Pd	1300 ^{*3}	mW
	SOP8		687.6 ^{*4}	
Operating Temperature Range		Topr	-40 to +105	°C
Ambient Storage Temperature		Tstg	-55 to +150	C°
Maximum Junction	Temperature	Tjmax	150	°C

*1 Must not exceed Pd

*2 When a 70mm×1.6mm glass epoxy board is used. Reduce by 9.6 mW/°C over 25°C.
*3 When a 70mm×1.6mm glass epoxy board is used. Reduce by 10.4mW/°C over 25°C.

*4 When a 70mm×1.6mm glass epoxy board is used. Reduce by 5.5 mW/°C over 25°C.

Recommended Operating Ratings (Ta=25°C)

Parameter	Symbol	Min.	Max.	Unit.
Input Power Supply Voltage	Vcc	2.3	5.5	V
Output Current	lo	0	500	mA
Output Voltage Configuration Range ^{*5}	Vo	1.0	4.0	V
Output Control Terminal Voltage	VCTL	0	Vcc	V

*5 Only BD00KA5WFP and BD00KA5WF

• Electrical Characteristics

BDxxKA5 Series BDxxKA5W Series

 $(Unless otherwise specified, Ta=25^{\circ}C, VCTL=2V, Vcc=2.5V(Vo=1.0V, 1.2V, 1.5V, 1.8V), Vcc=3.3V(Vo=2.5V), Vcc=5.0V(Vo=3.0V, 3.3V))$

Parameter	Symbol		Limit	-	Unit	Conditions	
Falametei	Symbol	Min Typ Max		Unit	Conditions		
	Vo	Vo(T)-0.015	Vo(T)	Vo(T)+0.015	V	Io=200mA (Vo=1.0V,1.2V)	
Output Voltage	VO	Vo(T) × 0.99	Vo(T)	Vo(T) × 1.01	v	lo=200mA (Vo≧1.5V)	
Shut Down Current	lsd	—	0	1	μA	VCTL=0V, Io=0mA (OFFmode)	
Bias Current	lb	—	350	550	μA	lo=0mA	
Dropout Voltage *6	$\Delta V d$	—	0.12	0.20	V	Io=200mA, Vcc=0.95 × Vo	
Peak Output Current	lo	500	_	—	mA		
Ripple Rejection	R.R.	_	50	_	dB	f=120Hz, ein ^{%9} =-10dBV, Io=100mA	
Line Regulation *7	Reg.I	_	10	35	mV	Vcc=Vo+0.5V→5.5V, Io=200mA	
Load Regulation	Reg.L	_	25	75	mV	lo=0mA→500mA	
Temperature Coefficient of Output Voltage *8	Тсvо	—	±100	-	ppm/°C	lo=5mA,Tj=0 to 125°C	
CTL ON Mode Voltage	VCTLON	2.0	-	—	V	ACTIVE MODE, Io=0mA	
CTL OFF Mode Voltage	VCTLOFF	—	_	0.8	V	OFF MODE, Io=0mA	
CTL Input Current	ICTL	20	40	60	μA	lo=0mA	

Vo(T) : Output Voltage

Vo≧2.5V

*7 1.0≦Vo≦1.8V,Vcc=2.3V→5.5V

*8 Not 100% tested

*9 ein : Input Voltage Ripple

Electrical Characteristics – continued

BD00KA5W Series

(Unless otherwise specified, Ta=25°C, Vcc=2.5V, V_{CTL}=2V ,Vo=1.5V)

Baramatar	Symbol Limit		Unit	Conditions			
Parameter	Symbol	Min	Тур	Max	Unit	Conditions	
Shut Down Current	lsd		0	1	μA	VCTL=0V, Io=0mA (OFFmode)	
Bias Current	lb		350	550	μA	lo=0mA	
Reference Voltage	Vadj	0.742	0.750	0.758	V	Io=50mA	
Dropout Voltage *10	$\Delta V d$	1	0.12	0.20	V	Io=200mA, Vcc=0.95 × Vo	
Peak Output Current	lo	500	1	—	mA		
Ripple Rejection	R.R.	1	50	—	dB	f=120Hz, ein ^{%12} =-10dBV, lo=100mA	
Line Regulation	Reg.I	1	10	35	mV	Vcc=Vo+0.5V→5.5V, Io=200mA	
Load Regulation	Reg.L	-	25	75	mV	Io=0mA→500mA	
Temperature Coefficient of Output Voltage ^{*11}	Тсvо		±100	_	ppm/°C	lo=5mA,Tj=0 to 125°C	
CTL ON Mode Voltage	VCTLON	2.0	-	—	V	ACTIVE MODE, Io=0mA	
CTL OFF Mode Voltage	VCTLOFF	_	_	0.8	V	OFF MODE, Io=0mA	
CTL Input Current	ICTL	20	40	60	μA	Io=0mA	

*¹⁰ Vo≧2.5V *¹¹ Not 10000

*¹² ein : Input Voltage Ripple

•Typical Performance Curves

(Unless specified otherwise, Vcc=25V,V_{CTL} =2V,and Io=0mA)



Typical Performance Curves - continued



Typical Performance Curves - continued



●I/O equivalence circuit



With BD00KA5WFP/WF,R1and R2 are connected outside the IC between ADJ and GND and between OUT and ADJ.

Power Dissipation



Fig.20 Power Dissipation heat reducing characteristics



Fig.21 Power Dissipation heat reducing characteristics





When using at temperatures over Ta=25°C, please refer to the power dissipation shown in Fig.20 through 22.

The IC characteristics are closely related to the temperature at which the IC is used, so if the temperature exceeds the maximum junction temperature TjMAX, the device may malfunction or be destroyed. The heat of the IC requires sufficient consideration regarding instantaneous destruction and long-term operation reliability. In order to protect the IC from thermal damage, it is necessary to operate it at temperatures less than the maximum junction temperature TjMAX. Even when the ambient temperature Ta is a normal temperature (25°C), the chip(junction) temperature Tj may be quite high,

Even when the ambient temperature I a is a normal temperature (25°C), the chip(junction) temperature I j may be quite high, so please operate the IC at temperatures less than the acceptable loss Pd.

Vcc : Input voltage Vo : Output voltage

lo : Load current

Icca : Circuit current

The calculation method for power consumption Pc(W) is as follows :

Pc = (Vcc-Vo)×lo+Vcc×lcca Acceptable loss Pd≧Pc

Solving for the load current I_0 in order to operate within the acceptable loss,

 $lo \leq \frac{Pc - Vcc \times lcca}{Vcc - Vo}$

It is then possible to find the maximum load current IOMAX with respect to the applied voltage Vcc at the time of thermal design.

Calculation Example

Example 1) When Ta=85°C, Vcc=2.5V, Vo=1.0V

· , , , , , ,	BA10KA5WFP (TO252-5 packaging)
$lo \le \frac{0.676 - 2.5 \times lcca}{2.5 - 1.0}$	θ ja=96.2°C/W \rightarrow -10.4mW/°C
$Io \leq 440 \text{mA}$ (Icca : 6mA)	$25^{\circ}C=1300$ mW $\rightarrow 85^{\circ}C=676$ mW

Please refer to the above information and keep thermal designs within the scope of acceptable loss for all operating temperature ranges.

The power consumption Pc of the IC when there is a short circuit (short between Vo and GND) is :

Pc=Vccx(lcca+lshort)

*Ishort : Short circuit current

Terminal Vicinity Settings and Cautions

Vcc Terminal

Please attach a capacitor (greater than 1μ F) between Vcc and GND.

The capacitance values differ depending on the application, so chose a capacitor with sufficient margin and verify the operation on actual board.

GND Terminal

Please be sure to keep the set ground and IC ground at the same potential level so that a potential difference does not arise between them. If a potential difference arises between the set ground and the IC ground, the preset voltage will not be output properly, causing the system to become unstable. Please reduce the impedance by making the ground patterns as wide as possible and reducing the distance between the set ground and the IC ground as much as possible.

CTL Terminal



Fig.23 Input equivalent circuit

The CTL terminal is turned ON at 2.0V and higher, and OFF at 0.8V and lower, within the operating power supply voltage range. The power supply and the CTL terminal may be started up and shut down in any order without problems.

●Vo Terminal

Please be sure to attach an anti-oscillation capacitor between V_0 and GND.



Be sure to place an anti-oscillation capacitor between the output terminal and the GND. Oscillations may arise if the capacitance value changes, due to factors such as temperature changes. A 1μ F capacitor with small internal series resistance (ESR) such as a ceramic capacitor is recommended as an anti-oscillation capacitor. Ceramic capacitors generally have favorable temperature characteristics and DC bypass characteristics. When selecting a ceramic capacitor, a high voltage capacitor (good DC bypass characteristics) with temperature characteristics that are superior to those of X5R or X7R, is recommended. In applications where input voltage and load fluctuations are rapid, please decide on a capacitor after sufficiently confirming its properties according to its specifications in the actual application.



Fig.26 General characteristics of ceramic capacitors

Operational Notes

OProtection Circuits

Over-current Protection Circuit

A built-in over-current protection circuit corresponding to the current capacity prevents the destruction of the IC when there are load shorts. This protection circuit is a "7"-shaped current control circuit that is designed such that the current is restricted and does not latch even when a large current momentarily flows through the system with a high-capacitance capacitor. However, while this protection circuit is effective for the prevention of destruction due to unexpected accidents, it is not suitable for continuous operation or transient use. Please be aware when creating thermal designs that the over-current protection circuit has negative current capacity characteristics with regard to temperature.

OThermal Shutdown Circuit (Thermal Protection)

This system has a built-in temperature protection circuit for the purpose of protecting the IC from thermal damage. As shown in Fig. 20-22, this must be used within the range of acceptable loss, but if the acceptable loss is continuously exceeded, the chip temperature Tj increases, causing the thermal shutdown circuit to operate. When the thermal shutdown circuit operates, the operation of the circuit is suspended. The circuit resumes operation immediately after the chip temperature Tj decreases, so the output repeats the ON and OFF states (Please refer to Fig.17 for the temperatures at which the temperature protection circuit operates).

There are cases in which the IC is destroyed due to thermal runaway when it is left in the overloaded state. Be sure to avoid leaving the IC in the overloaded state.

OReverse Current

In order to prevent the destruction of the IC when a reverse current flows through the IC, it is recommended that a diode be placed between the Vcc and Vo and a pathway be created so that the current can escape (Refer to Fig.27).



Fig.27 Bypass diode

OThis IC is BI-CMOS IC that has a P-board (substrate) and P+ isolation between each element, as shown in Fig.28. A P-N junction is formed between this P-layer and the N-layer of each element, and the P-N junction operates as :

- a parasitic diode when the electric potential relationship is GND> Pin A, GND> Pin B, or
- a parasitic transistor when the electric potential relationship is Pin B > GND> Pin A.

Parasitic elements are structurally inevitable in the IC. The operation of parasitic elements induces mutual interference between circuits, causing malfunctions and eventually the destruction of the IC. Take precaution as not to use the IC in ways that would cause parasitic elements to operate. For example, applying a voltage that is lower than the GND (P-board) to the input terminal.



Fig.28 Basic structure example

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

Physical Dimension Tape and Reel Information



TO252-3



TO252-5



Marking Diagrams



Revision History

Date	Revision	Changes
26.Jun.2012	001	New Release

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