

## TDA51SCANHC SOIC package isolated CAN transceiver

### Features

- Ultra-small, ultra-thin, chip scale SOIC package
- Compliant with ISO11898-2 standard
- Integrate efficiently power supply
- I/O power supply range supports 4.5V to 5.5V
- High isolation to 5000Vrms
- Bus-Pin ESD protection up to 5kV(HBM)
- Baud rate up to 1Mbps
- -40V to +40V bus fault protection
- High CMTI: 150 kV (typical)
- TXD dominant time-out function
- Nanosecond communication delay
- The bus supports maximum 110 nodes
- Industrial operating ambient temperature range: -40°C to +125°C

### Package



### Applications

- Industrial automation, control, sensors and drive systems
- Building and greenhouse environmental control(HVAC) automation
- Security system
- Transport
- Medical treatment
- Telecommunication
- CAN Bus standard such as CAN open, Device Net, NMEA2000, ARNIC825, ISO11783, CAN Kingdom, CAN aerospace

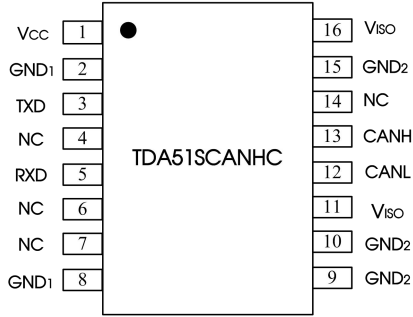
### Functional Description

TDA51SCANHC is a isolated CAN Bus transceiver, which is compliant with ISO11898-2 standard. TDA51SCANHC integrate 5 V efficiently power. The TDA51SCANHC provide differential transmitting and receiving capability between the CANH protocol controller and the physical layer bus. It is capable of running at data rates of up to 1 Mbps. The device has the function of series line, over-voltage(-40V to 40V), ground loss protection and thermal shutdown so that it is especially suitable for working in harsh environment.

# Contents

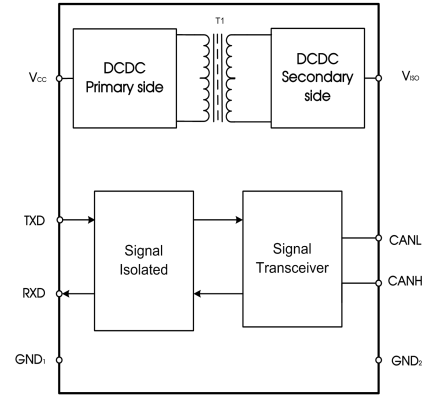
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## Pin Connection



Note: All GND<sub>1</sub> pins are internally connected;  
All GND<sub>2</sub> pins are internally disconnected.

## Internal Block Diagram



## Function Table

Letter	Description
H	High-Level
L	Low-Level
X	Unrelated
Z	High Impedance

Table 1. Driver Function table

INPUTS	OUTPUTS		Bus State
	CANH	CANL	
TXD			
L	H	L	Dominant
H(Or No Connection)	Z	Z	Recessive

Table 2. Receiver Function table

V <sub>ID</sub> =CANH-CANL	RXD	Bus State
V <sub>ID</sub> ≥0.9V	L	Dominant
0.5 < V <sub>ID</sub> < 0.9V	Uncertainty	Uncertainty
V <sub>ID</sub> ≤0.5V	H	Recessive
Open	H	Recessive

## Pin Descriptions

Pin Number	Pin Name	Pin Functions
1	V <sub>CC</sub>	Power supply pin. By using 0.1uF and 10uF ceramic capacitance ground (GND <sub>1</sub> ).
2	GND <sub>1</sub>	Ground (Logic side)
3	TXD	Driver input pin
4	NC	No connect
5	RXD	Receiver output pin.
6	NC	No connect
7	NC	No connect
8	GND <sub>1</sub>	Ground (Logic side)
9	GND <sub>2</sub>	Ground (Bus side)
10	GND <sub>2</sub>	Ground (Bus side)
11	V <sub>ISO</sub>	Insulation power output. The pin needs to be connected to pin16 in application.
12	CANL	Low level CAN voltage input/output
13	CANH	High level CAN voltage input/output
14	NC	No connect
15	GND <sub>2</sub>	Ground (Bus Side)
16	V <sub>ISO</sub>	Insulation power output. By using 0.1uF and 10uF ceramic capacitance ground2. The pin needs to be connected to pin11 in application.

Note : All GND<sub>1</sub> pins are internally connected; All GND<sub>2</sub> pins are internally disconnected.

## Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

PARAMETERS	UNIT
Supply voltage V <sub>CC</sub>	-0.5V to +6V
Digital input voltage V <sub>in</sub>	-0.5V to V <sub>CC</sub> +0.5V
Bus voltage (CANH , CANL)	-40 to 40V
Receiver output current I <sub>o</sub>	-15mA to +15mA
Junction temperature T <sub>J</sub>	< 150°C
Operating temperature range	-40°C to +125°C
Storage temperature range	-65°C to +150°C

Important: Exposure to absolute maximum rated conditions for an extended period may severely affect the device reliability, and stress levels exceeding the "Absolute Maximum Ratings" may result in permanent damage.

## Recommended Operating Conditions

PARAMETERS		Min.	Nom.	Max.	Unit
V <sub>CC</sub>	Power supply	4.5	5	5.5	V
V <sub>I</sub> or V <sub>IC</sub>	Voltage at any bus terminal (differential mode)	-12		12	V
V <sub>IH</sub>	High-level input voltage (TXD)	2		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage (TXD)	-0.3		0.8	V
V <sub>ID</sub>	Differential input voltage	-7		7	V
I <sub>OH</sub>	High-level output current	Driver			mA
		Receiver	-70		
I <sub>OL</sub>	Low-level output current	Driver		70	mA
		Receiver		2.5	
T <sub>A</sub>	Operating temperature range	-40		125	°C
T <sub>J</sub>	Junction temperature	-40		150	°C
P <sub>D</sub>	Total power consumption	V <sub>CC</sub> = 5.5V, T <sub>A</sub> = 125°C, R <sub>L</sub> = 60Ω; TXD signal: f=500kHz; Duty=50%		900	mW
T <sub>J(shutdown)</sub>	Thermal shutdown temperature		165		°C

	Signaling rate			1000	kbps
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## Electrical Characteristics

General test conditions and  $V_{CC}=V_{ISO}=5V$ ,  $T_a = 25^\circ C$  (unless otherwise specified).

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
<b>Driver</b>						
VO(D)	Dominant CANH output voltage	Figure 8 $V_{TXD} = 0V$ , $R_L = 60\ \Omega$	2.9	3.4	4.5	V
	Dominant CANL output voltage		0.5		2	
VO(R)	Recessive bus voltage	Figure 8 $V_{TXD} = 2V$ , $R_L = 60\ \Omega$	2	2.5	3	V
VOD(D)	Differential output voltage	Figure 8 $V_{TXD} = 0V$ , $t < t_{lo(dom)TXD}$ , $V_{CC}=4.75V$ to $5.25V$ , $R_L = 45\ \Omega$	1.5		3	V
		Figure 8 $V_{TXD} = 0V$ , $R_L = 60\ \Omega$	1.3		3	V
VOD(R)	Recessive differential output voltage	Figure 8 $V_{TXD} = 3V$ , $R_L = 60\ \Omega$	-0.8		0.08	V
		$V_{TXD} = 3V$ , No load	-0.5		0.05	
VOC(D)	Common-mode output voltage		2	2.5	3	V
VOC(PP)	Common-mode output voltage peak to peak			60		mV
I <sub>IH</sub>	TXD High-level input current	$V_{TXD} = 2V$			20	$\mu A$
I <sub>IL</sub>	TXD Low-level input current	$V_{TXD} = 0.8V$	-20			$\mu A$
CMTI	Common mode transient immunity	$V_I = 0V$ or $V_{CC}$	100	150		$kV/\mu S$
<b>Receiver</b>						
V <sub>IT+</sub>	Positive-going input threshold voltage	Figure 11		800	900	mV
V <sub>IT-</sub>	Negative-going input threshold voltage		500	650		mV
V <sub>hys</sub>	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )		50	125		mV
V <sub>OH</sub>	High-level output voltage	$I_{OH} = -4mA$ , Figure 9	$V_{CC} - 0.8$	4.8		V
		$I_{OH} = -20\ \mu A$ , Figure 9	$V_{CC} - 0.1$	5		
V <sub>OL</sub>	Low-level output voltage	$I_{OL} = 4mA$ , Figure 9		0.2	0.4	V
		$I_{OL} = 20\ \mu A$ , Figure 9		0	0.1	
C <sub>I</sub>	Input capacitance to ground (CANH or CANL)	$V_{TXD} = 3V$ , $V_I = 0.4 \sin(4E6\ \pi t) + 2.5V$		13		pF
C <sub>ID</sub>	Differential input capacitance	$V_{TXD} = 3V$ , $V_I = 0.4 \sin(4E6\ \pi t)$		5		pF
R <sub>ID</sub>	Input resistance (CANH or CANL)	$V_{TXD} = 3V$	28	32	36	$k\ \Omega$
R <sub>IN</sub>	Differential input resistance	$V_{TXD} = 3V$	56	62	68	$k\ \Omega$
R <sub>I(m)</sub>	Input resistance matching: [1 - $R_{IN(CANH)} / R_{IN(CANL)}$ ] × 100%	$V_{CANH} = V_{CANL}$	-5%	0%	5%	
<b>Power supply and safeguard characteristic</b>						
V <sub>ISO</sub>	Isolated power supply output voltage	No load, $I_{ISO}=0mA$	4.65	5.05	5.47	V
I <sub>VCC</sub>	Logic side supply current	$V_I = 0V$ , $R_L = 60\ \Omega$ , Dominant	14	20	29	mA
		$V_I = V_{CC}$ , Recessive	14	20	29	
ESD	HBM	CANH, CANL pin to GND			±5	kV
	Isolation voltage				5000	V <sub>rms</sub>
	Insulation resistance		1			G $\Omega$
	Isolation capacitor			3		pF

## Transmission Characteristics

General test conditions and  $V_{CC}=V_{ISO}=5V$ ,  $T_a = 25^\circ C$  (unless otherwise specified).

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
t <sub>onTXD</sub>	Propagation delay TXD On to bus active	$R_L = 60\ \Omega$ , $C_L = 100\ pF$ , see Figure 10 and Figure 12	35	75	130	ns
t <sub>offTXD</sub>	Propagation delay TXD Off to bus inactive		35	55	100	ns
t <sub>r</sub>	Differential output rise time			40	60	ns
t <sub>f</sub>	Differential output fall time			40	60	ns

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
$t_{onRXD}$	Propagation delay RXD On to receiver active		55	110	140	ns
$t_{offRXD}$	Propagation delay RXD Off to receiver inactive		55	80	140	ns
$t_r$	Output rise time			2.5	6	ns
$t_f$	Output fall time			2.5	6	ns
$T_{loop}$	Loop delay time		110	150	210	ns
$t_{TXD\_DTC}$	Dominant time-out time	$C_L=100\text{ pF}$	300	450	700	us

## Physical Specifications

PARAMETERS	Value	Unit
Weight	0.4(Typ.)	g

## Test Circuits

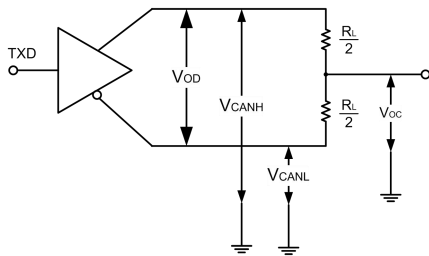


Figure 8. Driver test circuit

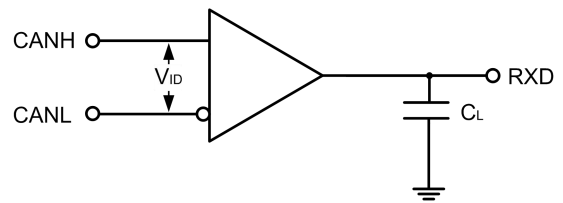


Figure 9. Receiver test circuit

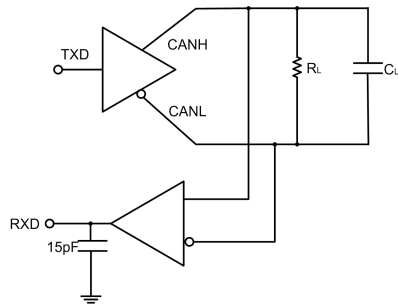


Figure 10. Switching characteristics test circuit

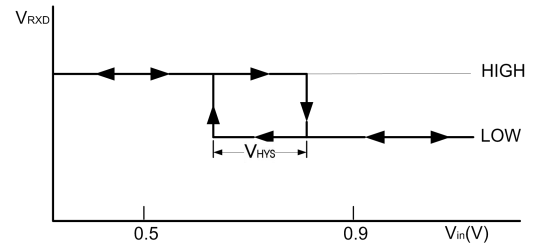


Figure 11. Receiver input hysteresis

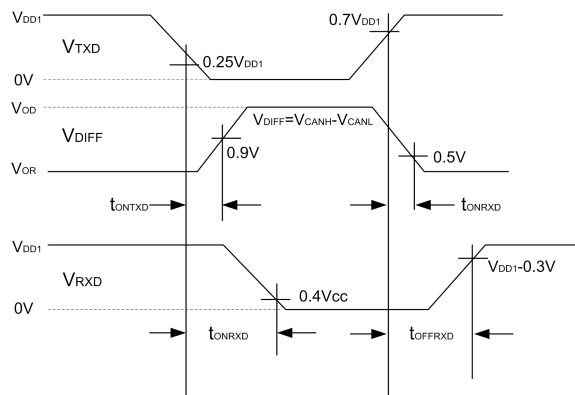


Figure 12. Drive and receiver propagation delay

## Detailed Description

TDA51SCANHC is a CAN of a style of separation transceiver with the ability of differential signal transmission between the bus and CAN protocol controller, it the inner integration insulate DC/DC power supply. which is compliant with ISO11898-2 standard.

Short-circuit protection: TDA51SCANHC has current-limiting protection to prevent the drive circuit from short-circuiting to positive and negative supply voltages. The power dissipation increases when a short circuit occurs. The short-circuit protection function protects the driver stage from damage.

Over-temperature protection: TDA51SCANHC has over-temperature protection. When the junction temperature exceeds 160°C, the current in the driver stage will decrease. Because the drive tube is the primary energy consuming component, current reduction can reduce power consumption and reduce chip temperature. At the same time, the rest of the chip remains functional.

Dominant time-out function: TDA51SCANHC has dominant time-out function to prevent if the pin TXD is forced to a permanent low level due to a hardware or software application failure, the built-in TXD dominant timeout timer circuit prevents the bus line from being driven to a permanent dominant state (blocking all network traffic). The timer is triggered by the negative edge on pin TXD.

If the low level on pin TXD lasts longer than the internal timer value ( $t_{TXD\_DTC}$ ), the transmitter will be disabled and the drive bus will enter a recessive state. The timer is reset by the positive edge on pin TXD.

## Application circuit

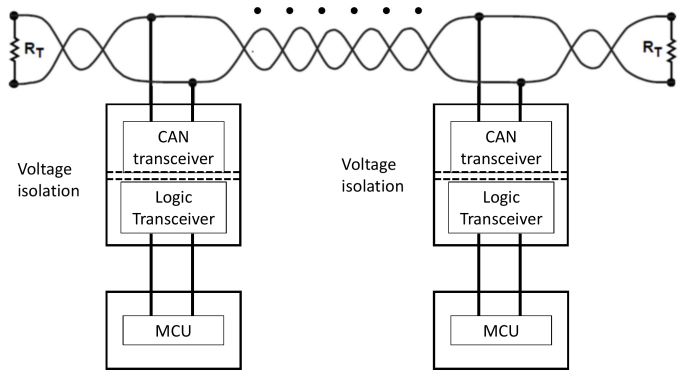


Figure 13. The typical model applies telephone

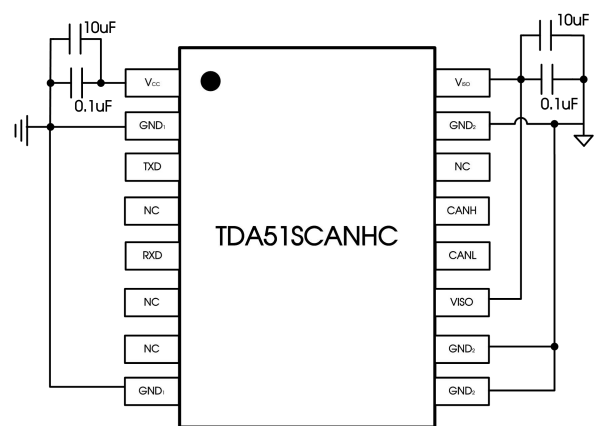


Figure 14. Type PCB layout

### PCB Design Instructions

1. The decoupling capacitors and energy storage capacitor of VCC and GND1, VISO and GND2 should be placed as close the chip pins as possible to the chip pins to reduce loop area and parasitic inductance of PCB traces. General control should be within 2mm. The decoupling capacitor is placed close the chip, and the energy storage capacitor is placed outside. As shown in Figure 14-1.

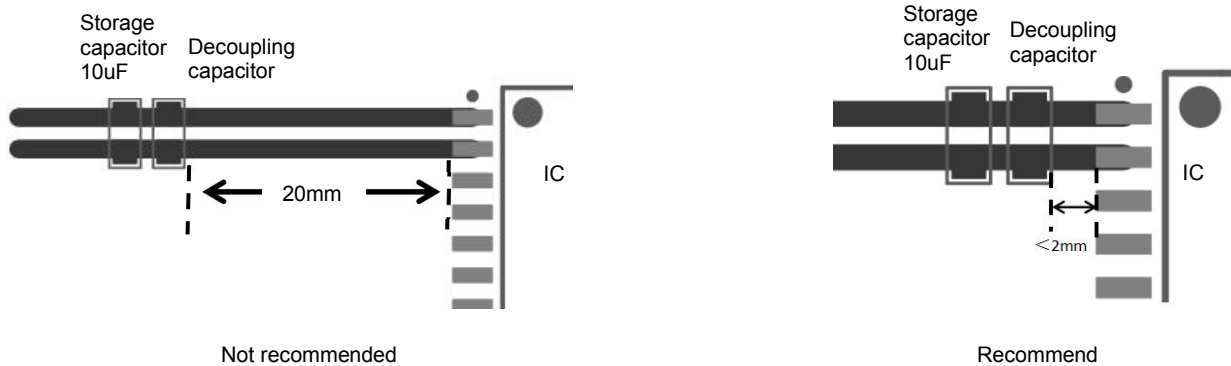


Figure 14-1

2. The power line width should be designed at least 0.5 when wiring.

3. When it is necessary to place vias in the power supply line and the ground wire, the position of the vias should be placed on the outside of the capacitor relative to the chip pins, rather than between the capacitor and the chip, as shown in the figure 14-2 below to reduce the number of vias effect of parasitic inductance.

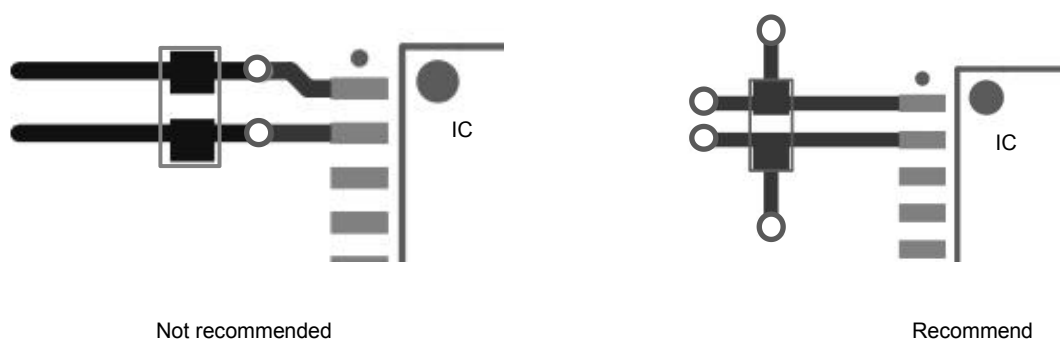


Figure 14-2

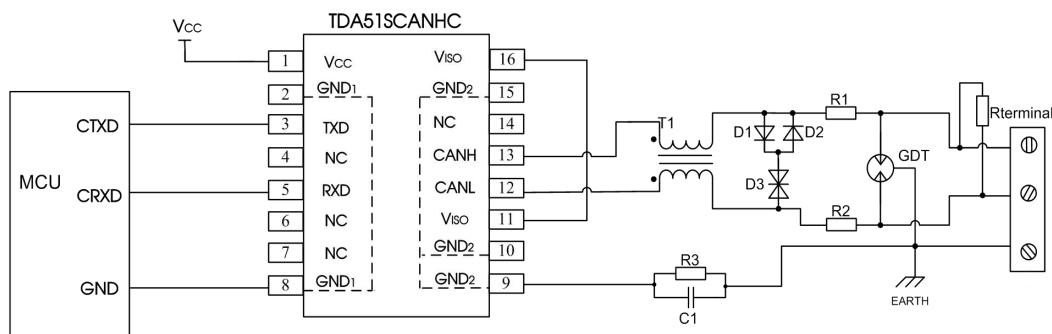


Figure 15. Port protection circuit for harsh environments

Recommended components and values:

Component	Recommended part, value	Component	Recommended part, value
R3	1MΩ	D1、D2	1N4007
C1	1nF, 2kV	D3	SMBJ30CA
T1	ACM2520-301-2P	R <sub>terminal</sub>	120 Ω
GDT	B3D090L	R1、R2	2.7Ω/2W

When the module is used in applications with harsh environment, it can be susceptible to large energy like lightning strike, etc. in which case, it is essential to add an adequate protection circuit to the CAN signal ports to protect the system from failure and maintain a reliable bus communication. Figure 15 provides a recommended protection circuit design for high-energy lightning surges, with a degree of protection related to the selected

protection device. Parameter description lists a set of recommended circuit parameters, which can be adjusted according to the actual application situation. Also, when using the shielded cable, the reliable single-point grounding of the shield must be achieved.

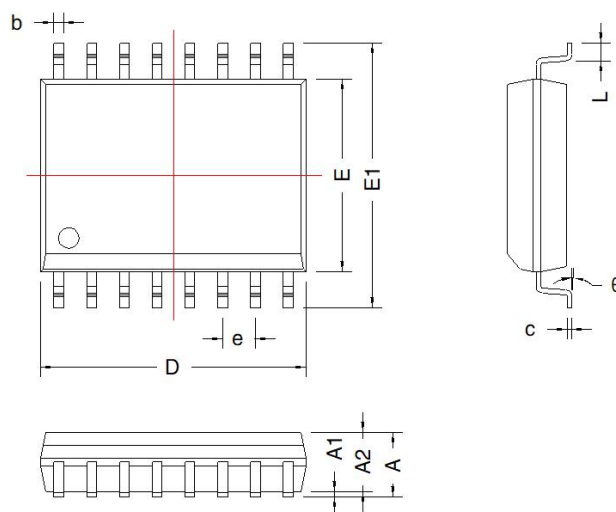
Note: The recommended components and values is a general guideline only and must be verified for the actual user's application. We recommended using PTC's for R1 and R2 and to use fast recovery diodes for D1 and D2.

## Ordering Information

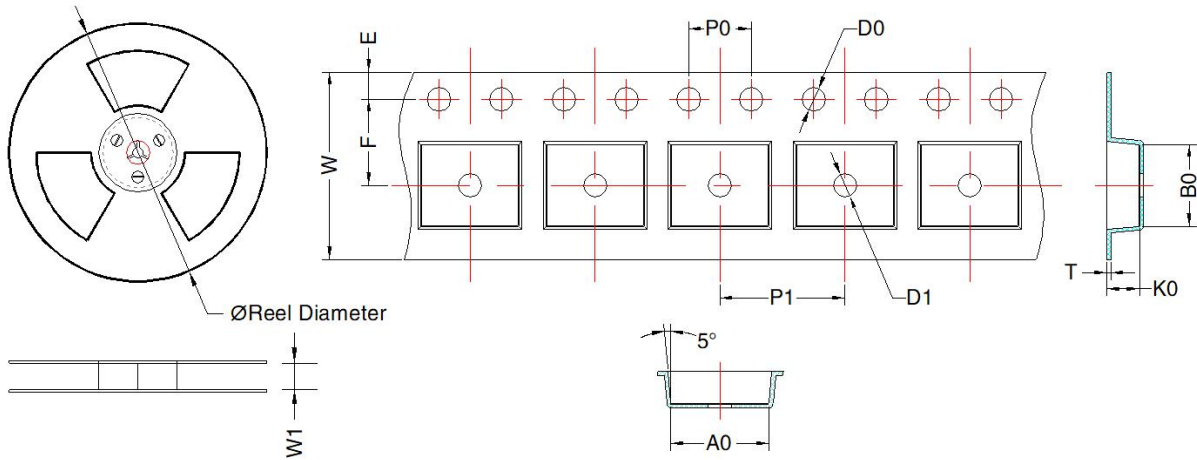
Part number	Package	Number of pins	Product marking	Tape & Reel
TDA51SCANHC	SOIC	16	TDA51SCANHC	1K/REEL

## Package Information

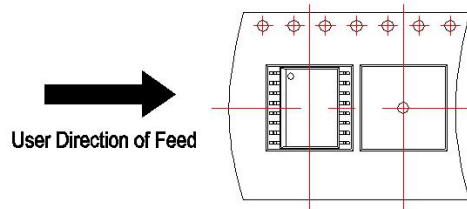
THIRD ANGLE PROJECTION 



SOIC-16				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
A2	2.25	2.35	0.089	0.093
D	10.2	10.4	0.402	0.409
E	7.4	7.6	0.291	0.299
E1	10.1	10.5	0.340	0.413
L	0.55	0.85	0.022	0.033
b	0.35	0.43	0.014	0.017
e	1.27TYP		0.05TYP	
c	0.15	0.30	0.006	0.012
$\theta$	0°	8°	0°	8°



The orientation of IC in tape



Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)
TDA51SCANHC	SOIC-16	1000	330.0	24.4	10.8 ± 0.2	10.7 ± 0.2	2.9 ± 0.2	0.3 ± 0.05	24.0 ± 0.3	1.75 ± 0.1	10.5 ± 0.1	12.0 ± 0.1	4.0 ± 0.1	1.5 ± 0.1	1.5 ± 0.1

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