

N-channel 950 V, 2 Ω typ., 3.5 A MDmesh™ K5
Power MOSFETs in DPAK, TO-220FP, TO-220 and IPAK

Datasheet - production data

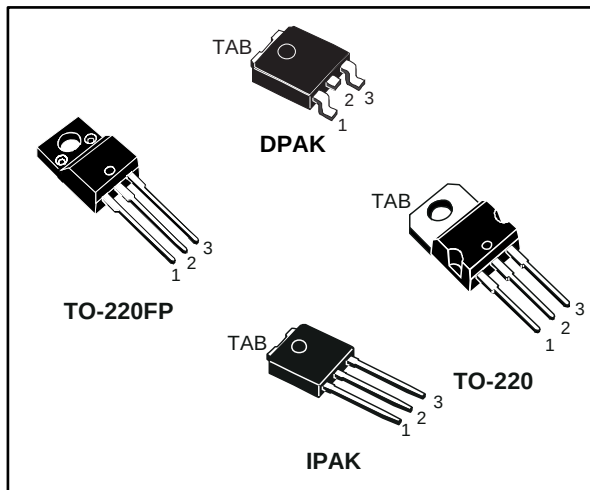
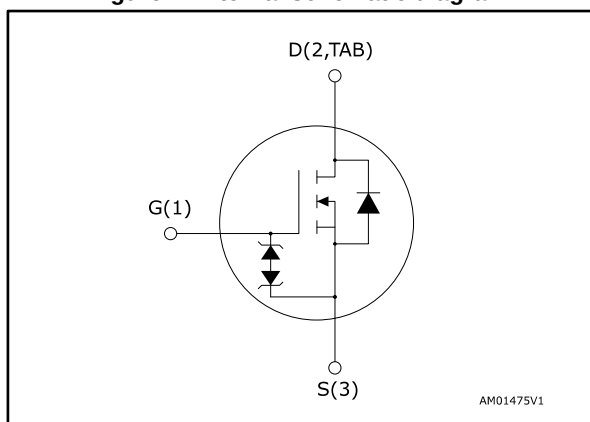


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{tot}
STD5N95K5	950 V	2.5 Ω	3.5 A	70 W
STF5N95K5				25 W
STP5N95K5				70 W
STU5N95K5				70 W

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STD5N95K5	5N95K5	DPAK	Tape and reel
STF5N95K5		TO-220FP	Tube
STP5N95K5		TO-220	
STU5N95K5		IPAK	

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	9
4	Package information	10
4.1	DPAK (TO-252) type A2 package information.....	11
4.2	DPAK (TO-252) type C2 package information	14
4.3	DPAK (TO-252) packing information.....	17
4.4	TO-220FP package information	19
4.5	TO-220 type A package information.....	21
4.6	IPAK (TO-251) type A package information	23
5	Revision history	25

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	TO-220FP	
V _{GS}	Gate-source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	3.5	3.5 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	2.2	2.2 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current pulsed	14		A
P _{TOT}	Total dissipation at T _C = 25 °C	70	25	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)		2500	V
T _j	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			

Notes:⁽¹⁾Limited by maximum junction temperature.⁽²⁾Pulse width limited by safe operating area.⁽³⁾I_{SD} ≤ 3.5 A, di/dt ≤ 100 A/μs, V_{DS} (peak) ≤ V_{(BR)DSS}⁽⁴⁾V_{DS} ≤ 640 V

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	TO-220	IPAK	
R _{thj-case}	Thermal resistance junction-case	1.47	5	1.47		°C/W
R _{thj-amb}	Thermal resistance junction-ambient		62.5		100	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	50				°C/W

Notes:⁽¹⁾When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	1	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	70	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	950			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 950\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 950\text{ V}$, $V_{GS} = 0\text{ V}$ $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			50	μA
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.5\text{ A}$		2	2.5	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	220	-	pF
C_{oss}	Output capacitance		-	17	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }760\text{ V}$	-	30	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	11	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	17	-	Ω
Q_g	Total gate charge	$V_{DD} = 760\text{ V}$, $I_D = 3.5\text{ A}$	-	12.5	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$	-	2	-	nC
Q_{gd}	Gate-drain charge	(see Figure 19: "Test circuit for gate charge behavior")	-	10	-	nC

Notes:

⁽¹⁾ $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁽²⁾ $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$, $I_D = 1.75\text{ A}$, $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see Figure 18: "Test circuit for resistive load switching times" and Figure 23: "Switching time waveform")	-	12	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
t_f	Fall time		-	25	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.5	A
I_{SDM}	Source-drain current (pulsed)		-		14	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 3.5\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 3.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 20: "Test circuit for inductive load switching and diode recovery times")	-	330		ns
Q_{rr}	Reverse recovery charge		-	2.2		μC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	$I_{SD} = 3.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 20: "Test circuit for inductive load switching and diode recovery times")	-	525		ns
Q_{rr}	Reverse recovery charge		-	3.2		μC
I_{RRM}	Reverse recovery current		-	12		A

Notes:⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for DPAK and IPAK

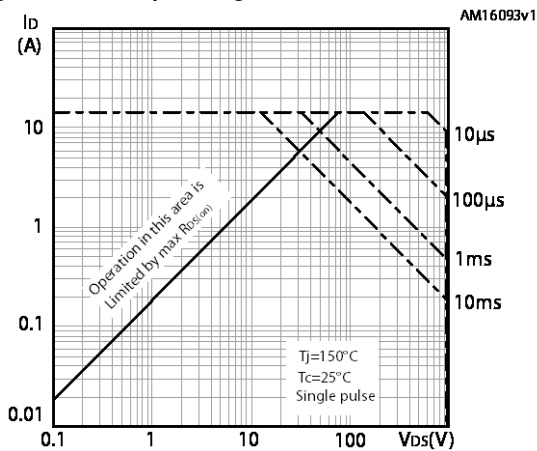


Figure 3: Thermal impedance for DPAK and IPAK

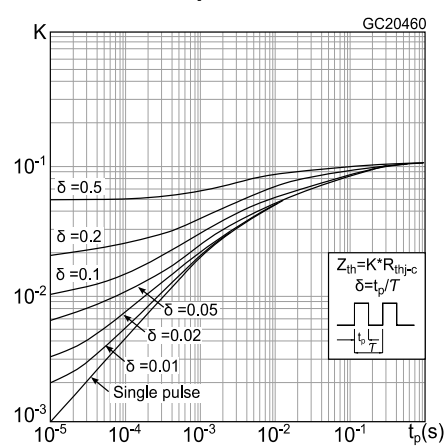


Figure 4: Safe operating area for TO-220FP

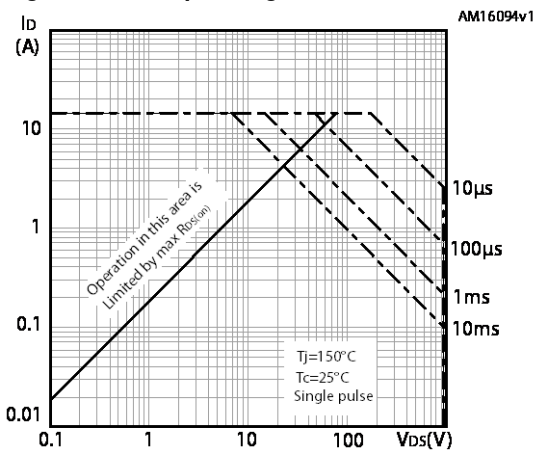


Figure 5: Thermal impedance for TO-220FP

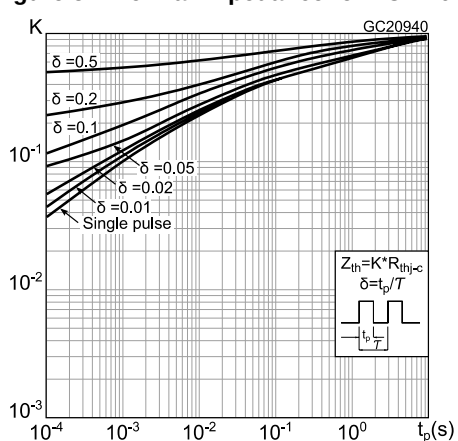


Figure 6: Safe operating area for TO-220

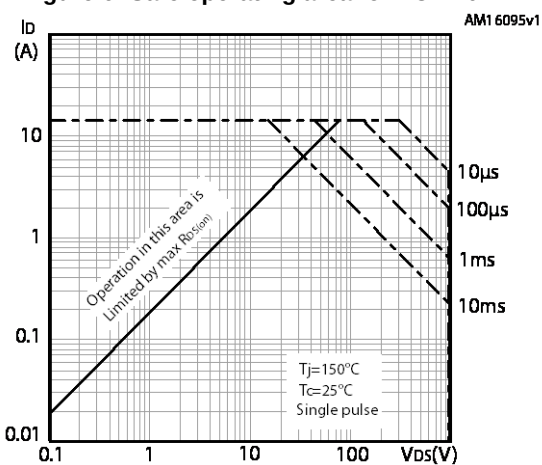
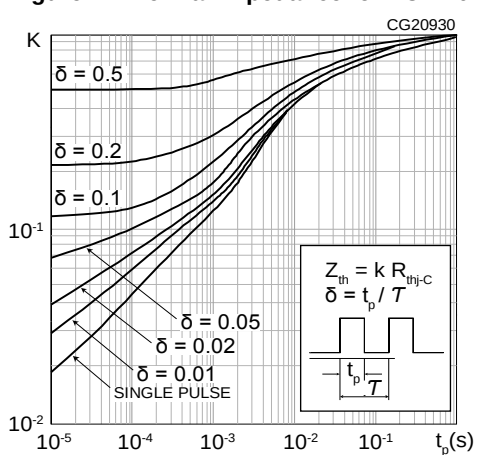


Figure 7: Thermal impedance for TO-220



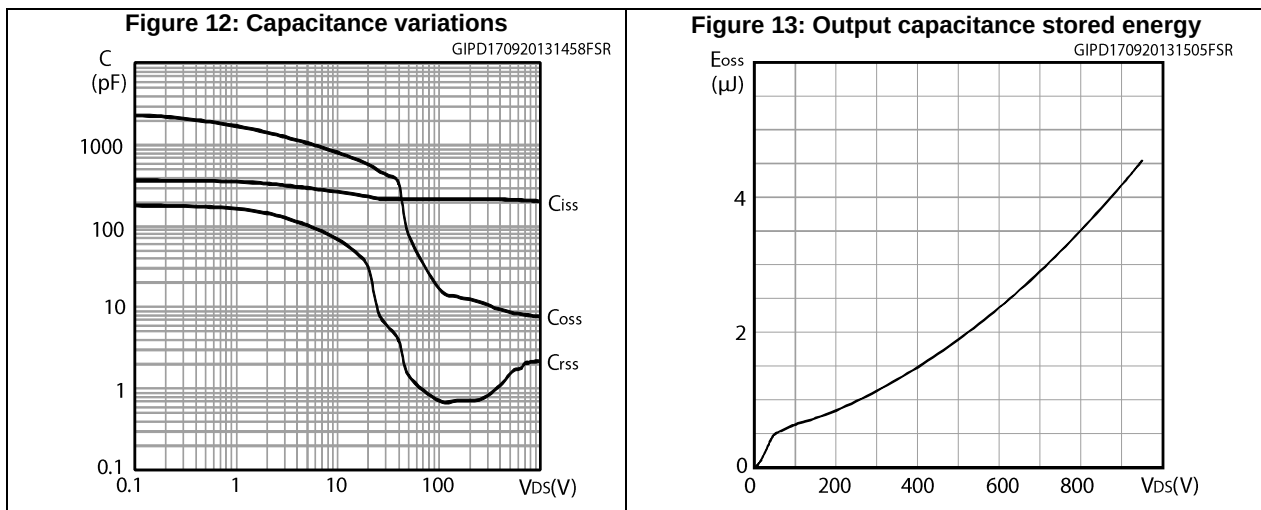
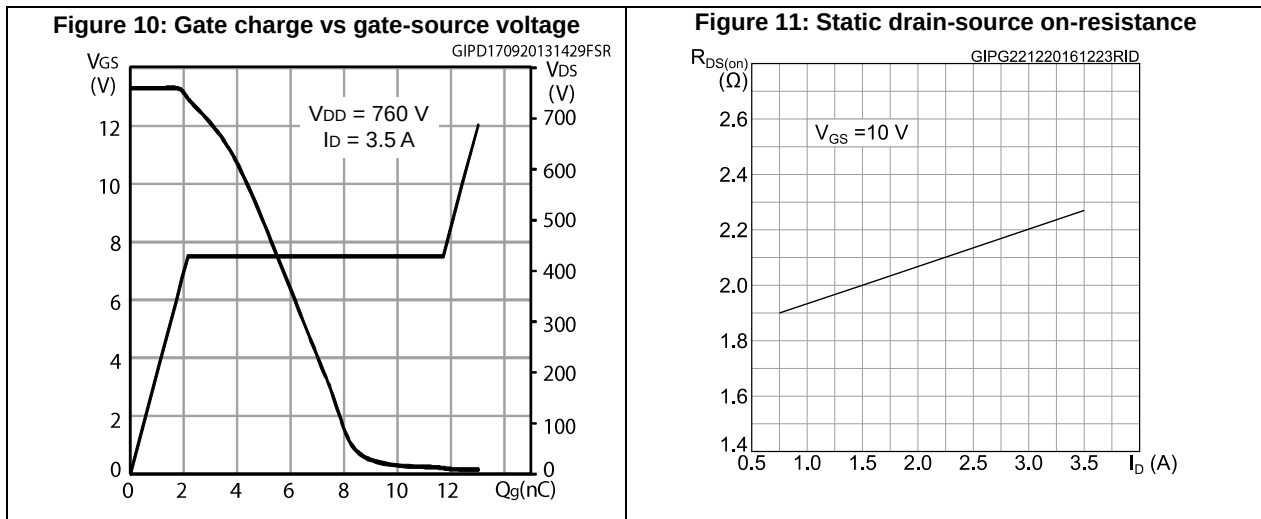
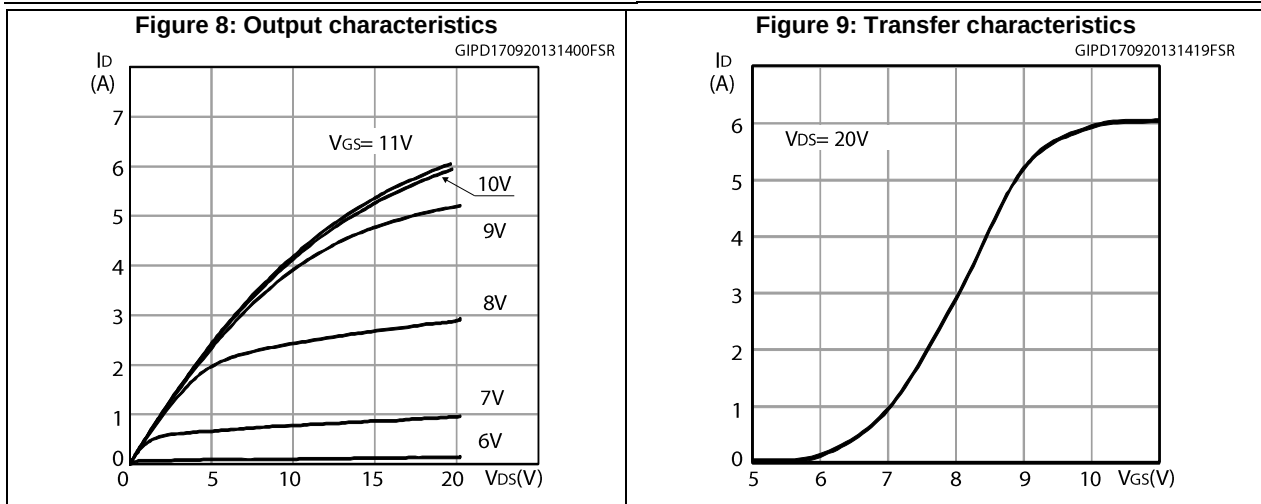


Figure 14: Normalized gate threshold voltage vs temperature

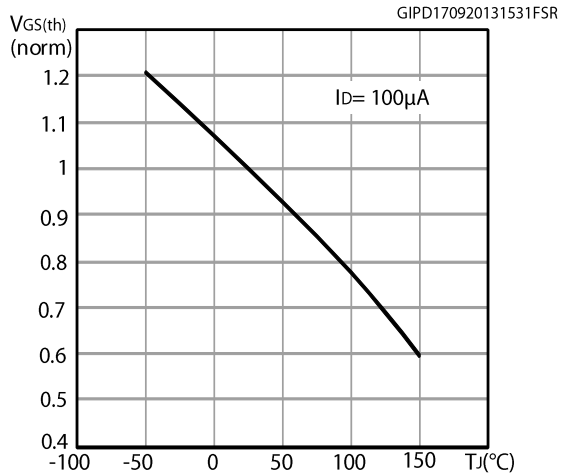


Figure 15: Normalized $V_{(BR)DSS}$ vs temperature

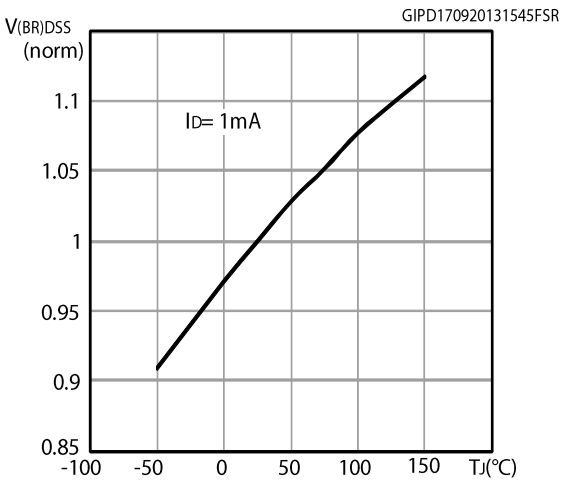


Figure 16: Normalized on-resistance vs temperature

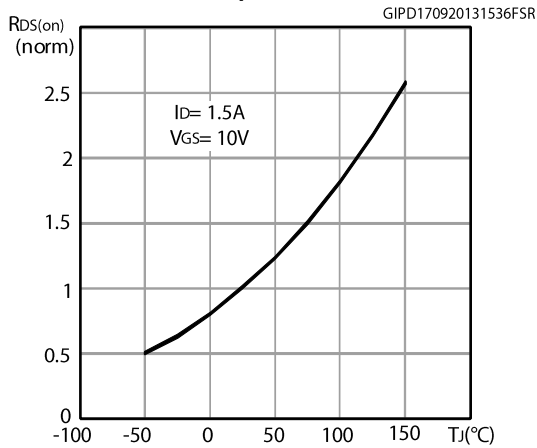
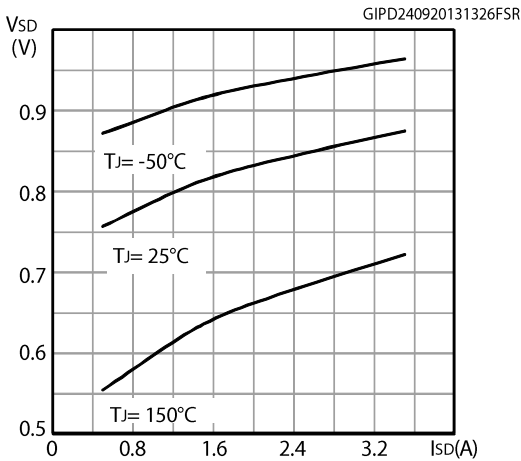
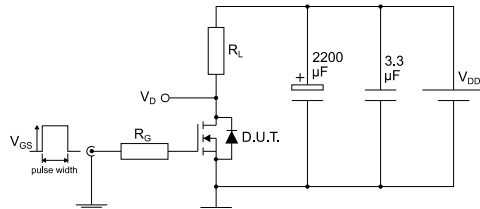


Figure 17: Source-drain diode forward characteristics



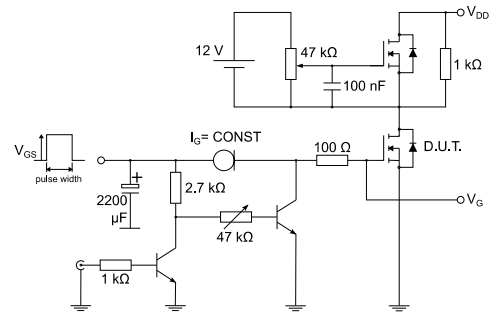
3 Test circuits

Figure 18: Test circuit for resistive load switching times



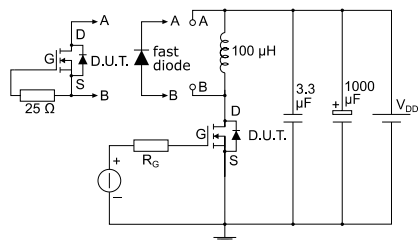
AM01468v1

Figure 19: Test circuit for gate charge behavior



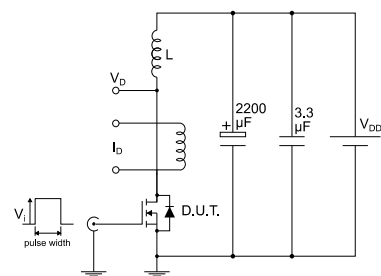
AM01469v1

Figure 20: Test circuit for inductive load switching and diode recovery times



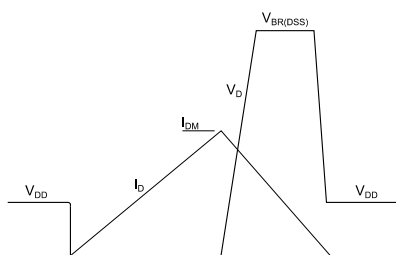
AM01470v1

Figure 21: Unclamped inductive load test circuit



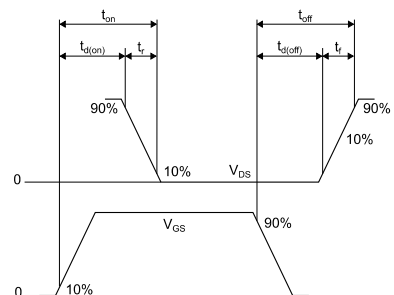
AM01471v1

Figure 22: Unclamped inductive waveform



AM01472v1

Figure 23: Switching time waveform



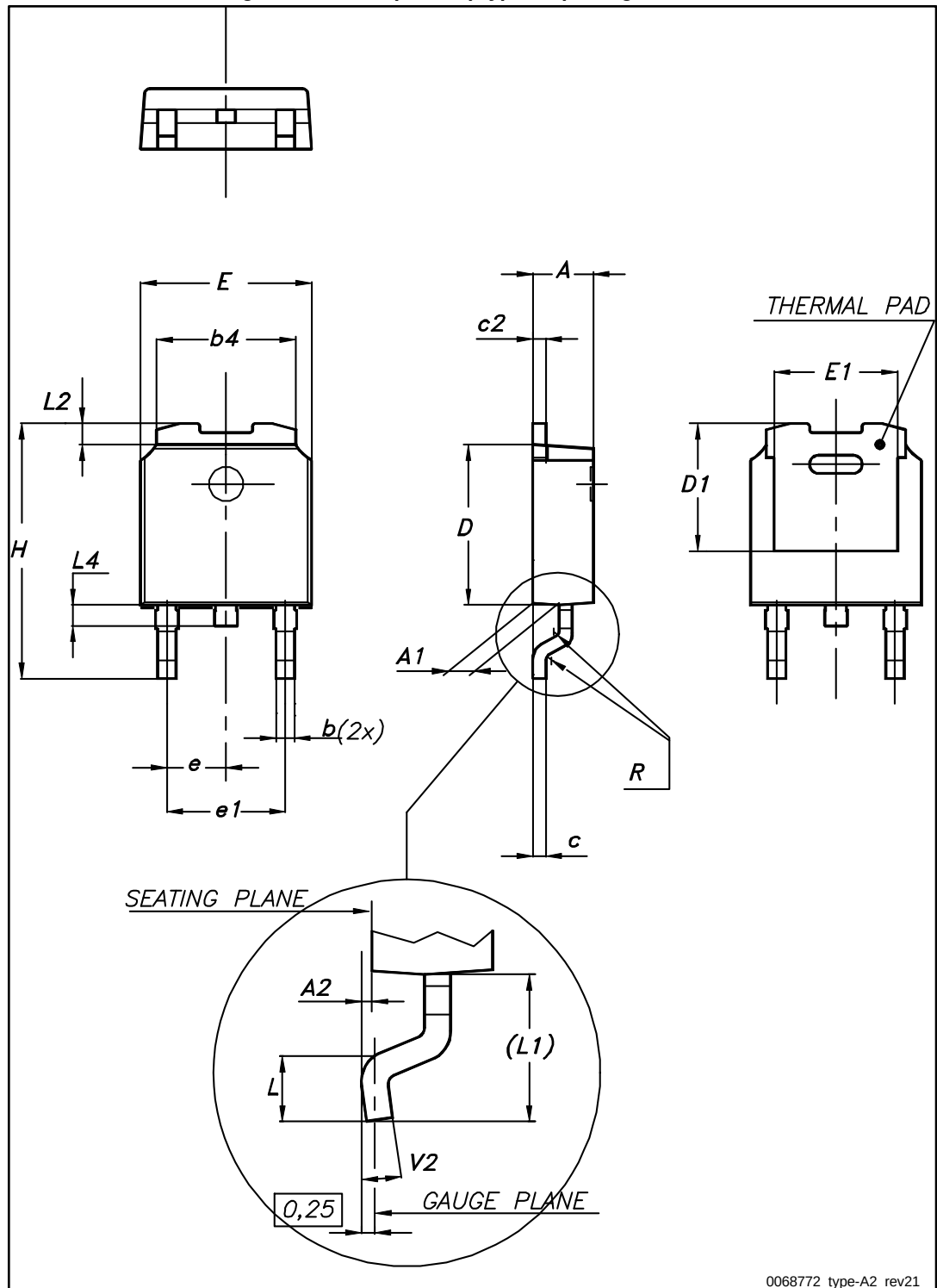
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 24: DPAK (TO-252) type A2 package outline

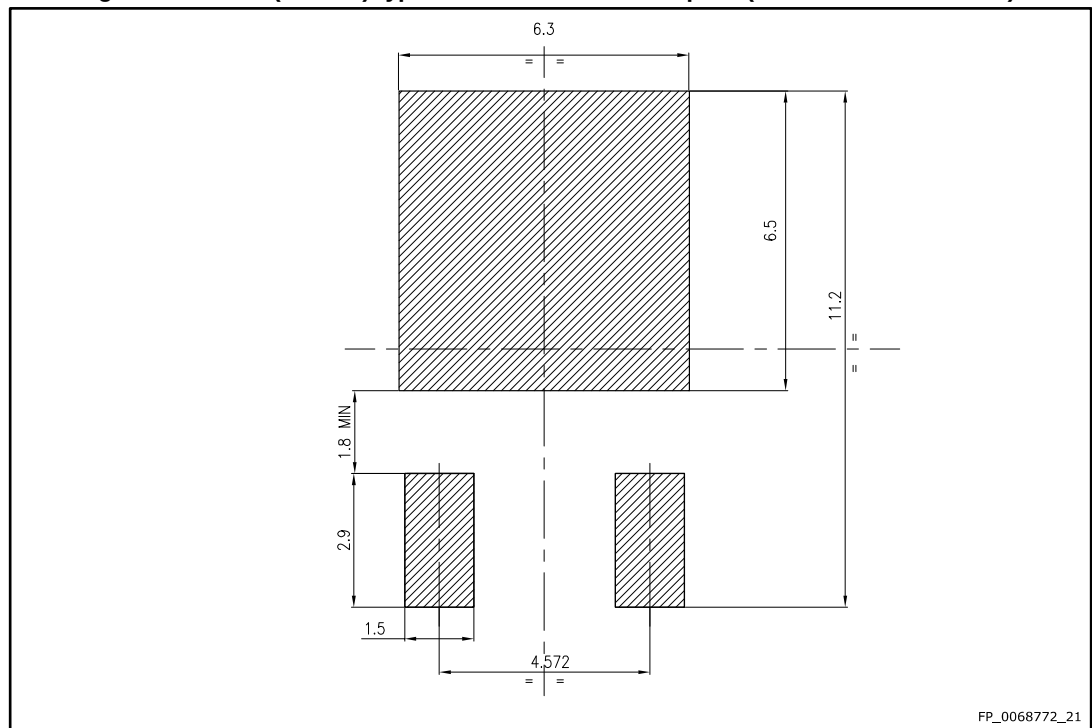


0068772_type-A2_rev21

Table 10: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) type C2 package information

Figure 26: DPAK (TO-252) type C2 package outline

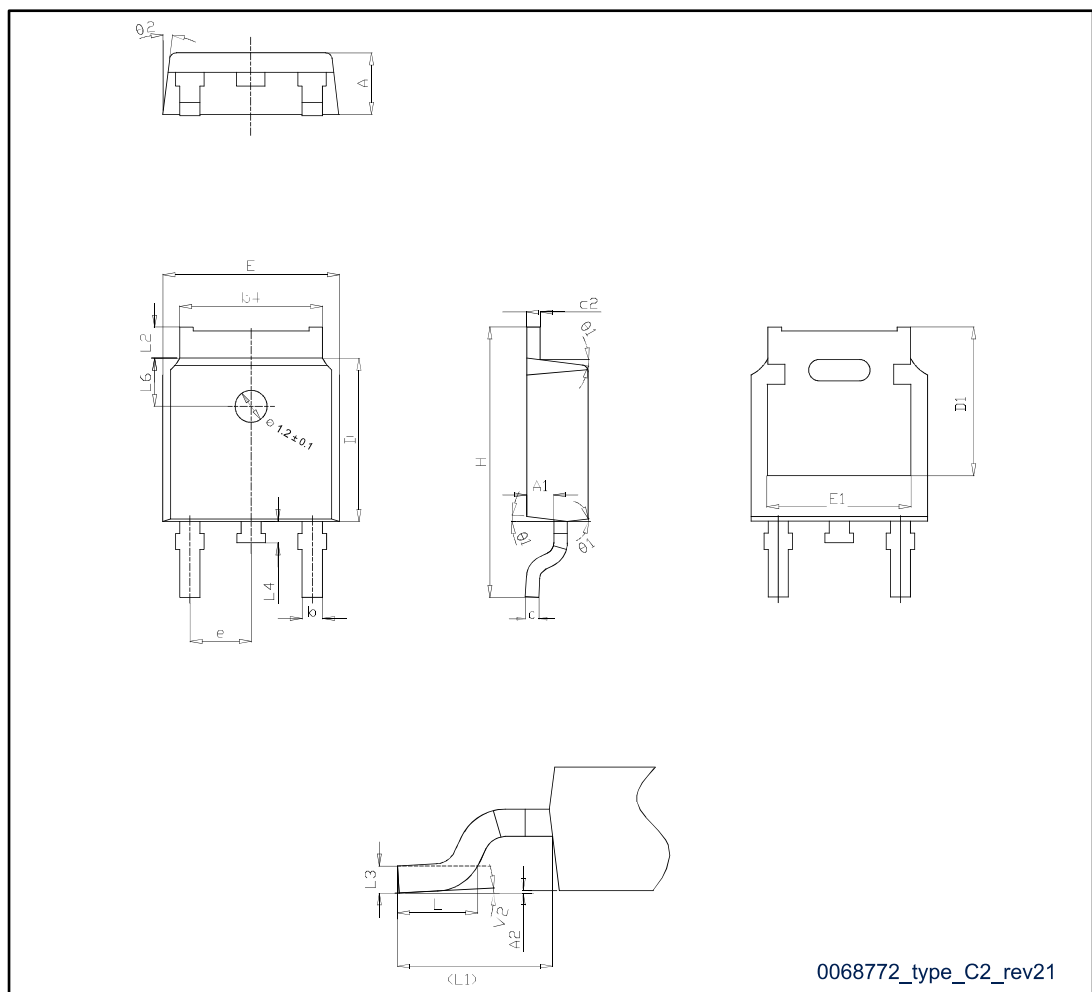


Table 11: DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Technical drawing of a mechanical part, likely a bracket or support, showing dimensions in millimeters (mm). The drawing includes a top view and a side view.

Top View Dimensions:

- Overall width: 6.3
- Overall height: 11.2
- Width of the central rectangular feature: 6.5
- Width of the left rectangular feature: 2.9
- Width of the right rectangular feature: 1.5
- Distance between the centers of the two rectangular features: 4.572
- Minimum distance from the top edge to the center of the left rectangular feature: 1.8 MIN

Side View Dimensions:

- Overall height: 11.2
- Width of the central rectangular feature: 6.5
- Width of the left rectangular feature: 2.9
- Width of the right rectangular feature: 1.5
- Distance between the centers of the two rectangular features: 4.572
- Minimum distance from the top edge to the center of the left rectangular feature: 1.8 MIN

The drawing uses standard engineering notation, including dimension lines, extension lines, and center lines. The rectangular features are shaded with diagonal lines.

4.3 DPAK (TO-252) packing information

Figure 28: DPAK (TO-252) tape outline

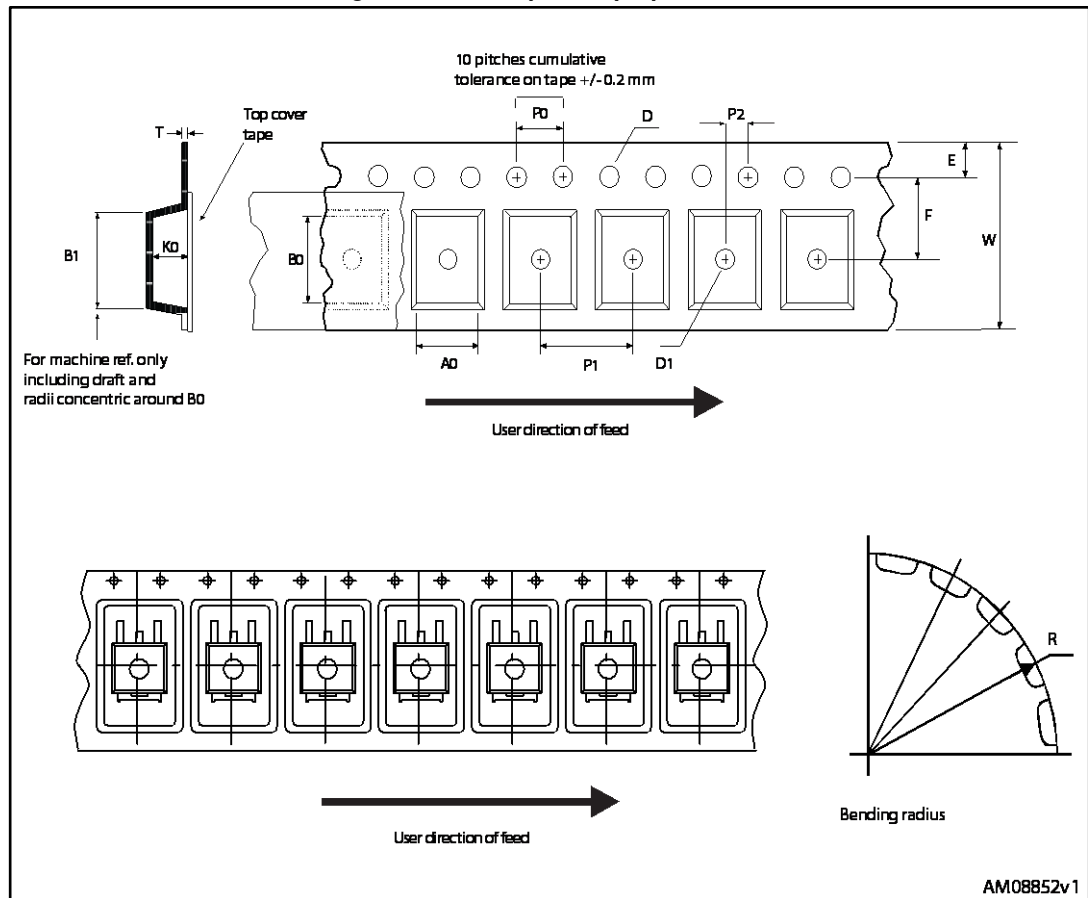


Figure 29: DPAK (TO-252) reel outline

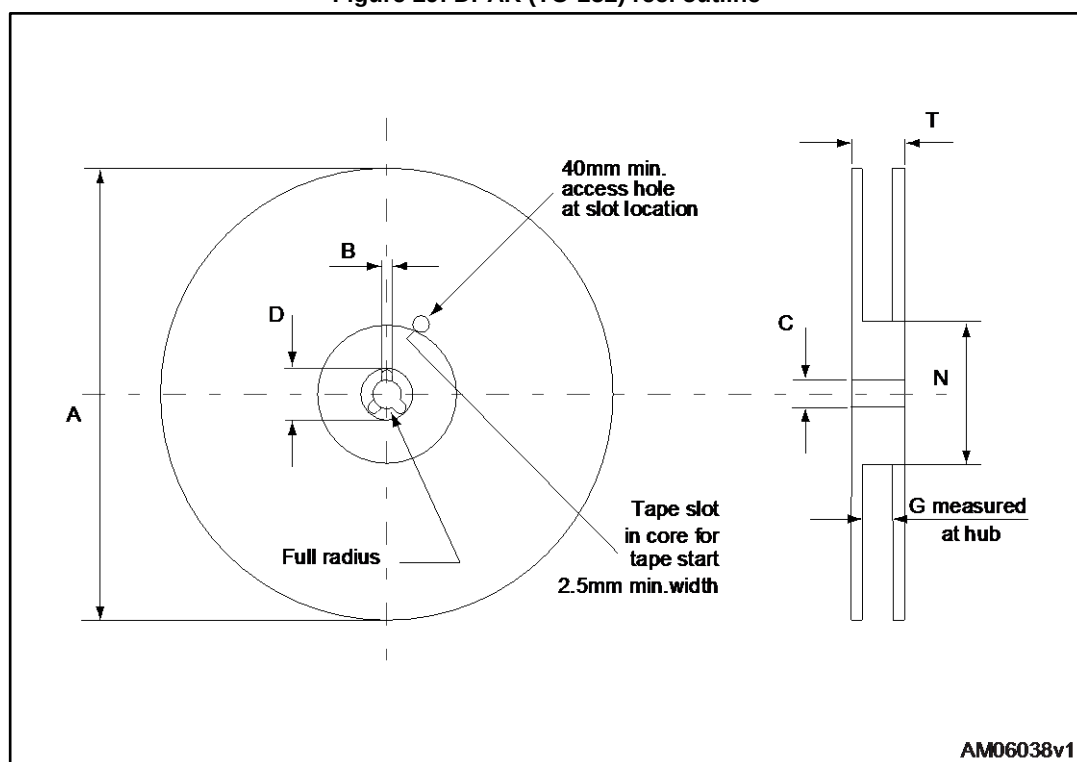


Table 12: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220FP package information

Figure 30: TO-220FP package outline

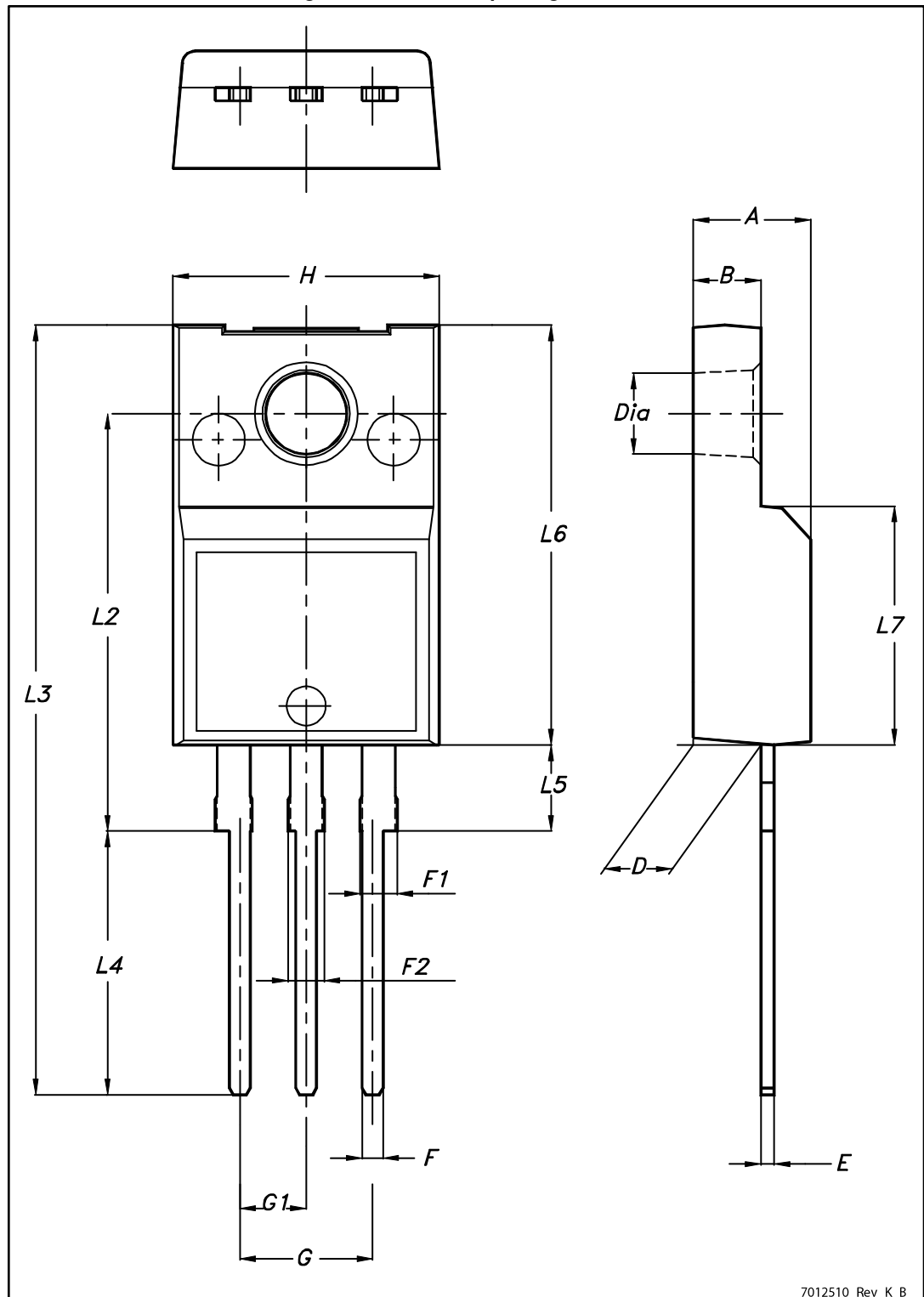


Table 13: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.5 TO-220 type A package information

Figure 31: TO-220 type A package outline

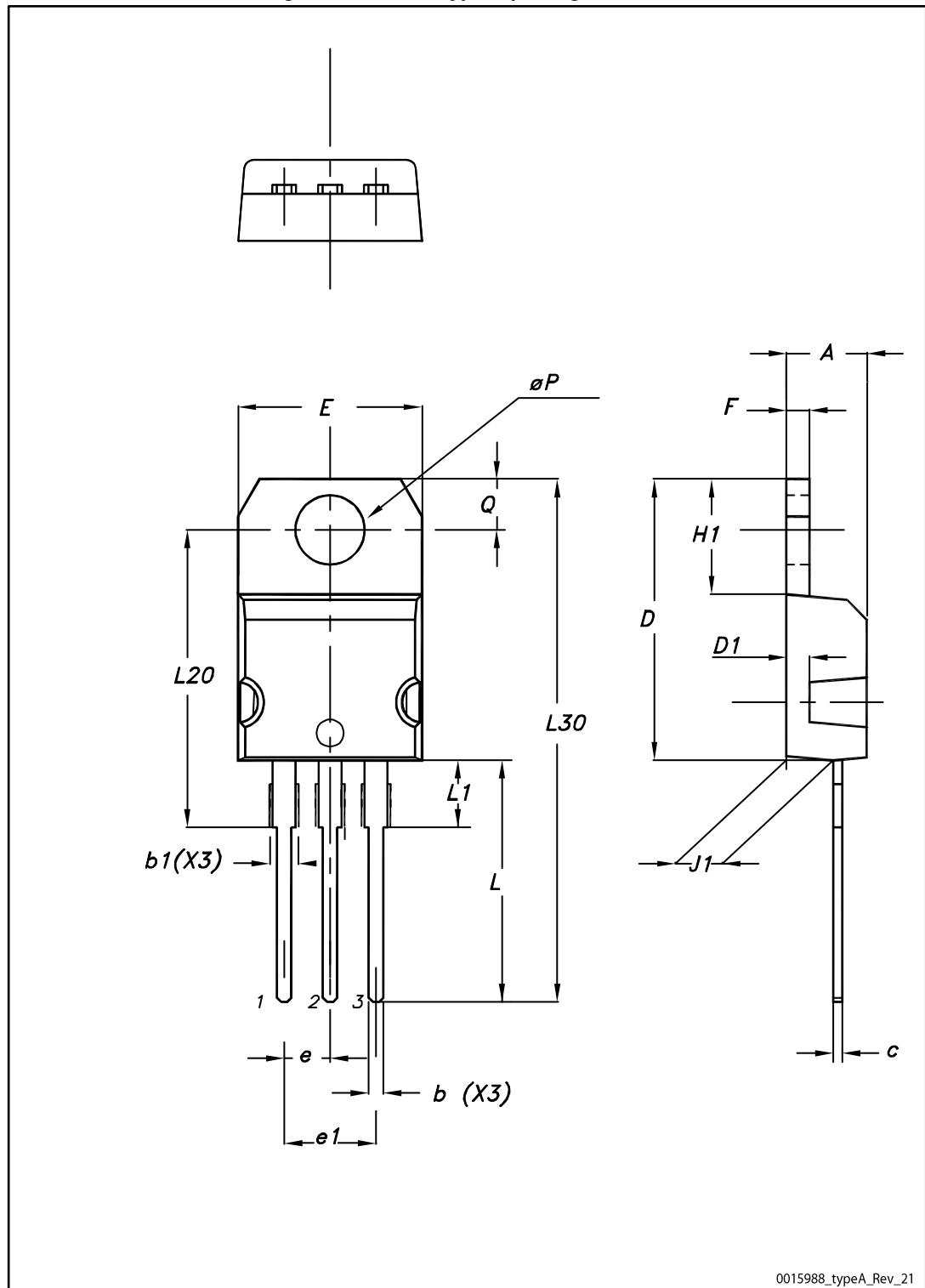


Table 14: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.6 IPAK (TO-251) type A package information

Figure 32: IPAK (TO-251) type A package outline

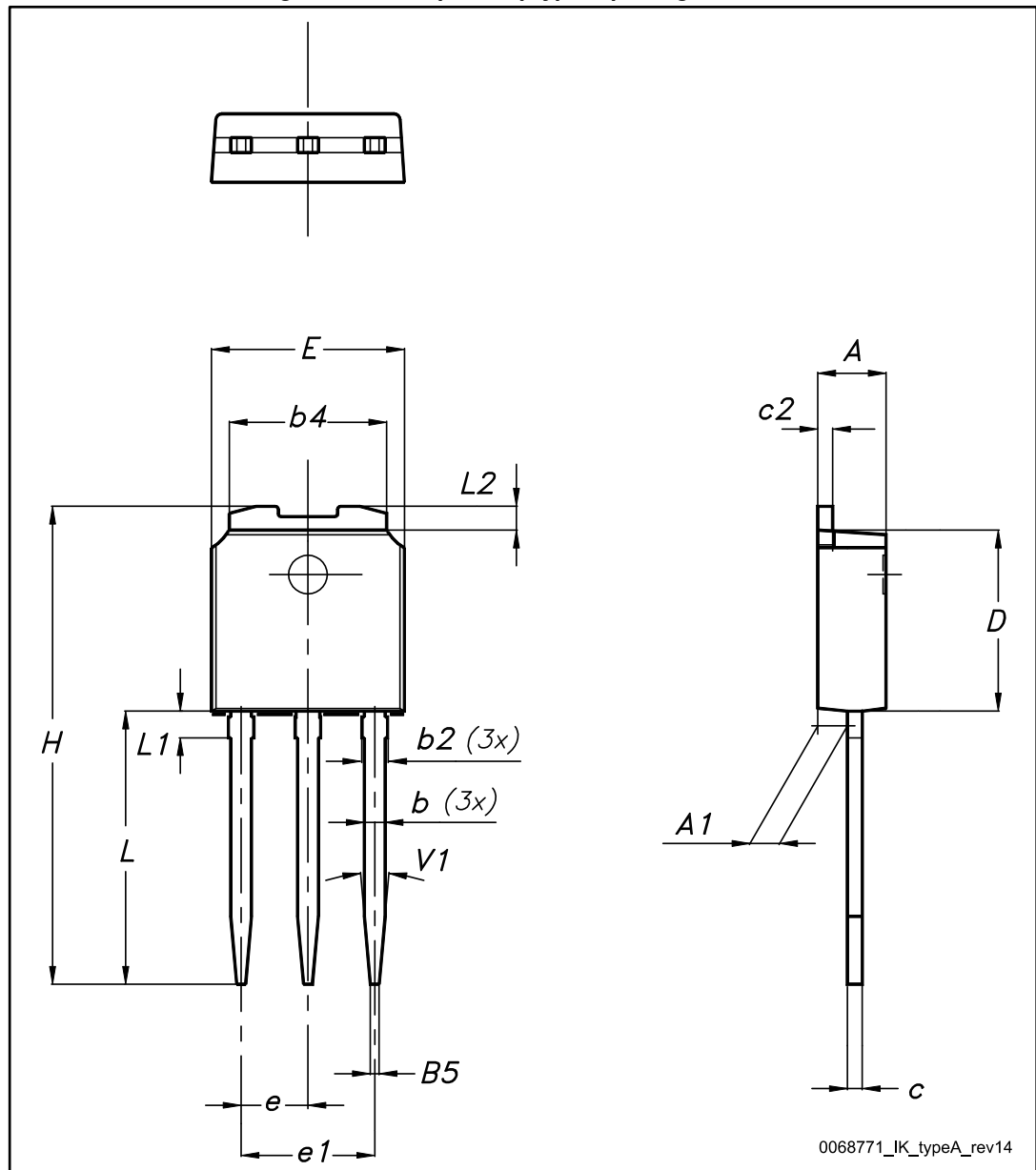


Table 15: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Revision history

Table 16: Document revision history

Date	Revision	Changes
08-May-2013	1	First release.
18-Sep-2013	2	Document status promoted from preliminary to production data. Added <i>Section 2.1: Electrical characteristics (curves)</i> . Updated DPAK mechanical data.
25-Sep-2013	3	Inserted <i>Figure 17: Source-drain diode forward characteristics</i> .
04-Jan-2017	4	Added IPAK package. Modified title, features and description on cover page. Modified Table 2: "Absolute maximum ratings" , Table 3: "Thermal data" , Table 5: "On/off-state" . Modified Figure 11: "Static drain-source on-resistance" . Updated Section 4: "Package information" . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved