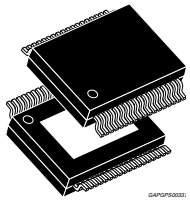
L9960 L9960T

Automotive Single/Dual H-Bridge, SPI programmable DC Brushed Motor Driver

Datasheet - production data



PowerSSO-36

Features

- AEC-Q100 qualified
- Flexible driving strategy via configurable pins PWM/DIR (IN1/IN2)
- RDSon < 400 mΩ (full path at T_j =150° C)
- Operating battery supply voltage from 4.5 V up to 28 V
- Operating VDD5 supply voltage from 4.5 V to 5.5 V
- Input switching frequency up to 20 kHz
- Built in charge pump supporting 100% duty cycle
- Logic levels compatible to 3.3 V and 5 V
- Monitoring of VDD5 supply voltage with bidirectional switch-off pin
- Current limitation SPI-adjustable in four steps.
- Output stage current limitation with dependence on temperature
- 2 Programmable voltage and current slew rate control
- Short circuit and programmable thermal warning and shutdown thresholds
- Open Load diagnosis in ON condition
- All I/O pins can withstand up to 19 V
- SPI interface for configuration and diagnosis
- Two independent enable/disable pins NDIS and DIS and SOPC (Switch-off Path Check) available
- Spread Spectrum function for EMI reduction
- Available in single (L9960) and Twin (L9960T) option, both in PSSO36 package

Description

The device is an integrated H-Bridge for resistive and inductive loads for automotive applications. Target application includes throttle control actuators, exhaust gas recirculation control valves and general purpose DC motors such as turbo, flap control and electric pumps.

The driving strategy is enhanced by configurable PWM / DIR pins and IN1/IN2.

The H-Bridge contains integrated free-wheel diodes. In case of freewheeling condition, the low-side only is switched on in parallel of its diode to reduce power dissipation.

The integrated Serial Peripheral Interface (SPI) makes it possible to adjust device parameters, to control all operating modes and read out diagnostic information.

Table 1. Device summary

Order code	Package	Packing
L9960	PowerSSO-36	Tube
L9960TR		Tape and Reel
L9960T		Tube
L9960T-TR		Tape and Reel

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Contents

1 **Block diagram and pin description 8**
1.1 Block diagram 8
1.2 Pin description 9
1.2.1 PowerSSO36 package 9

2 **Application description 12**
2.1 Application circuit 12
2.2 Bill of materials 13

3 **General electrical characteristics 14**
3.1 Absolute maximum ratings 14
3.2 Thermal ratings 15
3.3 Range of functionality 15
3.4 Electrical characteristics 16
3.5 Timing characteristics 17

4 **Functional description 18**
4.1 Device supply 18
4.1.1 Functional State 18
4.1.2 Vps power supply 18
4.1.3 VDD5 regulated voltage supply 22
4.1.4 VDDIO voltage supply 26
4.1.5 Device supply electrical characteristics 27
4.2 Power on reset (POR) and SW reset 27
4.2.1 Power on reset (POR) electrical characteristics 29
4.3 System clock electrical characteristics 29
4.4 Hardware self check (HWSC) and LBIST 30
4.4.1 HWSC test procedure 30
4.4.2 HWSC/LBIST electrical characteristics 32
4.5 Digital input controls 33
4.5.1 Bridge functional modes 33
4.5.2 Disable inputs DIS and NDIS 36
4.5.3 Control inputs DIR and PWM 37
4.5.4 Digital inputs control electrical characteristics 41

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4.6 Driver configuration 42
4.6.1 Slew rate control 42
4.6.2 Current slew rate 42
4.6.3 Voltage slew rate 43
4.6.4 Current limitation 46
4.7 Driver protections 54
4.7.1 Over-temperature protection 54
4.7.2 Over-temperature monitoring electrical characteristics 56
4.7.3 Short-circuit to battery: over-current detection in low-side transistors . . 57
4.7.4 Short-circuit to ground: over-current detection in high-side transistor . . 58
4.7.5 Load in short-circuit 58
4.7.6 Over-current detection electrical characteristics 59
4.8 Diagnostics and registers descriptions in case of validity bit configuration 60
4.8.1 Diagnostic Reset strategy 60
4.8.2 Diagnostic reset bit 61
4.8.3 Global Failure Bit NGFAIL definition 64
4.8.4 Diagnostic of "Over-current" in on-state 65
4.8.5 Diagnostic of "Open Load" in on-state 69
4.8.6 On-state diagnostics electrical characteristics 70
4.8.7 Off-state diagnostic 71
4.8.8 Off-state diagnostic electrical characteristics 73
4.9 SPI 73
4.9.1 Protocol description 74
4.9.2 SPI command and response words format 75
4.9.3 Read ASIC traceability number 77
4.9.4 Read Logic HW version 78
4.9.5 Parity bit 78
4.9.6 SPI communication mode (Parallel and Daisy chain mode) 79
4.9.7 Communication check 80
4.9.8 Electrical characteristics 81

5 Package information 89
5.1 PowerSSO-36 (exposed pad) package mechanical data 89

6 Reference document 92

7 Revision history 93

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List of tables

Table 1. Device summary . . . 1
Table 2. Pin definition (PSSO36twin die) and function . . . 10
Table 3. Application circuit - BOM . . . 13
Table 4. Absolute maximum ratings . . . 14
Table 5. Thermal ratings . . . 15
Table 6. Range of functionality . . . 15
Table 7. Bridge output drivers . . . 16
Table 8. Timing characteristics . . . 17
Table 9. VPS_UV . . . 19
Table 10. VPS_UV_REG . . . 19
Table 11. VPS electrical characteristics . . . 20
Table 12. UV_PROT_EN . . . 20
Table 13. UV_PROT_EN_echo . . . 20
Table 14. UV_WIN . . . 21
Table 15. UV_WIN_echo . . . 21
Table 16. UV_CNT_REACHED . . . 21
Table 17. VDD_UV_REG . . . 23
Table 18. VDD_UV . . . 23
Table 19. VDD_OV_REG . . . 24
Table 20. VDD_OV . . . 24
Table 21. VDD_OV_L[2:0] . . . 25
Table 22. VDD5 voltage monitoring Electrical characteristics . . . 26
Table 23. Device supply electrical characteristic . . . 27
Table 24. SW reset [1:0] . . . 28
Table 25. POR status . . . 28
Table 26. POR electrical characteristics . . . 29
Table 27. System clock electrical characteristics . . . 29
Table 28. NSPREAD . . . 29
Table 29. NSPREAD_echo . . . 29
Table 30. HWSC/LBIST Trigger . . . 30
Table 31. HWSC/LBIST_status . . . 31
Table 32. HWSC/LBIST electrical characteristics . . . 32
Table 33. VVL_MODE . . . 34
Table 34. VVL_MODE echo . . . 34
Table 35. TVVL[3:0] (µs) . . . 34
Table 36. TVVL_echo[3:0] . . . 35
Table 37. BRIDGE_EN . . . 36
Table 38. NDIS_status . . . 37
Table 39. DIS_status . . . 37
Table 40. Normal mode H-bridge input . . . 37
Table 41. IN1/IN2 mode H-bridge input . . . 37
Table 42. VVL mode H-bridge input . . . 38
Table 43. TSW_low_current . . . 38
Table 44. TSW_low_current_echo . . . 39
Table 45. Digital inputs control electrical characteristics . . . 41
Table 46. ISR . . . 42
Table 47. Range current slew rate . . . 42
Table 48. ISR_echo . . . 43

Downloaded from Arrow.com.

Table 49. VSR . . . 43
Table 50. Voltage slew rate . . . 43
Table 51. VSR_echo . . . 43
Table 52. NOSR . . . 44
Table 53. NOSR_echo . . . 44
Table 54. TDSR . . . 44
Table 55. TDSR_ECHO . . . 44
Table 56. ILIM_REG . . . 46
Table 57. CL[1:0] . . . 49
Table 58. CL_echo[1:0] . . . 49
Table 59. OTwarn_thr_var . . . 50
Table 60. OTwarn_thr_var_echo . . . 50
Table 61. OTsd_thr_var . . . 51
Table 62. OTsd_thr_var_echo . . . 51
Table 63. Electrical characteristics . . . 52
Table 64. NOTSD . . . 54
Table 65. NOTSD_REG . . . 54
Table 66. OTWARN_TSEC_EN . . . 55
Table 67. OTWARN_TSEC_EN_echo . . . 55
Table 68. OTWARN . . . 56
Table 69. OTWARN_REG . . . 56
Table 70. Over-temperature monitoring electrical characteristics . . . 56
Table 71. Over-current detection electrical characteristics . . . 59
Table 72. DIAG_CLR_EN . . . 61
Table 73. DIAG_CLR_EN_echo . . . 61
Table 74. Status bits description . . . 62
Table 75. Diagnostics bits description . . . 62
Table 76. NGFAIL . . . 64
Table 77. Diagnostic of "Over-current" in on-state . . . 65
Table 78. Error_count[3:0] . . . 67
Table 79. TDIAG1 (µs) . . . 67
Table 80. TDIAG1_echo[2:0] . . . 68
Table 81. OL_ON . . . 69
Table 82. OL_ON_STATUS [1:0] . . . 69
Table 83. Open Load in ON-state electrical characteristics . . . 70
Table 84. TRIG . . . 71
Table 85. DIAG_OFF[2:0] . . . 72
Table 86. Off-state diagnostic electrical characteristics . . . 73
Table 87. SPI command word format . . . 75
Table 88. SPI response word format . . . 75
Table 89. Supplier ID code . . . 76
Table 90. Silicon version identifier . . . 76
Table 91. Wafer coordinate . . . 77
Table 92. Traceability code and wafer number . . . 77
Table 93. CC_latch . . . 80
Table 94. Config_CC . . . 80
Table 95. Config_CC_state_echo7 . . . 80
Table 96. Electrical characteristics serial data output . . . 81
Table 97. SPI electrical characteristics . . . 82
Table 98. SPI communication command and answer words . . . 84
Table 99. SPI communication configuration . . . 86
Table 100. PowerSSO-36 (exposed pad) package mechanical data . . . 90

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Table 101. Document revision history 93

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List of figures

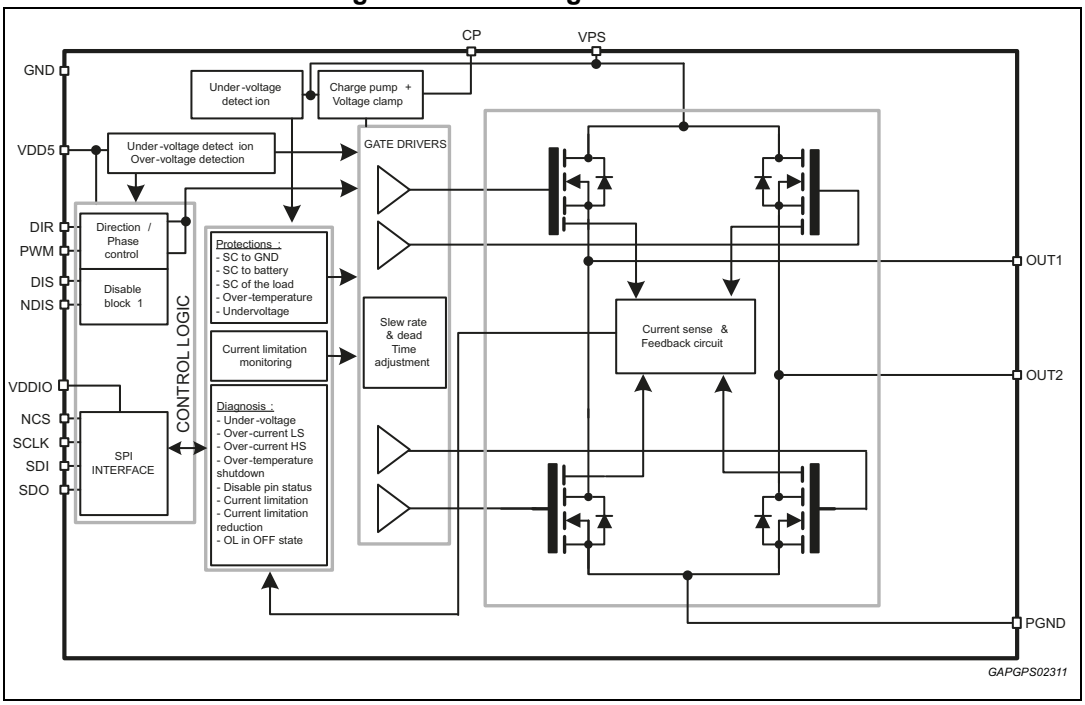
Figure 1. Block diagram for L9960 . . . 8
Figure 2. Pin connection of L9960 version (top view) . . . 9
Figure 3. Pin connection of L9960T version (top view) . . . 9
Figure 4. Application circuit . . . 12
Figure 5. Example of VDD5 slopes . . . 16
Figure 6. External power supply circuitry . . . 18
Figure 7. Battery voltage monitoring – case1 . . . 21
Figure 8. Battery voltage monitoring – case2 . . . 22
Figure 9. VDD5 under voltage monitoring . . . 23
Figure 10. VDD5 over voltage monitoring . . . 24
Figure 11. POR timing diagram . . . 28
Figure 12. HWSC timing diagram . . . 31
Figure 13. HWSC state diagram . . . 32
Figure 14. Bridge STATE diagram . . . 33
Figure 15. Bridge STATE diagram in VVL mode . . . 34
Figure 16. Bridge STATE diagram in IN1/IN2 mode . . . 36
Figure 17. 4 cases of high-side/low-side activation (normal mode) . . . 39
Figure 18. 4 cases of high-side/low-side activation (IN1/IN2 mode) . . . 40
Figure 19. Ideal waveforms of switching with slew rate control . . . 45
Figure 20. Tdiag2 blanking time depends on the Vps voltage . . . 47
Figure 21. Slew rate switching strategy . . . 47
Figure 22. Current limitation schemes . . . 48
Figure 23. Effect of the temperature diagram . . . 49
Figure 24. Thermal current limitation adjustment . . . 55
Figure 25. Example of low-side transistor low impedance short circuit to battery ($I < I_{oc_ls}$) . . . 57
Figure 26. Over-current detection . . . 58
Figure 27. Example of correct Overcurrent detection . . . 65
Figure 28. Example of NO Overcurrent detection by Tdiag2 . . . 66
Figure 29. Current diagnostic state diagram for each MOS . . . 67
Figure 30. Open load timing diagram . . . 70
Figure 31. Structure and detection criteria . . . 71
Figure 32. Open load off state diagnosis diagram . . . 72
Figure 33. SPI SDO update at 2nd SPI command . . . 74
Figure 34. SPI SDO is clocked on SCLK rising edge . . . 74
Figure 35. In case of no SCLK edge when NCS=0 . . . 74
Figure 36. Wafer XY coordinate . . . 77
Figure 37. Daisy chain operation example . . . 79
Figure 38. SPI timings . . . 83
Figure 39. PowerSSO-36 (exposed pad) package mechanical drawing . . . 89

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1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram for L9960



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1.2 Pin description

1.2.1 PowerSSO36 package

Figure 2. Pin connection of L9960 version (top view)

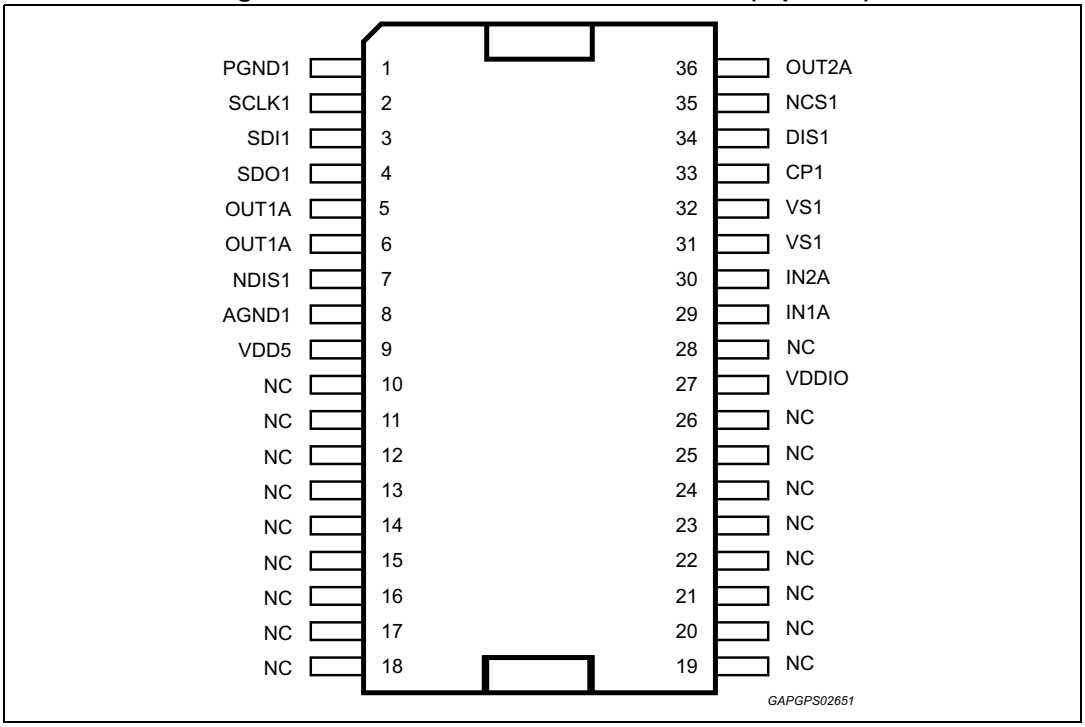
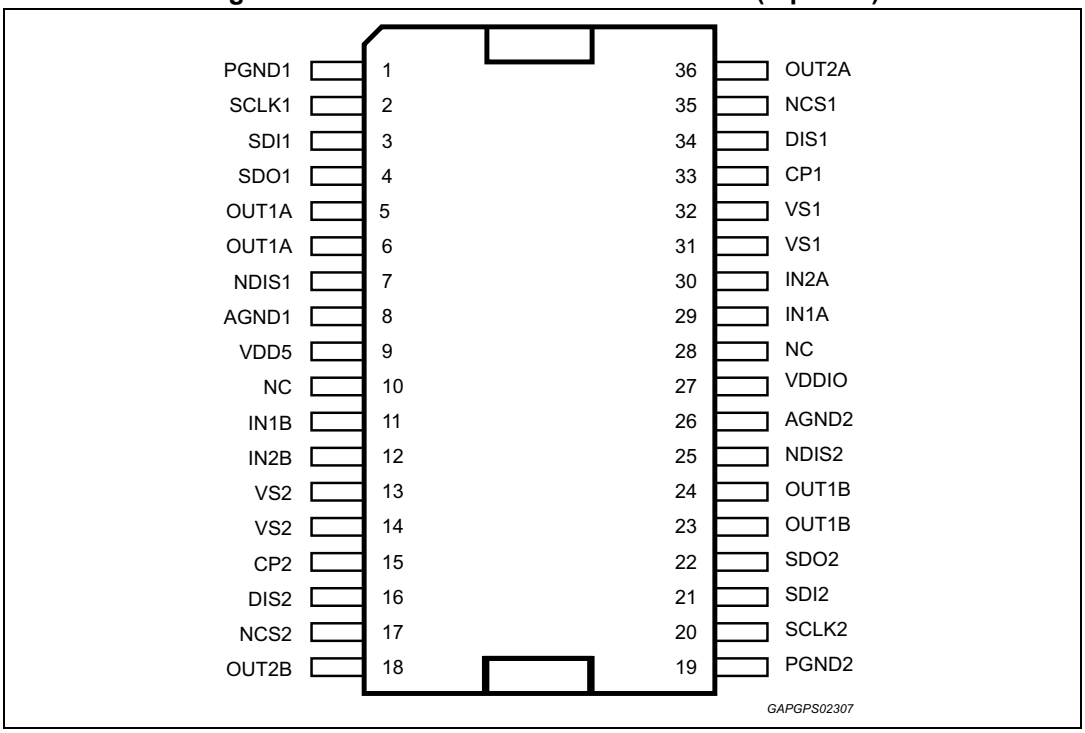


Figure 3. Pin connection of L9960T version (top view)



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Table 2. Pin definition (PSSO36twin die) and function

Pin #	Pin name	Function	I/O Type
1	PGND1	Power Ground	GND
2	SCLK1	SPI Serial Clock Input (internal pull-up)	I
3	SDI1	SPI Data In Input (internal pull-up)	I
4	SDO1	SPI Serial Data Out. Tri-state output buffer, Transfers data to the µC	O
5	OUT1A	Output of DMOS half bridge 1 [device A]	O
6			
7	NDIS1	Bidirectional Enable pin: open drain output pulled low in case of VDD over/under voltage. If the input is pulled low OUT 1-2 go to tri-state.	I/O
8	AGND1	Analog Ground pin	GND
9	VDD5	Regulated 5V supply	I
10	NC	Not connected pin	
11(1)	IN1B	Input Half Bridge 1 (internal pull-down) [device B]. Acting as PWM at power-up, can be configured to IN1 via SPI frame	I
12(1)	IN2B	Input Half Bridge 2 (internal pull-down) [device B]. Acting as DIR at power-up, can be configured as IN2 via SPI frame.	I
13(1)	VS2	Power supply voltage for Power Stages (external reverse protection required)	I
14(1)			
15(1)	CP2	Tank capacitor for Charge Pump output	O
16(1)	DIS2	Disable pin: if it is pulled high Out1-2 are in tri-state (internal pull-up)	I
17(1)	NCS2	SPI Chip Select Input (internal pull-up)	I
18(1)	OUT2B	Output of DMOS half bridge 2 [device B]	O
19(1)	PGND2	Power Ground	GND
20(1)	SCLK2	SPI Serial Clock Input (internal pull-up)	I
21(1)	SDI2	SPI Data In Input (internal pull-up).	I
22(1)	SDO2	SPI Serial Data Out	O
23(1)	OUT1B	Output of DMOS half bridge 1 [device B]. multi-bonding	O
24(1)			
25(1)	NDIS2	Bidirectional Enable pin: open drain output pulled low in case of VDD over/under voltage. If the input is pulled low OUT 1-2 go to tri-state.	I/O
26(1)	AGND2	Analog Ground pin	GND
27	VDDIO	Regulated 3.3/5V supply for SDO output buffer	I
28	NC	Not connected pin	-
29	IN1A	Input Half Bridge 1 (internal pull-down) [device A]. Acting as PWM at power-up, can be configured to IN1 via SPI	I
30	IN2A	Input Half Bridge 2 (internal pull-down) [device A]. Acting as DIR at power-up, can be configured as IN2 via SPI.	I

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Table 2. Pin definition (PSSO36twin die) and function (continued)

Pin #	Pin name	Function	I/O Type
31	VS1	Power supply voltage for Power Stages (external reverse protection required)	I
32			
33	CP1	Charge Pump output	O
34	DIS1	Disable pin: if it is pulled high Out1-2 are in tri-state (internal pull-up)	I
35	NCS1	SPI Chip Select Input (internal pull-up)	I
36	OUT2A	Output of DMOS half bridge 2 [device A]. multi-bonding	O
EP	AGND1	Exposed Pad connected to PCB Ground	

1. For L9960 version in PSSO36, the pins from 11 to 26 are not connected.

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2 Application description

The L9960 is dedicated to be part of an H-Bridge module for automotive applications. It can be used in all the applications requiring an H-Bridge power stage configuration in order to drive DC motors or bi-directional solenoid-controlled actuators. Device configurability allows to choose the best current or voltage slew rate for the optimization of motor control and noise suppression.

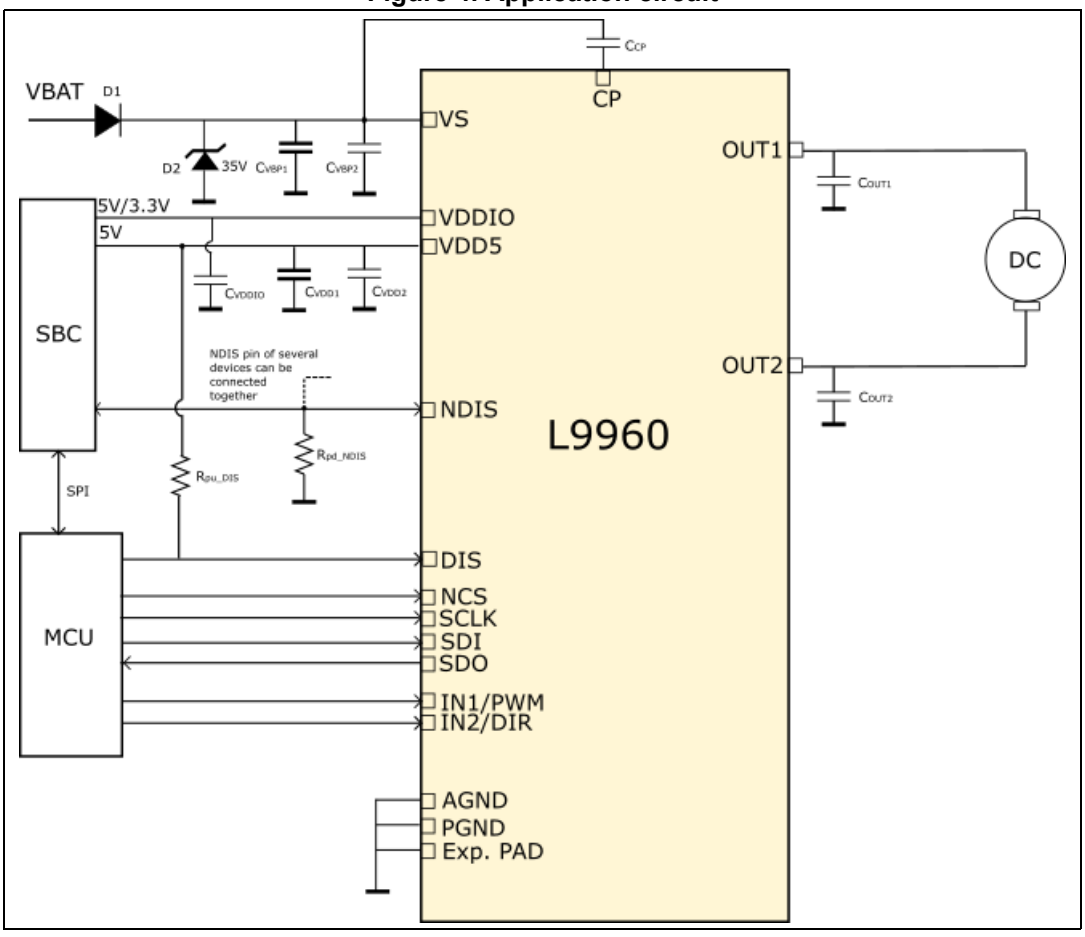
Typical applications are:

- Electronic throttle control;
- Exhaust gas recirculation (EGR) or waste flap control;
- Swirl actuator control;
- Electric pumps, motor control and auxiliaries;
- Generic DC or Stepper motors driving.

The module is implemented with a microcontroller, an input filter (fulfillment of the EMC/EMI requirements) and an over-voltage protection diode (optional).

2.1 Application circuit

Figure 4. Application circuit



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2.2 Bill of materials

Table 3. Application circuit - BOM

Component	Requirement	Comment	Min	Typ	Max	Unit
C_{VBP1}		50 V	-	100	-	µF
C_{VBP2}	To be mounted close to the pin		-	1	-	µF
C_{VDD1}		50 V	-	10	-	µF
C_{VDD2}	To be mounted close to the pin		-	100	-	nF
C_{VDDIO}	To be mounted close to the pin		-	100	-	nF
C_{CP}	To be mounted close to the pin		-	100	-	nF
C_{OUT1}	To be mounted close to the pin	Values as big as possible (max 47 nF) are recommended if Open Load in OFF detection is disturbed	10	-	47	nF
C_{OUT2}	To be mounted close to the pin	Values as big as possible (max 47 nF) are recommended if Open Load in OFF detection is disturbed	10	-	47	nF
R_{pd_NDIS}			-	10	-	KΩ
R_{pu_DIS}			-	10	-	KΩ
D1	STPS5L60S		-	-	-	-
D2	SMA6T33AY	Clamp max: 35 V	-	-	-	-

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3 General electrical characteristics

3.1 Absolute maximum ratings

Warning: **Warning: stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect the device reliability.**

Table 4. Absolute maximum ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{ps}	Supply voltage	Continuous	-1	40	V
$V_{out1,2}$	Output voltage	Continuous. OUT is limited by VPS	-1	40	V
VDD5	Logic supply voltage	0 V < Vps < 40 V	-0.3	19	V
VDDIO	SDO supply voltage	0V<Vps<40V	-0.3	19	V
VCP	VCP output voltage	-	-0.3	Vps+5	V
V_{IN}	Logic input voltage (NCS, SDI, SCLK, DIR, PWM, DIS, NDIS)	0 V < Vps < 40 V 0 V < VDD5 < 19 V	-0.3	19	V
V_o	Logic output voltage (SDO, NDIS)		-0.3	19	V
-	Human body model ESD compliance for pins: OUTx,VPS (not tested at ATE)(1)	HBM (100 pF/1.5 kohm)	-4	4	kV
-	Human body model ESD compliance for other pins than OUTx, VPS (not tested at ATE)	HBM (100 pF/1.5 kohm)	-2	2	kV
-	Charge Device Model ESD compliance for all pins (not tested at ATE)	CDM; according to Q100-011 classification C3B	-750 -500	750(2) 500(3)	V V
-	ISO 7637 pulses	Cf. standards	-	-	-
-	Latch-up immunity	According to JEDEC 78 class 2 level A			

1. Versus GND.
2. Corner pins.
3. All pins.

Note: Test circuit according to HBM (EIA/JESD22-A114-B) and CDM (EIA/JESD22-C101-C).

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3.2 Thermal ratings

Table 5. Thermal ratings

Symbol	Parameter	Condition	Min	Max	Unit
Tstore	Storage temperature	-	-55	150	°C
$R_{Th\ j\text{-}case}$	Junction-case thermal resistance	With power applied on 2 power MOS	-	2	°C/W

3.3 Range of functionality

All voltages refer to GND.

Currents are positive into and negative out of the specified pin.

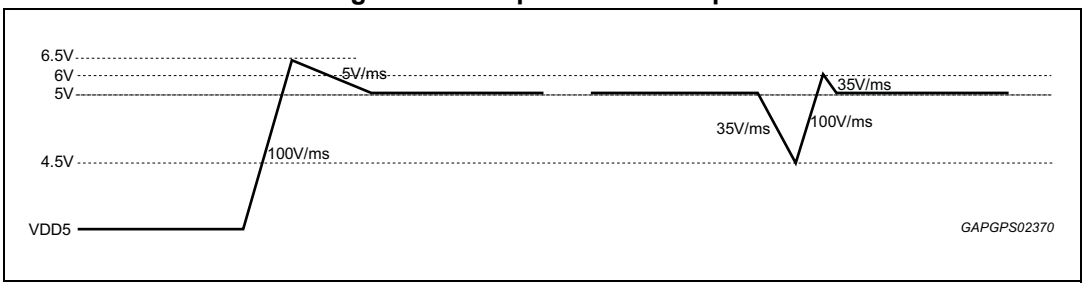
Table 6. Range of functionality

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{ps}	Supply voltage	Up to 40 V for transient pulses	$V_{ps_uv_off}$	14	28	V
dVps/dt	Supply voltage slew rate *(Application info)*	Up to 28 V	-20		20	V/µs
VDD5	Logic supply voltage	-	VDD5_uv	5	VDD5_ov	V
dVdd5/dt	Supply voltage slew rate *(Application info)*	See shapes here below	-35		100	V/ms
V_i	Logic input voltage (SDI, SCLK, NCS, DI, NDIS, DIR, PWM)	See also Max ratings	-0.3		VDD5_ov	V
VDDIO	SDO, NDIS output voltage	-	3	-	5.5	V
f_{spi}	SPI max clock frequency	Guaranteed up to a value of 5 MHz	-	-	5	MHz
f_{pwm}	PWM frequency	Guaranteed up to a value of 20 kHz	-	-	20	kHz
T_j	Junction temperature	(1)	-40	-	170	°C
		Failure condition	170	-	OTsd	°C
R L	Equivalent load range *(Application info)*	-	0.5 0.3	-	10 10	Ohm mH

1. The device is qualified according to mission profile covering 1300 hrs at T_j = 170 °C.

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Figure 5. Example of VDD5 slopes



3.4 Electrical characteristics

Tj = -40°C to 150°C unless otherwise specified.

VDD5 = 4.5V to 5.5V unless otherwise specified.

Vps = 4V to 28V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 7. Bridge output drivers

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{dson_tot}	Half bridge total Rdson (High-side + Low-Side)	T_j = -40 °C to 25 °C, I_{out} = 3 A; 4 V < V_{ps} < 7 V	-	-	300	mΩ
		T_j = 25 °C to 170 °C, $T_{case} \leq$ 140 °C I_{out} = 3 A; 4 V < V_{ps} < 7 V	-	-	450	
		T_j = -40 °C to 25 °C, I_{out} = 9 A; V_{ps} > 7V	-	-	300	
		T_j = 25 °C to 150 °C, I_{out} = 7.5 A; V_{ps} > 7 V	-	-	400	
		T_j = 25 °C to 170 °C, $T_{case} \leq$ 140 °C I_{out} = 7.5 A; V_{ps} > 7 V	-	-	450	
V_{bd_h}	Body diode forward voltage drop High-side transistor	Idiode = 9A	-	2	3	V
V_{bd_l}	Body diode forward voltage drop Low-side transistor	Idiode = 9A	-	2	3	V

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3.5 Timing characteristics

Table 8. Timing characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{don}	Delay time for switch-on	R_{load} 6 Ω, ISR = 1; VSR = 1 PWM edge → 10%, TSW_low_current = 0, V_{out} (or 10% I_{out})	-	-	10.5	µs
		R_{load} 6 Ω, ISR = 0; VSR = 0 PWM edge → 10%, TSW_low_current = 0, V_{out} (or 10% I_{out})	-	-	11.5	µs
		NOSR mode: PWM edge → 10%, TSW_low_current = 0, V_{out} (or 10% I_{out})	-	-	7	µs
T_{doff}	Delay time for switch-off	R_{load} 6 Ω, ISR = 1; VSR = 1 PWM edge → 90%, TSW_low_current = 0, V_{out} (or 90% I_{out})	-	-	12	µs
		R_{load} 6 Ω, ISR = 0; VSR = 0 PWM edge → 90%, TSW_low_current = 0, V_{out} (or 90% I_{out})	-	-	13	µs
		NOSR mode PWM edge → 90%, TSW_low_current = 0, V_{out} (or 90% I_{out})	-	-	5.5	µs
T_d	Delay time: symmetry	$\lvert T_{don}-T_{doff}\rvert$ NOSR mode	-	-	5	µs
		$\lvert T_{don}-T_{doff}\rvert$ ISR/VSR mode	2	-	8	µs
T_{rise_L}	Low-side transistor rise time	Non selectable by SPI 10%-90% V_{out} , I_{load} = 3 A	0.04	-	0.5	µs
T_{fall_L}	Low-side transistor fall time		5	-	10	µs

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4 Functional description

4.1 Device supply

The L9960 is supplied through 3 pins connected to 3 different external voltage supply sources:

- **VPS,** battery voltage to supply the bridge,
- **VDD5,** 5 V regulated voltage to supply chip digital I/O's,
- **VDDIO,** the supplying SDO output buffer voltage.

4.1.1 Functional State

Following functional states are defined for L9960:

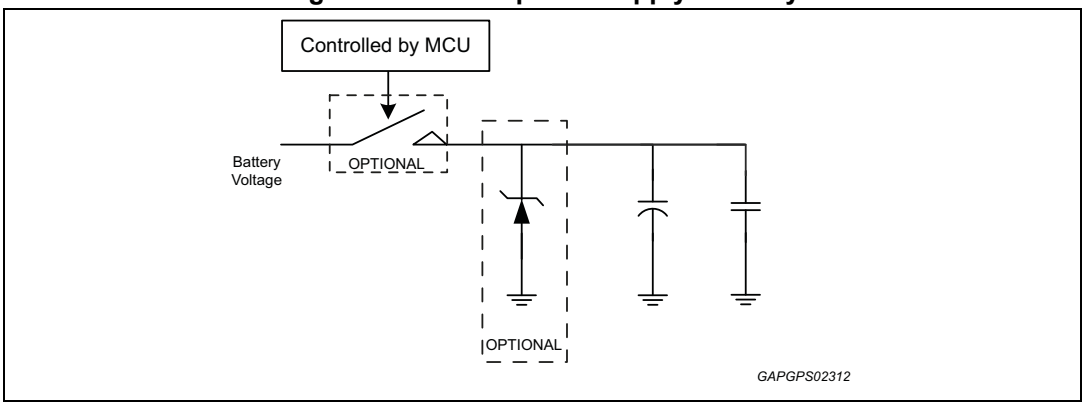
- **Normal Mode**
  - supply voltages are present and no failure. H-bridge is driven by the selected driving control mode (PWM/DIR, IN1/IN2) and it is configurable via SPI (i.e slew rate, current limitation and overcurrent thresholds, OT warning thresholds).
- **Tri-state**
  - H-bridge gate drivers are disabled due to a fault independently from PWM signal (IN1 or IN2). Once the fault condition is disappeared, L9960 restarts working without dedicated fault recovery procedure.
- **Disabled**
  - H-bridge is disabled due to a fault condition and it is necessary to execute the dedicated procedure to initialize the device (please review the below table for the dedicated procedure for each fault). In case the fault is related to an overvoltage or undervoltage on VDD5, the H-bridge is set to tri-state with **NDIS low**.

Note: Please review the dedicated Section 4.8.1: Diagnostic Reset strategy in application note.

4.1.2 Vps power supply

VPS pin is the power supply of the H-bridge. A filter could be implemented, mainly to fulfill the EMC requirements, and an over-voltage protection diode can also be added (optional).

Figure 6. External power supply circuitry



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Tri-state mode power consumption

Depending on the error detection affecting L9960, the bridge is switched to tri-state. In this status the output leakage current is less than "**Iout**" (refer to *Table 23*) on the overall range of functionality (Vps and temperature ranges).

Normal and VVL modes power consumption

In normal and VVL modes, the current consumption on Vps is mainly based on the output current delivered to the load and the High-Side Power MOS supply consumption.

Battery voltage monitoring

The Vps voltage is monitored internally to detect undervoltage conditions on power supply line.

When Vps decreases below the under-voltage threshold "***Vps_uv***" longer than a filter "***Tvps_uv***", the bridge is disabled (*SPI communication is still working*).
The filtering time "***Tvps_uv***" is implemented to avoid unwanted detection due to parasitic glitches when Vps increases as well as decreases.

As soon as the voltage rises again above the Vps under-voltage threshold (***hysteresis implemented***), the bridge is switched back to normal mode driven by DIR and PWM levels (or IN1/IN2). All the settings are kept as before the under-voltage event. No PWM toggle is necessary to restart the H-bridge if the condition is disappeared.

The Vps voltage monitoring information is readable via SPI by ***VPS_UV*** bit which is not latched.

Table 9. VPS_UV

Bit status	Description	Condition
0	Vps > Vps_uv longer than Tvps_uv	Default value
1	Vps < Vps_uv longer than Tvps_uv	-

The info is available in position R0 of the answer frame 8a.

The information is also readable by ***VPS_UV_REG*** bit which is latched.

Table 10. VPS_UV_REG

Bit status	Description	Condition
0	latched Vps > Vps_uv longer than Tvps_uv	Default value
1	latched Vps < Vps_uv longer than Tvps_uv	-

The info is available in position R5 of the answer frame 8a.

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Battery voltage monitoring electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 11. VPS electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Vs_clamp_neg	Negative clamp on VPS battery line	-3 A from VPS, 3 ms	-2.5	-	-0.5	V
Vps_uv_off	Vps under-voltage threshold	Vps decreasing	3.7	-	4.2	V
Vps_uv_on	Vps under-voltage threshold	Vps increasing	4.2	-	4.7	V
Vps_uv_hys	Vps under-voltage hysteresis	-	0.1	-	1	V
Tvps_uv	Vps under-voltage filtering time (guaranteed by scan)	Digital filter	1	-	3	µs

Undervoltage protection

A counter is implemented to measure if two consecutive Vps under-voltage events occur within a fixed time frame, defined by the parameter (**UV_WIN**), which is programmable via SPI in two different values: 20 or 40 µs; if it happens, a specific bit named **"UV_CNT_REACHED"** is set to 1 and the bridge is disabled.

The **"UV_PROT_EN**" bit is used to enable the counter **UV_WIN** and an echo answer is available. In the tables below, the configuration and functions for each of these parameters are shown:

Table 12. UV_PROT_EN

Bit status	Description	Condition
0	Counter and disabling protection are not enabled	Reset value
1	Counter and disabling protection are enabled	-

Note: (-) available in position D3 of the SPI command frame 4.

Table 13. UV_PROT_EN_echo

Bit status	Description	Condition
0	Echo counter and disabling protection not enabled	Reset value
1	Echo counter and disabling protection enabled	-

Note: (-) available in position R3 of the SPI answer frame 7b.

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Table 14. UV_WIN

Bit status	Description	Condition
0	UV_WIN window is set to 20 µs	Reset value
1	UV_WIN window is set to 40 µs	-

Note: (-) available in position D0 of the SPI command frame 4.

Table 15. UV_WIN_echo

Bit status	Description	Condition
0	Echo: UV_WIN window is set to 20 µs	Reset value
1	Echo: UV_WIN window is set to 40 µs	-

Note: (-) available in position R0 of the SPI answer frame 7b.

Table 16. UV_CNT_REACHED

Bit status	Description	Condition
0	No VS under voltage events closer than UV_WIN	Default Value
1	Two VS under voltage events closer than UV_WIN	-

Note: (-) available in position R5 of the SPI answer frame 8c.

If this UV protection option is not enabled, an indefinite number of consecutive battery under-voltage events can occur with the only action taken by the device to disable the bridge, when the battery level is below **“vps_uv threshold”**.

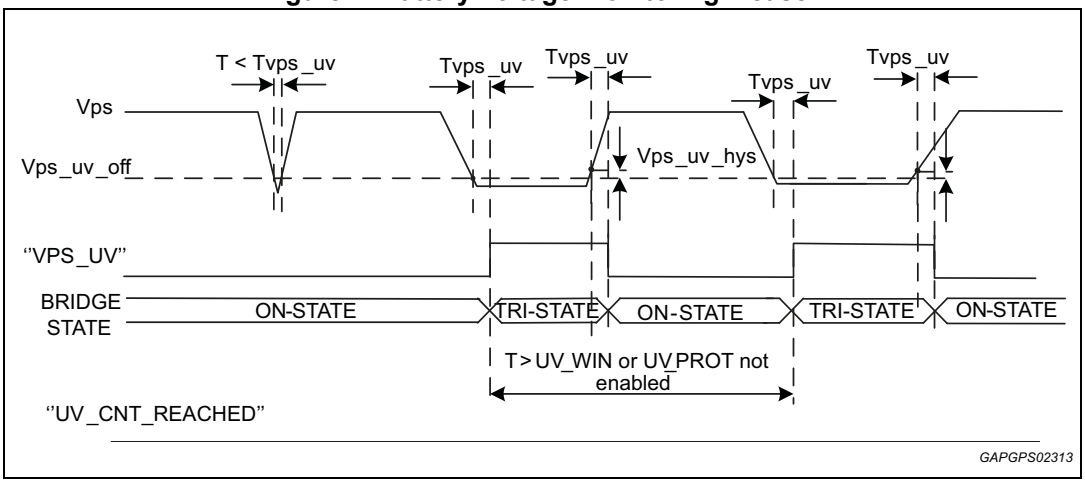
Figure 7 and *Figure 8* show the cases of **VPS UV** events greater or smaller than 2 in the time frame defined by **UV_WIN**.

Case 1 (no enabled protection)

The first VPS transition under the **VPs_uv_off** threshold is disregarded, due to the event duration less than **Tvps_uv**.

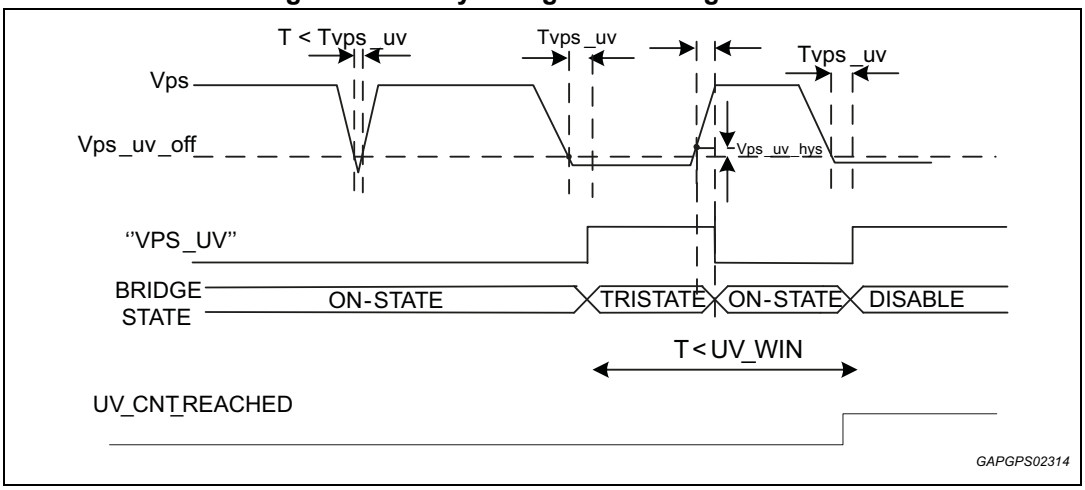
After the second UV transition on Vps, the bridge is put in tri-state. As the protection has not been enabled via **UV_PROT** bit, the H-bridge keeps on switching between On-state and tri-state.

Figure 7. Battery voltage monitoring – case1



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Figure 8. Battery voltage monitoring – case2



Case 2

In this scenario, after the second UV transition on VPS, with the enabled protection via **UV_PROT** set to 1, if two UV events occur by the **UV_WIN** timeframe expiration, the H-bridge is set in Disable condition consequently.

4.1.3 VDD5 regulated voltage supply

The VDD5 Input voltage is provided by an external power supply, supplying the corresponding L9960 digital I/O's.

When VDD5 is not supplied, there is only a small leakage current sank from VPS, see parametric table with condition VDD5 <0.7V.

Voltage supply range

The L9960 has a VDD5 operating voltage supply range from "***VDD5_uv***" up to "***VDD5_ov***" thresholds, however, the absolute maximum rating is defined up to 19 V DC.

VDD5 under-voltage detection

NDIS status depends on the UV event duration affecting VDD5:

- When the VDD5 voltage falls below the under-voltage detection threshold "***VDD5_uv_th***" longer than a filter "***TVDD5_uv1***", the bridge is switched to **disable**.
- When VDD5 voltage falls below the under-voltage detection threshold "***VDD5_uv_th***" longer than "***TVDD5_uv2***", the condition is feedbacked to control logic, pulling LOW the pin NDIS, **NDIS pin is pulled to LOW**.

When VDD5 voltage increases above the "*VDD5_uv_th" threshold* (hysteresis and ***TVDD5_uv1*** filtering implemented), under-voltage condition is removed and L9960 keeps all the settings set.

The NDIS pin is released when under-voltage condition is removed, in condition that NDIS was hold at least for a minimum time ***"Thold_ndis"***.

The UV detection information is readable via 2 diagnostics bits called ***VDD_UV_REG*** (latched) and ***VDD_UV*** (unlatched).

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Table 17. VDD_UV_REG

Bit status	Description	Condition
0	Latched Vdd > Vdd_uv longer than Tvdd_uv1	Default Value
1	Latched Vdd < Vdd_uv longer than Tvdd_uv1	-

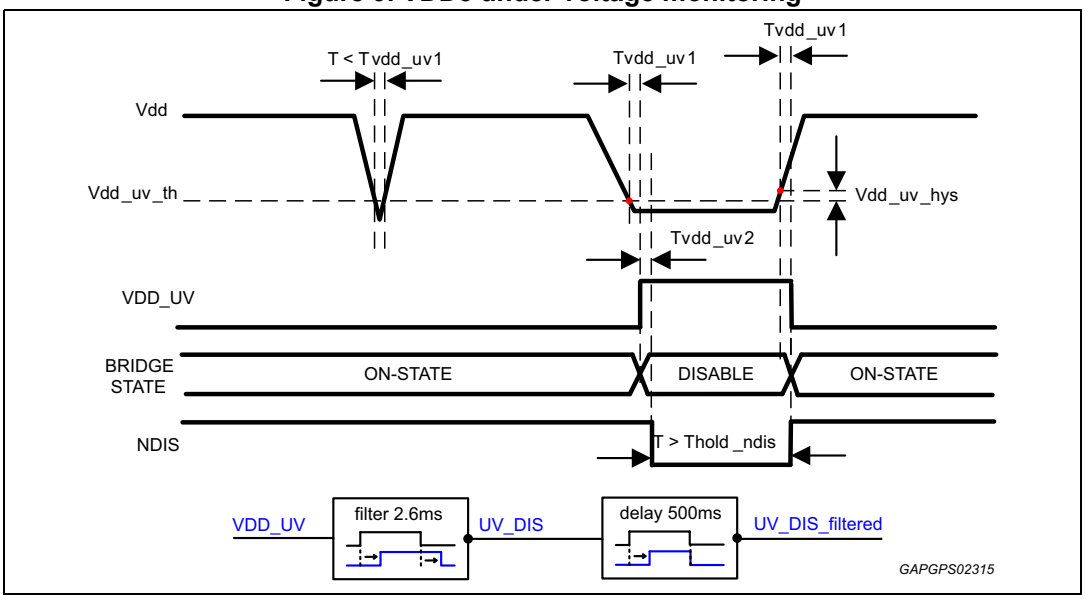
Note: (-) available in position R1 of the SPI answer frame 8a.

Table 18. VDD_UV

Bit status	Description	Condition
0	Vdd > Vdd_uv longer than Tvdd_uv1	Default Value
1	Vdd < Vdd_uv longer than Tvdd_uv1	-

Note: (-) available in position R0 of the SPI answer frame 12b.

Figure 9. VDD5 under voltage monitoring



VDD5 over-voltage protection

Although the VDD5 input pin and all I/O's withstand up to 19 V, an over-voltage circuitry is implemented to ensure that the bridge is kept in disable condition when VDD5 voltage is higher than the VDD5 over-voltage threshold (***VDD5_ov_th)*** for duration longer than "***TVDD5_ov***".

This VDD5 over-voltage condition is also feedbacked directly to NDIS pin, by pulling NDIS to LOW after the filter time "***TVDD5_ov*** ".

The NDIS pin is released when VDD5 voltage decreases below the "***VDD5_ov_th***" threshold and wait hysteresis as well as ***TVDD5_ov*** filtering implemented + **Thold_ndis** filter time are expired.

The information is readable via 2 diagnostics bits called ***VDD5_OV_REG*** (latched) and ***VDD_OV*** (unlatched).

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Table 19. VDD_OV_REG

Bit status	Description	Condition
0	Latched Vdd < Vdd_ov_th longer than Tvdd_ov	Default Value
1	Latched Vdd > Vdd_ov_th longer than Tvdd_ov	-

Note: (-) available in position R2 of the SPI answer frame 8a.

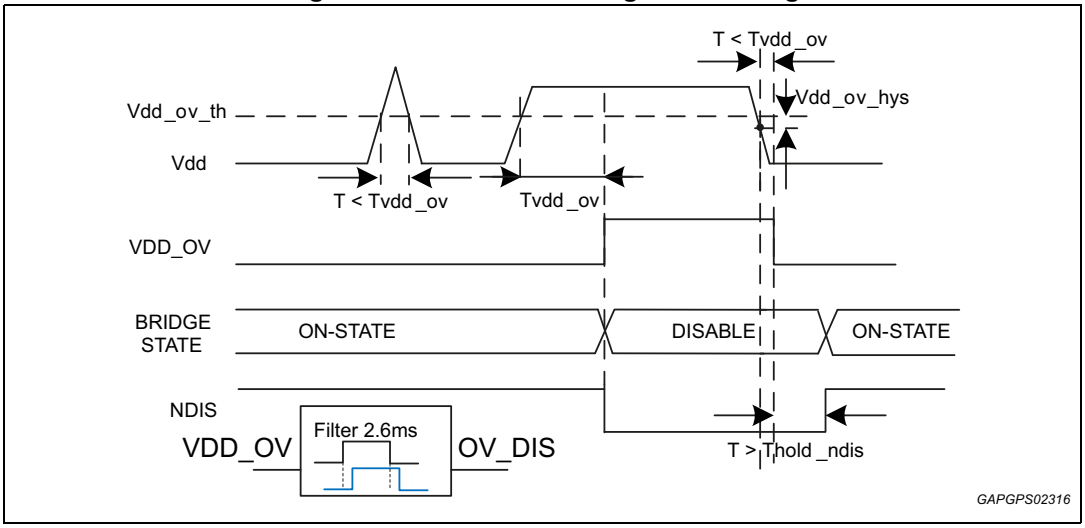
Table 20. VDD_OV

Bit status	Description	Condition
0	Vdd < Vdd_ov_th longer than Tvdd_ov	Default value
1	Vdd > Vdd_ov_th longer than Tvdd_ov	-

Note: (-) available in position R1 of the SPI answer frame 12b.

In case of VDD5 over-voltage condition, the bridge is kept in disable until the over-voltage condition is removed (hysteresis as well as ***TVDD5_ov*** filtering implemented).

Figure 10. VDD5 over voltage monitoring



This information is filtered, and reported in **NGFAIL** (*Global Failure Bit NGFAIL definition on page 64*).

A counter is available to inform about the overvoltage event length *(guaranteed by scan)*.

The counter starts as soon as ***VDD5_OV*** event occurs.

The counter stops for the following conditions:

- when its max value was reached,
- when the ***VDD5_OV*** condition is removed.

The ***VDD5_OV*** length information is readable in a latched 3 bits word called ***VDD5_OV_L***.

These 3 bits define the time range of the current counter value, according to the following table:

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Table 21. VDD_OV_L[2:0]

Bit status	min	max	Condition
000	not used	-	-
001	No VDD_OV event	-	default value
010	T_vdd_ov	10 ms	-
011	10 ms	30 ms	-
100	30 ms	100 ms	-
101	100 ms	300 ms	-
110	300 ms	1000 ms	-
111	1000 ms	-	-

Note: (-) available in positions R11/R10/R9 of the SPI answer frame 12a.

- A new ***VDD5_OV*** event overwrites the previous **VDD5_OV** length, except if the new event length is shorter than the value defined in ***VDD5_OV_L***.
- A reading of ***VDD5_OV_L*** through SPI clears the current value; if an event is still present when SPI reading occurs, the counter restarts counting until **VDD5_OV** condition is removed or the counter itself has reached its max value.

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VDD5 voltage monitoring electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 22. VDD5 voltage monitoring Electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD5_uv_th	VDD5 under-voltage detection threshold	VDD5 decreasing Valid for the extended range of temperature (1)	4.45	-	4.7	V
VDD5_uv_hys	VDD5 under-voltage hysteresis	VDD5 increasing	10	-	50	mV
TVDD5_uv1	VDD5 under-voltage filtering time for bridge switched to Tri-state	Vpor < VDD5 < VDD5_uv_off Digital filter (guaranteed through scan)	2	-	3.25	ms
TVDD5_uv2	VDD5 under-voltage filtering time for NDIS pin pulled to ”LOW” level	VDD5 decreasing Digital filter (guaranteed through scan)	415	-	625	ms
VDD5_ov_th	VDD5 over-voltage detection threshold	VDD5 increasing Valid for the extended range of temperature	5.2	-	5.55	V
TVDD5_ov	VDD5 over-voltage filtering time	VDD5 increasing Digital filter (guaranteed through scan)	2	-	3.25	ms
VDD5_ov_hys	VDD5 over-voltage hysteresis	VDD5 decreasing	10	-	50	mV
NDIS_VOL	NDIS output ON state threshold	On Load current = 5 mA	0	-	0.4	V
Thold_ndis	NDIS Hold time	Minimum time before releasing NDIS after fault disappearance (guaranteed through scan)	2	-	3.25	ms

1. Extended range of temperature (150, 170 °C)

4.1.4 VDDIO voltage supply

In order to ensure a full compatibility with 5 V and 3.3V MCU peripherals, a pin VDDIO is dedicated to supply the output buffer of SDO.

The overall current consumption on VDDIO is "I_{VDDIO}".

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4.1.5 Device supply electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 23. Device supply electrical characteristic

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{ps}	Power supply current	VDD5 < 0.7 V; Vps < 16 V T_j < 85 °C; L9960	-	10	40	µA
		VDD5 < 0.7 V; Vps ≥ 16 V T_j > 85 °C; L9960	-	-	180	µA
		F_{PWM} = 0; I_{out} = 0 (L9960, L9960T)	-	-	5	mA
		For F_{PWM}=20 kHz; I_{out} = 0 (L9960)	-	-	5	mA
		For F_{PWM} = 20 kHz; I_{out} = 0 (L9960T)	-	-	10	mA
I_{out}	Leakage current on output	Bridge in tri-state All current sources switched OFF Measured between OUT1 and OUT2	-100	-	100	µA
I_{cc}	Logic-supply current	VDD5 >VDD5_uv_on F_{PWM} = 0, for L9960 for L9960T	- -	- -	9 18	mA
		FPWM = 20 kHz for L9960 for L9960T	- -	- -	9 18	
I_{VDDIO}	SPI controller current consumption on VDDIO	SDO not connected (L9960) for L9960T	- -	- -	1 2	mA

4.2 Power on reset (POR) and SW reset

POR is a **low active** internal reset signal, leading the H-bridge in tri-state. It is released in case the VDD5 is higher than the POR threshold (***hysteresis implemented***). The POR input has a hysteresis to avoid unstable behaviors during ramp up and down of VDD5.

The POR is active for VDD5 from 0V to [**Vpor + Vpor_hys**] (POR threshold + hysteresis).

When ***RESET*** state is active, the bridge is switched to **tri-state**.

When VDD5 voltage increases above the POR (Power On Reset) threshold (hysteresis implemented), the L9960 starts with all the settings reset to their default values.

In *Figure 11* is shown an example of POR timing diagram.

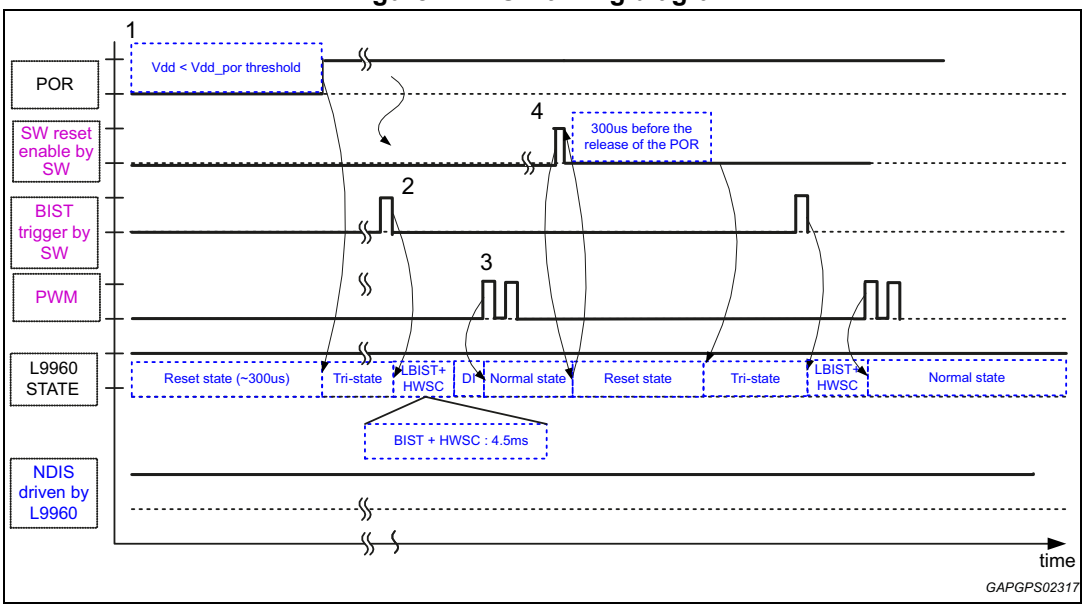
At point 1, due to a POR condition on VDD5 supply, the POR signal is set to low and it is released after 300 µs. L9960 is in disable state and the ***LBIST+HWSC*** (condition 2) is

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executed by application SW by **HWSC/LBIST Trigger** bit. If passed the H-bridge switches to Normal Mode after the first PWM transition.

At point 4 is shown the case, in which a SW reset is enabled by µC, with no impact on internal POR signal.

Figure 11. POR timing diagram



The SW reset configuration comes into a 2-bit register

Table 24. SW reset [1:0]

Bit status	Description	Condition
01	SW reset command	-
All except 01	no action	-

Note: (-) available in positions D10/D9 of the SPI command frame 2.

The SW reset lasts 2-clock periods.
The device goes back to **RESET** state immediately in case of POR condition on VDD5 or in case of SW reset.
This reset is asynchronous, with a synchronous release.
After a POR condition on VDD5 or a SW reset, the register bit called "**POR**" is set to "1"; it is cleared by read back via SPI.
Once cleared, this bit indicates a further Power On Reset.

Table 25. POR status

Bit status	Description	Condition
0	After SPI reading (not submitted to DIAG_CLR_EN)	-
1	after Power On Reset	Default value

Note: (-) available in the R11 bit position in SPI answer frame 7e.

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4.2.1 Power on reset (POR) electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 26. POR electrical characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{por}	POR threshold	VDD5 decreasing	3	3.7	V
V_{por_hys}	POR hysteresis	For VDD5 increasing, Bridge is switched ON at VDD5_uv_off+VDD5_uv_hys or (Vpor + Vpor_hys)	0.1	0.3	V
T_{por}	POR filtering time	VDD5 decreasing Analog filtering (guaranteed by design)	0.01	4	µs
T_{d_pow}	Power-on delay time	DIR = PWM = NDIS = 1 / DIS = 0 (guaranteed by scan)	-	300	µs
V_{por_int}	POR threshold on internal regulator	-	1	3	V

4.3 System clock electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 27. System clock electrical characteristics

Symbol	Parameter	Condition	Min.	Typ	Max.	Unit
Fclock	Internal System clock	±10% accuracy	4.5	5	5.5	MHz

A Spread Spectrum function can be an optional solution to reach EMC performance. The effect is a reduction on emission peak values by spreading the energy in the frequency domain.

Table 28. NSPREAD

Bit status	Description	Condition
0	Spread Spectrum Activate	Reset value
1	Spread Spectrum Disable	-

Note: (-) available in the R2 position in SPI answer frame 4.

A register report the echo of **NSPREAD** Config: "**NSPREAD** echo"

Table 29. NSPREAD_echo

Bit status	Description	Condition
0	echo Spread Spectrum Activate	Default value
1	echo Spread Spectrum Disable	-

Note: (-) available in the R2 position of the SPI answer frame 7b.

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4.4 Hardware self check (HWSC) and LBIST

The target of the hardware self check is to check the proper function of the VDD5 over voltage detection. Due to the fact that over voltage is impossible in a proper working ECU, it is necessary to simulate an over voltage situation, by changing the over voltage threshold during HWSC/LBIST test.

The target of the LBIST is to cover the disable path of the device, for safety aspects.

As long as the HWSC/LBIST has not been performed (indicated by the signal **HWSC/LBIST_done** = "0") the bridge outputs remain disabled in tri-state.

The start condition for the HWSC/LBIST is triggered by a SPI bit “**HWSC/LBIST Trigger**”. It is considered as a valid command only after a POR or a SW reset or a failed HWSC/BIST. If passed, it cannot be triggered again and the SPI answer remains the same.

HWSC/LBIST can be re-triggered only in case of FAIL result, or SW reset.

Table 30. HWSC/LBIST Trigger

Bit status	Description	Condition
0	HWSC/LBIST not requested	Reset value
1	request for HWSC/LBIST	-

Note: (-) available in the D8 position in SPI command frame 2, please refer to Application Note for MISO response in case of SW reset and for HWSC trigger.

4.4.1 HWSC test procedure

Once the HWSC is started, the reference voltage of the VDD5 over-voltage comparator is reduced to the lower value "**VDD5_ov_hwsc**", by the signal **o_VDD5_ov_ref**, as shown in the *Figure 12* below.

At the same time, the filters “**Thwsc_fil**”, “**Thwsc_ref**” and “**Thwsc_dur**” are started.

"**Thwsc_dur**" indicates the duration of the LBIST test.

"**Thwsc_dur**" indicates the duration of the dynamical adjustment of the VDD overvoltage threshold.

In case the VDD5 over-voltage comparator indicates an over voltage condition when the filter time “**Thwsc_fil**” has expired the HWSC status bits indicate that the test has successfully passed.

In case the VDD5 over-voltage indicates no over voltage condition when the filter time “**Thwsc_fil**” has expired the HWSC status bits are set to indicate that the test has failed.

In case the filter time **Thwsc_fil** is not yet fully expired at the end of “**Thwsc_ref**” (e.g. due to several restarts of “**Thwsc_fil**”) the HWSC status bits are set to indicate that the test has failed.

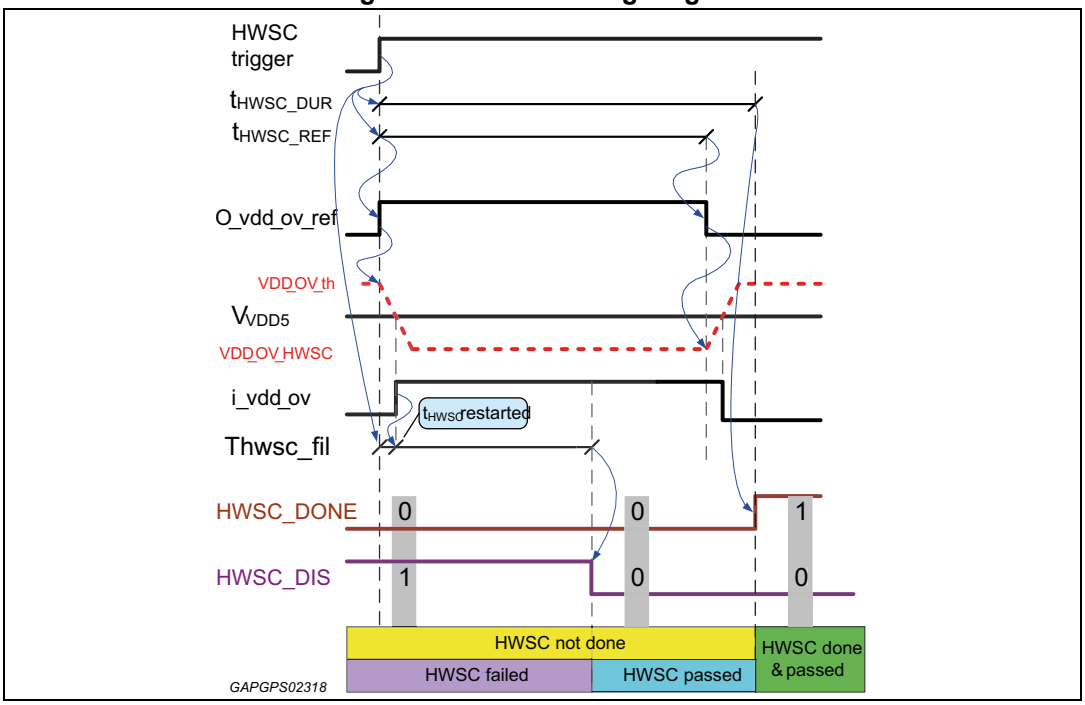
After “**Thwsc_ref**” has expired, the reduced VDD5 over-voltage comparator reference voltage returns back to the VDD5 over voltage disable threshold “**Vdd_ov_th**”.

tHWSC is re-triggered with every transition of the VDD5 OV comparator from "0" to "1"

In *Figure 12* "**o_VDD5_ov_ref**" is an internal signal which controls the reduction of the VDD5 over voltage threshold.

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Figure 12. HWSC timing diagram



Stop conditions for HWSC test

The HWSC is stopped by one of the following conditions:

- HWSC duration time “**Thwsc_dur**” has expired
- in case of a reset condition (RESET active)

Once the HWSC duration time “**Thwsc_dur**” has expired the internal signal **HWSC_done** is set to "1", independently of the HWSC result.

HWSC failed

In case the HWSC has failed or is not done, all outputs are disabled.

HWSC is not done if it was not triggered or if is not finished (“**Thwsc_dur**” not expired)

Result of HWSC/LBIST test

HWSC/LBIST test status (3 bits) is requested by SPI command "states request 1":

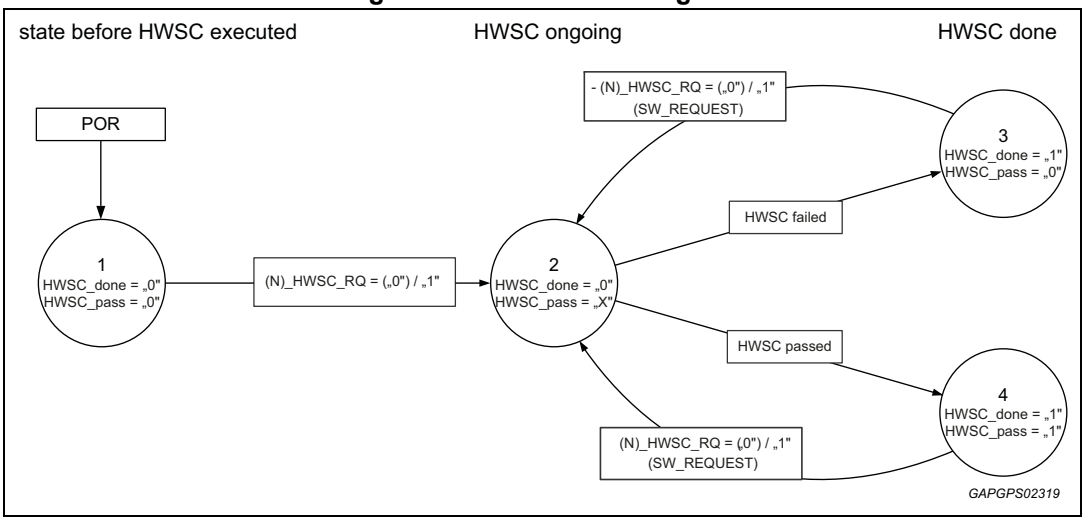
Table 31. HWSC/LBIST_status

Bit status (b2 b1 b0)	Description	Condition
0xx	HWSC/LBIST not done	Default value
100	HWSC/LBIST done - HWSC FAIL/LBIST FAIL	
101	HWSC/LBIST done - HWSC running/LBIST PASS	
110	HWSC/LBIST done - HWSC FAIL/LBIST PASS	
111	HWSC/LBIST done - HWSC PASS/LBIST PASS	

Note: (-) available in the R8/R7/R6 positions in SPI answer frame 8a.

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Figure 13. HWSC state diagram



4.4.2 HWSC/LBIST electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 32. HWSC/LBIST electrical characteristics

Pos.	Symbol	Parameter	Condition	Min.	Max.	Unit
6.1	VDD5_ov_hw	VDD5 over-voltage disable threshold in HWSC mode	-	3.7	4.2	V
6.2	Thwsc_ch_ov	Analog settling time for changing in HWSC mode and back	Settling time for changing the VDD5 overvoltage disable threshold includes analog filter time t_{A_FIL}, (guaranteed by design)	0	10	µs
6.3	Thwsc_dur	HWSC duration time	(guaranteed through scan)	100	160	µs
6.4	Thwsc_fil	HWSC filter time	(guaranteed through scan)	40	70	µs
6.5	Thwsc_ref	HWSC reference time	(guaranteed through scan)	80	130	µs
6.6	-	LBIST coverage for the disable path	(design info)	95	-	%
6.7	LBIST_dur	LBIST duration at start-up	(guaranteed through scan)	-	4.34	ms

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4.5 Digital input controls

All the digital inputs and outputs of the L9960 must be compatible with 3.3V and 5V CMOS technologies, but must also withstand up to 19V.

4.5.1 Bridge functional modes

Three functional modes are available on L9960, listed below:

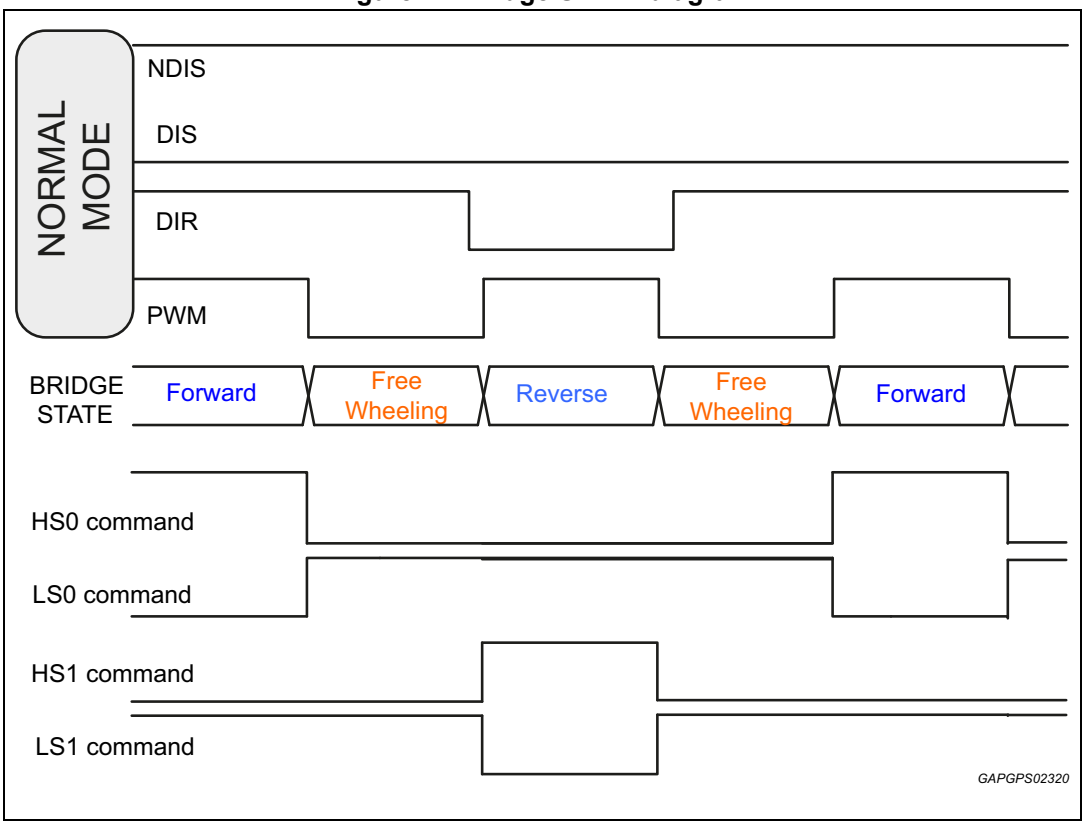
- Normal mode (via PWM / DIR)
- VVL
- IN1 / IN2

Normal mode

L9960 is in Normal Mode when the PWM / DIR control interface is selected.

In the below example it is showed the case of LS active freewheeling.

Figure 14. Bridge STATE diagram

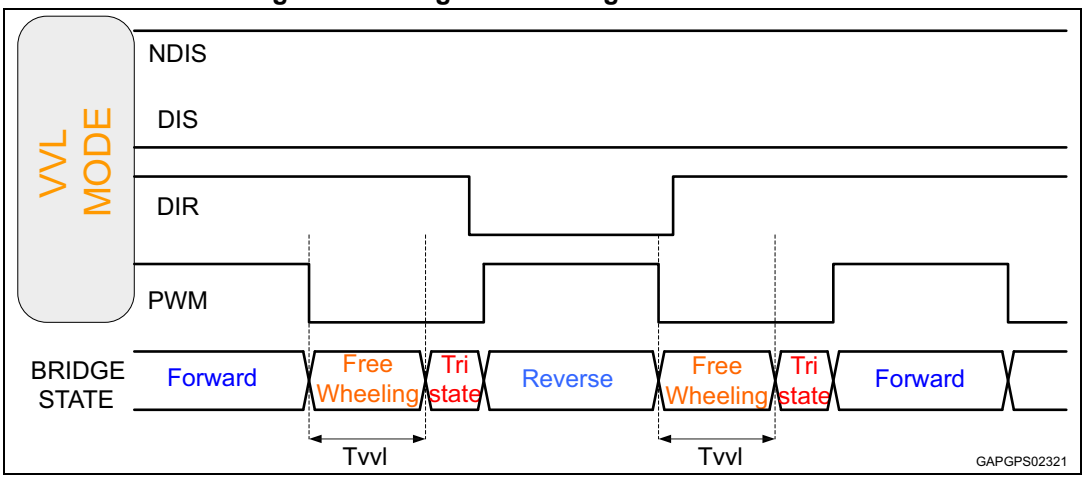


VVL mode

VVL mode is programmed through a dedicated SPI command “**VVL mode**” (configuration 3). This mode is used to drive valves in Forward or Reverse mode.

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Figure 15. Bridge STATE diagram in VVL mode



Programming the bridge in normal or VVL mode is performed through dedicated SPI command to setup the MODE configuration bit:

Table 33. VVL_MODE

Bit status	Description	Condition
0	No VVL mode	Reset value
1	VVL mode	-

Note: (-) available in the D10 bit position in SPI command frame 5.

The status of the VVL is echoed through a SPI configuration request

Table 34. VVL_MODE echo

Bit status	Description	Condition
0	No VVL mode	Reset value
1	VVL mode	-

Note: (-) available in the R11 bit position in SPI answer frame 7c.

In VVL mode, once PWM is set to LOW, the bridge is put in tri-state after a programmable time “Tvvl” from 0us to 26ms by the register defined below.

Table 35. TVVL[3:0] (µs)

4 bits combination	Description	Condition
0000	0	Not to be used if IN1/IN2 interface is selected
0001	6.4	
0010	12.6	
0011	24.8	
0100	50.4	-
0101	100	-
0110	200	-
0111	400	-

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Table 35. TVVL[3:0] (µs) (continued)

4 bits combination	Description	Condition
1000	800	-
1001	1600	-
1010	3200	-
1011	6500	-
1100	13000	-
1101	26000	-
1111	26000	Reset value

Note: (-) available in the D9/D8/D7/D6 bit position in SPI command frame 5.

VVL mode is deactivated (no tri-state phase) when the current limitation is active

The status of the TVVL is echoed through a SPI configuration request

Table 36. TVVL_echo[3:0]

4 bits Status combination	Description	Condition
0000	0	Not to be used if IN1/IN2 interface is selected
0001	6.4	
0010	12.6	
0011	24.8	
0100	50.4	-
0101	100	-
0110	200	-
0111	400	-
1000	800	-
1001	1600	-
1010	3200	-
1011	6500	-
1100	13000	-
1101	26000	-
1111	26000	Default value

Note: (-) available in the R10/R9/R8/R7 bit position in SPI answer frame 7c.

IN1_IN2 mode

This mode changes the meaning of PWM/DIR and allows driving directly the half-bridge.

To enable this mode it is necessary:

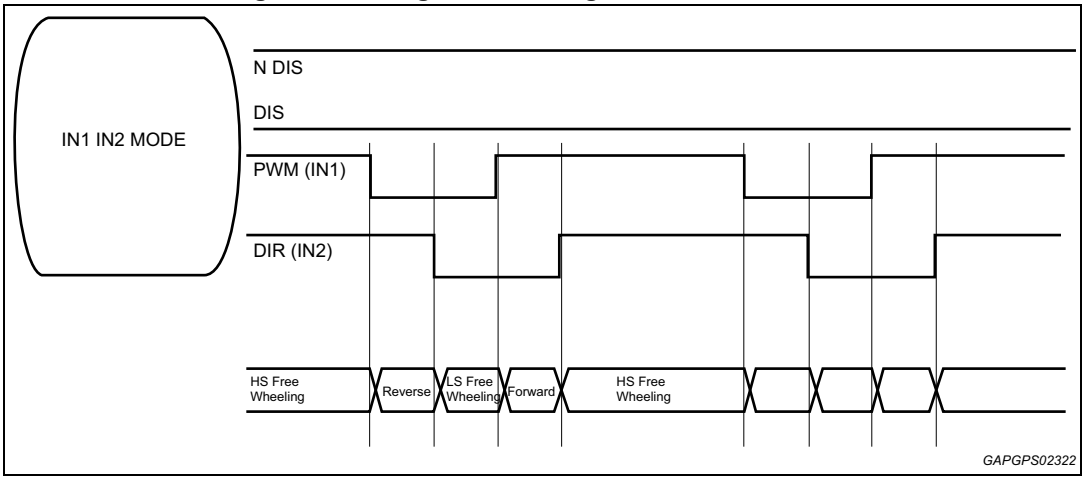
1. Program a dedicated SPI register (configuration2: **IN1_IN2_if**) set to '1'.
2. PWM/DIR (IN1/IN2) inputs must be low to latch and apply the configuration (see *Note*).

Note: In order to set back the default driving control mode (PWM/DIR) the same procedure has to be followed: the SPI command bit IN1_IN2_if bit has to be set to '0' and IN1=IN2 has to be set to '0' to latch and apply the configuration.

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Status of the SPI register (**IN1_IN2_if**) and its internally latched version are available through SPI (configuration request 2: “(**IN1_IN2_if**)” echo and "**IN1_IN2_if_latched_echo**")

Figure 16. Bridge STATE diagram in IN1/IN2 mode



4.5.2 Disable inputs DIS and NDIS

The pin DIS is internally **pulled-up** and **high active**.

When DIS is active (set to HIGH), the bridge is set to **disabled** independently from the internal clock (asynchronous switch-off path), whatever the state of the DIR and PWM inputs. All the data stored in SPI registers are not reset and SPI communication with the MCU is still possible.

When DIS is inactive (set to LOW) and NDIS is active (set to HIGH), the bridge is controlled by the DIR and PWM inputs, synchronously. After DIS or NDIS release, the bridge waits for the next PWM rising edge before being released from disable (see *Note*).

The pin NDIS is internally **pulled down** and **high active**.

When NDIS is inactive (set to LOW) either by NDIS pin or by protection schemes, the bridge is set disabled independently from the internal clock (asynchronous switch-off path), whatever the state of the DIR and PWM inputs. All the data stored in SPI registers are not reset and SPI communication with the MCU is still possible.

The “real-time” state of the bridge is a bit called "**BRIDGE_EN**". It reflects the disabling of the bridge, (including disabling by internal protection schemes), and not the tri-state linked to VVL mode activation.

Note: In case of IN1/IN2 mode, a rising edge either on IN1 or on IN2 is valid to release the disable mode. A minimum delay of 1us is suggested to be applied between DIS fall edge and rising edge on driving control pins.

Table 37. BRIDGE_EN

Bit status	Description	Condition
0	Bridge disabled	Default value
1	Bridge Enabled	-

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Note: (-) available in the R9 bit position in SPI answer frame 8a.

The µC should be able to perform a SOPC (Switch-off path check). For that purpose, the status of each disable line is also provided through SPI status of the followings pins: **NDIS**, **DIS**, **VDD5_OV**, **VDD5_UV**.

The status of NDIS and DIS can be monitored by 2 SPI registers:

Table 38. NDIS_status

Bit status	Description	Condition
0	NDIS pin = '0'	-
1	NDIS pin = '1'	-

Note: (-) available in the R11 bit position in SPI answer frame 8a.

Table 39. DIS_status

Bit status	Description	Condition
0	DIS pin = '0'	-
1	DIS pin = '1'	-

Note: (-) available in the R10 bit position in SPI answer frame 8a.

4.5.3 Control inputs DIR and PWM

The pins DIR and PWM are internally pulled down. In normal mode, the bridge is controlled by these two inputs according to the following table:

Table 40. Normal mode H-bridge input

DIR	PWM	OUT1_HS	OUT1_LS	OUT2_HS	OUT2_LS	Condition
1	1	1	0	0	1	Forward
0	1	0	1	1	0	Reverse
x	0	0	1	0	1	Freewheeling

Note: A minimum pulse width of 1 µs has to be guaranteed on driving control pins PWM/DIR for the relative command acknlowdgement by internal logic.

In **IN1/IN2 mode**, the bridge is controlled by these two inputs according to the table below:

Table 41. IN1/IN2 mode H-bridge input

Inputs		Outputs (MOS Driver)				Condition
IN2 (DIR)	IN1 (PWM)	OUT1_HS	OUT1_LS	OUT2_HS	OUT2_LS	
0	0	0	1	0	1	LS Freewheeling
0	1	1	0	0	1	Forward

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Table 41. IN1/IN2 mode H-bridge input (continued)

Inputs		Outputs (MOS Driver)				Condition
IN2 (DIR)	IN1 (PWM)	OUT1_HS	OUT1_LS	OUT2_HS	OUT2_LS	
1	0	0	1	1	0	Reverse
1	1	1	0	1	0	HS Freewheeling(1)

1. It is advised against using this recirculation option in IN1/IN2 mode as L9960 is not safely protected against external failures (i.e SCG). For IN1/IN2 mode only it is advised to recirculate (active freewheeling) on low-side drivers only.

Note: A minimum pulse width of 1 µs has to be guaranteed on driving control pins PWM/DIR for the relative command acknlowdgement by internal logic.

In ***VVL mode***, the bridge is controlled by these two inputs and according to the VVL status as described in the table below:

Table 42. VVL mode H-bridge input

DIR	PWM	VVL phase	OUT1_HS	OUT1_LS	OUT2_HS	OUT2_LS	Condition
1	1	no active with PWM=1	1	0	0	1	Forward
0	1		0	1	1	0	Reverse
x	0	T < TVVL	0	1	0	1	Freewheeling
x	0	T > TVVL	0	0	0	0	Tri-state

A specific dead-time "**TSW**" is implemented between high-side and low-side transistors switching to avoid cross-conduction. It applies when switching from on-state to freewheeling state and viceversa, regardless of the actual way to drive the H-bridge (PWD/DIR or IN1/IN2). The total delay may be related to the switching Current slew rate selected by SPI.

The dead time is managed in the digital design, using analog feedback information from the gate driver.

Table 43. TSW_low_current

Bit config	Description	Condition
0	Tsw activated on i_gate_fb only	-
1	Tsw activated on the last event between i_gate_fb or i_out_on	Reset value

In order to avoid h-bridge misbehavior, it is strongly recommended to avoid working with default settings: TSW_low_current = 0 is the only configuration allowed for all the applications.

POR, BIST/HWSC and SW reset commands overwrite the configuration TSW_low_current=0, so the application SW shall take care of resuming TSW_low_current=1.

The bit TSW_low_current_echo is available for reading on the Configuration Request 1 register, for eventual runtime configuration check

Note: (-) available in the D2 bit position in SPI command frame 3.

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A register report the echo of Tsw_low_current Config: "Tsw_low_current echo"

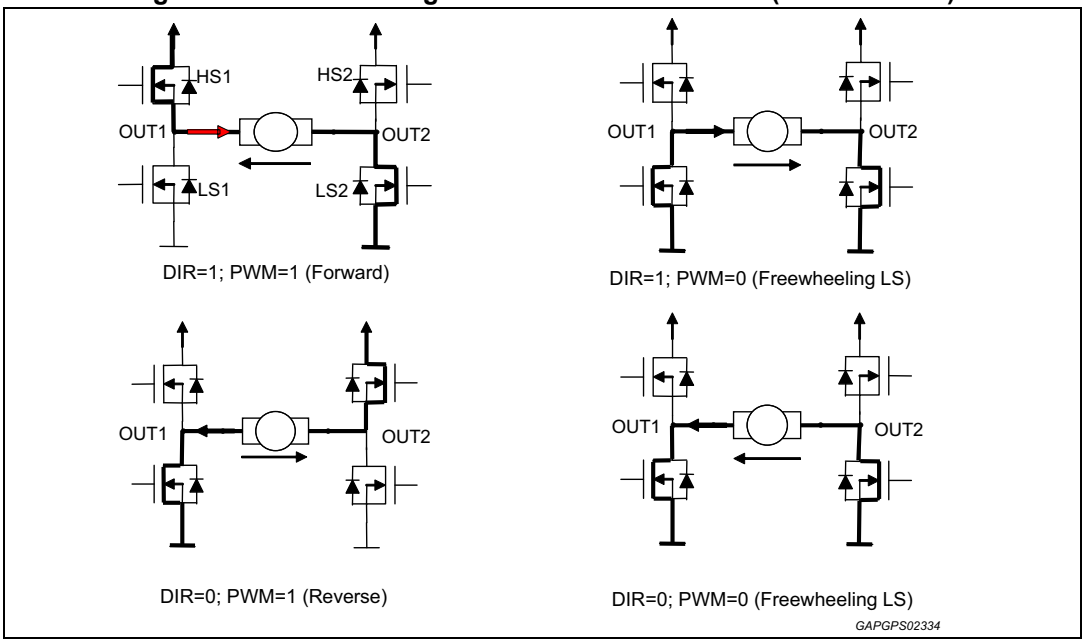
Table 44. TSW_low_current_echo

Bit status	Description	Condition
0	echo Tsw activated on i_gate_fb only	-
1	echo Tsw activated on the last event between i_gate_fb or i_out_on	Default value

Note: (-) available in the R3 bit position in SPI answer frame 7a.

By convention (normal mode), for DIR=1, the current flows from OUT1 to OUT2, for DIR = 0, the current flows from OUT2 to OUT1.

Figure 17. 4 cases of high-side/low-side activation (normal mode)

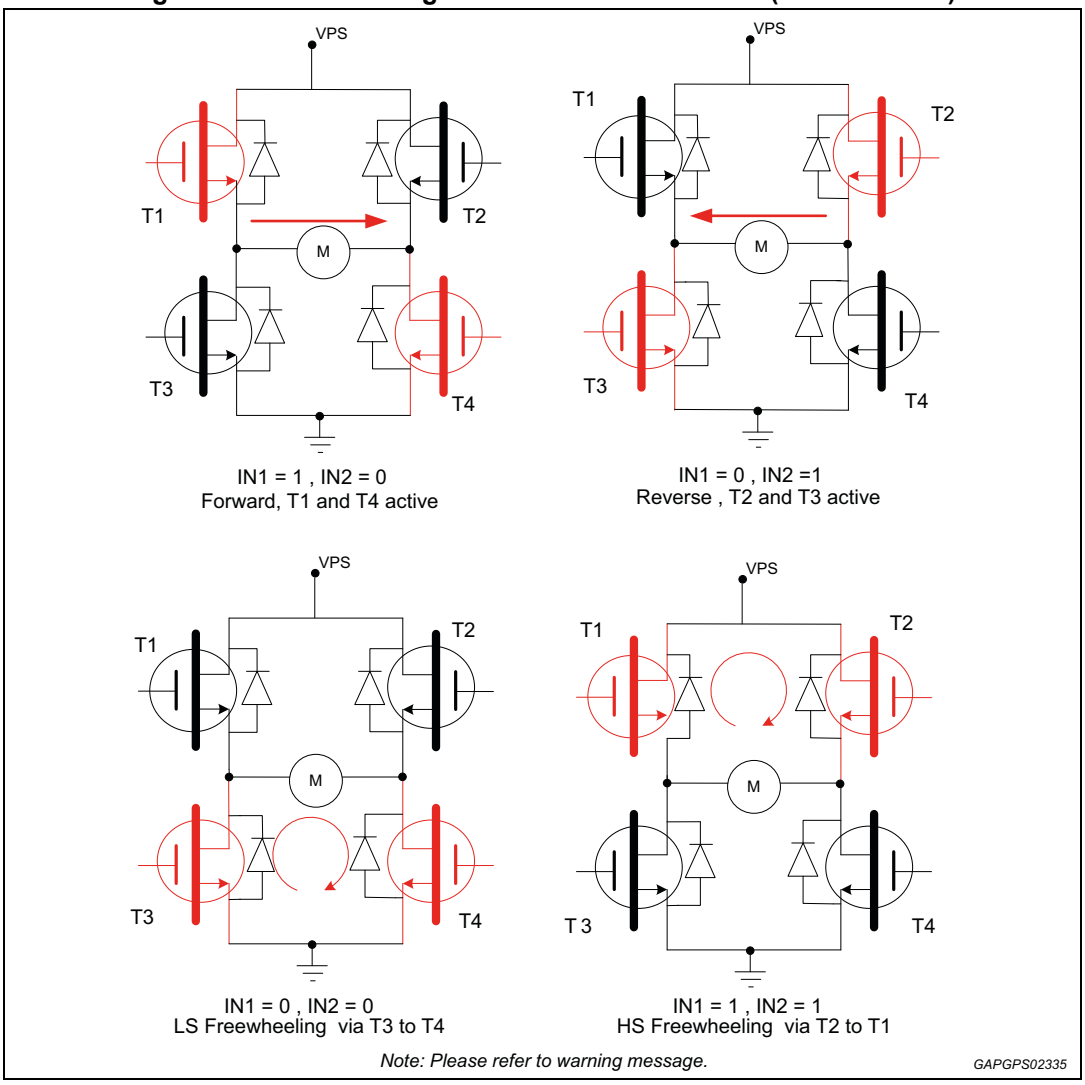


If **IN1/IN2** mode is selected the convention is the following:

- IN1=1, IN2=0 -> OUT1=1, OUT2=0 (***Forward***)
- IN1=0, IN2=1 -> OUT1=0, OUT2=1 (***Reverse***)
- IN1=0, IN2=0 -> OUT1=0, OUT2=0 (***Freewheeling Low-Side***)
- IN1=1, IN2=1 -> OUT1=1, OUT2=1 (***Freewheeling High-Side***)

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Figure 18. 4 cases of high-side/low-side activation (IN1/IN2 mode)



An active freewheeling is automatically set, at the end of the dead time, which means that the power transistor in parallel to the internal freewheeling diode is switched on during freewheeling phase.

This should lead to a power dissipation decrease when driving inductive loads.

Warning: **In case of current limitation event in IN1/IN2 mode, the freewheeling is automatically set back to LS drivers.**

It is advised against selecting the HS recirculation in IN1/IN2 mode as L9960 is not safely protected against external failures (i.e SCG).
For IN1/IN2 mode it is advised to recirculate (active freewheeling) on low-side drivers only.
For PWM mode the recirculation is set by design on LS drivers only.

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4.5.4 Digital inputs control electrical characteristics

Tj = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 45. Digital inputs control electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{ih}	Digital input voltage HIGH (NDIS, DIS, DIR, PWM)	Valid for the extended range of temperature (note(1))	1.75	-	VDD5 +0.3	V
V_{il}	Digital input voltage LOW (NDIS, DIS, DIR, PWM)	Valid for the extended range of temperature	-0.3	-	0.75	V
V_{ihys}	Hysteresis of digital input voltage (NDIS, DIS, DIR, PWM)		100	-	1000	mV
I_{inl}	Input current source for DIS	V_{in} = 0 V	-100	-	-30	µA
		V_{in} = 5 V no back supply vs. the inputs allowed	-5	-	5	
		V_{in} = 19 V Device is kept in tri-state	-50	-	130	µA
I_{inh}	Input current sink for: NDIS / DIR / PWM	3 V < V_{in} < 5.5 V (Iinh_NDIS VDD5>VDD5_UV)	30	-	100	µA
		V_{in} = 19 V Device stays in normal state (Iinh_NDIS VDD5>VDD5_UV)	30	-	100	
		V_{in} < 0.75V (Iinh_NDIS VDD5>VDD5_UV)	-5	-	+90	
Tvvl_acc	TVVL accuracy	-	-25	-	+25	%
T_{SW}	Dead time between active MOS switched OFF to freewheel MOS switched ON	Valid for the extended range of temperature (guaranteed by scan)	1.8	2	2.5	us
Tsw_sr	Dead time between freewheel MOS switched OFF to active MOS switched ON	Including freewheeling MOS Slew Rate delay Valid for the extended range of temperature (guaranteed by scan)	4.1	4.6	5.1	us
Td_dis	NDIS/DIS delay time	DIS / NDIS → 90% OUTx @ I_{out} = 3 A Analog delay at turn-off	-	-	5	µs
Td_filter	DIS asynchronous filtering	Analog EMC filtering (guaranteed by design)	0.2	-	1	µs

1. Extended range of temperature (150, 170°C).

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4.6 Driver configuration

The following features of the driver stage are configurable by SPI allowing to better fit it to the application requirements and also to the type of load.

- Slew rate control
- Current limitation thresholds
- Overcurrent thresholds
- Thermal warning and Shutdown thresholds

4.6.1 Slew rate control

The slew rate of each high side power transistor of the bridge is controlled either during turn-on and turn-off (current and voltage slew rate). The same setting is applied for both switching phases. Moreover, the slew rate is configurable by SPI in order to get the best trade-off between conducted/radiated EMI and power dissipation during switching.

The overall delay implemented between high-side and low-side transistor switching is adjusted automatically to avoid any cross-conduction through one half-bridge in all conditions (**Tsw**).

4.6.2 Current slew rate

The current slew rate can be set in real time by SPI.

The corresponding read/write bit is "**ISR**".

No external component is needed to select the current slew rate range.

Table 46. ISR

Bit config	Description	Condition
0	see table below	-
1	default value see table	Reset value

Note: (-) available in the D7 bit position in SPI command frame 3.

Current slew rate depends upon the ISR/NOSR configuration also on the following bits and conditions (ILIM_REG, overcurrent or T_j) as defined in the table below.

Table 47. Range current slew rate

Range/ condition	ISR	TDSR	NOSR	Comment
SLOW	0	X	0	Slow DI/DT
FAST	1	X	0	Fast DI/DT
SR disabled if ILIM_REG = 1 Or NOC=0	X	X	X	current slew rate not controlled
Slew rate disabled if tj > Otwam	X	1	X	
Slew rate disabled	X	X	1	

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The current SR setting is reported by bit "**ISR_echo**"

Table 48. ISR_echo

Bit status	Description	Condition
0	echo ISR SLOW config	-
1	echo ISR FAST config	Default value

Note: (-) available in the R8 bit position in SPI answer frame 7a.

4.6.3 Voltage slew rate

The voltage slew rate on HS FETs can be set in real time by SPI.

The corresponding read/write bit is "**VSR**". Only the power transistors not used for freewheeling are adjustable, the two others are controlled with a preset slew rate.

Table 49. VSR

Bit status	Description	Condition
0	see table below	-
1	default value see table	Reset value

Note: (-) available in the R6 bit position in SPI command frame 3.

Voltage Slew rate depends upon the **VSR/NOSR** bit configuration also on the following bit/conditions (ILIM_REG, overcurrent or T_j (and TDSR)) as defined in the table below.

Table 50. Voltage slew rate

Range/ condition	VSR	TDSR	NOSR	Condition
SLOW	0	X	0	Slow dV/dT
FAST (Default at POR)	1	X	0	Fast dV/dT
SR disabled if ILIM_REG = 1 Or NOC = 0	X	X	X	Very fast dv/dt
Slew rate disabled if tj > OTwam	X	1	X	Very fast dv/dt
Slew rate disabled	X	X	1	Very fast dv/dt

The voltage SR setting is reported by bit "**VSR_echo**".

Table 51. VSR_echo

Bit status	Description	Condition
0	echo VSR SLOW config	-
1	echo VSR FAST config	Default value

Note: (-) available in the R7 bit position in SPI answer frame 7a.

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The current slew rate control can be disabled and the voltage slew rate can be overwritten by a faster SR when **Tj > OTwarn, ILIM_REG = 1, NOC = 0 or NOSR bit is set**.

Table 52. NOSR

Bit status	Description	Condition
0	NOSR mode NOT allowed	Reset value
1	NOSR mode allowed	-

Note: (-) available in the D8 bit position in SPI command frame 3.

The NOST configuration is reported by bit "**NOSR_echo**"

Table 53. NOSR_echo

Bit status	Description	Condition
0	Echo NOSR mode NOT allowed	Default value
1	Echo NOSR mode allowed	-

Note: (-) available in the R9 bit position in SPI answer frame 7a.

Temperature Dependent Slew Rate: When Tj > OTwarn and in case **TDSR=1** (TDSR bit configuration defined below), the current and voltage slew rates are automatically switched from current configuration mode (SLOW or FAST) to the very fast configuration. In case **TDSR='0'** the current SR mode is kept as selected during OTwarn condition.

Table 54. TDSR

Bit status	Description	Condition
0	TDSR mode NOT allowed condition	Default value
1	TDSR mode allowed	-

Note: (-) available in the D10 bit position in SPI command frame 6.

The TDSR configuration is reported by bit "**TDSR_ECHO**"

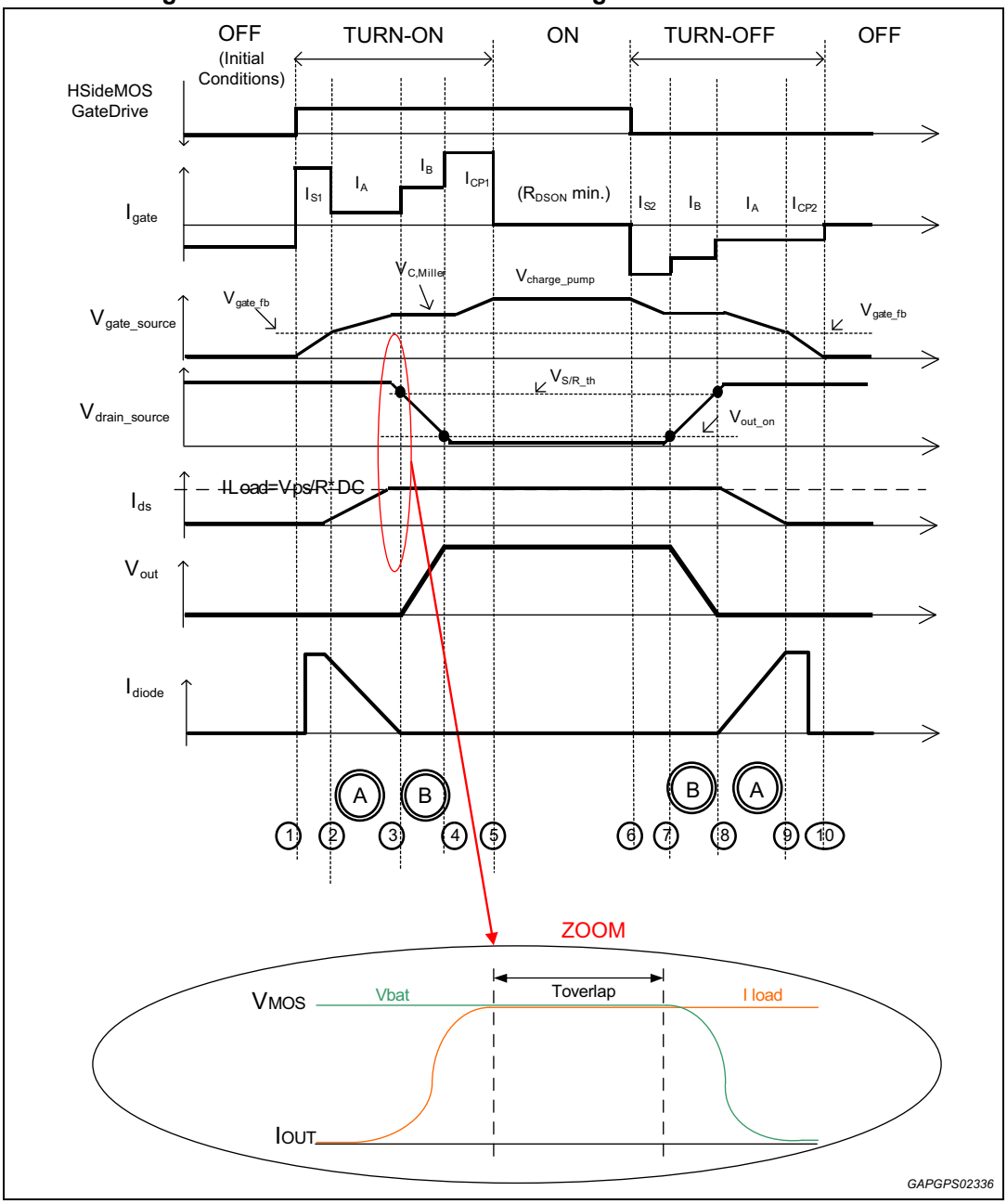
Table 55. TDSR_ECHO

Bit status	Description	Condition
0	TDSR mode NOT allowed condition	Default value
1	TDSR mode allowed	-

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The ideal switching waveforms generated by an inductive load operating in switching mode are described in the following figure. The Initial state of the bridge shown in the figure corresponds to a freewheeling phase.

Figure 19. Ideal waveforms of switching with slew rate control



There are **two phases** during each turn-on and turn-off, in which the output slew-rate is controlled: current slope control for **phase A**, and voltage slope control for phase B (phase A and B refer to *Figure 19*).

During **phase A (current slope control)**, a constant gate current $\mathbf{I_A}$ results in a defined dI_{out}/dt due to the transconductance of the output stage (no closed loop control).

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During **phase B (voltage slope control)**, a constant gate current I_B results in a defined dVMOS/dt due to the Miller capacitance of the output stage. **VS/R_th** is the threshold voltage for the voltage comparator connected to the output. VL is the low voltage of the transistor.

4.6.4 Current limitation

A chopper current limitation is integrated in the L9960. This current limitation is used during transient phases (for instance, fast move of the throttle) or in case of stalled motor shaft, mainly to protect the actuator and also reduce the power dissipation inside the L9960.

When the current reaches the current limitation threshold, the information is stored and latched in a bit called "**ILIM_REG**". This bit can be reset by the three methods defined previously (SPI, DIS, RESET).

Table 56. ILIM_REG

Bit status	Description	Condition
0	Latched I < Ilim_H and Toff > Toffmin	default value
1	Latched I > Ilim_H and Tdiag2 expired	-

Note: (-) available in the R3 bit position in SPI answer frame 8a.

The current limitation strategy is based on one threshold with hysteresis that leads to a controlled current ripple.

As soon as current reaches ILIMH threshold **(TlimH** filter expiration**)** L9960 switches to NOSR mode, the internal SR control (very fast SR), and the **ILIM_REG** bit in ON-Diagnosis will be set to "1". **Tdiag2** timing starts and overcurrent control is now enabled.

The **Tdiag2** timing is used to ensure short circuit detection: in case current reaches Ioc threshold (Toc filter implemented) before Tdiag2 expiration, the device will set the relative OVC diagnosis bits (OCH0,OCH1,OCL0,OCL1) according to the 4 MOS overcurrent thresholds data. L9960 is put in Tristate due to an "overcurrent" event that has been detected on at least one MOS.

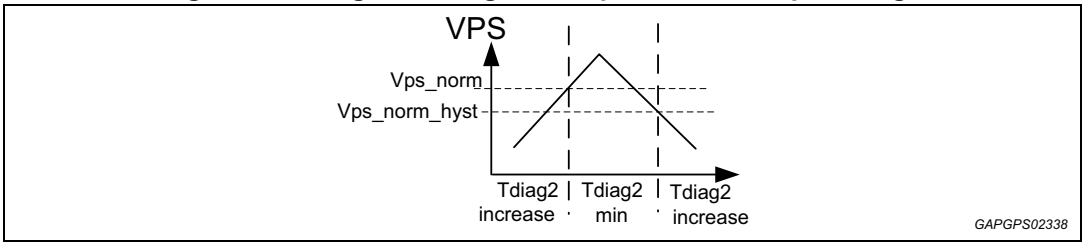
In case of NO OVC detection (no Ioc threshold reached) at the end of the Tdiag2 timing, the device takes the control, deactivates the VVL mode (if selected), and enters current limitation. The HS driver is switched off and it is forced an active freewheeling phase on both LS drivers that decreases current during **t_off_min**. This timing is used to assure a minimum recirculation time, to avoid any switch-on of the HS driver regardless of the PWM="1" user command (**T-off-min** timing will be also triggered by any possible falling edge on PWM before the end of Tdiag2 timing, since PWM information is still being analyzed).

The value of the blanking time depends on a Vps threshold ***Vps_norm***.

If VPS crosses the ***Vps_norm*** threshold while Tdiag2 has already started, its value is not affected.

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Figure 20. Tdiag2 blanking time depends on the Vps voltage



During the active freewheeling phase, the current continues decreasing down to **I_lim_L** threshold (with TlimL filter time implemented).

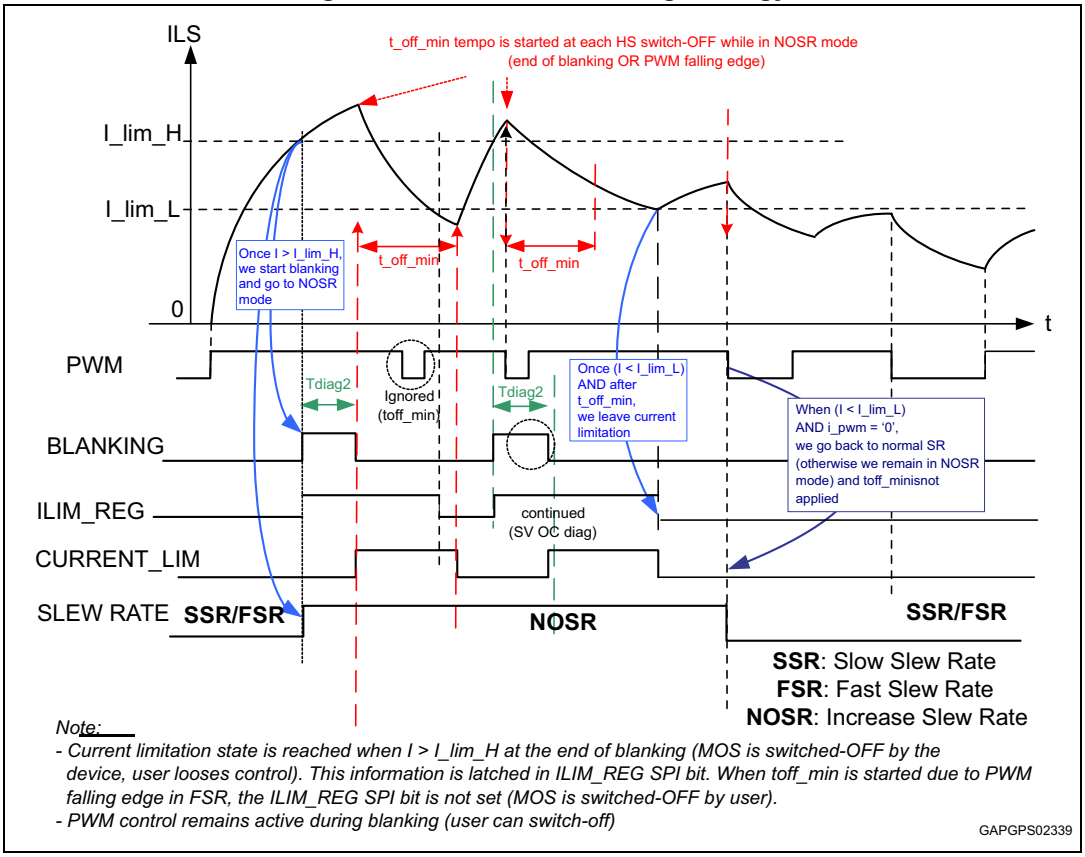
ILIM_REG diagnosis bit is set to "0" as soon as current goes below **I_lim_L+hyst**.

After current is below I_lim_L threshold during at least TlimL and t_off_min is elapsed, L9960 exits CURRENT_LIMITATION (still with NOSR active).

The programmed VSR and ISR are set back if I < I_LIM_L and PWM='0'.

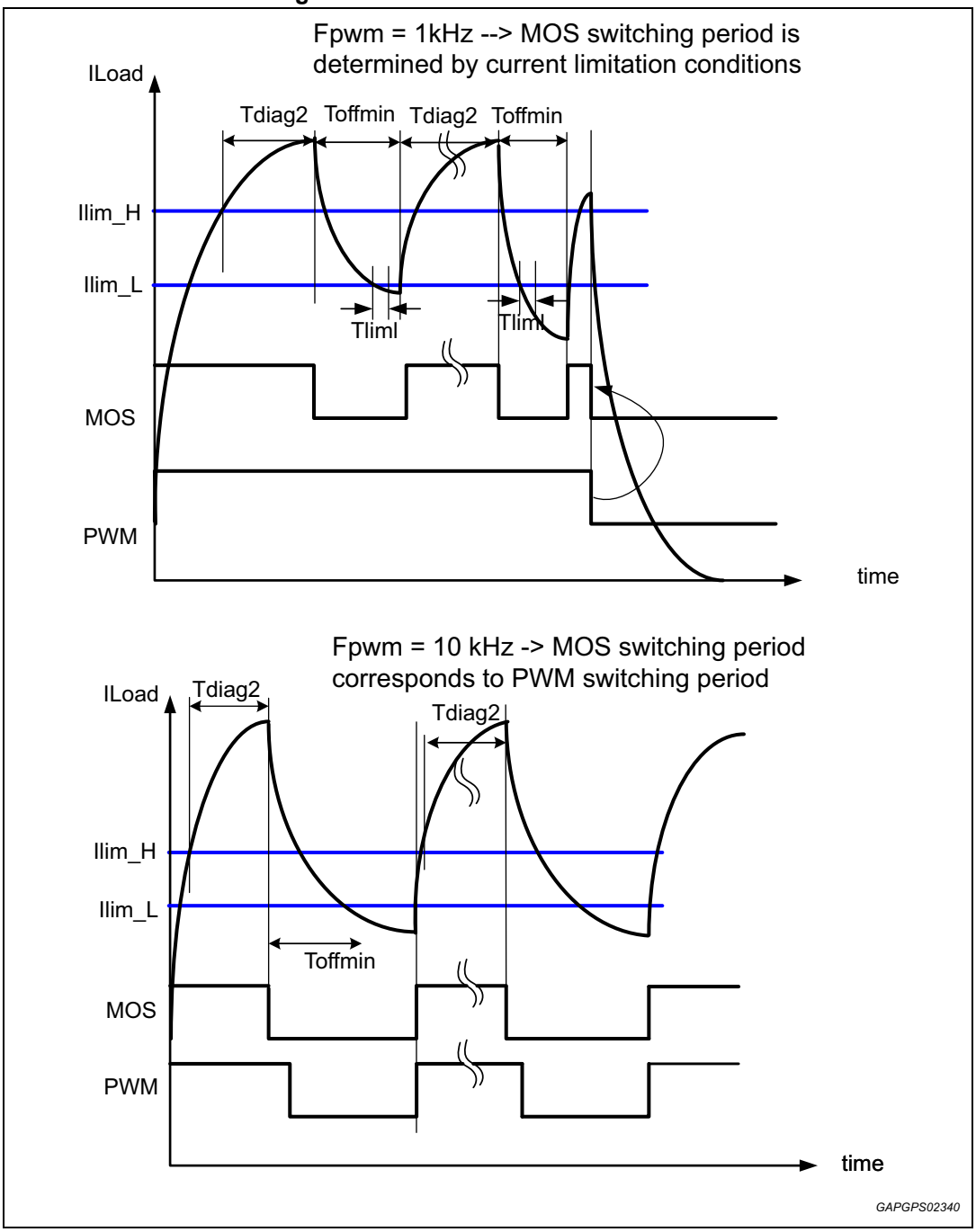
When IN1-IN2 mode, VSR and ISR are set back if I < I_LIM_L and IN1 (or IN2)='0', depending on the toggling pin.

Figure 21. Slew rate switching strategy



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Figure 22. Current limitation schemes



Note: See also Figure 21: Slew rate switching strategy.

The high threshold "**Ilim_H**" of the current limit is selectable by SPI through the bits called "**CL[1:0]**". Four current limits are available to fulfill the transient current requirements of the application. The default value is set to Range 1.

The low threshold "Ilim_L" is based on the high threshold (Ilim_L = Ilim_H – 0.5 (TYP)).

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Table 57. CL[1:0]

2 bits combination	Description	Condition
00	Range 0	-
01	Range 1	reset value
10	Range 2	-
11	Range 3	-

Note: (-) available in the R10,R9 bit positions in SPI command frame 3.

A register report the echo of CL[1:0] configuration register: "**CL_echo[1:0]**"

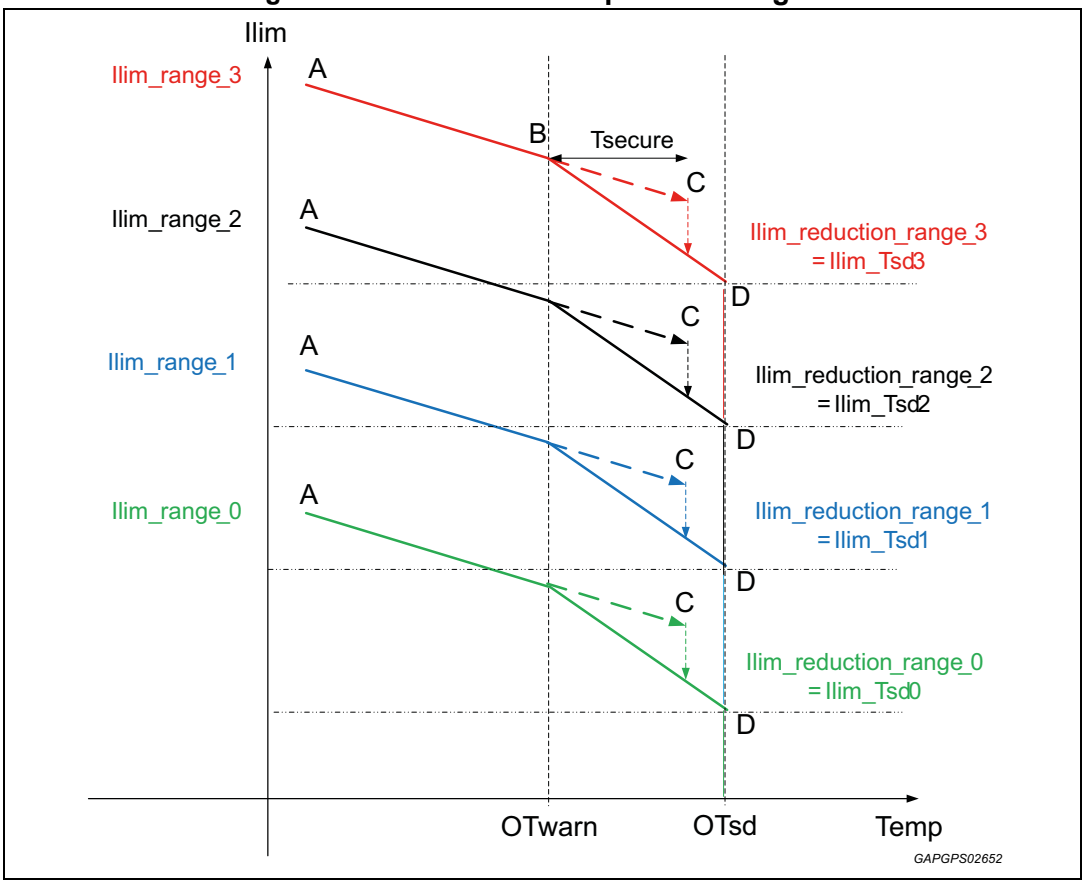
Table 58. CL_echo[1:0]

2 bits status combination	Description	Condition
00	Echo Range 0 config	-
01	Echo Range 1 config	reset value
10	Echo Range 2 config	-
11	Echo Range 3 config	-

Note: (-) available in the R11,R10 bit position in SPI answer frame 7a.

Effect of the temperature

Figure 23. Effect of the temperature diagram



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In order to take into account the junction temperature increase, the current limitation threshold is dynamically adjusted.

Below a junction temperature of "**OTwarn**", the current limit "**Ilim_H**" linearly decreases from dot **A** to dot **B** like as showed in *Figure 24*: Thermal current limitation adjustment.

When Tj exceeds OTwarn, then the **Ilim_H** is automatically decreased, proportionally with temperature, down to **Ilim_Tsd** (dot C on *Figure 24*) in order to reduce the power dissipation and preserve the device.

If, in case of a lower power dissipation, the junction temperature decreases below **OTwarn_hyst**, then the **Ilim_H** consequently would increase staying always on **C-B** or **B-A** line.

It is possible changing the OTwarn and OTsd thresholds via SPI, and reading the ECHO response as showed in the following tables.

Table 59. OTwarn_thr_var

Bit status	Description	Condition
000	0	Default value, Otwarn (150, 170) °C
001	-5	-
010	not allowed	-
011	not allowed	-
100	+5	-
101	+10	-
110	+15	-
111	+20	-

Note: (-) available in the R6,R5,R4 bit position in SPI command frame 4.

Table 60. OTwarn_thr_var_echo

Bit status	Description	Condition
000	0	Default value, Otwarn (150, 170) °C
001	-5	-
010	not allowed	-
011	not allowed	-
100	+5	-
101	+10	-
110	+15	-
111	+20	-

Note: (-) available in the R6,R5,R4 bit position in SPI answer frame 7b.

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Table 61. OTsd_thr_var

Bit status	Description	Condition
000	0	Default value, Otsd (170, 200) °C
001	-5	-
010	-10	-
011	-15	-
100	+5	-
101	+10	-
110	+15	-
111	+20	-

Note: (-) available in the R9,R8,R7 bit position in SPI command frame 4.

Table 62. OTsd_thr_var_echo

Bit status	Description	Condition
000	0	Default value
001	-5	-
010	-10	-
011	-15	-
100	+5	-
101	+10	-
110	+15	-
111	+20	-

Note: (-) available in the R9,R8,R7 bit position in SPI answer frame 7b.

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Table 63. Electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{lim_H}	Current limitation high threshold CL1:0 = 00 / range 0	Tj = -40°C Point A Tj = Otwarn Point B	3.4 3.2	4.5 4.3	5.6 5.4	A A
	Current limitation high threshold CL1:0 = 01 / range 1	Tj = -40°C Point A Tj = Otwarn Point B	5.4 5.1	7 6.6	8.6 8.2	A A
	Current limitation high threshold CL1:0 = 10 / range 2	Tj = -40°C Point A Tj = Otwarn Point B	6.4 6.1	8.3 7.9	10.2 9.7	A A
	Current limitation high threshold CL1:0 = 11 / range 3	Tj = -40°C Point A Tj = Otwarn Point B	8.8 8.1	10.7 10.1	12.8 12.2	A A
I_{lim_Tsd3}	Current limitation high threshold Above OTsd	Tj = Otsd Point C CL1:0 = 11 / range 3	1.25	2.5	3.75	A
I_{lim_Tsd2}	Current limitation high threshold	CL1:0 = 10 / range 2	0.97	1.95	2.92	
I_{lim_Tsd1}		CL1:0 = 01 / range 1	0.83	1.65	2.48	
I_{lim_Tsd0}		CL1:0 = 00 / range 0	0.54	1.08	1.62	
I_{hyst}	Current hysteresis	T_j = -40 °C to T_j = Otwarn; Segment AB (range 1 and range 2)	0.35	0.5	0.8	A
		$T_j \leq 25$ °C range 0 and range 3	0.35	0.5	0.88	A
		T_j > 25 °C to T_j = Otwarn; Segment AB; range 0 and range 3	0.35	0.5	0.8	A
T_{offmin}	Current limitation delay time	Digital delay (guaranteed through scan)	30	-	45	µs
$T_{overlap}$	VMOS high and Iout low overlapping time	Guaranteed by design	0	-	5	µs
T_{diag2}	Blanking time	$V_{ps} > V_{ps_norm}$ Digital filter (guaranteed through scan)	10	-	15	µs
		$V_{ps} < V_{ps_norm}$ Digital filter (guaranteed through scan)	15	-	20	µs
V_{ps_norm}	Beside this V_{ps} threshold the blanking time is low	-	8.9	-	9.6	V

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Table 63. Electrical characteristics (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{ps_norm_hyst}$	Below V_{ps} norm – $V_{ps_norm_hyst}$ threshold blanking time increase	-	0.001	0.1	0.2	V
T_{limh}	High current limitation threshold filtering time	Digital anti glitch filters *(guaranteed through scan)*	0.1	0.55	1	µs
T_{liml}	Low current limitation threshold filtering time		1	2	3	µs
SlowDI/DT	Slow current slew rate on HS drivers	Measured between 20% and 80% of the output current. (*Following limits are related to SR measured with VPS at 16 V and with resistive load (6 Ω). SR are referred to HS drivers only).* (1)	0.3	0.6	0.9	A/µs
FastDI/DT	Fast current slew rate on HS drivers		1	2	3	A/µs
SlowDV/DT	Slow current slew rate on HS drivers	Measured between 20% and 80% of the output voltage. *(Following limits are related to SR measured with VPS at 16 V and pure resistive load (6 Ω). SR are valid for HS drivers only.)*	2	4	7	V/µs
FastDV/DT	Fast current slew rate on HS drivers		5	10	17	V/µs
VFastDV/DT	Very fast voltage slew rate on HS drivers		16	20	30	V/µs

1. Application note will include SR trend with different battery voltage and resistive/inductive load.

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4.7 Driver protections

4.7.1 Over-temperature protection

In case of over-temperature detection (Tj > OTsd), the bridge is disabled. The information is stored on both latched and unlatched bits called ***NOTSD_REG*** and ***NOTSD***.

This bit can be reset by the three different ways. The real-time status of over-temperature is indicated in a bit called ***NOTSD***.

A double flag strategy is implemented: NOTSD indicates real time status, NOTSD_REG latches the fault until cleared.

Table 64. NOTSD

Bit status	Description	Bridge state	Condition
0	Tj>Otsd	Disabled	-
1	Tj<Otsd	Active	Default value

Note: (-) available in the R3 bit position in SPI answer frame 8b.

Table 65. NOTSD_REG

Bit status	Description	Bridge state	Condition
0	Latched if Tj>Otsd	Disabled	-
1	Latched if Tj<Otsd	Active	Default value

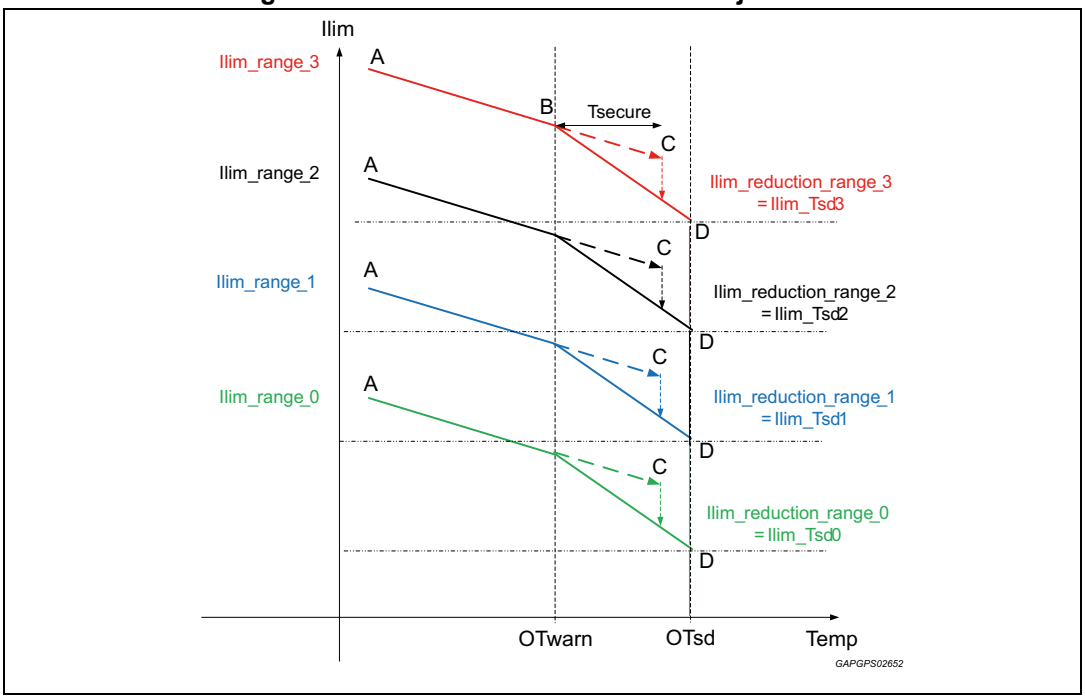
Note: (-) available in the R2 bit position in SPI answer frame 8b.

In case of recurrent thermal shutdown, it is important to preserve chip reliability. A counter "**OTSDcnt**" is implemented and is incremented each time the L9960 enters in thermal shutdown. This counter value "**OTSDcnt**" is accessible through SPI command, and resets either after SPI reading or Low to High transition of the DIS input, once condition below thermal warning (cool down) is reached.

The cool-down condition leads to an automatic self re-engagement of the the bridge, independently of the status of OTSDcnt counter or NOTSD_REG bit.

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Figure 24. Thermal current limitation adjustment



An option (**Tsecure**) can be enabled via SPI and used to delay the decreasing of the Ilim_H when temperature exceeds the OTwarn.

When this function is enabled if the temperature of the chip stays between OTwarn and OTsd shorter than "**OTWARN_TSEC_EN**", Ilim_H is not decreased and the device continues working between dot **B** and **C**. After Tsecure if Tj is still higher than OTwarn, the Ilim_H is reduced letting the device working on **B-D** line.

In case the option is not selected via SPI, once Otwarn thresholds is reached, the current limitation will be adjusted according to line from dot B to D.

Table 66. OTWARN_TSEC_EN

Bit config	Description	Comment
0	OTWARN_TSEC_EN not enabled	Default value
1	OTWARN_TSEC_EN enabled	-

Note: (-) available in the 0 (LSB) bit position in SPI command frame 5.

Table 67. OTWARN_TSEC_EN_echo

Bit config	Description	Comment
0	Echo OTWARN_TSEC_EN not enabled	Default value
1	Echo OTWARN_TSEC_EN enabled	-

Note: (-) available in the 0 (LSB) bit position in SPI answer frame 7c.

When OTwarn thermal threshold is reached, after a debouncing filter" **T_OTwarn**" the information is stored and latched in a bit called **OTWARN_REG**.

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This bit can be reset by (SPI request, DIS or RESET) only if the settings conditions are not present anymore (Tj < OTwarn). This feature is mainly used to reduce the power dissipation and thus the junction temperature.

Table 68. OTWARN

Bit config	Description	Comment
0	if Tj < OTwarn	Default value
1	if Tj > OTwarn	-

Note: (-) available in the R4 bit position in SPI answer frame 8b.

Table 69. OTWARN_REG

Bit status	Description	Comment
0	Latched if Tj < OTwarn-	Default value
1	Latched if Tj > OTwarn-	-

Note: (-) available in the R5 bit position in SPI answer frame 8a.

4.7.2 Over-temperature monitoring electrical characteristics

Table 70. Over-temperature monitoring electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
OTwarn	Over-temperature warning	OTwarn_thr_var set to 000 (default value)	150	-	170	°C
		OTwarn_thr_var set to 001	145	-	165	°C
		OTwarn_thr_var set to 100	155	-	175	°C
		OTwarn_thr_var set to 101	160	-	180	°C
		OTwarn_thr_var set to 110	165	-	185	°C
		OTwarn_thr_var set to 111	170	-	190	°C
OTsd	Over-temperature shut-down threshold	OTsd_thr_var set to 000 (default value)	170	-	200	°C
		OTsd_thr_var set to 001	165	-	195	°C
		OTsd_thr_var set to 010	160	-	190	°C
		OTsd_thr_var set to 011	155	-	185	°C
		OTsd_thr_var set to 100	175	-	205	°C
		OTsd_thr_var set to 101	180	-	210	°C
		OTsd_thr_var set to 110	185	-	215	°C
		OTsd_thr_var set to 111	190	-	222	°C
OThyst	Over-temperature hysteresis	Applicable for OTwarn and OTsd	0	-	5	°C

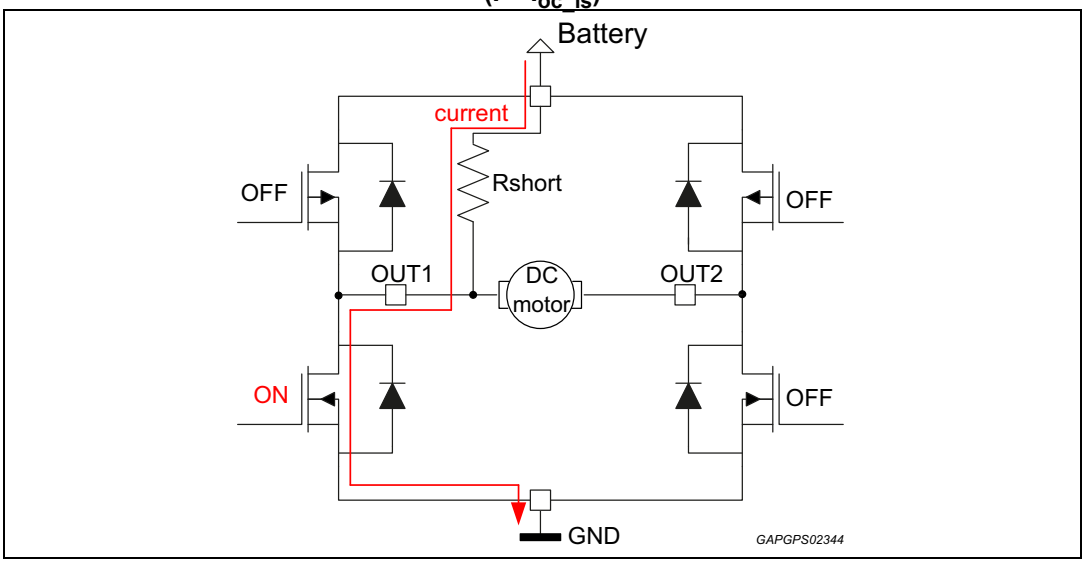
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Table 70. Over-temperature monitoring electrical characteristics (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{TSD}	Over-temperature filtering time	Guaranteed by clock measurement	1.7	2	2.3	µs
Tsecure	Time out to decrease Ilim	Guaranteed through scan	1.5	-	2	s
T_{sdoff}	Over-temperature shutdown release time	Filter on OTSD release (guaranteed through scan)	90	100	110	ms
OTsd-OTwarn	Rang of temperature dependent current reduction	-	20	-	-	°C
T_{j_range}	Junction temperature analog output range	-	125	-	190	°C
T_{j_acc}	Junction temperature analog output accuracy	Guaranteed through scan	-	-	3	°C
T_{OT_warn}	Temperature warning filtering time	-	1	-	3	µs

4.7.3 Short-circuit to battery: over-current detection in low-side transistors

Figure 25. Example of low-side transistor low impedance short circuit to battery ($I < I_{oc_ls}$)



The low-side transistors are protected against over-current due to an output short-circuited to battery. When a low-side transistor is switched on, the current is monitored and if the low-side over-current threshold "**Ioc_ls**" is overtaken for duration longer than "**Toc_ls**", the bridge is switched to disable. This information is stored and latched in bits called "**OCL_x**".

The bits "**OCL_x**" are reset and the bridge is released when diagnostics is read by SPI (if **DIAG_CLR_EN=1** only), or by DIS level change (falling edge) or by RESET.

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4.7.4 Short-circuit to ground: over-current detection in high-side transistor

The high-side transistors are protected against over-current due to an output short-circuited to ground. When a high-side transistor is switched on, the current is monitored and if the high-side over-current threshold "**Ioc_hs**" is overtaken for duration longer than "**Toc_hs**", the bridge is switched to tri-state. This information is stored and latched in bits called "**OCH_x**".

The bits "**OCH_x**" are reset and the bridge is released when diagnostics is read by SPI if **DIAG_CLR_EN=1**, or by DIS level change (falling edge) or by **RESET**.

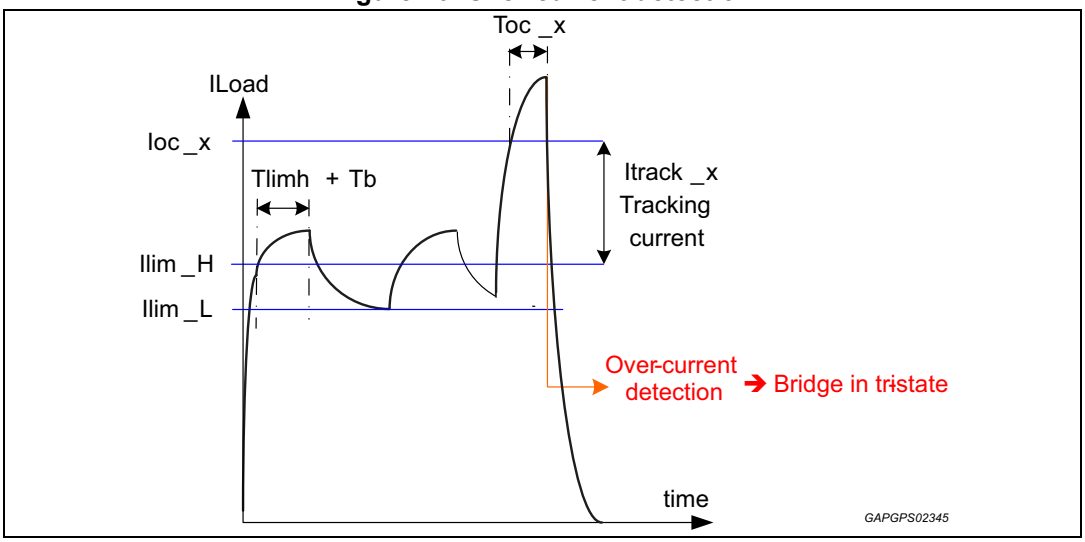
The low-side and high-side over-current thresholds, in case of current limitation on low-side transistors, are respecting the following conditions:

- Itrack_ls = Ioc_ls - Ilim_H
- Itrack_hs = Ioc_hs - Ilim_H

Itrack_ls and **Itrack_hs** are defined as follows:

- In forward condition, the reference for tracking is **Ilim_H** (threshold is referred to LS1)
  - Itrack(HS0) = Ioc(HS0) - Ilim_H(LS1)
  - Itrack(LS1) = Ioc(LS1) - Ilim_H(LS1)
- In reverse condition, the reference for tracking is **Ilim_H** (threshold is referred to LS0)
  - Itrack(HS1) = Ioc(HS1) - Ilim_H(LS0)
  - Itrack(LS0) = Ioc(LS0) - Ilim_H(LS0)

Figure 26. Over-current detection



4.7.5 Load in short-circuit

In order to discriminate between the short circuit of an output to GND and the load in short circuit, a current detection threshold is available for all 4 MOS transistors of the bridge:

- for the 2 freewheeling transistors, **Ilim_H** current detection threshold is used,
- for the 2 other transistors, a current detection threshold called **Ion_th** = Ilim_H is implemented.
- Ion_th only follows AC slope when the temperature is changing
- Bits are to be stored when validity bit is set.

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4.7.6 Over-current detection electrical characteristics

Parameters are specified at 2 temperatures -40°C and +150°C;
for temperatures between -40°C and +170°C, the current values are interpolated.

Table 71. Over-current detection electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{oc_ls} I_{oc_hs}	Over-current threshold CL1:0 = 00 / range 0	Tj = -40°C	5.4	7	8.6	A
		Tj = 150°C	5.2	6.8	8.4	
	Over-current threshold CL1:0 = 01 / range 1	Tj = -40°C	7.4	9.5	11.6	A
		Tj = 150°C	7.1	9.2	11.2	
	Over-current threshold CL1:0 = 10 / range 2	Tj = -40°C	8.4	10.8	13.2	A
		Tj = 150°C	8.1	10.4	12.7	
	Over-current threshold CL1:0 = 11 / range 3	Tj = 150°C	9.8	12.1	14.3	A
		Tj = -40°C for I_{oc_ls}	10.4	12.6	15.8	A
		Tj = -40°C for I_{oc_hs}	10.4	12.6	14.9	A
I_{track_ls} I_{track_hs}	Tracking current for CL1:0 ≠ 10 & 11	-	2	2.5	5	A
I_{track_ls} I_{track_hs}	Tracking Current for CL1:0 =10	Tj ≤ 25 °C	1.8	2.5	5	A
	Tracking Current for CL1:0 =10	Tj = 150 °C	2	2.5	5	A
I_{track_ls}	Tracking current for CL1:0 = 11	-	1.6	1.9	5	A
I_{track_hs}	Tracking current for CL1:0 = 11	Tj ≤ 25 °C	1.1	1.9	5	A
	Tracking current for CL1:0 = 11	Tj = 150 °C	1.6	1.9	5	A
Toc_ls Toc_hs	Low-side & high-side over-current detection filtering time	-40°C ≤ Tj ≤ 150°C Digital filter (guaranteed through scan)	1	-	2	µs
I_{oc_on}	Non-Freewheeling MOS LSC threshold CL1:0 = 11 / range 0	Tj = -40°C	3.4	-	5.6	A
		Tj = 150°C	3.2	-	5.4	
	Non-Freewheeling MOS LSC threshold CL1:0 = 11 / range 1	Tj = -40°C	5.4	-	8.6	A
		Tj = 150°C	5.1	-	8.2	
	Non-Freewheeling MOS LSC threshold CL1:0 = 11 / range 2	Tj = -40°C	6.4	-	10.2	A
		Tj = 150°C	6.1	-	9.7	
	Non-Freewheeling MOS LSC threshold CL1:0 = 11 / range 3	Tj = -40°C	8.8	-	12.8	A
		Tj = 150°C	8.1	-	12.2	

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Table 71. Over-current detection electrical characteristics (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{ionh}	I_{on} threshold filtering time	Digital anti glitch filters on rising edge (guaranteed through scan)	1	2	3	µs
T_{ionl}		Digital anti glitch filters on falling edge (guaranteed through scan)	1	2	3	µs
I_{hyst}	Current hysteresis on Ion	Tj = -40°C to +150°	0.4	0.5	0.6	A

4.8 Diagnostics and registers descriptions in case of validity bit configuration

A detailed diagnostic of the H-bridge is available through SPI communication.

The diagnostic words are used to report the following information:

- H-Bridge failures,
- H-bridge functional status,
- H-bridge HWSC test result.

A detailed diagnostic is performed using a validity concept. The concept of the validity of the diagnostic is to provide the information “diagnostic done” OR “diagnostic NOT done”.

4.8.1 Diagnostic Reset strategy

When diagnosis bits are latched, they can only be released by one of the following conditions:

- Transition from "Disable" (High) to "Enable" (Low) on DIS pin,
- Diagnostic register read by SPI (see details on each failure release) depending on "**DIAG_CLR_EN**" bit status,
- Reset condition.

Usually, when the diagnostic register is reset, the bridge is switched back to normal mode driven by DIR and PWM or IN1 and IN2. All the settings are kept as before the failure. In case of SPI read, no additional action on DIS is needed.

When the diagnosis is combined with a protection of the driver (**driver put into tri-state**), a reading by spi clears the diagnosis, but the bridge is released only at the next PWM rising edge event.

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4.8.2 Diagnostic reset bit

In case of "**DIAG_CLR_EN**" set to **HIGH** (RESET value), all the bits of the diagnostic register can be cleared by the three possibilities described in the previous section.

In case of "**DIAG_CLR_EN**" set to **LOW**, the SPI diagnostics reading doesn't clear the flag for diagnostics flags bits reported in *Table 72*. Therefore, the bridge is kept in **disable state** until a transition from "high" to "low" on DIS pin or RESET condition.

Table 72. DIAG_CLR_EN

Bit config	Description	Comment
0	OC and OT diagnostic status bits not cleared by SPI reading	-
1	Clear of diagnostic status bits by SPI reading	Reset value

Note: (-) available in the R0 bit position in SPI command frame 3.

A register reports the echo of **DIAG_CLR_EN** configuration regsiter: "**DIAG_CLR_EN_echo**"

Table 73. DIAG_CLR_EN_echo

Bit config	Description	Comment
0	OC and OT diagnostic status bits not cleared by SPI	-
1	Clear of diagnostic status bits by SPI reading	Default value

Note: (-) available in the 1st bit position in SPI answer frame 7a.

If a new diagnostic occurs simultaneously with diagnostic register reset, this new diagnostic becomes the new status of the diagnostic register (new information must not be lost).

Known limitation:

This diagnostic reset strategy has a limitation: if the SPI transfer is not correct (for example only 15 clock periods instead of 16) and the diagnostic register has already been cleared, if the failure is no more present, the information is lost (it has not been transferred to the µcontroller).

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Status bits description

Note: usually status bits information is not impacted by any SPI communication, whatever the "DIAG_CLR_EN" state is.

Table 74. Status bits description

Name	Description	SPI read impact
Config_CC_state_echo	Echo of programmed the Communication Check	No
CL[1:0]	Echo of the programmed Current Limitation Range	No
NOSR echo	Echo of the programmed Increased Slew Rate	No
ISR echo	Echo of the programmed Current Slew Rate range	No
VSR echo	Echo of the programmed Voltage Slew Rate	No
DIAG_CLR_EN echo	Echo of the programmed DIAG_CLR_EN bit	No
VVL_MODE echo	Echo of the programmed VVL mode	No
TVVL[3:0]	Echo of the programmed freewheel duration in VVL mode	No
ASSP Name[9:0]	ASSP Name	No
Silicon Version[3:0]	Silicon Version	No
NSPREAD echo	Echo of the programmed Spread Spectrum mode	No
TSW_low_current_echo	Echo of the programmed Cross- condition improve mode	No
I[23:0]	Echo of tracking part number	No
ASSP	Echo of ASSP device	No
Code version[7:0]	Echo of digital tracking version	No
TDIAG1[2:0]	Echo of programmed TDIAG1 validation time	No

Table 75. Diagnostics bits description

Name	Description	POR value	Bit State	DIAG_CLR_EN impact	H-bridge state	reported in NGFAIL
DIAG_OFF[2:0]	Off-state diagnostic (open-load, short-circuit)	111	**Latched**	No	-	**Yes**
OL_ON_STATUS[1:0]	On-state diagnostic (open-load)	01	Not latched	No	-	**Yes**
VPS_UV	Vps Under-voltage detection	0	Not latched	No	Hi-Z if "0"	No
VPS_UV_REG	Vps Under-voltage detection	0	**Latched**	Yes	Hi-Z if "0"	No
VDD_UV	Vdd Under-voltage detection	0	Not latched	No	-	No
VDD_UV_REG	Vdd Under-voltage detection	0	**Latched**	Yes	-	**Yes**
VDD_OV_REG	Vdd Over-voltage detection	0	**Latched**	Yes	-	**Yes**
VDD_OV	Vdd Over-voltage detection	0	Not latched	No	Hi-Z if "0"	No

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Table 75. Diagnostics bits description (continued)

Name	Description	POR value	Bit State	DIAG_CLR_EN impact	H-bridge state	reported in NGFAIL
ILIM_REG	Current limitation mode	1	**Latched**	No	-	No
OTWARN	Over-temperature warning	0	Not latched	No	-	No
OTWARN_REG	Over-temperature warning	0	**Latched**	No	-	No
NOTSD	Over-temperature shut down	1	Not latched	Yes	-	No
NOTSD_REG	Over-temperature shut down	1	**Latched**	Yes	-	**Yes**
BRIDGE_EN	Bridge “Enable”	0	Not latched	No	Hi-Z if “0”	No
OCH0[1:0]	Over-current on high-side transistor OUT 0	10	**Latched**	Yes	Hi-Z if “00”	**Yes**
OCL0[1:0]	Over-current on low-side transistor OUT 0	10	**Latched**	Yes	Hi-Z if “00”	**Yes**
OCH1[1:0]	Over-current on high-side transistor OUT 1	10	**Latched**	Yes	Hi-Z if “00”	**Yes**
OCL1[1:0]	Over-current on low-side transistor OUT 1	10	**Latched**	Yes	Hi-Z if “00”	**Yes**
VDD_OV_L[2:0]	Counter for duration of VDD_OV event	001	**Latched**	No	-	No
Error_count[3:0]	Number of over-current events	0000	**Latched**	Yes	-	no
CC_latch	-	1	**Latched**	No	Hi-Z if "0"	**Yes**
NDIS status	-	-	Not Latched	No	-	**Yes**
HWSC/LBIST_status (1)	status of the HWSC/LBIST	000	Not Latched	No		**Yes**
OTSDcnt[5:0]	Number of OTSD events	000000	Not Latched	No		No
Load in Short Circuit	part of the general Overcurrent Diagnostics	10	**Latched**	Yes	Hi-Z if "11"	**Yes**

1. In case of SPI interrogation for HWSC/LBIST in between test execution, the answer could be "0xx".

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4.8.3 Global Failure Bit NGFAIL definition

NGFAIL groups the following failures:

- Over-current on each of the 4 MOS (Ion threshold not taken into account, validity bit not taken into account), including the load in short-circuit
- Open-load in ON-state
- Open-load (or shorts) in OFF-state
- HWSC (or BIST) not executed or failing
- CC_latch_status
- VDD Over-voltage (latched)
- VDD Under-voltage (latched)
- NOTSD_REG
- UV_CNT_REACHED = 1 and UV counter stop
- NDIS = 0 (also when forced low externally)

Once all the conditions which determine the assertion of **NGFAIL** are cleared (failure no more present and the latched version of the failure bit is cleared), the bit is de-asserted.

In case **NGFAIL** is flagged because of NOTSD_REG assertion, the flag remains set until a toggle of DIS pin is performed.

There is no failure considered on Vps undervoltage, despite the bridge goes in OFF-state. There is no clear of **NGFAIL** by itself, the reported error itself has to be cleared in order to clear **NGFAIL**.

Table 76. NGFAIL

Bit status	Description	Condition
0	failure	-
1	no failure	default value

Note: (-) available in the R4 bit position in SPI answer frame 8a.

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4.8.4 Diagnostic of "Over-current" in on-state

The diagnostics of over-current on high-side and low-side transistors are based on 2 bits for each transistor.

Table 77. Diagnostic of "Over-current" in on-state

2 Bits status by MOS		OCH0[1:0] / OCH1 [1:0] / OCL0[1:0] / OCL1[1:0]	Priority	Condition
Bits Status 1	Bits Status 0			
NOC	ION_TH			
1	0	Diag not done or no over current detection	3 (lowest)	Default value
0	0	Diag done, over current detection	1 (highest)	-
1	1	Diag done,load short detect on diagonal MOS	2	-

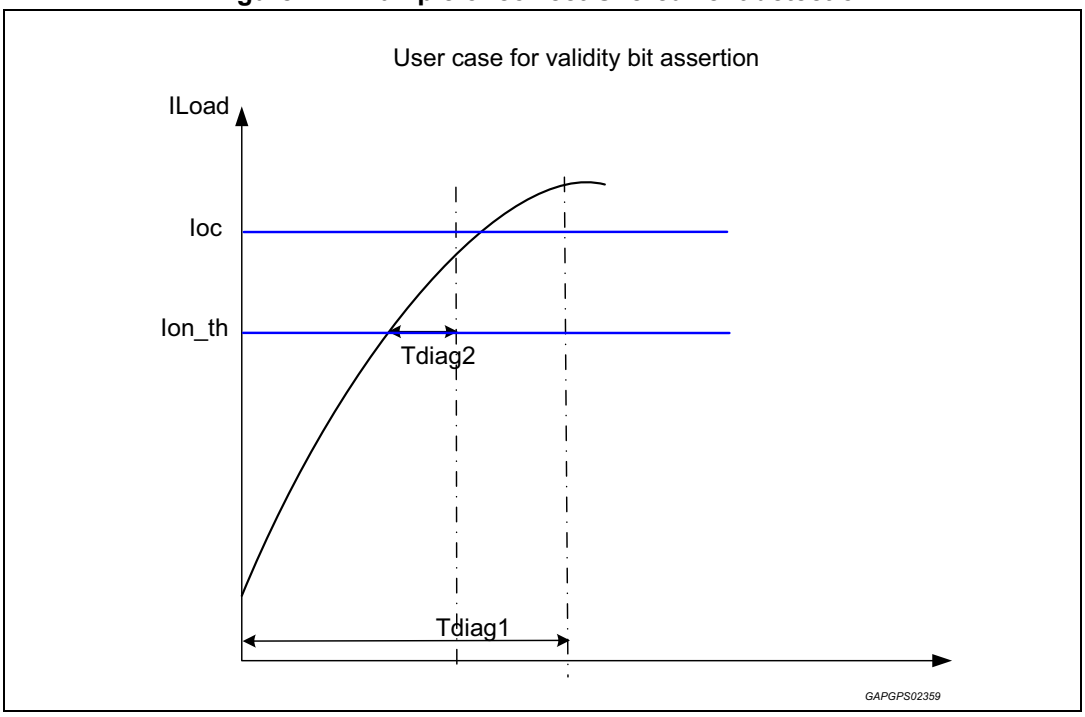
Note: (-) available in the R10,R9,R7,R6,R4,R3,R1,R0 bit position in SPI answer frame 1.

First bit is overcurrent and second bit is load short detection.

- **OCxx[1]** bit is ***over current detection***: “0” means over current detection
- **OCxx[0]** bit is ***Ion current threshold*** detection: “1” means above **Ion_th threshold + Ioc** on diagonal MOS (this bit allows a reliable detection of load in short circuit).

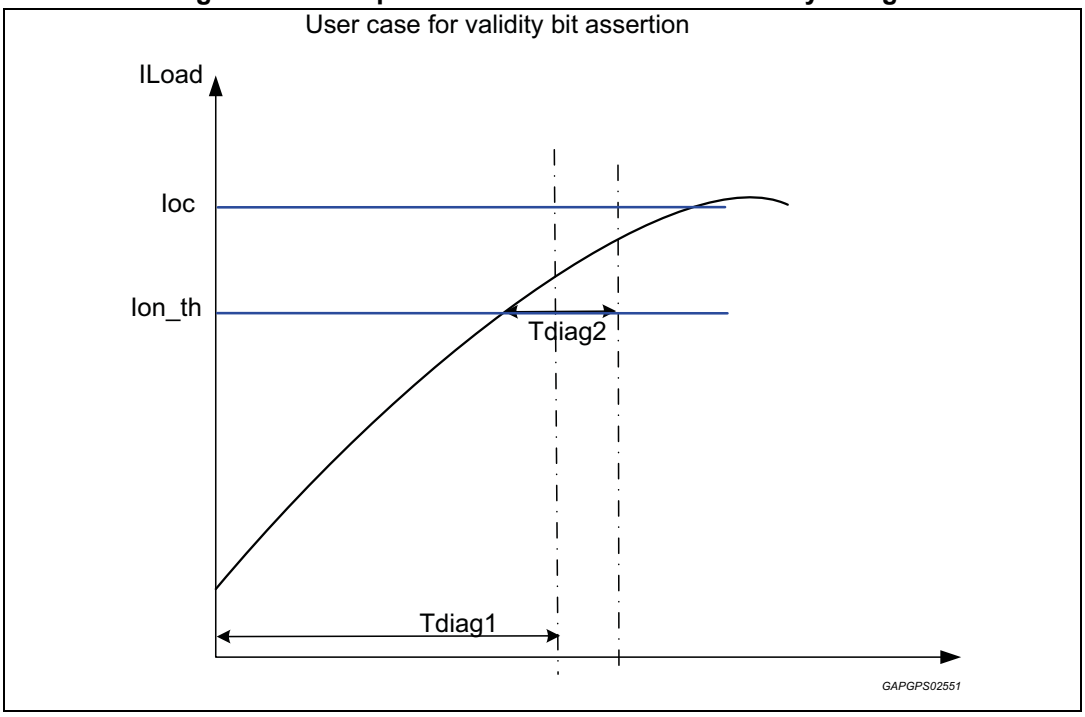
Note: OCxx[1:0] = 2’b01 is not a possible condition.

Figure 27. Example of correct Overcurrent detection



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Figure 28. Example of NO Overcurrent detection by Tdiag2



The way to define the validity of the diagnostic is based on a programmable time called "**Tdiag1**" and the fixed time "**Tdiag2**". As soon as an activation command is set (PWM edge or IN1!=IN2), the timing "**Tdiag1**" starts.

Tdiag1 is defined as the maximum programmable time in which it is expected that the current reaches the current limitation threshold for a valid detection. **Tdiag2** starts automatically when **Ion_th** is overcome and depends on the conditions on Vps (pls refer to **Vps_norm** thresholds on *Table 63*). Both are digital filters and guaranteed through scan. Depending on the load current profile the two filters could be overlapped or as worst case, sequential.

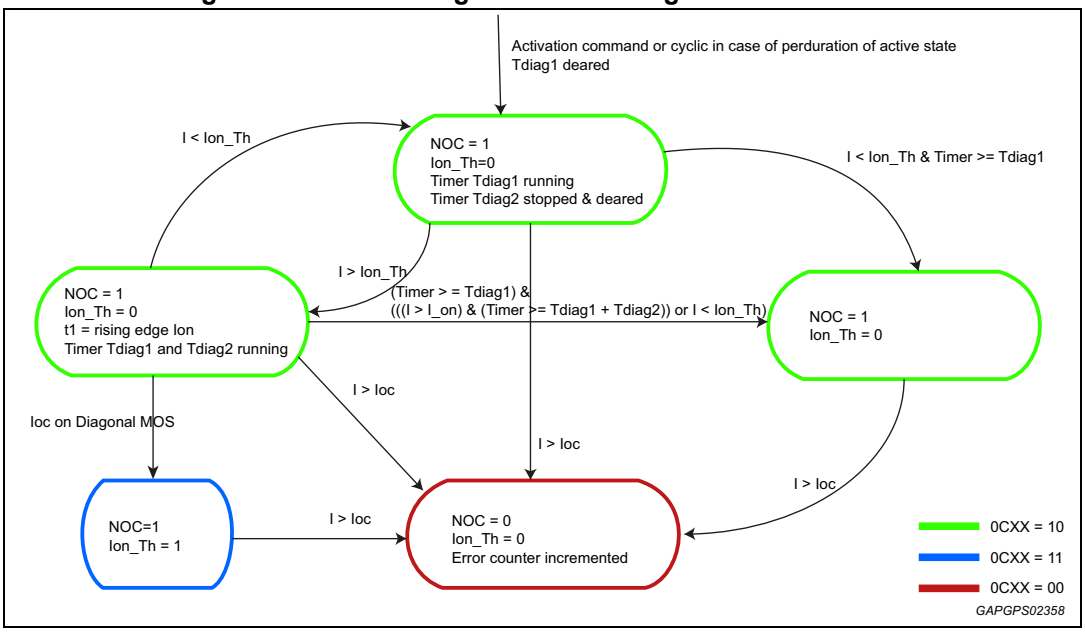
Here below it is explained the diagnostics result, with respect to **Iload** and **Tdiag1** and **Tdiag2**:

- If the current reaches the over-current threshold "OC_hs(ls)" for a duration "**Toc_hs** (ls)" during diagnostics (Tdiag1, Tdiag2), the failure is detected and the bits "OCxx1:0" are set to "00", which means "**OVER-CURRENT** ".
- If the current is above **I_lim_H** and below the over-current threshold "**OC_hs**(ls)" and the duration above Ion_threshold is shorter than "**Tdiag2**", then "OCxx1:0" are set to "10" which means "**NO OVER-CURRENT**".
- If the current is above **I_lim_H** and below the over-current threshold "OC_hs(ls)" and the duration above Ion_threshold is longer than "**Tdiag2**", then "OCxx1:0" are set to "10" which means "**NO OVER-CURRENT**" (current limitation reached).
- If the **Tdiag1** duration cannot be reached and no overcurrent detected for duration **Toc_hs**(ls), then "OCxx1:0" are set to "10" which means "**NO OVER-CURRENT**".
- If the current is above Ion_threshold and below the over-current threshold "OC_hs(ls)" and an overcurrent is detected in same time as diagonal MOS, then "OCxx1:0" are set to "11" which means "**NO OVER-CURRENT BUT IO-ON** is above threshold"

In case the overcurrent threshold is reached after Tdiag1+Tdiag2 expiration (worst case), the device is still protected by an automatic shut-off after Timer expiration.

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Figure 29. Current diagnostic state diagram for each MOS



The condition ***I > Ioc*** means a current higher than **Ioc_ls** (or **Ioc_hs**) during the confirmation time ***Toc_ls*** (or ***Toc_hs***).

The condition ***I > Ion_th*** means a current higher than **Ion_th** during the confirmation time ***Tion_th***.

Error_count is incremented each time one MOS goes into over-current condition after the end of the timers. This reflects short-circuit conditions while ON. In case after overcurrent condition, the DIS pin is set to '1' by µC, the register is cleared at the next fall edge of DI signal or after SPI reading.

Table 78. Error_count[3:0]

4-bit combination	Description	Condition
0000		Default value
xxxx	Decimal value accordingly	-

Note: (-) available in the R4,R3,R2,R1 bit position in SPI answer frame 8c

Here below it is shown the validity bit time programming for **Tdiag1** (guaranteed through scan):

Table 79. TDIAG1 (µs)

3-bit config combination	Description	Condition
000	9	-
001	14	-
010	20	-
011	25	-
100	30	-

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Table 79. TDIAG1 (µs) (continued)

3-bit config combination	Description	Condition
101	35	-
110	40	-
111	45	Reset value

Note: (-) available in the R6,R5,R4 bit position in SPI command frame 3.

Validity echo bit time programming status of Tdiag1:

Table 80. TDIAG1_echo[2:0]

3-bit status combination	Description	Condition
000	echo 9 µs config	-
001	echo 14 µs config	-
010	echo 20 µs config	-
011	echo 25 µs config	-
100	echo 30 µs config	-
101	echo 35 µs config	-
110	echo 40 µs config	-
111	echo 45 µs config	Default value

Note: (-) available in the R6,R5,R4 bit position in SPI answer frame 7a.

Validity bit time programming **Tdiag2**:

- **Tdiag2** is the blanking time when the MOS is involved for the current limitation (not belonging to the free wheel).

Overcurrent diagnostic reset

The overcurrent diagnostics bit can be cleared by means of one of the following conditions:

- **Power On Reset** sequence
- Transition from "Disable" to "Enable" on the pin DIS,
- Diagnostic register read by SPI (in case bit "***DIAG_CLR_EN***" = 1).

Note: if several diagnostics are performed between two SPI reads, the over-current diagnostic bits can only be overwritten if the new diagnostic has a higher priority than the one already stored in the register.

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4.8.5 Diagnostic of "Open Load" in on-state

The diagnostic of the Open Load in on-state is possible as long as, at least, one freewheeling cycle (meaning PWM = 0) is done through the body diode of the low-side transistor meaning "passive freewheeling". The diagnostics is consequently available in PWM/DIR and IN1/IN2 mode when the recirculation is performed through LS drivers.

After OL diagnostics activation, to update the OL status register it is needed that a time **Tstable_on** is expired.

This is allowed by setting the bit **OL_ON** = “1” each time the open-load diagnostic is requested:

Table 81. OL_ON

Bit config	Description	Condition
0	Open Load in on-state disabled	Reset value
1	Open Load in on-state enabled	-

Note: (-) available in the D9 bit position in SPI command frame 6.

After the first PWM ='0' cycle the active HS is turned-off and a passive recirculation phase is present to avoid shoot-through before enabling the ls driver and perform the OL diagnostics after **T_stable_on**.

The voltage of the low-side transistor drain is monitored to track a recirculation current (drain voltage below ground in case of current recirculation).

Table 82. OL_ON_STATUS [1:0]

Bit status	Description	Priority	Condition
00	OL disabled	-	-
01	No diag done	Low	Default value
10	OL / Diag done	High	-
11	No OL / Diag done	Medium	-

Note: (-) available in the R1,R0 in SPI answer frame 8b.

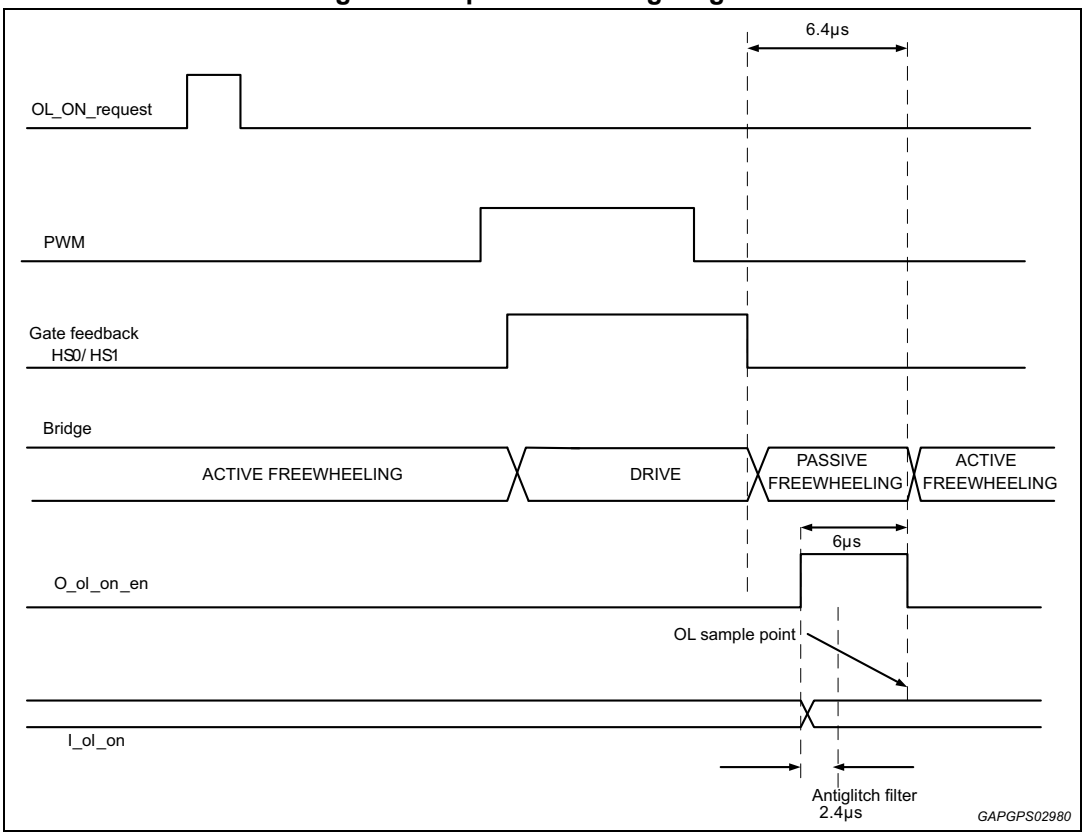
In case **OL_ON** bit = “0” (Diag function disabled), the **OL_ON_STATUS**=[00].

Note: if several diagnostics are performed between two SPI reads, the open-load diagnostic bits can only be overwritten if the new diagnostic has a higher priority than the one already stored in the register.

After the OL fault disappears there is no need to perform any action on DIS or PWM in order to come back to Normal mode (bridge directly switch to Normal operating).

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Figure 30. Open load timing diagram



4.8.6 On-state diagnostics electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 83. Open Load in ON-state electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{stable_On}	On-state diagnostic filtering time	Digital filter not re-triggerable (guaranteed by scan)	4	6	8	µs
t_{OI_On}	Anti glitch filter	Digital filter applied on i_ol_on (guaranteed by scan)	1	2	4	µs
V_{outx_SR}	Voltage during passive freewheeling	Passive freewheeling phase	-150	-	-10	mV

When operating at low duty cycle and high frequency, in case the load current is very small, it may occur that the toggling VOUT_x stays almost at ground level during passive freewheeling; this may lead to not fully operating Open Load diagnostic in ON state.

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4.8.7 Off-state diagnostic

The Off-state diagnostic is activated via a dedicated SPI command “**OFF STATE diagnosis**” by enabling the bit **TRIG**.

Table 84. TRIG

Bit config	Description	Condition
0	OFF-state diagnosis not triggered	Reset value
1	Trigger OFF-state diagnosis	-

Note: (-) available in the D0 bit position in SPI command frame 9.

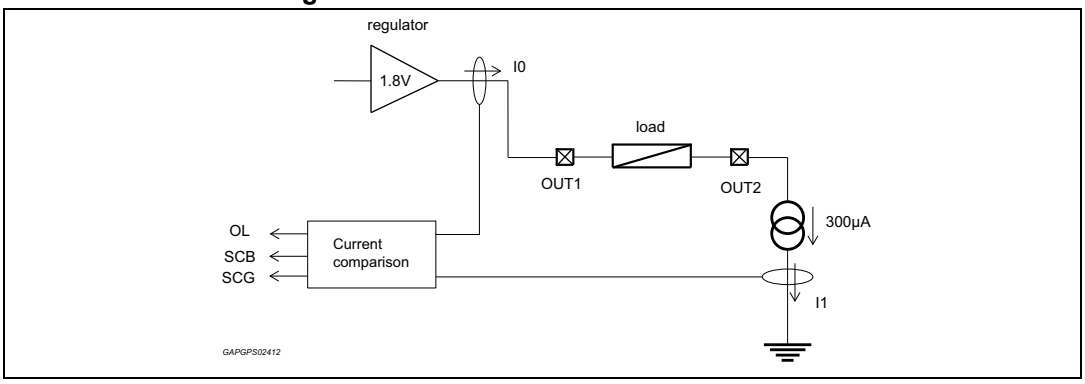
Once diagnosis sequence was performed, Off-state Diagnostic result is available through the same SPI command “**OFF STATE diagnosis**”.

This diagnostic is performed in **disable state condition**, set only by DIS activation and on the condition that there was not a protection previously set (reported in **NGFAIL** and **VPS_UV**), which means during a disable state phase occurring after an active-state phase of the bridge or after reset state only in case of DIS activation.

Off state diag is allowed when **NGFAIL** = '1' - Off state diag is allowed when **NGFAIL** = '0' only when the source of failure is from OFF state diagnostics itself.

Off-state diagnostic sequence

Figure 31. Structure and detection criteria



If the load is connected and when the off state diagnostics is enabled, L9960 aims at regulating the voltage on OUT1 at a typical value of 1.8 V with a typical current consumption of 300 µA.

- **Short to Ground** is detected if I0 < - 930 µA (typ). SCG fault is guaranteed for currents higher than SCG threshold.
- **Short to Battery** is detected if I0 is >190 µA (typ). SCB fault is guaranteed for currents lower than SCB threshold.
- **Openload** is detected if I0 > min (OUT1_OL_Thr) to min (OUT1_SCB_Thr)

In order to avoid any wrong diagnostic, a filtering time "**Thz**" is implemented before performing the diagnostic.

Thz is started on DIS rising edge event or reset (POR/SW) event only.

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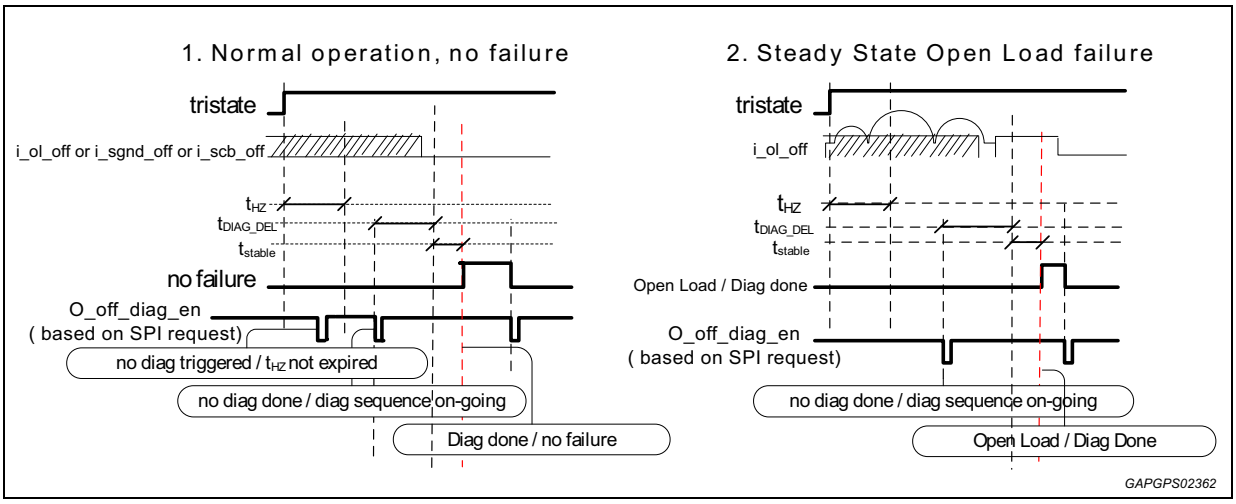
When the **TRIG** command is set, the current sources needed to run the OFF state diagnosis are turned-on. A delay is implemented to complete the settling of the current sources (**Tdiag_del**).

Additionally, a filtering of the diagnosis is done. This filter time is **Tstable_off** and if the diagnosis input is stable during **Tstable_off**, the diag is performed and the failure is latched. If the diagnosis input is switching during **Tstable_off**, the diag is not performed and the filter time is re-triggered on each edge of the diagnosis input.

A time-out (**Ttimeout)** is implemented in parallel to **Tstable_off** in order to filter out too long and unstable input.

Here below the OpenLoad in Offstate diagram, showing two application cases.

Figure 32. Open load off state diagnosis diagram



The Off-state diagnostic table is reported as follows:

Off-state diagnostic principle

Table 85. DIAG_OFF[2:0]

Bits status	Description	Priority	Condition
000	Not used	-	-
001	Open Load / Diag done	6(Highest)	-
010	Short circuit to BAT	5	-
011	Short circuit to GND	4	-
100	No failure / Diag done	3	-
101	No Diag triggered / incorrect state (active state or vps_uv state)	2	-
110	No Diag triggered / Thz not expired	1	-
111	No Diag done / Diag sequence (tdiag_del + tstable) on going	0 (Lowest)	Default value

Note: (-) available in the R2/R1/R0 bit position in SPI answer frame 9.

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4.8.8 Off-state diagnostic electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 86. Off-state diagnostic electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
OUT1_OL_Thr	Current threshold for OpenLoad detection (in relation with SCB range defined below)	-	-30	-	OUT1_SCB _Thr - 3µA	µA
OUT1_SCG_Thr	Current threshold for SCG detection	-	-1200	-	-500	µA
OUT1_SCB_Thr	Current threshold for SCB detection	-	100	-	500	µA
Thz	Delay time before allowing off-state diagnostic	After disable, including reset (guaranteed through scan)	200	250	300	ms
Tstable_off	Off-state diagnostic filtering time	Starts at the end of Tdiag_del Applied to the combination of the 3 inputs (guaranteed through scan)	36	40	50	µs
Tdiag_del	Settling time for Off-state diagnostics current generators; Timing for reliable diagnostic	(guaranteed through scan)	600	749	900	µs
IOL (OUT2 pull down current)	Current source used for the detection	-	200	-	400	µA
Ttimeout	Off-state diagnosis time-out (unstable diagnostics input during Tstable_off)	Starts at the end of Tdiag_del (guaranteed through scan)	7	8.4	10	ms
Vout_reg	OUT1 regulator output voltage during Offstae diagnostics	-	1.3	1.8	2.3	V
C_ESD	ESD capacitors connected to OUT1 and OUT2. (1)	-	10	-	47	nF

1. See also paragraph 3.13.1 of the application note AN4867 on *www.st.com* website.

4.9 SPI

A standard 16 bits Serial Peripheral Interface (SPI) is implemented to allow bi-directional communication between the L9960 and the MCU.

The SPI is used for configuration and diagnostic purposes as well as identifying the L9960 (ASSP name).

The SPI interface of L9960 is a slave SPI interface: the master is the µcontroller which provides NCS and SCLK to L9960. As far as MSB/LSB order is concerned, **MSB** is sent **first**.

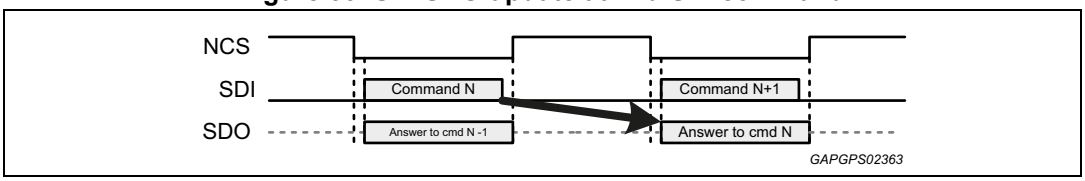
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4.9.1 Protocol description

Transfer format uses 16 bits word in case of single device configuration and multiple of 16 bits word in case of daisy chain configuration (number of devices in the daisy chain is not limited).

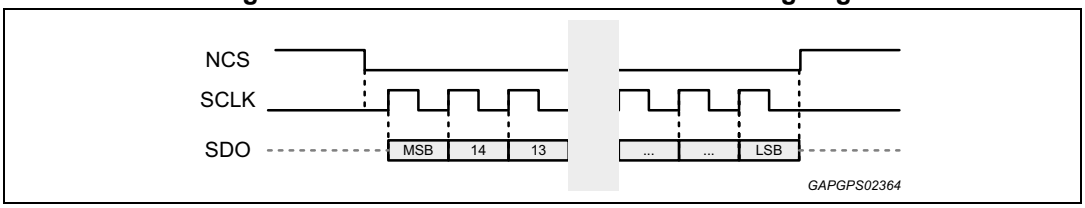
A command sent by the µcontroller during transfer N is answered during transfer N+1.

Figure 33. SPI SDO update at 2nd SPI command



SDO is clocked on SCLK rising edge.

Figure 34. SPI SDO is clocked on SCLK rising edge



SDI is sampled on falling edge.

When NCS = '1' and during Reset, any signals at the SCLK and SDI pins have to be ignored, and SDO remains in a high impedance state. Otherwise, the SPI interface is always active.

SCLK is guaranteed to be at '0' when NCS rises and falls (guaranteed by application).

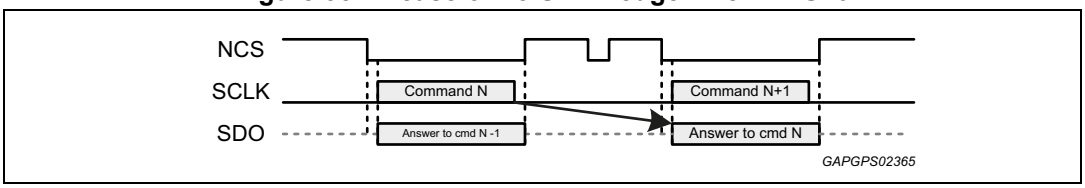
At each rising edge of the clock pulse after NCS goes low, the response word is serially shifted out on the SDO pin.

At each falling edge of the clock pulse (after NCS goes low) the new control word is serially shifted in on the SDI pin. The SPI command bits are decoded to determine the destination address for the data bits. After the 16th (or multiple of 16, for daisy chains) clock cycle, at the next NCS low to high transition, the SPI shift register data bits are transferred into the latch whose address was decoded from the SPI shift register command bits.

A command is executed after 16 SCLK cycles (or a multiple of 16) and NCS goes high.

In case of "no SCLK edge" when NCS = '0', the transfer is considered as valid: no error is returned to the µcontroller. The answer of last command is sent during next transfer.

Figure 35. In case of no SCLK edge when NCS=0



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4.9.2 SPI command and response words format

L9960 is controlled with a **16 bits** command word including:

- **4 Address bits**, **11 data bits** and 1 parity bit:

Table 87. SPI command word format

MSB															LSB
Address				D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	parity_bit
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The command is stored in a command register after the rising edge of NCS

The response consists of a 16 bits word which contains:

- 4 Address bits of the command word
- 12 bits as payload corresponding to the command word requested information like diagnostic, output state, etc.

Table 88. SPI response word format

MSB															LSB
Address				R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Response after reset

1st response after reset is 0000 0000 0000 0000.

Response after communication error

In case of communication error (**not used commands, wrong parity bit, number of clocks not multiples of 16**) the following response is sent: 0000 0000 0000 0000.

Command Chip Select (NCS) LOW without clock is ignored.

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Read ASIC name (ID), and ASIC silicon version

ASIC name (ID) can be read back after the following command word “Electronic ID request“:

Address				D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	parity_bit
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Following, the Response to Command word “Electronic ID request“:

Address				R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
1	1	1	1	0	0	0	0	1	1	1	0	1	1	0	0
				ASIC name [00 1110 0100]											

L9960 silicon version can be read back after the following command word “Silicon version request“:

Address				D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	parity_bit
1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0

Response to Command word “Silicon version request“:

Address				R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
1	1	1	1	x	x	x	x	x	x	0	0	0	0	0	0
				Supplier		Silicon version									

Table 89. Supplier ID code

-	R11	R10	Description
Supplier ID[1:0]	0	0	1st source
-	0	1	2nd source

Table 90. Silicon version identifier

Silicon version	R9	R8	R7	R6	Description
-	0	0	0	0	Silicon AA
-	0	0	0	1	Silicon AB
-	0	0	0	1	Silicon AC
-	…	…	…	…	…

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4.9.3 Read ASIC traceability number

ASIC traceability number can be read back after the following 2 command words “Component traceability number request“:

Address				D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	parity_bit
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1

Response to command words “Component traceability request” 1 & 2

Address				R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
1	1	0	1	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
1	1	0	1	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12

Table 91. Wafer coordinate

24-bit config[23:0]	Component traceability
I[11:6]	Wafer Y coordinate
I[5:0]	Wafer X coordinate

Figure 36. Wafer XY coordinate

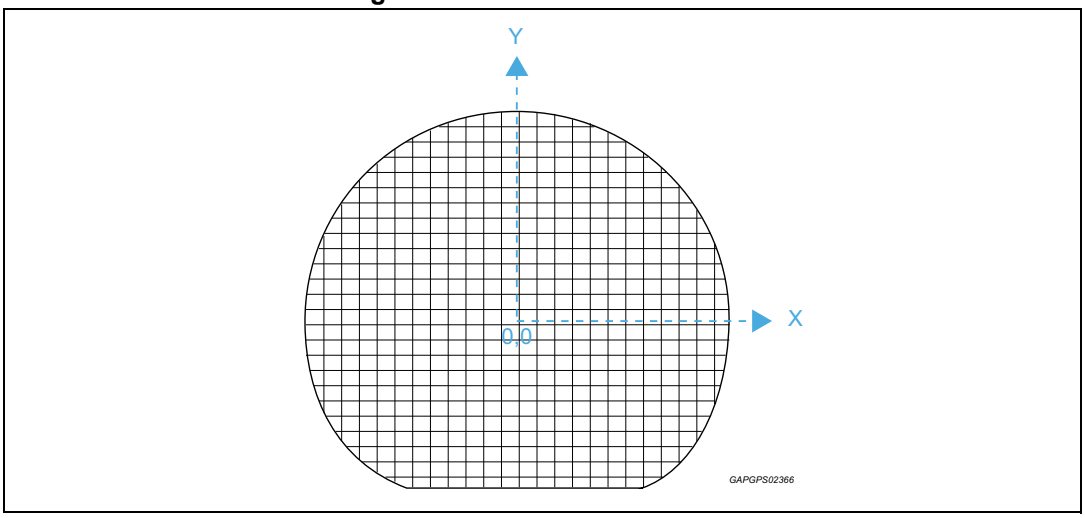


Table 92. Traceability code and wafer number

24-bit config[23:0]	Component traceability
I[16:12]	Wafer number

Die coordinate and wafer number bits are defined by specification.

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4.9.4 Read Logic HW version

Logic HW version can be read back after the following command word “Logic HW version request“:

Address				D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	parity_bit
1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0

Response to command word “Logic HW version request”

Address				R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
1	1	1	1					Code_version[7:0]							

4.9.5 Parity bit

The LSB (Least Significant Bit i.e. the last sent bit) of the word sent by the MCU to the L9960 is the parity bit.

ODD parity is being used.

No parity bit generation is used in response words for the slave device.

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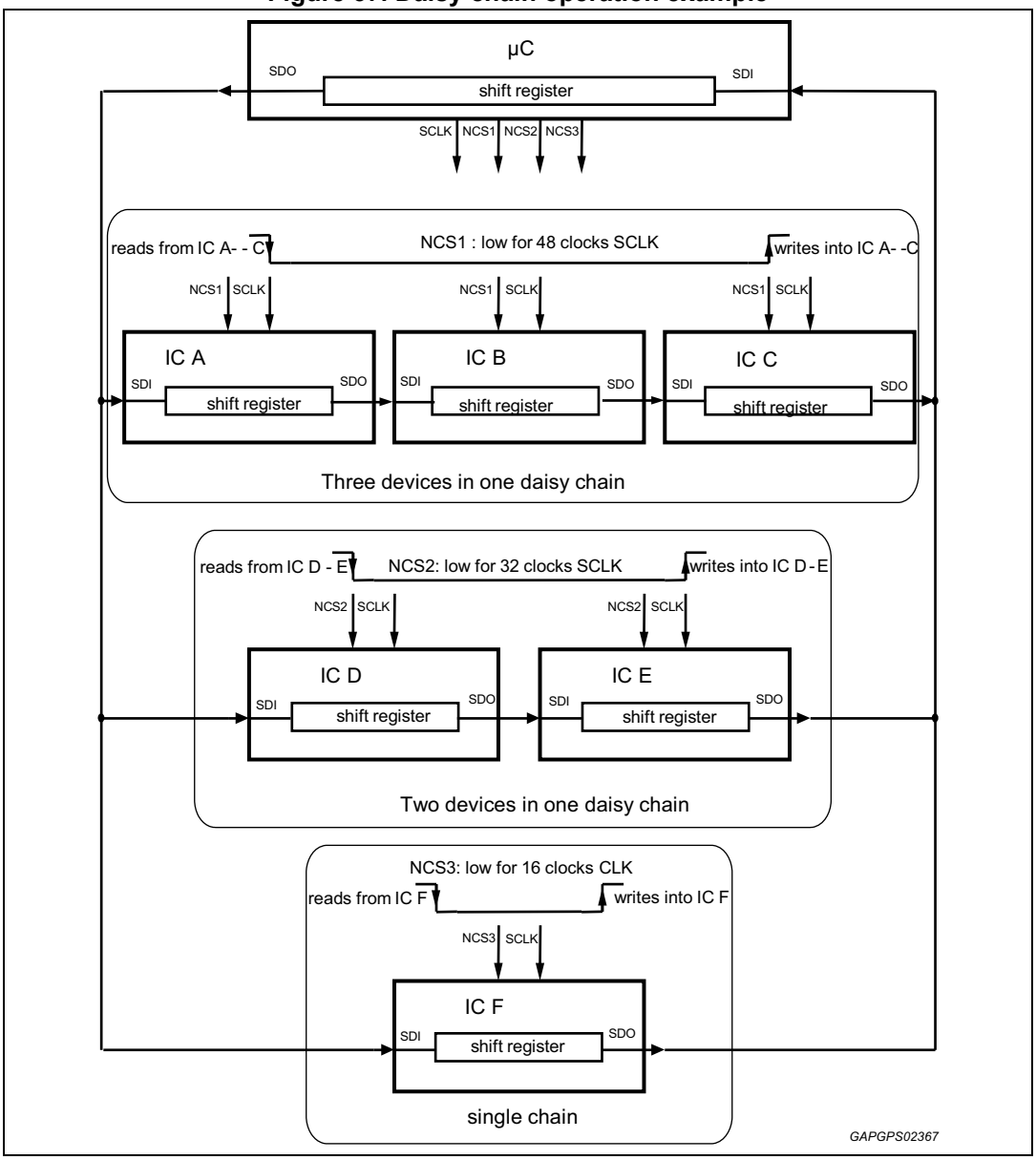
4.9.6 SPI communication mode (Parallel and Daisy chain mode)

The SPI communication between one master and multiple slaves can be operated in parallel or in daisy chain.

Parallel operation: several SPI-slaves can be connected to one SPI channel. The communication lines SDI, SDO and CLK are shared, and every slave has its own chip select line (NCS).

Daisy chain operation: several L9960 can be connected to one SPI connection in daisy chain operation to save µC interface pins. The number of devices connected in daisy chain is unlimited.

Figure 37. Daisy chain operation example



Software constraint: daisy chain is only possibly for ASICs using the same SPI protocol.

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4.9.7 Communication check

The purpose of this SPI communication self-check is to detect errors in the SPI communication from the µC.

In case of no communication or of communication failure into the defined time frame, the bridge is put into tri-state.

After the RESET state release, the communication check time-out timer **Tcc** is started by NDIS HIGH and DIS LOW from a pre-loaded value:

- If NDIS = '0' and DIS='1' when the RESET state is released, the pre-load is **Tcc**
- If NDIS='1' and DIS='0' when the RESET state is released, the pre-load is **Tcc*2** for the first communication, Tcc for the next communications.

In case the timer has expired (time-out), a status bit is registered **CC_latch**.

Table 93. CC_latch

Bit config	Description	Condition
0	Communication Check Fail	-
1	Communication Check Pass or Disable	Default value

Note: Available in D9 bit position in SPI answer frame 7e.

The communication check can be disabled by SPI via dedicated bit **Config_CC**.

Table 94. Config_CC

Bit config	Description	Condition
0	Disable communication check	-
1	enable communication check	Reset value

Note: (-) available in D7 bit position in SPI answer frame 2.

The status of config register is inverted in a status bit.

Table 95. Config_CC_state_echo7

Bit config	Description	Condition
0	echo communication check active	Default value
1	echo communication check inactive	-

Note: (-) available in the R10 bit position in SPI answer frame 7e.

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4.9.8 Electrical characteristics

The component guarantees the functionality of the SPI interface for a VDD5 voltage down to Vpor (Max frequency define in parameter f_{SCLK}).

4.5 < VDD5 < 5.5 V; 3.0 < VDDIO < 5.5 V unless otherwise noted.

Positive current is flowing into pin.

Table 96. Electrical characteristics serial data output

symbol	Parameters	Conditions	Min.	Max.	Value
V_{SDOH}	High output level (I_{SDO} = -2 mA)	Back to back structure used	VDDIO -0.4V	-	V
V_{SDOL}	Low output level (I_{SDO} = 3.2 mA)	-	-	0.4	V
I_{SDOL}	Tri state leakage current (NCS = HIGH)	VDDIO = 5 V VDDIO = 19 V For 0 < SDO < VDDIO (-40 °C ≤ T_j ≤ 25 °C)	-5	5	µA
		VDDIO = 5 V VDDIO = 19 V For 0 < SDO < VDDIO (25 °C > T_j ≤ 150 °C)	-5	10	µA
V_{OV_SDO}	Over voltage detection threshold at SDO output	Prevent output from damage; avoid back supply to VDDIO	VDDIO+0.05	VDDIO+0.2	V
t_{OFF_PROT}	Turn-off delay for over voltage reverse supply protection	direct control of back to back in HS path; VDDIO+1V; Measure at 0.5*Ipeak	0	1.5	µs
VSDO	Voltage range w/o damage	SDO driven High or Low No damage of the part in short-circuit condition	-0.3	19	V
Inputs NCS; SCLK; SDI					
V_{INL}	Low input level	-	-0.3	0.75	V
V_{INH}	High input level	-	1.75	VDD5+0.3	V
V_{hyst}	Hysteresis	-	0.1	1	V
I_{IN}	Input current for NCS; SCLK; SDI (Vin= VDD5)	-	-50	5	µA
$I_{IN,pu}$	Input pull up current source for NCS; SCLK; SDI (VDD5 ≥ VPOR) & (VIN < 2.5V)	Pull-up circuit protected against supply back feeding injection	-30	-100	µA

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Table 97. SPI electrical characteristics

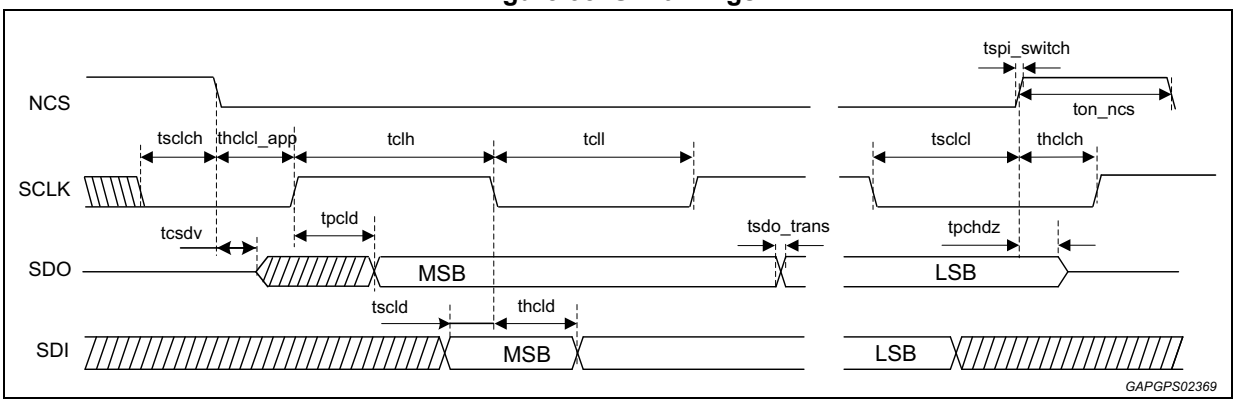
Symbol	Parameters	Conditions	Min.	Max.	Value
f_{SCLK}	Clock frequency (50% duty cycle)	SPI has to work for all frequencies	0	5	MHz
t_{sdo_trans}	SDO rise and fall time 20% to 80% VSDOH	guaranteed by design, 20pF…150pF load	5	35	ns
t_{clh}	Minimum time SCLK = HIGH	-	75	-	ns
t_{cll}	Minimum time SCLK = LOW	-	75	-	ns
t_{pcld}	Propagation delay – incl. rise/fall time (SCLK to data at SDO active)	150pF load	-	50	ns
t_{csdv}	NCS = LOW to output SDO active (SDO gets the same value as the last value from the previous communication)	150pF load	-	75	ns
t_{sclch}	SCLK low before NCS low (setup time SCLK to NCS change H/L)	-	75	-	ns
t_{hclcl_app}	SCLK change L/H after NCS = low	VHDL relevant(1)	950	-	ns
t_{scld}	SDI input setup time (SCLK change H/L after SDI data valid)	-	15	-	ns
t_{hcld}	SDI input hold time (SDI data hold after SCLK change H/L)	-	15	-	ns
t_{sclcl}	SCLK low before NCS high	-	100	-	ns
t^{hclch}	SCLK high after NCS high	-	100	-	ns
t_{pchdz}	NCS L/H to SDO @ high impedance	-	-	75	ns
t_{onNCS}	NCS min. high time	VHDL relevant (1)	950	-	ns
-	Capacitance at SDI; SDO; SCLK; NCS	-	-	10	pF
t_{fNCS}	NCS Filter time (Pulses ≤ tfNCS are ignored)	-	10	40	ns
t_{SPI_switch}	Minimum Input Rise and Fall time; 20-80% at SDI; SCLK; NCS	-	-	2	ns
t_{SPI_ovuv}	Minimum input over/undershoot	guaranteed by design	-200	200	mV
T_{cc}	Communication check timer	-	54	80	ms

1. Application relevant: VHDL design needs at least 4 clock cycles (e.g. System Clock 5MHz) to process assertion of NCS (low active Chip Select).

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The following timing diagram enumerates the timing parameters applicable to the SPI interface:

Figure 38. SPI timings



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The command and answer words of an SPI communication are described below:

Table 98. SPI communication command and answer words

Word ID	Address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Parity bit	ON state
#0[1]	0 0 0 0	-	-	-	-	-	-	-	-	-	-	-	-	Not used
#1 [2]	0 0 0 1	0	0	0	0	0	0	0	0	0	0	0	-	overcurrent monitoring
#2 [2]	0 0 1 0	SW reset[1:0] (00)		HWSC/LBIST Trigger (0)	Config CC (1)	0	0	0	0	0	0	0	-	restart trigger
#3	0 0 1 1	CL[1:0] (01)		NOSR (0)	ISR (1)	VSR (1)	TDIAG1[2:0] (111)			TSW_low_current (1)	$1^{(3)}$	DIAG_CLR_EN (1)	-	configuration 1
#4 [2]	0 1 0 0	in1_in2_if (0)	OTsd_thr_var (000)			OTwarn_thr_var (000)			UV_PROT_EN (0)	NSPREAD (0)	$0^{(4)}$	UV_WIN (0)	-	configuration 2
#5 [2]	0 1 0 1	VVL_MODE (0)	TVVL[3:0] (1111)				0	0	0	0	0	OTWARN_TSEC_EN (0)	-	configuration 3 (WL mode trigger)
#6 [5]	0 1 1 0	TDSR (0)	OL_ON (0)	X	X	X	X	X	X	X	X	X	-	configuration 4

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Table 98. SPI communication command and answer words (continued)

Word ID	Address				D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Parity bit	ON state
#7a	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	configuration request 1
#7b	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1	configuration request 2
#7c	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	1	configuration request 3
#7d	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1	configuration request 4
#7e	0	1	1	1	0	0	0	0	0	0	1	0	0	0	0	1	configuration request 5
#8a	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	states request 1
#8b	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	states request 2
#8c	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	states request 3
#9	1	0	0	1	0	0	0	0	0	0	0	0	0	0	TRIG (0)		OFF STATE diagnosis
#10a(6)	1	0	1	0	Reserved												Reserved
#10b(6)	1	0	1	0	Reserved												Reserved
#11(6)	1	0	1	1	Reserved												Reserved
#12a	1	1	0	0	All '0's (D10:D0), parity bit (1)												Reserved
#12b	1	1	0	0	'00000000001' + parity bit at 0												Reserved
#13a	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	component traceability number request 1
#13b	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	component traceability number request 2
#14	1	1	1	0	Reserved												Reserved
#15a	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	electronic id request
#15b	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	silicon version request
#15c	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	Logic HW version request

1. Command frame '0' is not used.
2. In command frames 1, 2, 4 and 5 the bitfileds set to '0' must be respected otherwise internal logic will discard the command. These bits are consequently used as internal cross-check by logic on valid address for correct frame processing
3. D[1] BITFIELD IN SPI COMMAND #3 must be kept at 1.
4. D[1] bitfield in SPI command #4 must be kept at 0.
5. After POR or SW reset, D[8]..D[0] bitfield is set at ' 0_0111_1101 '. This POR value is not processed by the logic as whatever further configuration. This bitfield status is mirrored in bitfield R[9]..R[1] in answer frame #7d.
6. Frame 10a, 10b and 11 are reserved SPI command frames for ATE. If sent by, the SDO response will be the error frame 0x0000h.

Table 99. SPI communication configuration

Word ID	Address				R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	Description
answer to error	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Error because not use
answer to #1	0	0	0	1	0	OCH1[1:0]		0	OCH0[1:0]		0	OCL1[1:0]		0	OCL0[1:0]		overcurrent monitoring
answer to #2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Nothing report
answer to #3	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Nothing report
answer to #4	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Nothing report
answer to #5	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Nothing report
answer to #6	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Nothing report
answer to #7a	0	1	1	1	CL_echo[1:0]		NOSR_echo	ISR_echo	VSR_echo	TDIAG1_echo[2:0]			TSW_low_current_echo	1	DIAG_CLR_EN	0	Configuration request 1
answer to #7b	0	1	1	1	in1_in2_if_echo		OT_sd_thr_var_echo			OTwarn_thr_var_echo			UV_PROT_EN_echo	NSPREAD_echo	0	UV_WIN_echo	Configuration request 2
answer to #7c	0	1	1	1	WLMODE_echo		TVVL_echo[3:0]			0	0	0	0	0	0	OTWARN_TSEC_EN_echo	Configuration request 3

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Table 99. SPI communication configuration (continued)

Word ID	Address				R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	Description
answer to #7d (1)	0	1	1	1	TDSR_echo	0	X									0	Configuration request 4
answer to #7e	0	1	1	1	POR status	config_CC_status_echo	CC latch_state	0	0	0	0	0	0	0	0	0	Configuration request5
answer to #8a	1	0	0	0	NDIS_status	DIS_status	BRIDGE_EN	HWSC/LBIST_status			VPS_UV_REG	NGFAIL	ILIM_REG	VDD_OV_REG	VDD_UV_REG	VPS_UV	states request 1
answer to #8b	1	0	0	0	OTSDcnt[5:0]						OTWARN	OTWARN_REG	NOTSD	NOTSD_REG	OL_ON_STATUS [1:0]		states request2
answer to #8c	1	0	0	0	0	0	0	0	0	0	UV_CNT_REACHED	Error_count[3:0]				0	states request3

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Table 99. SPI communication configuration (continued)

Word ID	Address				R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	Description
answer to #9	1	0	0	1	0	0	0	0	0	0	0	0	0	DIAG_OFF[2:0]			OFF STATE diagnosis
answer to #10a	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Nothing report
answer to #10b	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Nothing report
answer to #11	1	0	1	1	Reserved												Reserved for supplier test mode
answer to #12a	1	1	0	0	VDD_OV_L[2:0]		Reserved										-
answer to #12b	1	1	0	0	Reserved								-	-	VDD_OV	VDD_UV	-
answer to #13a	1	1	0	1	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	component traceability number request 1
answer to #13B	1	1	0	1	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	component traceability number request 2
answer to #14	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Nothing report
answer to #15a	1	1	1	1	ASIC name [9:0]										0	ASSP	electronic id request
answer to #15b	1	1	1	1	0	0	Silicon version(3:0]				0	0	0	0	0	0	silicon version request
answerto#15c	1	1	1	1	0	0	0	0	code_version[7:0]								Logic HW version request

1. Bitfield R9..R1 is the mirror of the bitfield D8..D0 in command frame 6

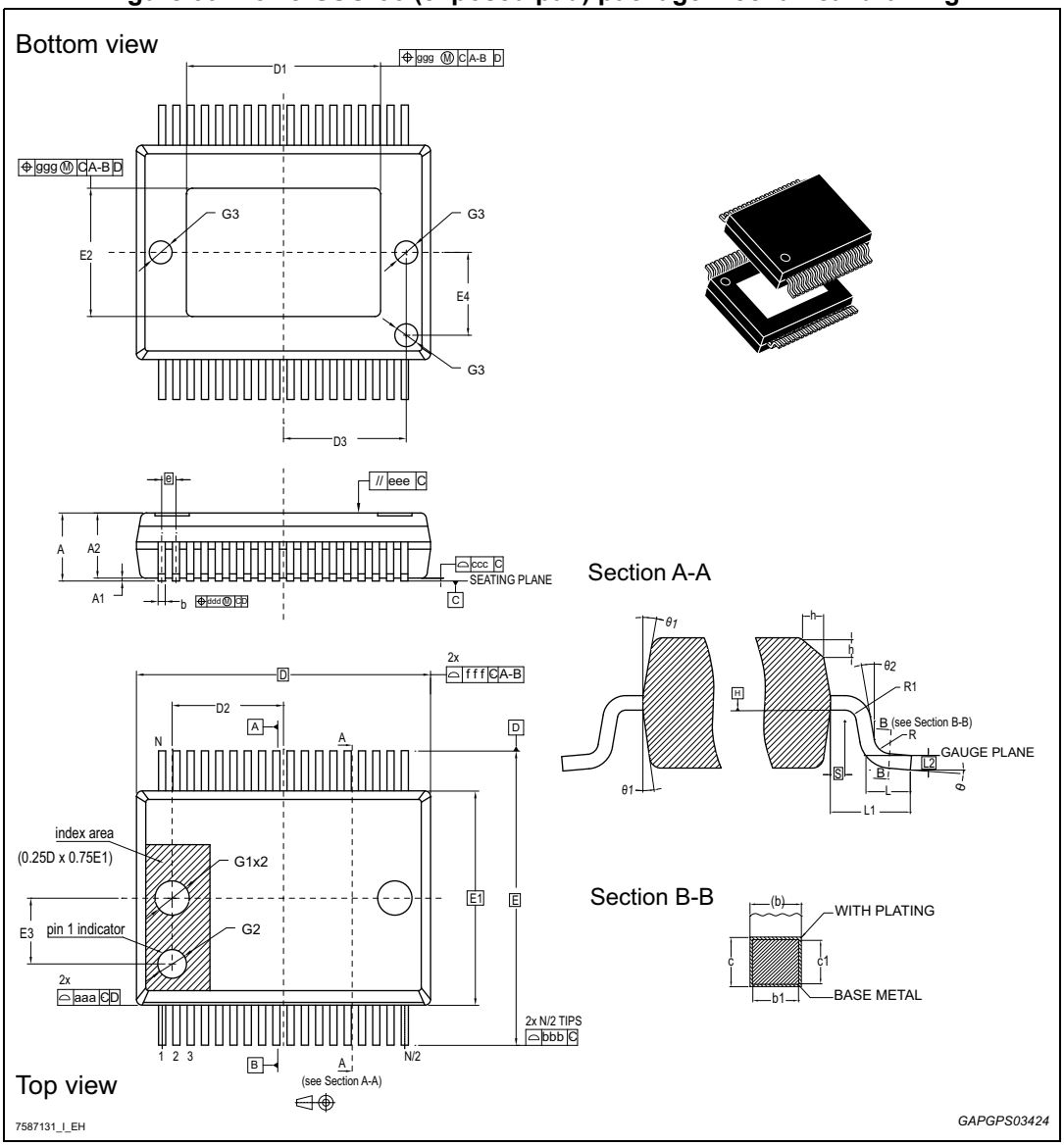
5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK is an ST trademark.

5.1 PowerSSO-36 (exposed pad) package mechanical data

Figure 39. PowerSSO-36 (exposed pad) package mechanical drawing



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Table 100. PowerSSO-36 (exposed pad) package mechanical data

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	-	8°	0°	-	8°
Θ1	5°	-	10°	5°	-	10°
Θ2	0°	-	-	0°	-	-
A	2.15	-	2.45	0.0846		0.0965
A1	0.0	-	0.1	0.0		0.0039
A2	2.15	-	2.35	0.0846		0.0925
b	0.18	-	0.32	0.0071		0.0126
b1	0.13	0.25	0.3	0.0051	0.0098	0.0118
c	0.23	-	0.32	0.0091		0.0126
c1	0.2	0.2	0.3	0.0079	0.0079	0.0118
D(1)	10.30 BSC			0.4055 BSC		
D1	6.9	-	7.5	0.2717	-	0.2953
D2	-	3.65	-	-	0.1437	-
D3	-	4.3	-	-	0.1693	-
e	0.50 BSC			0.0197 BSC		
E	10.30 BSC			0.4055 BSC		
E1(1)	7.50 BSC			0.2953 BSC		
E2	4.3	-	5.2	0.1693	-	0.2047
E3	-	2.3	-	-	0.0906	-
E4	-	2.9	-	-	0.1142	-
G1	-	1.2	-	-	0.0472	-
G2	-	1	-	-	0.0394	-
G3	-	0.8	-	-	0.0315	-
h	0.3	-	0.4	0.0118	-	0.0157
L	0.55	0.7	0.85	0.0217	-	0.0335
L1	1.40 REF			0.0551 REF		
L2	0.25 BSC			0.0098 BSC		
N	36			1.4173		
R	0.3	-	-	0.0118	-	-
R1	0.2	-	-	0.0079	-	-
S	0.25	-	-	0.0098	-	-
Tolerance of form and position						
aaa	0.2			0.0079		

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Table 100. PowerSSO-36 (exposed pad) package mechanical data (continued)

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
bbb		0.2			0.0079	
ccc		0.1			0.0039	
ddd		0.2			0.0079	
eee		0.1			0.0039	
ffff		0.2			0.0079	
ggg		0.15			0.0059	

1. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is ‘0.25 mm’ per side D and ‘0.15 mm’ per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.

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6 Reference document

Application Note AN4867 “*L9960 ETC H-bridge*”, *www.st.com* website.

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7 Revision history

Table 101. Document revision history

Date	Revision	Changes
22-Jun-2015	1	Initial release.
25-Jun-2015	2	Updated CDM results in *Section Table 4.*.
14-Sep-2015	3	Document status promoted from target specification to production. Updated: – *Description on page 1*; – *Table 8: Timing characteristics* (LS rise/fall time); – *Table 11: VPS electrical characteristics* (Inserted limits for Vs_clamp_neg); – *Table 63: Electrical characteristics* (Updated limit for Itrack HS range 2 and range 3, and update limits for CL hysteresis , range 0 and range 3); – *Table 71: Over-current detection electrical characteristics*. (corrected typo: thresholds range swap for OC range 3 for LS/HS); – *Table 4: Absolute maximum ratings* (added note for ESD table concerning HBM for OUTx and VPS). – *Table 98: SPI communication command and answer words* (added note for SPI command frame #3, #4 and #6).
07-Oct-2015	4	*Table 71: Over-current detection electrical characteristics* corrected USL for I_{track}. *Table 98: SPI communication command and answer words* updated Word ID “#6” from 0 to X; updated note “5”. *Table 99: SPI communication configuration* updated Word ID answer to #7d# (R9-R1 from 0 to X; updated note “1”.
02-Sep-2016	5	Modified title in cover page and added “AEC-Q100 qualified” as first feature. Updated: – *Table 6: Range of functionality*: added note for Tj; – *Table 8: Timing characteristics* for timings Td-On and Td_off; – *Figure 11: POR timing diagram*; – *Table 32: HWSC/LBIST electrical characteristics*: LBIST duration and LBIST coverage; – *Section 4.6.2: Current slew rate*, – *Section 4.6.3: Voltage slew rate*: removed wrong note for OL diagnostics in On-state not available during NOSR mode; – *Section 4.6.4: Current limitation*: updated general description on current limitation fucntionality, and corrected figure *20*, *21* and *22* for Tdiag2 and ILIM_REG references. Updated description and references for table *48* , *49* and *50*; – *Table 8: Timing characteristics*; – *Table 63: Electrical characteristics*; – *Section 4.8.4: Diagnostic of "Over-current" in on-state* corrected typo in ISR limits; – *Section 4.8.5: Diagnostic of "Open Load" in on-state* description and corrected label for figure *28*; – *Section 4.8.7: Off-state diagnostic*. Added *Section 6: Reference document*.

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Table 101. Document revision history (continued)

Date	Revision	Changes
22-Jun-2017	6	Updated: – The values of 'T_{TSD}' parameter in *Table 70*; – The values of 'OUT1_OL_Thr' parameter in *Table 86*; – *Table 100: PowerSSO-36 (exposed pad) package mechanical data*.
21-Dec-2017	7	Updated: – *Battery voltage monitoring on page 19*; – *Section 4.8.6: On-state diagnostics electrical characteristics on page 70*.
21-Jun-2018	8	Updated: – *Figure 2.2: Bill of materials on page 13*; – *Table 8: Timing characteristics on page 17* with condition TSW_low_current = 0; – *Section 4.7.1*: corrected description for **OTSDcnt** reset; – *Section 4.8.3*: corrected statement for **NGFAIL** bit deassertion; – Added range for C_ESD capacitors (as application info only) on OUT1 and OUT2 in *Table 86*.
04-Oct-2019	9	Updated: – *Table 2: Pin definition (PSSO36twin die) and function*; – *Table 96: Electrical characteristics serial data output*. Minor text changes.
02-Feb-2021	10	Updated: – Title; – *Figure 1: Block diagram for L9960*; – *Section 2: Application description*. Added: – *Section 2.1: Application circuit*; – *Section 2.2: Bill of materials*. Minor text changes in: – Description; – *Section 4.9.4: Read Logic HW version*; – *Table 97: SPI electrical characteristics*; – *Table 98: SPI communication command and answer words*.

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