

SELECTION GUIDE

| Part Number | Packing | Package | Operating Ambient Temperature, T_A (°C) |
|--------------|----------------------|---|---|
| A4931METTR-T | 1500 pieces per reel | 5 mm × 5 mm, 0.90 mm nominal height QFN | -20 to 105 |
| A4931GETTR-T | 1500 pieces per reel | 5 mm × 5 mm, 0.90 mm nominal height QFN | -40 to 105 |



ABSOLUTE MAXIMUM RATINGS

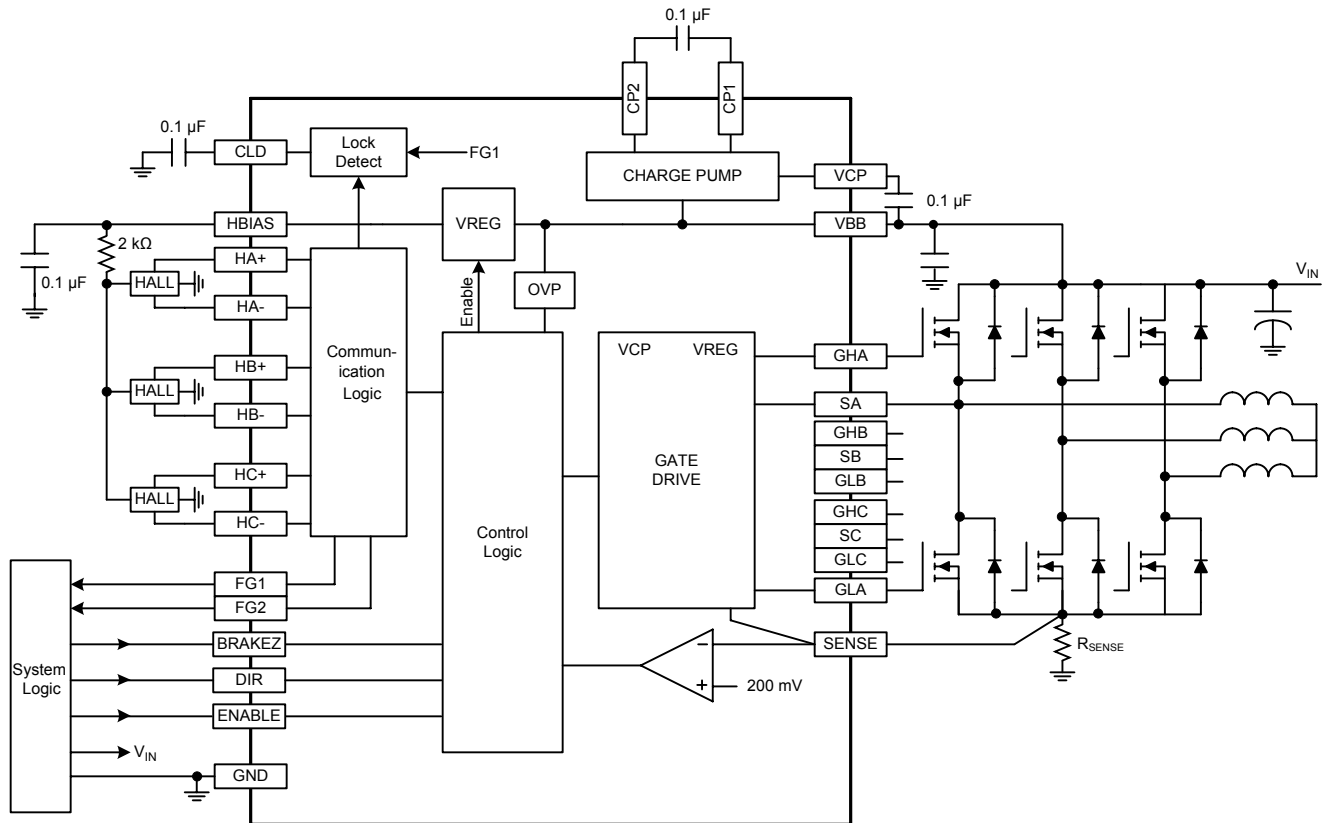
| Characteristic | Symbol | Notes | Rating | Units |
|-------------------------------|-------------------|----------------|------------|-------|
| Load Supply Voltage | V_{BB} | | 38 | V |
| Motor Phase Output | S_X | $t_w < 500$ ns | -3 | V |
| Hall Input | V_{HX} | DC | -0.3 to 7 | V |
| Logic Input Voltage Range | V_{IN} | | -0.3 to 7 | V |
| Logic Output Voltage Range | V_{FG} | FG1, FG2 pins | -0.3 to 7 | V |
| Operating Ambient Temperature | T_A | Range M | -20 to 105 | °C |
| | | Range G | -40 to 105 | °C |
| Maximum Junction Temperature | $T_J(\text{max})$ | | 150 | °C |
| Storage Temperature | T_{stg} | | -40 to 150 | °C |

THERMAL CHARACTERISTICS

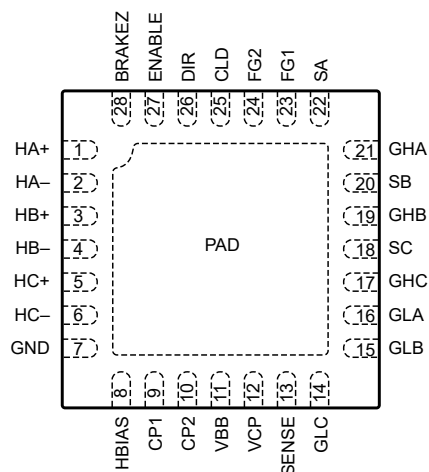
| Characteristic | Symbol | Test Conditions* | Rating | Units |
|---|-----------------|-------------------------------------|--------|-------|
| Package Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 4-layer PCB based on JEDEC standard | 32 | °C/W |
| Package Thermal Resistance, Junction to Exposed Pad | $R_{\theta JP}$ | | 2 | °C/W |

*For additional information, refer to the Allegro website.

FUNCTIONAL BLOCK DIAGRAM



PINOUT DIAGRAM AND TERMINAL LIST



ET Package Pinout Diagram

Terminal List

| Number | Name | Description |
|--------|-------|--------------------------------|
| 1 | HA+ | Hall input A |
| 2 | HA - | Hall input A |
| 3 | HB+ | Hall input B |
| 4 | HB - | Hall input B |
| 5 | HC+ | Hall input C |
| 6 | HC- | Hall input C |
| 7 | GND | Ground |
| 8 | HBIAS | Hall bias power supply output |
| 9 | CP1 | Charge pump capacitor terminal |
| 10 | CP2 | Charge pump capacitor terminal |
| 11 | VBB | Supply voltage |
| 12 | VCP | Reservoir capacitor terminal |
| 13 | SENSE | Sense resistor connection |
| 14 | GLC | Low side gate drive C |

| Number | Name | Description |
|--------|--------|--|
| 15 | GLB | Low side gate drive B |
| 16 | GLA | Low side gate drive A |
| 17 | GHC | High side gate drive C |
| 18 | SC | High side source connection C |
| 19 | GHB | High side gate drive B |
| 20 | SB | High side source connection B |
| 21 | GHA | High side gate drive A |
| 22 | SA | High side source connection A |
| 23 | FG1 | FG 1 speed control output (3 Φ inputs) |
| 24 | FG2 | FG 2 speed control output (ΦA input) |
| 25 | CLD | Locked rotor detect timing capacitor |
| 26 | DIR | Logic input – motor direction |
| 27 | ENABLE | Logic input – external PWM control |
| 28 | BRAKEZ | Logic input – motor brake (active low) |

ELECTRICAL CHARACTERISTICS*: Valid at $T_A = 25^\circ\text{C}$, $V_{BB} = 24\text{ V}$, unless noted otherwise

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|-------------------------------------|----------------|---|------|-------|------------|------------------|
| Supply Voltage Range | V_{BB} | Operating | 8 | – | V_{BBOV} | V |
| Motor Supply Current | I_{BB} | $f_{PWM} < 30\text{ kHz}$, $C_{LOAD} = 1000\text{ pF}$ | – | 5 | 6 | mA |
| | | Charge pump on, outputs disabled, Standby mode | – | 3 | 3.5 | mA |
| HBIAS Voltage | V_{HBIAS} | $0\text{ mA} \leq I_{HBIAS} \leq 24\text{ mA}$ | 7.2 | 7.5 | 7.8 | V |
| HBIAS Current Limit | $I_{HBIASlim}$ | | 30 | – | – | mA |
| CONTROL LOGIC | | | | | | |
| Logic Input Voltage | $V_{IN(1)}$ | | 2 | – | – | V |
| | $V_{IN(0)}$ | | – | – | 0.8 | V |
| Logic Input Current | $I_{IN(1)}$ | $V_{IN} = 2\text{ V}$ | –1 | <1.0 | 1 | μA |
| | $I_{IN(0)}$ | $V_{IN} = 0.8\text{ V}$ | –1 | <–1.0 | 1 | μA |
| Input Pin Glitch Reject | t_{GLITCH} | ENB pin | 350 | 500 | 650 | ns |
| | | DIR, BRAKEZ pins | 700 | 1000 | 1300 | ns |
| ENB Standby Pulse Propagation Delay | t_{dENB} | To outputs off | 2.1 | 3 | 3.9 | ms |
| HBIAS Wake-Up Delay, Standby Mode | t_{dHBIAS} | $C_{HBIAS} = 0.1\text{ }\mu\text{F}$ | – | 15 | 25 | μs |
| GATE DRIVE | | | | | | |
| High-Side Gate Drive Output | $V_{GS(H)}$ | Relative to V_{BB} , $I_{GATE} = 2\text{ mA}$ | 7 | – | – | V |
| Low-Side Gate Drive Output | $V_{GS(L)}$ | $I_{GATE} = 2\text{ mA}$ | 7 | – | – | V |
| Gate Drive Current (Sourcing) | I_{Gate} | $V_{GH} = V_{GL} = 4\text{ V}$ | 20 | 30 | – | mA |
| Gate Drive Pull Down Resistance | R_{Gate} | | 10 | 28 | 40 | Ω |
| Dead Time | t_{dead} | | 700 | 1000 | 1300 | ns |
| Current Limit Input Threshold | V_{REF} | | 180 | 200 | 220 | mV |
| Fixed Off-Time | t_{OFF} | | 18 | 25 | 37 | μs |
| PROTECTION | | | | | | |
| Thermal Shutdown Temperature | T_{JTSD} | | 155 | 170 | 185 | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis | $T_{JTSDhys}$ | | 14 | 15 | 26 | $^\circ\text{C}$ |
| VBB UVLO Enable Threshold | V_{BBUV} | Rising V_{BB} | 6.2 | 7 | 7.85 | V |
| VBB UVLO Hysteresis | $V_{BBUVhys}$ | | 0.4 | 0.75 | 1 | V |
| VCP UVLO | V_{CPIV} | Relative to V_{BB} | 4.6 | – | 6 | V |
| Lock Detect Duration | t_{lock} | $C = 0.1\text{ }\mu\text{F}$ | 1.5 | 2 | 2.5 | s |
| VBB Overvoltage Threshold | V_{BBOV} | Rising V_{BB} | 30 | 33 | 37.5 | V |

Continued on the next page...

ELECTRICAL CHARACTERISTICS* (continued): Valid at $T_A = 25^\circ\text{C}$, $V_{BB} = 24\text{ V}$, unless noted otherwise

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|------------------------------|----------------------|--|------|----------|------|--------------------------|
| HALL LOGIC | | | | | | |
| Hall Input Current | I_{HALL} | $V_{\text{IN}} = 0.2\text{ to }3.5\text{ V}$ | -1 | 0 | 1 | μA |
| Common Mode Input Range | V_{CMR} | | 0.2 | - | 3.5 | V |
| AC Input Voltage Range | V_{HALL} | | 60 | - | - | $\text{mV}_{\text{p-p}}$ |
| Hall Thresholds | V_{th} | Difference between Hall inputs at transitions | - | ± 10 | - | mV |
| Hall Threshold Hysteresis | V_{HYS} | $T_J = 25^\circ\text{C}$ | 10 | 20 | 30 | mV |
| | | $T_J = -20^\circ\text{C to }125^\circ\text{C}$ | 5 | 20 | 40 | mV |
| Pulse Reject Filter | t_{pulse} | | - | 2 | - | μs |
| FG | | | | | | |
| FG Output Saturation Voltage | $V_{\text{FG(sat)}}$ | $I_{\text{FG}} = 2\text{ mA}$ | - | - | 0.5 | V |
| FG Leakage Current | I_{FGlkg} | $V_{\text{FG}} = 5\text{ V}$ | - | - | 1 | μA |

*Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

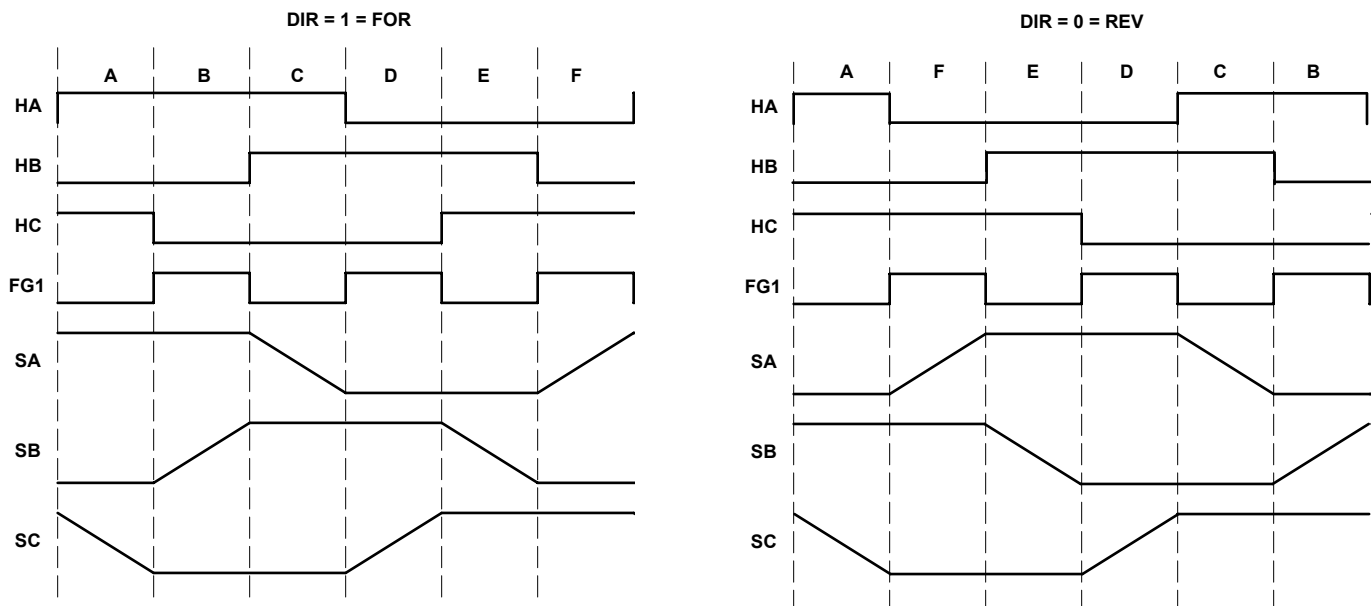
For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

Specifications throughout the allowed operating temperature range are guaranteed by design and characterization.

Logic States Table (See timing charts, below) X = Don't Care, Z = high impedance

| Condition | | Inputs | | | | | Resulting Pre-Driver Outputs | | | | | | Motor Output | | |
|----------------------|---|--------|----|----|--------|-----|------------------------------|-----|-----|-----|-----|-----|--------------|----|----|
| | | HA | HB | HC | BRAKEZ | ENB | GHA | GLA | GHB | GLB | GHC | GLC | A | B | C |
| DIR = 1 (Forward) | A | + | - | + | HI | LO | HI | LO | LO | HI | LO | LO | HI | LO | Z |
| | B | + | - | - | HI | LO | HI | LO | LO | LO | LO | HI | HI | Z | LO |
| | C | + | + | - | HI | LO | LO | LO | HI | LO | LO | HI | Z | HI | LO |
| | D | - | + | - | HI | LO | LO | HI | HI | LO | LO | LO | LO | HI | Z |
| | E | - | + | + | HI | LO | LO | HI | LO | LO | HI | LO | LO | Z | HI |
| | F | - | - | + | HI | LO | LO | LO | LO | HI | HI | LO | Z | LO | HI |
| DIR = 0 (Reverse) | A | + | - | + | HI | LO | LO | HI | HI | LO | LO | LO | LO | HI | Z |
| | F | - | - | + | HI | LO | LO | LO | HI | LO | LO | HI | Z | HI | LO |
| | E | - | + | + | HI | LO | HI | LO | LO | LO | LO | HI | HI | Z | LO |
| | D | - | + | - | HI | LO | HI | LO | LO | HI | LO | LO | HI | LO | Z |
| | C | + | + | - | HI | LO | LO | LO | LO | HI | HI | LO | Z | LO | HI |
| | B | + | - | - | HI | LO | LO | HI | LO | LO | HI | LO | LO | Z | HI |
| Fault* | | + | + | + | HI | X | LO | LO | LO | LO | LO | LO | Z | Z | Z |
| Fault* | | - | - | - | HI | X | LO | LO | LO | LO | LO | LO | Z | Z | Z |
| Brake* | | X | X | X | LO | X | LO | HI | LO | HI | LO | HI | LO | LO | LO |

* DIR = Don't Care



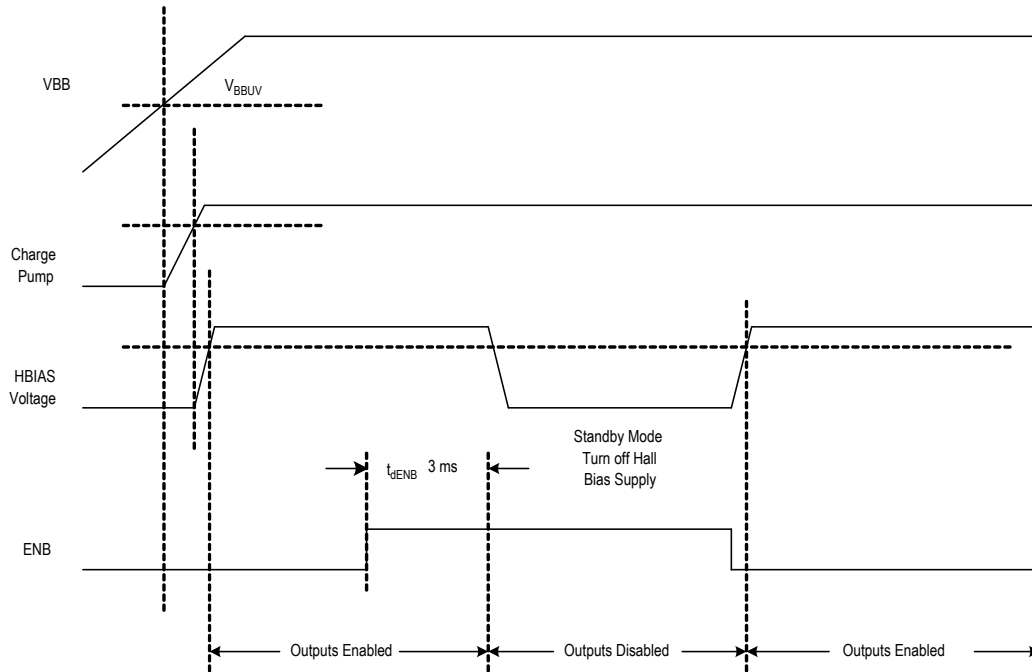


Figure 1: Power-Up and Standby Modes Timing Diagram

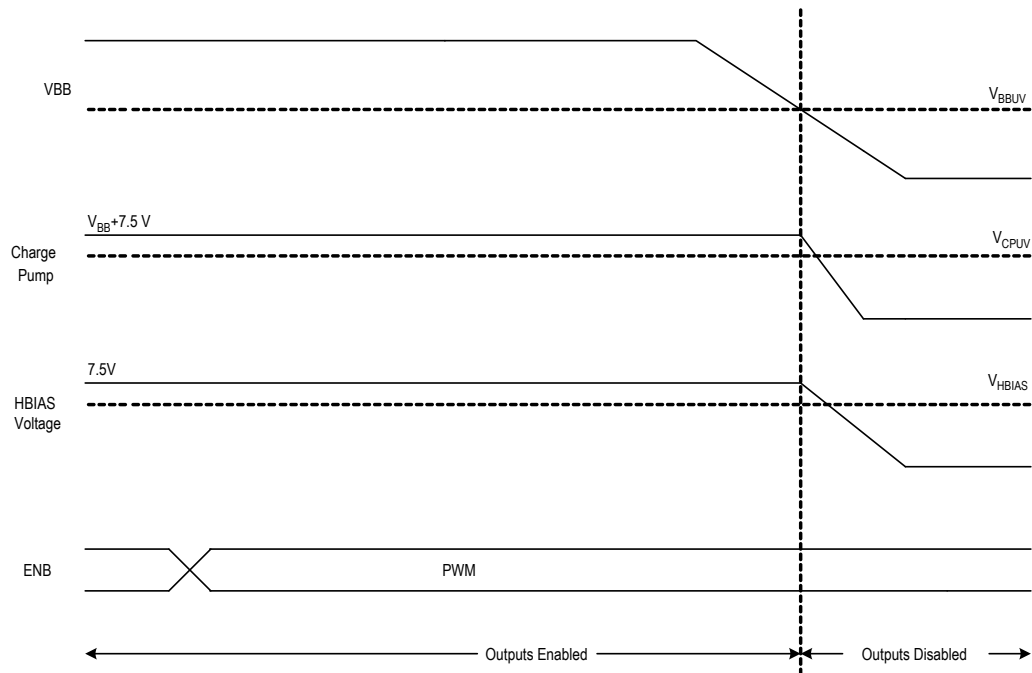


Figure 2: Power-Down Timing Diagram

FUNCTIONAL DESCRIPTION

Current Regulation

Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the full bridge are turned on, current increases in the motor winding until it reaches a value, I_{TRIP} , given by:

$$I_{TRIP} = 200 \text{ mV} / R_{SENSE}$$

When I_{TRIP} is reached, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for the fixed off-time period.

Enable Logic

The Enable input terminal (ENB pin) allows external PWM. ENB low turns on the selected sink-source pair. ENB high switches off the appropriate drivers and the load current decays. If ENB is held low, the current will rise until it reaches the level set by the internal current control circuit. Typically PWM frequency is in 20 to 30 kHz range. If the ENB high pulse width exceeds 3 ms, the gate outputs are disabled. The Enable logic is summarized in the following table:

| ENB Pin Setting | Outputs | Outputs State |
|----------------------|----------------|---|
| 0 | On | Drive |
| 1 | Source Chopped | Slow Decay with Synchronous Rectification |
| 1 for > 3 ms typical | Off | Disable |

Fixed Off-Time

The A4931 fixed off-time is set to 25 μs nominal.

PWM Blank Timer

When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes as well as switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source Enable latch, the sense comparator is blanked. The blanking timer runs after the off-time counter completes, in order to provide the blanking function. The blanking timer is reset when ENB is chopped or DIR is changed. With external PWM control, a DIR change or an ENB on triggers the blanking function. The duration is fixed at 1.5 μs .

Synchronous Rectification

When a PWM-off cycle is triggered, either by a chop command on ENB or by an internal fixed off-time cycle, load current recirculates. The A4931 synchronous rectification feature turns on the appropriate MOSFETs during the current decay, and effectively shorts out the body diodes with the low $R_{DS(on)}$ driver. This lowers power dissipation significantly and can eliminate the need for external Schottky diodes.

Brake Mode

A logic low on the BRAKEZ pin activates Brake mode. A logic high allows normal operation. Braking turns on all three sink drivers, effectively shorting out the motor-generated BEMF. The BRAKEZ input overrides the ENB input and also the Lock Detect function.

It is important to note that the internal PWM current control circuit does not limit the current when braking, because the current does not flow through the sense resistor. The maximum current can be approximated by V_{BEMF} / R_{LOAD} . Care should be taken to insure that the maximum ratings of the A4931 are not exceeded in the worse case braking situation, high speed and high inertial load.

HBIAS Function

This function provides a power supply of 7.5 V, current-limited to 30 mA. This reference voltage is used to power the logic sections of the IC and also to power the external Hall elements.

Standby Mode

To prevent excessive power dissipation due to the current draw of the external Hall elements, Standby mode turns off the HBIAS output voltage. Standby mode is triggered by holding ENB high for longer than 3 ms. Note that Brake mode overrides Standby mode, so hold the BRAKEZ pin high in order to enter Standby mode.

Charge Pump

The internal charge pump is used to generate a supply above V_{BB} to drive the high-side MOSFETs. The voltage on the VCP pin is internally monitored, and in case of a fault condition, the outputs of the device are disabled.

Fault Shutdown

In the event of a fault due to excessive junction temperature or due to low voltage on VCP or VBB, the outputs of the device are disabled until the fault condition is removed. At power-up, the UVLO circuit disables the drivers.

Overvoltage Protection

VBB is monitored to determine if a hazardous voltage is present due to the motor generator pumping up the supply bus. When the voltage exceeds V_{BBOV} , the synchronous rectification feature is disabled.

Overtemperature Protection

If die temperature exceeds approximately 170°C, the Thermal Shutdown function will disable the outputs until the internal temperature falls below the 15°C hysteresis.

Hall State Reporting

The FG1 pin is an open-drain output that changes state at each transition of an external Hall element. The FG2 pin is an open-drain output that changes state at each HAX transition.

Lock Detect Function

The IC will evaluate a locked rotor condition under either of these two different conditions:

- The FG1 signal is not consistently changing.
- The proper commutation sequence is not being followed. The motor can be locked in a condition in which it toggles between two specific Hall device states.

Both of these fault conditions are allowed to persist for period of time, t_{lock} . t_{lock} is set by capacitor connected to CLD pin. C_{LD} produces a triangle waveform (1.67 V peak-to-peak) with frequency linearly related to the capacitor value. t_{lock} is defined as 127 cycles of this triangle waveform, or:

$$t_{lock} = C_{LD} \times 20 \text{ s}/\mu\text{F}$$

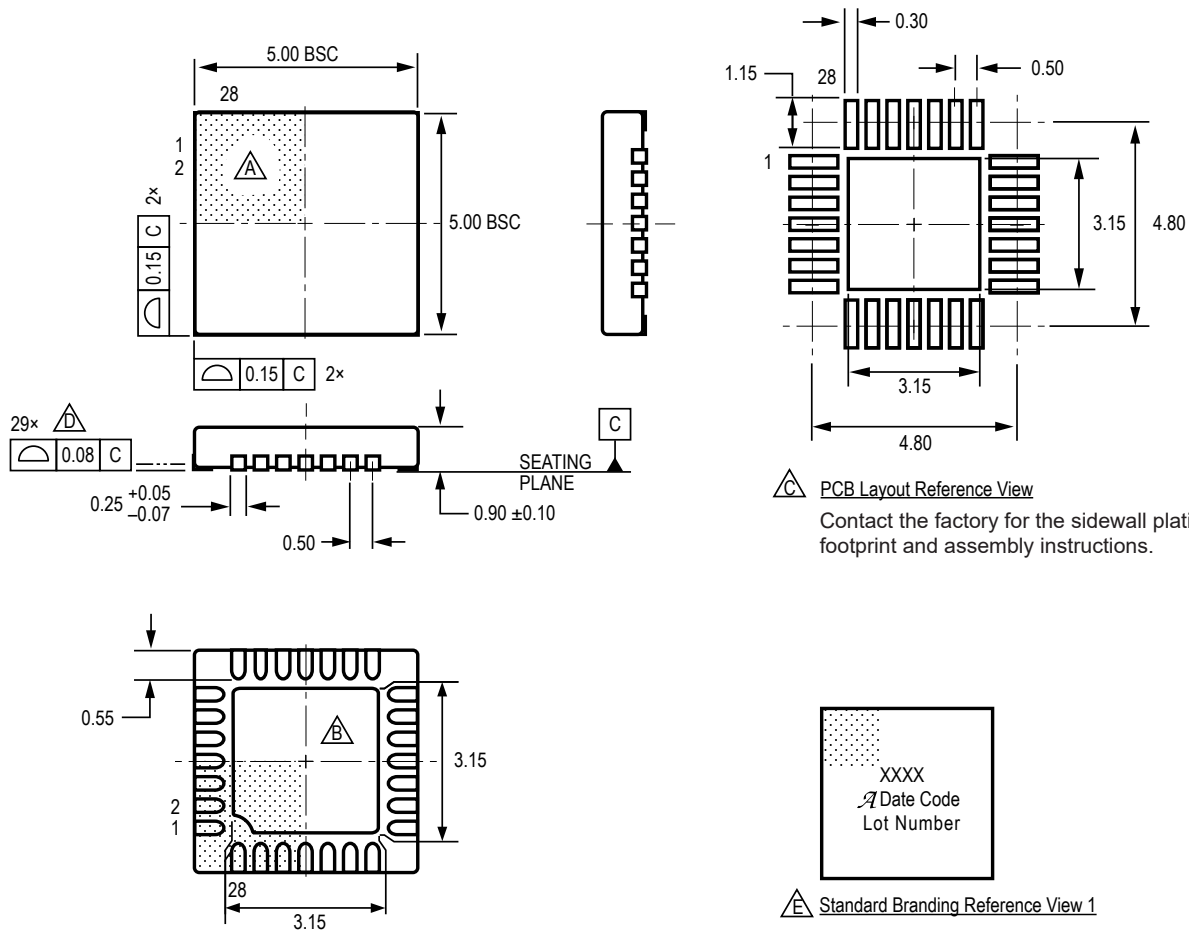
After the wait time, t_{lock} , has expired, the outputs are disabled, and the fault is latched. These fault conditions can only be cleared by any one of the following actions:

- Rising or falling edge on the DIR pin
- VBB UVLO threshold exceeded (during power-up cycle)
- ENB pin held high for $> t_{lock} / 2$

The Lock Detect function can be disabled by connecting CLD to GND.

When the A4931 is in Brake mode, the Lock Detect counter is disabled.

ET Package, 28-Contact QFN



PCB Layout Reference View

Contact the factory for the sidewall plating PCB footprint and assembly instructions.

Standard Branding Reference View 1

Line 1: Part Number
 Line 2: Logo A, 4-Digit Date Code
 Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

For Reference Only; not for tooling use
 (reference DWG-0000378, Rev. 3)
 Dimensions in millimeters
 Exact case and lead configuration at supplier discretion within limits shown

- △ Terminal #1 mark area
- △ Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- △ Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
 All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- △ Coplanarity includes exposed thermal pad and terminals
- △ Branding scale and appearance at supplier discretion

Revision History

| Number | Date | Description |
|--------|-------------------|--|
| 8 | February 10, 2020 | Added G temperature rated part option; minor editorial updates |
| 9 | February 10, 2022 | Updated package drawing (page 11) |

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