STM32F070CB STM32F070RB STM32F070C6 STM32F070F6

ARM®-based 32-bit MCU, up to 128 KB flash, USB FS 2.0, 11 timers, ADC, communication interfaces, 2.4 - 3.6 V

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology
- Core: Arm® 32-bit Cortex®-M0 CPU, frequency up to 48 MHz
- Memories
  - 32 to 128 Kbytes of flash memory
  - 6 to 16 Kbytes of SRAM with HW parity
- CRC calculation unit
- Reset and power management
  - Digital & I/Os supply: V_{DD} = 2.4 V to 3.6 V
  - Analog supply: V_{DDA} = V_{DD} to 3.6 V
  - Power-on/Power down reset (POR/PDR)
  - Low power modes: Sleep, Stop, Standby
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
- Up to 51 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 51 I/Os with 5V tolerant capability
- 5-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply: 2.4 V to 3.6 V
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- 11 timers
  - One 16-bit advanced-control timer for six-channel PWM output
  - Up to seven 16-bit timers, with up to four IC/OC, OCN, usable for IR control decoding
  - Independent and system watchdog timers
  - SysTick timer

LQFP64 (10 × 10 mm)
LQFP48 (7 × 7 mm)

TSSOP20 (6.4 × 4.4 mm)

- Communication interfaces
  - Up to two I^2C interfaces
    - Fast Mode Plus (1 Mbit/s) support, with 20 mA current sink
    - SMBus/PMBus support (on single I/F)
  - Up to four USARTs supporting master synchronous SPI and modem control; one with auto baud rate detection
  - Up to two SPIs (18 Mbit/s) with 4 to 16 programmable bit frames
  - USB 2.0 full-speed interface with BCD and LPM support
- Serial wire debug (SWD)
- All packages ECOPACK 2 compliant

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1 Introduction

This document provides information on STM32F070CB/RB/C6/F6 microcontrollers, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering codes.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32F070CB/RB/C6/F6 errata sheet ES0291.

Information on memory mapping and control registers is the subject of the reference manual RM0360 available from the STMicroelectronics website *www.st.com*.

Information on Arm®(a) Cortex®-M0+ core is available from the www.arm.com website.

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2 Description

The STM32F070CB/RB/C6/F6 microcontrollers incorporate the high-performance Arm® Cortex®-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 128 Kbytes of flash memory and up to 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I^2Cs, up to two SPIs and up to four USARTs), one USB Full speed device, one 12-bit ADC, seven general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F070CB/RB/C6/F6 microcontrollers operate in the -40 to +85 °C temperature range from a 2.4 to 3.6V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

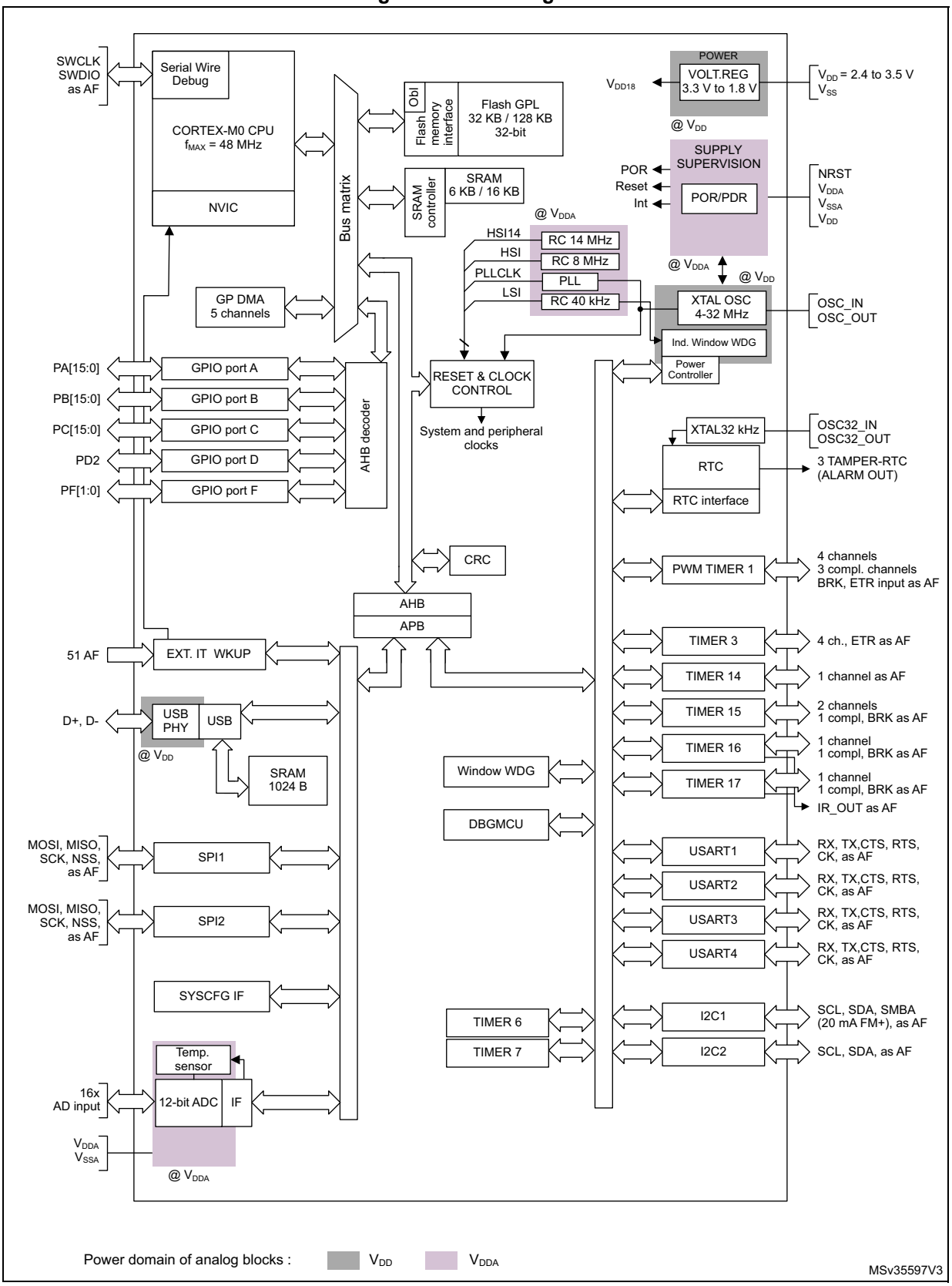
The STM32F070CB/RB/C6/F6 microcontrollers include devices in three different packages ranging from 20 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F070CB/RB/C6/F6 peripherals proposed.

These features make the STM32F070CB/RB/C6/F6 microcontrollers suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Table 1. STM32F070CB/RB/C6/F6 family device features and peripheral counts

Peripheral		STM32F070F6	STM32F070C6	STM32F070CB	STM32F070RB
Flash memory (Kbytes)		32		128	
SRAM (Kbytes)		6		16	
Timers	Advanced control	1 (16-bit)			
	General purpose	4 (16-bit)		5 (16-bit)	
	Basic	-		2 (16-bit)	
Comm. interfaces	SPI	1		2	
	I^2C	1		2	
	USART	2		4	
	USB	1			
12-bit ADC (number of channels)		1 (9 ext. + 2 int.)	1 (10 ext. + 2 int.)	1 (10 ext. + 2 int.)	1 (16 ext. + 2 int.)
GPIOs		15	37	37	51
Max. CPU frequency		48 MHz			
Operating voltage		2.4 to 3.6 V			
Operating temperature		Ambient operating temperature: -40°C to 85°C Junction temperature: -40°C to 105°C			
Packages		TSSOP20	LQFP48	LQFP48	LQFP64

Figure 1. Block diagram



3 Functional overview

3.1 Arm® Cortex®-M0 core with embedded flash memory and SRAM

The Arm® Cortex®-M0 processor is the latest generation of Arm processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The Arm® Cortex®-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

The STM32F0xx family has an embedded Arm core and is therefore compatible with all Arm tools and software.

Figure 1 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- 6 to 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 32 to 128 Kbytes of embedded flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- Boot from user flash memory
- Boot from system Memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the flash memory by using USART on pins PA14/PA15 or PA9/PA10, or I2C on pins PB6/PB7, or USB on pins PA11/PA12 (USB can be used only with HSE external clock equal to 24MHz, 18MHz, 16MHz, 12MHz, 8MHz, 6MHz, or 4MHz).

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a generated polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = 2.4 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F070CB/RB/C6/F6 microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines and RTC.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

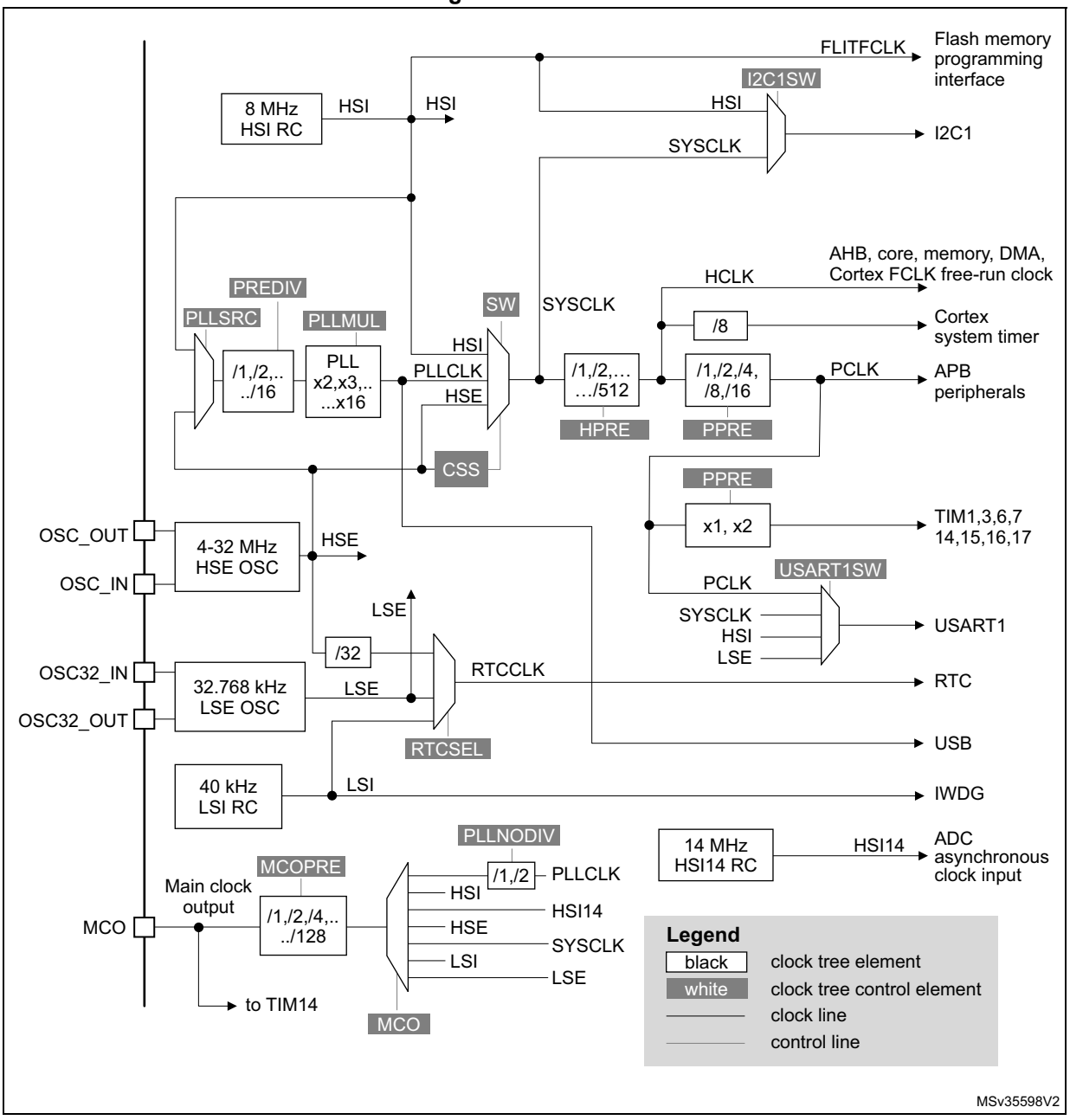
Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMA manages memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, USART, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 51 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and two internal (temperature sensor, voltage reference measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 2. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 3. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.11 Timers and watchdogs

The STM32F070CB/RB/C6/F6 devices include up to five general-purpose timers, two basic timers and one advanced control timer.

Table 4 compares the features of the different timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	-
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	-
	TIM15(1)	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6,(1) TIM7(1)	16-bit	Up	Any integer between 1 and 65536	Yes	0	-

1. Not available on STM32F070x6 devices.

3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.11.2 General-purpose timers (TIM3, TIM14...17)

There are five synchronizable general-purpose timers embedded in the STM32F070CB/RB/C6/F6 devices (see *Table 4* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM3

STM32F070CB/RB/C6/F6 devices feature one synchronizable 4-channel general-purpose timer. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM3 general-purpose timer can work with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM3 has an independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

The counter can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate withTIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.11.3 Basic timers TIM6 and TIM7

These timers can be used as a generic 16-bit time base.

3.11.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It

can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.11.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.11.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC)

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Tow anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.13 Inter-integrated circuit interfaces (I^2C)

Up to two I2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) or Fast mode (up to 400 kbit/s). I2C1 also supports Fast Mode Plus (up to 1 Mbit/s), with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 5. Comparison of I2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	-

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 6* for the differences between I2C1 and I2C2.

Table 6. STM32F070CB/RB/C6/F6 I^2C implementation(1)

I2C features	I2C1	I2C2(2)
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s), with 20mA output drive I/Os	X	-
Independent clock	X	-
SMBus	X	-
Wakeup from STOP	-	-

1. X = supported.
2. Only available on STM32F070xB devices.

3.14 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds up to four universal synchronous/asynchronous receivers/transmitters that communicate at speeds of up to 6 Mbit/s.

Table 7 gives an overview of features as implemented on the available USART interfaces. All USART interfaces can be served by the DMA controller.

Table 7. STM32F70x0 USART implementation(1)

USART modes/ features	STM32F070x6		STM32F070xB		
	USART1	USART2	USART1 USART2	USART3	USART4
Hardware flow control for modem	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	-
Multiprocessor communication	X	X	X	X	X
Synchronous mode	X	X	X	X	X
Smartcard mode	-	-	-	-	-
Single-wire Half-duplex communication	X	X	X	X	X
IrDA SIR ENDEC block	-	-	-	-	-
LIN mode	-	-	-	-	-
Dual clock domain and wakeup from Stop mode	-	-	-	-	-
Receiver timeout interrupt	X	-	X	-	-
Modbus communication	-	-	-	-	-
Auto baud rate detection (supported modes)	4	-	4	-	-
Driver Enable	X	X	X	X	X
USART data length	7, 8 and 9 bits				

1. **X = supported.**

3.15 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

SPI1 and SPI2 are identical and implement the set of features shown in the following table.

Table 8. STM32F070CB/RB/C6/F6 SPI implementation(1)

SPI features	SPI1	SPI2(2)
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
TI mode	X	X

1. X = supported.
2. Available on STM32F070xB only.

3.16 Universal serial bus (USB)

The STM32F070CB/RB/C6/F6 embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HSE crystal oscillator).

3.17 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin descriptions

Figure 3. TSSOP20 20-pin package pinout (top view)

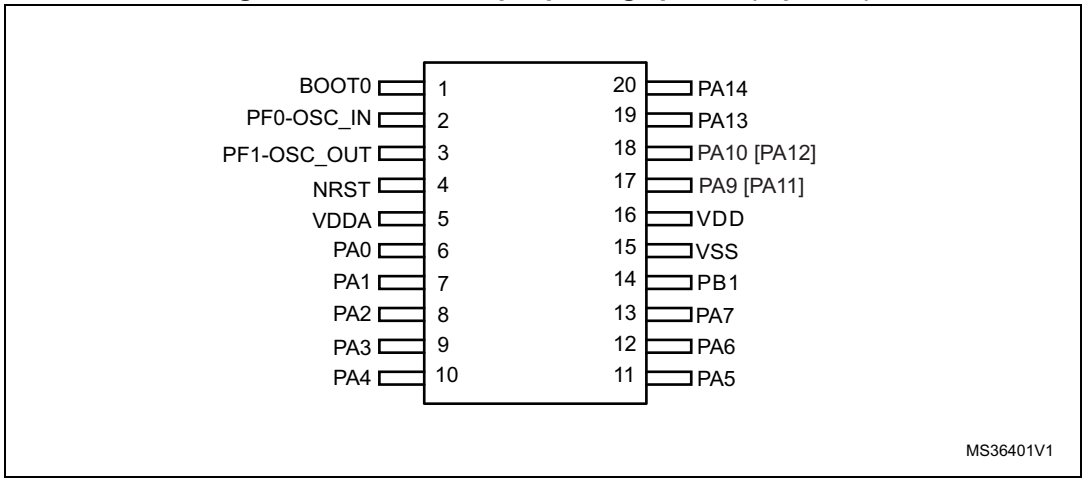


Figure 4. LQFP48 48-pin package pinout (top view)

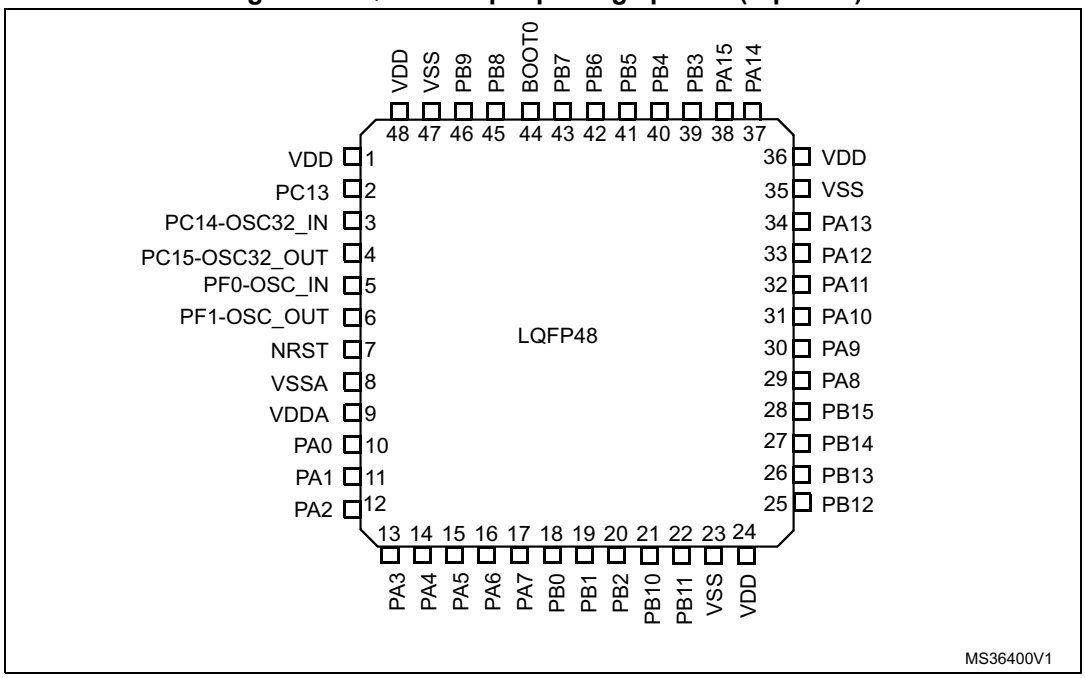


Figure 5. LQFP64 64-pin package pinout (top view)

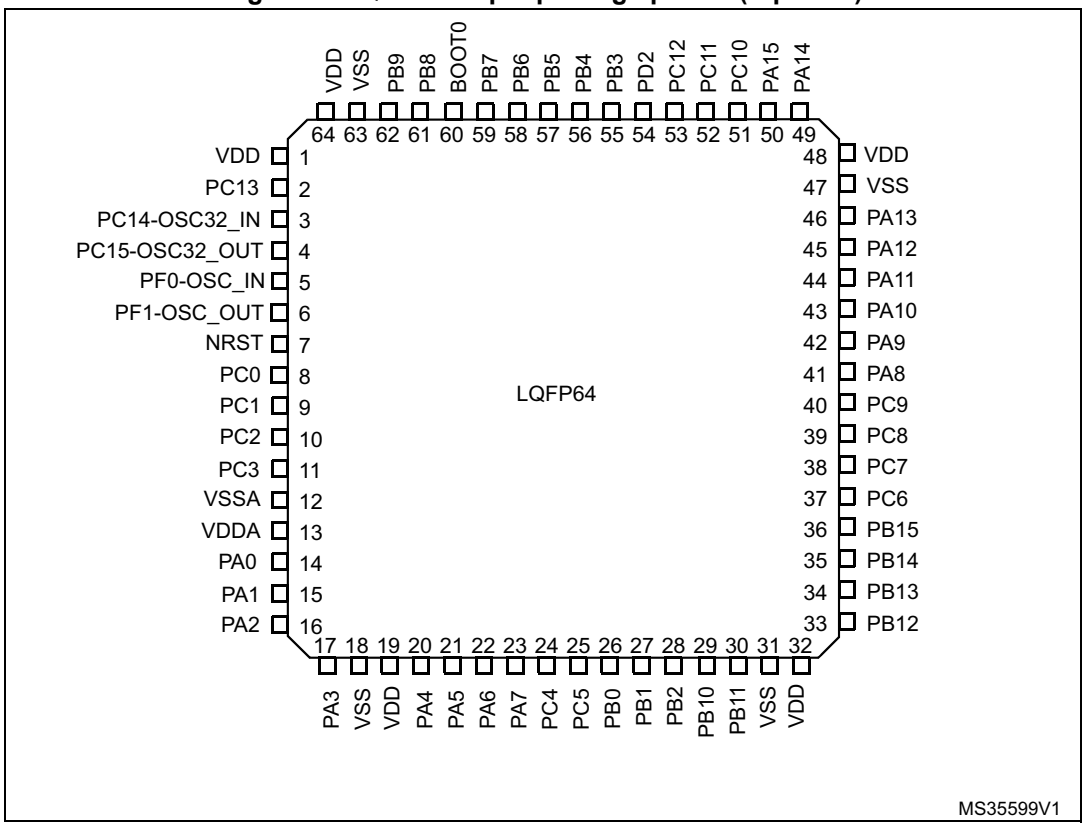


Table 9. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F070xB/6 pin definitions

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	TSSOP20					Alternate functions	Additional functions
1	1	-	VDD	S	-	-	Digital power supply	
2	2	-	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
3	3	-	PC14-OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
4	4	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
5	5	2	PF0-OSC_IN (PF0)	I/O	FT	-	I2C1_SDA(3)	OSC_IN
6	6	3	PF1-OSC_OUT (PF1)	I/O	FT	-	I2C1_SCL(3)	OSC_OUT
7	7	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	-	-	PC0	I/O	TTa	-	EVENTOUT	ADC_IN10
9	-	-	PC1	I/O	TTa	-	EVENTOUT	ADC_IN11
10	-	-	PC2	I/O	TTa	-	SPI2_MISO, EVENTOUT	ADC_IN12
11	-	-	PC3	I/O	TTa	-	SPI2_MOSI, EVENTOUT	ADC_IN13
12	8	-	VSSA	S	-	-	Analog ground	
13	9	5	VDDA	S	-	-	Analog power supply	
14	10	6	PA0	I/O	TTa	(4)	USART2_CTS, USART4_TX	RTC_ TAMP2, WKUP1, ADC_IN0,
15	11	7	PA1	I/O	TTa	(4)	USART2_RTS, TIM15_CH1N, USART4_RX, EVENTOUT	ADC_IN1
16	12	8	PA2	I/O	TTa	(4)	USART2_TX, TIM15_CH1	ADC_IN2, WKUP4
17	13	9	PA3	I/O	TTa	(4)	USART2_RX, TIM15_CH2	ADC_IN3
18	-	-	VSS	S	-	-	Ground	
19	-	-	VDD	S	-	-	Digital power supply	
20	14	10	PA4	I/O	TTa	-	SPI1_NSS, TIM14_CH1, USART2_CK, USB_NOE(3)	ADC_IN4
21	15	11	PA5	I/O	TTa	-	SPI1_SCK	ADC_IN5

Table 10. STM32F070xB/6 pin definitions (continued)

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	TSSOP20					Alternate functions	Additional functions
22	16	12	PA6	I/O	TTa	(4)	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT, USART3_CTS	ADC_IN6
23	17	13	PA7	I/O	TTa	-	SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
24	-	-	PC4	I/O	TTa	(4)	EVENTOUT, USART3_TX	ADC_IN14
25	-	-	PC5	I/O	TTa	(4)	USART3_RX	ADC_IN15, WKUP5
26	18	-	PB0	I/O	TTa	(4)	TIM3_CH3, TIM1_CH2N, EVENTOUT, USART3_CK	ADC_IN8
27	19	14	PB1	I/O	TTa	(4)	TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N	ADC_IN9
28	20	-	PB2	I/O	FT	-	-	-
29	21	-	PB10	I/O	FT	(4)	I2C2_SCL, SPI2_SCK, USART3_TX	-
30	22	-	PB11	I/O	FT	(4)	USART3_RX, EVENTOUT, I2C2_SDA	-
31	23	15	VSS	S	-	-	Ground	
32	24	16	VDD	S	-	-	Digital power supply	
33	25	-	PB12	I/O	FT	(4)	TIM1_BKIN, TIM15_BKIN, SPI2_NSS, EVENTOUT, USART3_CK	-
34	26	-	PB13	I/O	FTf	(4)	SPI2_SCK, I2C2_SCL, TIM1_CH1N, USART3_CTS	-
35	27	-	PB14	I/O	FTf	(4)	SPI2_MISO, I2C2_SDA, TIM1_CH2N, TIM15_CH1, USART3_RTS	-
36	28	-	PB15	I/O	FT	(4)	SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	WKUP7, RTC_REFIN
37	-	-	PC6	I/O	FT	-	TIM3_CH1	-
38	-	-	PC7	I/O	FT	-	TIM3_CH2	-
39	-	-	PC8	I/O	FT	-	TIM3_CH3	-

Table 10. STM32F070xB/6 pin definitions (continued)

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	TSSOP20					Alternate functions	Additional functions
40	-	-	PC9	I/O	FT	-	TIM3_CH4	-
41	29	-	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	30	17	PA9	I/O	FT	(4)	USART1_TX, TIM1_CH2, TIM15_BKIN, I2C1_SCL(3)	-
43	31	18	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN, I2C1_SDA(3)	-
44	32	17(5)	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, EVENTOUT	USB_DM
45	33	18(5)	PA12	I/O	FT	-	USART1_RTS, TIM1_ETR, EVENTOUT	USB_DP
46	34	19	PA13	I/O	FT	**(6)**	IR_OUT, SWDIO, USB_NOE	-
47	35	-	VSS	S	-	-	Ground	
48	36	-	VDD	S	-	-	Digital power supply	
49	37	20	PA14	I/O	FT	-	USART2_TX, SWCLK	-
50	38	-	PA15	I/O	FT	(4)	SPI1_NSS, USART2_RX, USART4_RTS, EVENTOUT	-
51	-	-	PC10	I/O	FT	(4)	USART3_TX, USART4_TX	-
52	-	-	PC11	I/O	FT	(4)	USART3_RX, USART4_RX	-
53	-	-	PC12	I/O	FT	(4)	USART3_CK, USART4_CK	-
54	-	-	PD2	I/O	FT	(4)	TIM3_ETR, USART3_RTS	-
55	39	-	PB3	I/O	FT	-	SPI1_SCK, EVENTOUT	-
56	40	-	PB4	I/O	FT	-	SPI1_MISO, TIM17_BKIN, TIM3_CH1, EVENTOUT	-
57	41	-	PB5	I/O	FT	(4)	SPI1_MOSI, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6
58	42	-	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N	-

Table 10. STM32F070xB/6 pin definitions (continued)

Pin numbers			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	TSSOP20					Alternate functions	Additional functions
59	43	-	PB7	I/O	FTf	(4)	I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N	-
60	44	1	BOOT0	I	B	-	Boot memory selection	
61	45	-	PB8	I/O	FTf	-	I2C1_SCL, TIM16_CH1	-
62	46	-	PB9	I/O	FTf	(4)	SPI2_NSS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-
63	47	-	VSS	S	-	-	Ground	
64	48	-	VDD	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. Available on STM32F070C6/F6 devices only.
4. TIM15, I2C2, WKUP4, WKUP5, WKUP6, WKUP7, SPI2, USART3 and USART4 are available on STM32F070CB/RB devices only.
5. On STM32F070C6/F6 devices, pin pair PA11/12 can be remapped instead of pin pair PA9/10 using SYSCFG_CFGR1 register.
6. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 11. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	-	-	USART4_TX(1)	-	-	-
PA1	EVENTOUT	USART2_RTS	-	-	USART4_RX(1)	TIM15_CH1N(1)	-	-
PA2	TIM15_CH1(1)	USART2_TX	-	-	-	-	-	-
PA3	TIM15_CH2(1)	USART2_RX	-	-	-	-	-	-
PA4	SPI1_NSS	USART2_CK	USB_NOE(2)	-	TIM14_CH1	-	-	-
PA5	SPI1_SCK	-	-	-	-	-	-	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	USART3_CTS(1)	TIM16_CH1	EVENTOUT	-
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-	-
PA9	TIM15_BKIN(1)	USART1_TX	TIM1_CH2	-	I2C1_SCL (2)	-	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA (2)	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	-	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	-	-	-	-
PA13	SWDIO	IR_OUT	USB_NOE	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS	USART2_RX	-	EVENTOUT	USART4_RTS(1)	-	-	-

1. Available on STM32F070CB/RB devices only.
2. Available on STM32F070C6/F6 devices only.

Table 12. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	USART3_CK(1)	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	USART3_RTS(1)	-
PB2	-	-	-	-	-	-
PB3	SPI1_SCK	EVENTOUT	-	-	-	-
PB4	SPI1_MISO	TIM3_CH1	EVENTOUT	-	-	TIM17_BKIN
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-	USART4_CTS(1)	-
PB8	-	I2C1_SCL	TIM16_CH1	-	-	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	-	SPI2_NSS(1)
PB10	-	I2C2_SCL(1)	-	-	USART3_TX(1)	SPI2_SCK(1)
PB11	EVENTOUT	I2C2_SDA(1)	-	-	USART3_RX(1)	-
PB12	SPI2_NSS(1)	EVENTOUT	TIM1_BKIN	-	USART3_CK(1)	TIM15_BKIN(1)
PB13	SPI2_SCK(1)	-	TIM1_CH1N	-	USART3_CTS(1)	I2C2_SCL(1)
PB14	SPI2_MISO(1)	TIM15_CH1	TIM1_CH2N	-	USART3_RTS(1)	I2C2_SDA(1)
PB15	SPI2_MOSI(1)	TIM15_CH2	TIM1_CH3N	TIM15_CH1N(1)	-	-

1. Available on STM32F070xB devices only.

Table 13. Alternate functions selected through GPIOC_AFR registers for port C

Pin name	AF0(1)	AF1(1)
PC0	EVENTOUT(1)	-
PC1	EVENTOUT(1)	-
PC2	EVENTOUT(1)	SPI2_MISO(1)
PC3	EVENTOUT(1)	SPI2_MOSI(1)
PC4	EVENTOUT(1)	USART3_TX(1)
PC5	-	USART3_RX(1)
PC6	TIM3_CH1(1)	-
PC7	TIM3_CH2(1)	-
PC8	TIM3_CH3(1)	-
PC9	TIM3_CH4(1)	-
PC10	USART4_TX(1)	USART3_TX(1)
PC11	USART4_RX(1)	USART3_RX(1)
PC12	USART4_CK(1)	USART3_CK(1)
PC13	-	-
PC14	-	-
PC15	-	-

1. Available on STM32F070xB devices only.

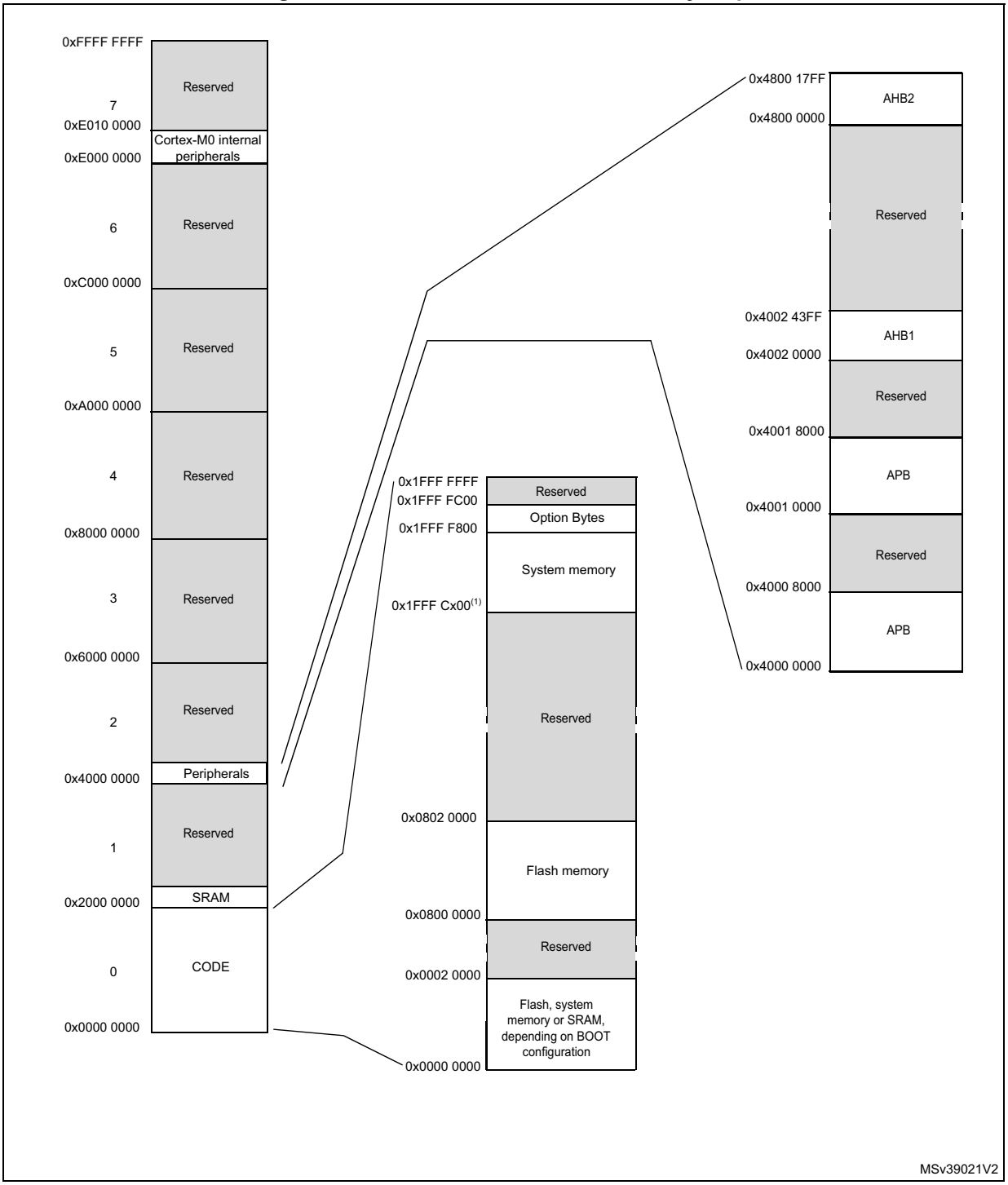
Table 14. Alternate functions selected through GPIOD_AFR registers for port D

Pin name	AF0(1)	AF1(1)
PD2	TIM3_ETR(1)	-

1. Available on STM32F070xB devices only.

5 Memory mapping

Figure 6. STM32F070CB/RB/C6/F6 memory map



1. The start address of the system memory is 0x1FFF C800 on STM32F070xB devices and 0x1FFF C400 on STM32F070x6 devices.

Table 15. STM32F070CB/RB/C6/F6 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
-	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 43FF	4 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
-	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
-	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 15. STM32F070CB/RB/C6/F6 peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7400 - 0x4000 7FFF	3 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	2 KB	Reserved
	0x4000 6000 - 0x4000 63FF	1 KB	USB RAM
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2(1)
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	3 KB	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4(1)
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3(1)
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2(1)
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	Reserved

1. Available on STM32F070CB/RB devices only.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

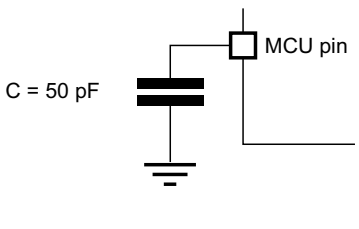
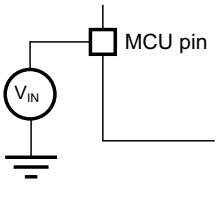
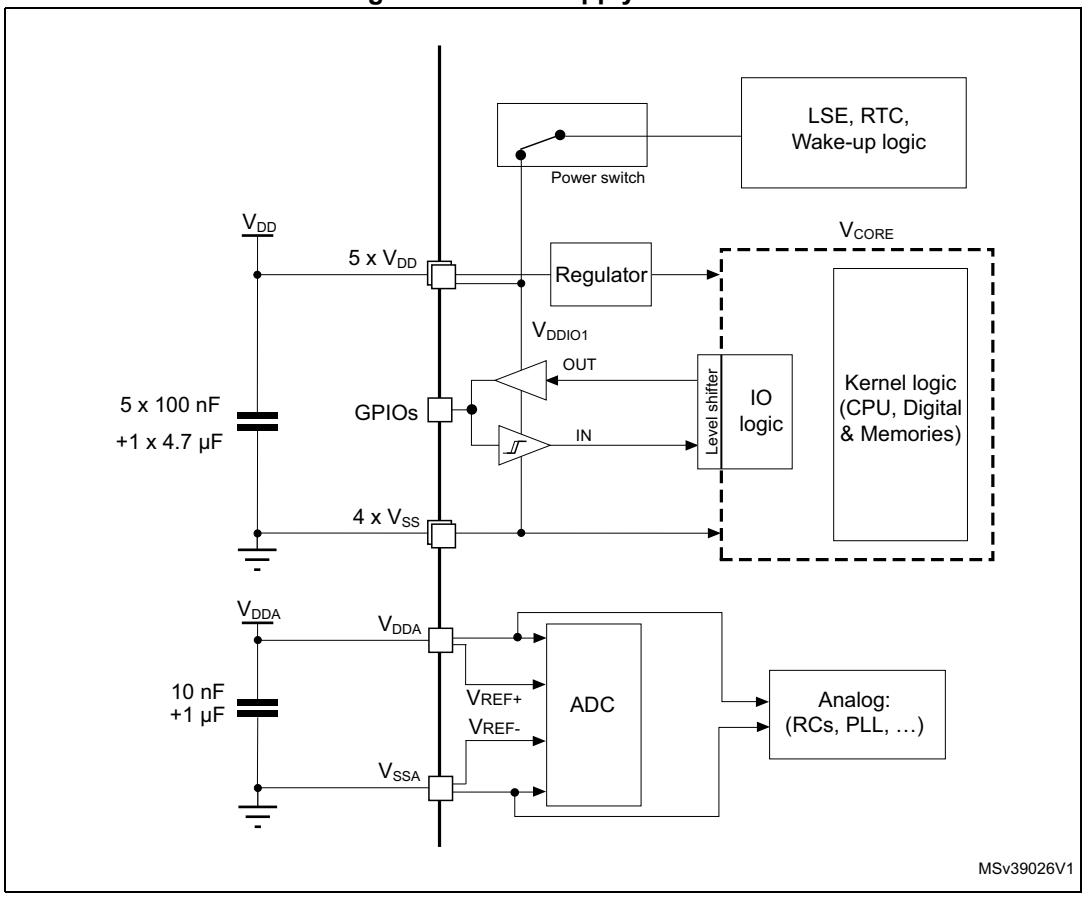


Figure 8. Pin input voltage



6.1.6 Power supply scheme

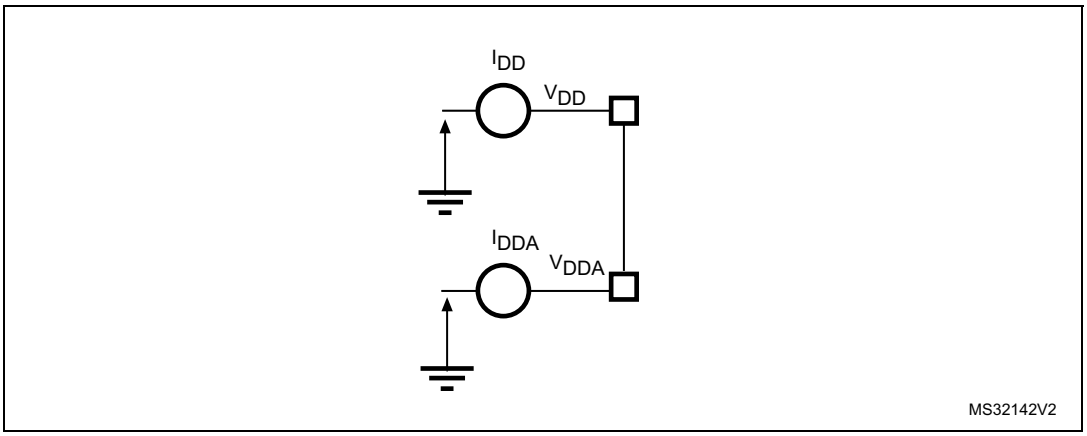
Figure 9. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16: Voltage characteristics*, *Table 17: Current characteristics* and *Table 18: Thermal characteristics* may cause permanent damage to the device. These are stress *ratings* only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 16. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage	-0.3	4.0	V
V_{DDA}–V_{SS}	External analog supply voltage	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DDIOx} + 4.0 (3)	V
	Input voltage on TTa pins	V_{SS} –0.3	4.0	V
	BOOT0	0	V_{DDIOx} + 4.0 (3)	V
	Input voltage on any other pin	V_{SS} –0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 17: Current characteristics* for the maximum allowed injected current values.
3. V_{DDIOx} is internally connected with VDD pin.

Table 17. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$(3)	Injected current on FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 16: Voltage characteristics* for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note (2) below *Table 50: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2.4	3.6	V

Table 19. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	Analog operating voltage	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	V_{DDIOx}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3(2)	
		FT and FTf I/O	-0.3	5.5(2)	
		BOOT0	0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 (1)	LQFP64	-	455	mW
		LQFP48	-	364	
		TSSOP20	-	263	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low power dissipation(2)	-40	105	
T_J	Junction temperature range	Suffix 6 version	-40	105	°C

1. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 20* are derived from tests performed under the ambient temperature condition summarized in *Table 19*.

Table 20. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 21* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 21. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge(2)	1.80	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.00	V

Table 21. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(4)	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 22* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 22. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40°C < T_A < +85°C	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10(1)	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4 (1)	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10(1)	mV
T_{Coeff}	Temperature coefficient	-	-100(1)	-	100(1)	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The flash memory access time is adjusted to the f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 23* to *Table 25* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 23. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled		Unit
				Typ	Max @ T_A(1)	
					85 °C	
I_{DD}	Supply current in Run mode, code executing from flash memory	HSI or HSE clock, PLL on	48 MHz	24.1	27.6	mA
			24 MHz	12.4	14.4	
		HSI or HSE clock, PLL off	8 MHz	4.52	5.28	
I_{DD}	Supply current in Run mode, code executing from RAM	HSI or HSE clock, PLL on	48 MHz	23.1	25.0	mA
			24 MHz	11.5	13.6	
		HSI or HSE clock, PLL off	8 MHz	4.34	5.03	
I_{DD}	Supply current in Sleep mode, code executing from flash memory or RAM	HSI or HSE clock, PLL on	48 MHz	15.0	17.3	mA
			24 MHz	7.53	8.87	
		HSI or HSE clock, PLL off	8 MHz	2.95	3.41	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 24. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions(1)	f_{HCLK}	V_{DDA} = 3.6 V		Unit
				Typ	Max @ T_A	
					85 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from flash memory or RAM	HSE bypass, PLL on	48 MHz	165	196	µA
		HSE bypass, PLL off	8 MHz	3.6	5.2	
			1 MHz	3.6	5.2	
		HSI clock, PLL on	48 MHz	245	279	
		HSI clock, PLL off	8 MHz	83.4	95.3	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.

Table 25. Typical and maximum consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})	Max(1)	Unit
				3.6 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF		15.9	49	µA
		Regulator in low-power mode, all oscillators OFF		3.7	33	
	Supply current in Standby mode	LSI ON and IWDG ON		1.5	-	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run or low-power mode, all oscillators OFF	2.8	3.6	
	Supply current in Standby mode		LSI ON and IWDG ON	3.5	-	
			LSI OFF and IWDG OFF	2.6	3.6	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run or low-power mode, all oscillators OFF	1.5	-	
	Supply current in Standby mode		LSI ON and IWDG ON	2.2	-	
			LSI OFF and IWDG OFF	1.4	-	

1. Data based on characterization results, not tested in production unless otherwise specified.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 3.3 V
- All I/O pins are in analog input configuration
- The flash memory access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 26. Typical current consumption in Run mode, code with data processing running from flash memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from flash memory	48 MHz	23.5	13.5	mA
			8 MHz	4.8	3.1	
I_{DDA}	Supply current in Run mode from V_{DDA} supply		48 MHz	163.3	163.3	µA
			8 MHz	2.5	2.5	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 44: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 27. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 3.3 V C_{EXT} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	4 MHz	0.18	mA
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V_{DDIOx} = 3.3 V C_{EXT} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V_{DDIOx} = 3.3 V C_{EXT} = 47 pF $C = C_{INT} + C_{EXT} + C_S$ $C = C_{int}$	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	

1. C_S = 7 pF (estimated value).

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 28* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop or Standby mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 28. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = V_{DDA} = 3.3 V	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	2.8	5	µs
$t_{WUSTANDBY}$	Wakeup from Standby mode	-	51	-	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4 SYSCLK cycles	-	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

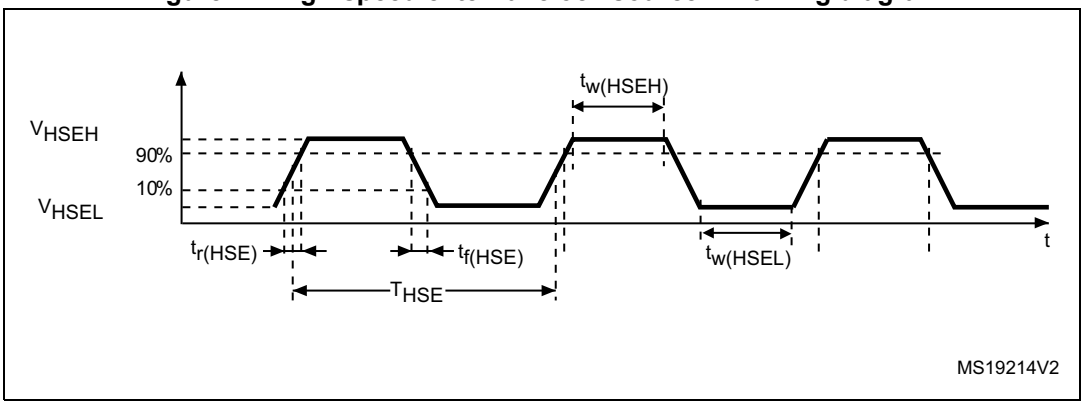
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 11: High-speed external clock source AC timing diagram*.

Table 29. High-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

1. Guaranteed by design, not tested in production.

Figure 11. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

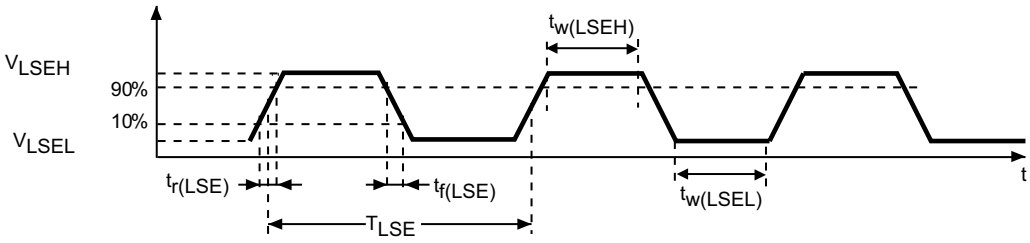
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 12*.

Table 30. Low-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 12. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 31*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ

Table 31. HSE oscillator characteristics

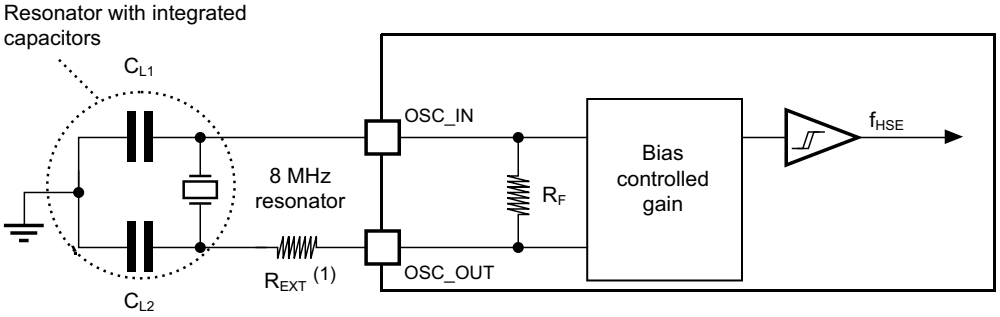
Symbol	Parameter	Conditions[1]	Min[2]	Typ	Max[2]	Unit
I_{DD}	HSE current consumption	During startup[3]	-	-	8.5	mA
		V_{DD} = 3.3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 13*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 13. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results

obtained with typical external components specified in *Table 32*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

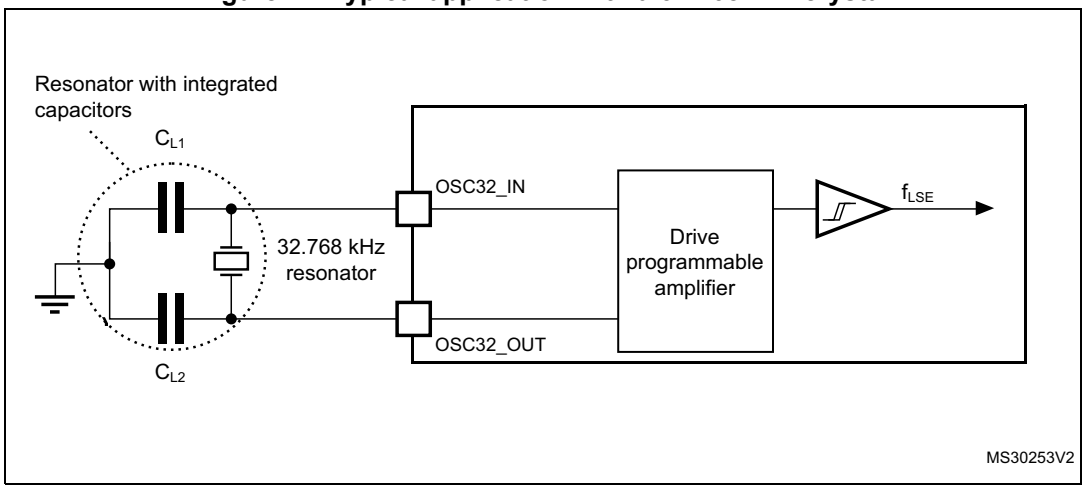
Table 32. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions[1]	Min[2]	Typ	Max[2]	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.5	0.9	µA
		medium-low drive capability	-	-	1	
		medium-high drive capability	-	-	1.3	
		high drive capability	-	-	1.6	
g_m	Oscillator transconductance	low drive capability	5	-	-	µA/V
		medium-low drive capability	8	-	-	
		medium-high drive capability	15	-	-	
		high drive capability	25	-	-	
$t_{SU(LSE)}$[3]	Startup time	V_{DDIOx} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 14. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 33* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 33. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{HSI}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = -40 to 85°C	-	±5	-	%
		T_A = 25°C	-	±1(3)	-	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	-	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 85°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. With user calibration.

High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 34. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 85 °C	-	±5	-	%
$t_{su(HSI14)}$	HSI14 oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	-	-	100	-	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 35. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz

Table 35. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	-	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 36* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 36. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	8.0	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 85 °C unless otherwise specified.

Table 37. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = -40 to +85 °C	-	53.5	-	µs
t_{ERASE}	Page erase time (2)	T_A = -40 to +85 °C	-	30	-	ms
t_{ME}	Mass erase time	T_A = -40 to +85 °C	-	30	-	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA
V_{prog}	Programming voltage	-	2.4	-	3.6	V

1. Guaranteed by design, not tested in production.
2. Page size is 1KB for STM32F070x6 devices and 2KB for STM32F070xB devices.

Table 38. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to +85 °C	1	kcycle
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	20	Years

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 39*. They are based on the EMS levels and classes defined in application note AN1709.

Table 39. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3V, LQFP48, T_A = +25 °C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3V, LQFP48, T_A = +25°C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-4	4B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 40. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-3	dBµV
			30 to 130 MHz	23	
			130 MHz to 1 GHz	17	
			EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 41. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	All	C4	500	V

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 42. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 43*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 43. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 and PF1 pins	-0	NA	mA
	Injected current on PA9, PB3, PB13, PF11 pins with induced leakage current on adjacent pins less than 50 µA	-5	NA	
	Injected current on PA11 and PA12 pins with induced leakage current on adjacent pins less than -1 mA	-5	NA	
	Injected current on all other FT and FTf pins	-5	NA	
	Injected current on PB0 and PB1 pins	-5	NA	
	Injected current on PC0 pin	-0	+5	
	Injected current on all other TTa, TC and RST pins	-5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under the conditions summarized in *Table 19: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 44. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DDIOx}+0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475\ V_{DDIOx}-0.2^{(1)}$	
		BOOT0	-	-	$0.3\ V_{DDIOx}-0.3^{(1)}$	
		All I/Os except BOOT0 pin	-	-	$0.3\ V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DDIOx}+0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5\ V_{DDIOx}+0.2^{(1)}$	-	-	
		BOOT0	$0.2\ V_{DDIOx}+0.95^{(1)}$	-	-	
		All I/Os except BOOT0 pin	$0.7\ V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(1)}$	-	mV
		FT and FTf I/O	-	$100^{(1)}$	-	
		BOOT0	-	$300^{(1)}$	-	

Table 44. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current(2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$	-	-	±0.1	µA
		TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O (3) $V_{DDIOx} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor (4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 43: I/O current injection susceptibility*.
3. To sustain a voltage higher than V_{DDIOx} + 0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 15* for standard I/Os, and in *Figure 16* for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 15. TC and TTa I/O input characteristics

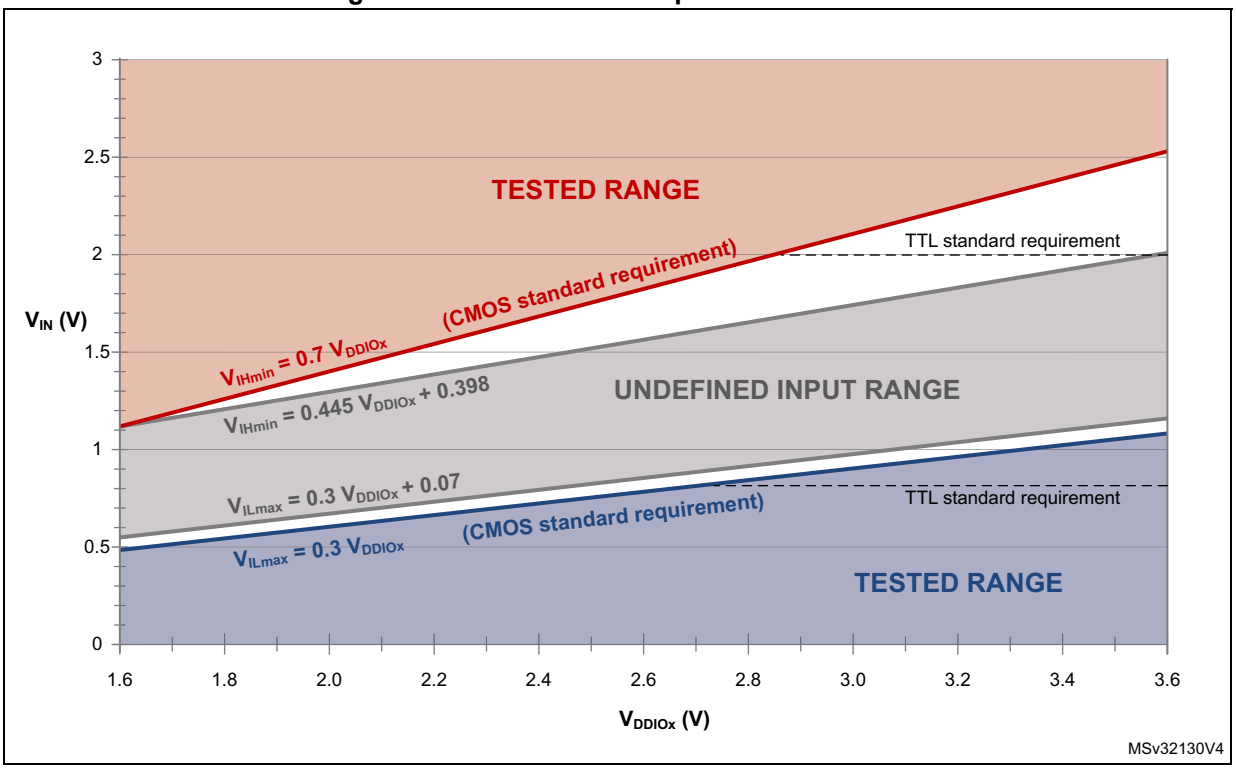
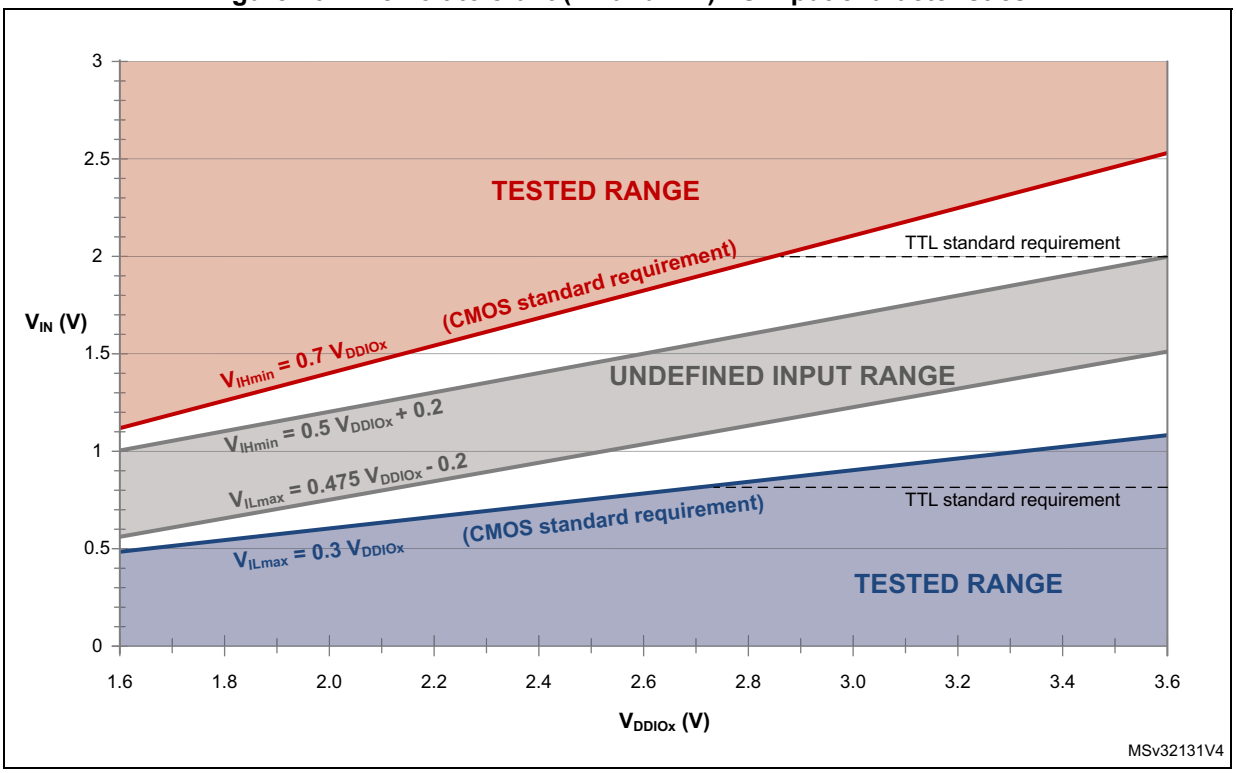


Figure 16. Five volt tolerant (FT and FTf) I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 16: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 16: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 45. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DDIOx}–1.3	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 6 mA	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OLFm+}(2)	Output low level voltage for an FTf I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
		$\|I_{IO}\|$ = 10 mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 16: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. Data based on characterization results. Not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 17* and *Table 46*, respectively.

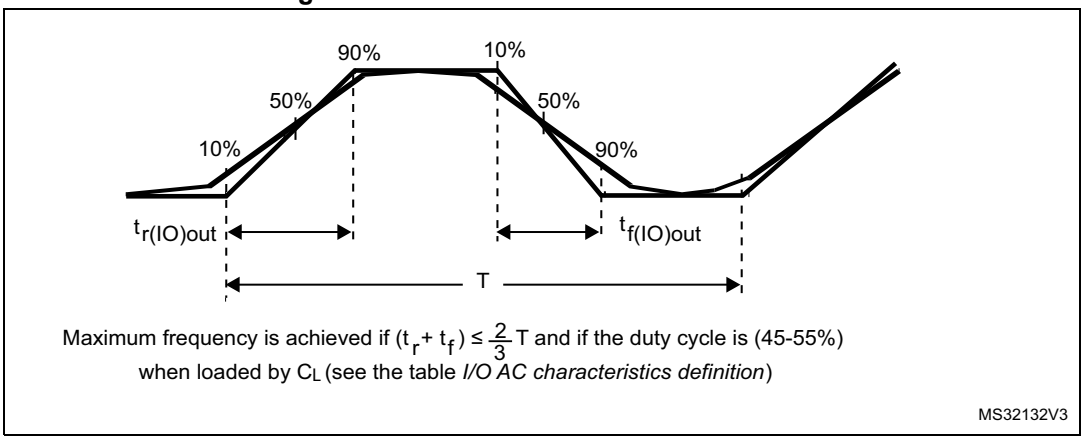
Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 46. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq$ 2.4 V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq$ 2.4 V	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, $V_{DDIOx} \geq$ 2.7 V	-	50	MHz
			C_L = 50 pF, $V_{DDIOx} \geq$ 2.7 V	-	30	
			C_L = 50 pF, 2.4 V $\leq V_{DDIOx} <$ 2.7 V	-	20	
	$t_{f(IO)out}$	Output fall time	C_L = 30 pF, $V_{DDIOx} \geq$ 2.7 V	-	5	ns
			C_L = 50 pF, $V_{DDIOx} \geq$ 2.7 V	-	8	
			C_L = 50 pF, 2.4 V $\leq V_{DDIOx} <$ 2.7 V	-	12	
	$t_{r(IO)out}$	Output rise time	C_L = 30 pF, $V_{DDIOx} \geq$ 2.7 V	-	5	
			C_L = 50 pF, $V_{DDIOx} \geq$ 2.7 V	-	8	
			C_L = 50 pF, 2.4 V $\leq V_{DDIOx} <$ 2.7 V	-	12	
Fm+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq$ 2.4 V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	12	ns
	$t_{r(IO)out}$	Output rise time		-	34	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0360 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 17*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0360 for a detailed description of Fm+ I/O configuration.

Figure 17. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

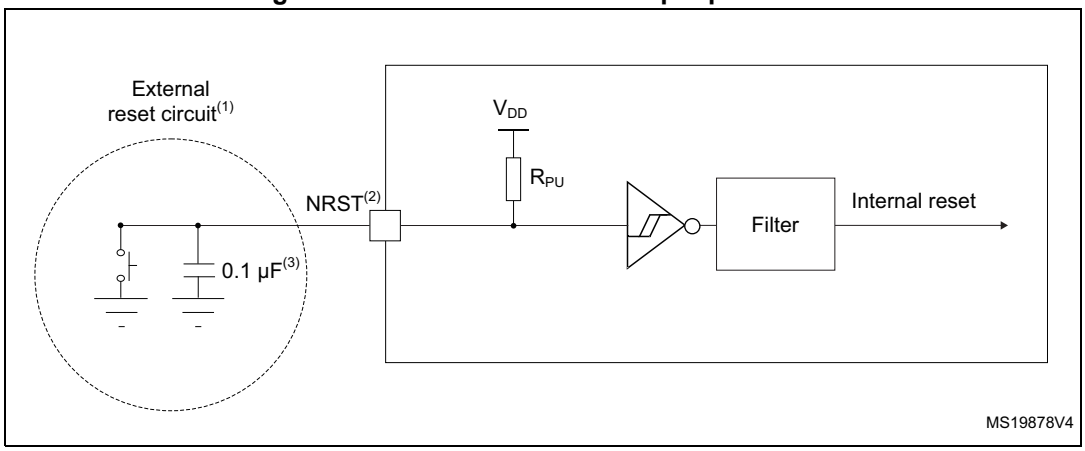
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 47. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3\ V_{DD}+0.07^{(1)}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.445\ V_{DD}+0.398^{(1)}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	$100^{(1)}$	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	$300^{(3)}$	-	-	ns
		$2.4 < V_{DD} < 3.6$	$500^{(3)}$	-	-	

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
3. Data based on design simulation only. Not tested in production.

Figure 18. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 47: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 48* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 19: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 48. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC(1)	$V_{DD} = V_{DDA} = 3.3$ V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 49* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF

Table 48. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CAL} (2)(3)	Calibration time	f_{ADC} = 14 MHz		5.9		µs
		-		83		$1/f_{ADC}$
$W_{LATENCY}$ (2)(4)	ADC_DR register write latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr} (2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 14 MHz		0.196		µs
		$f_{ADC} = f_{PCLK}/2$		5.5		$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 12 MHz		0.219		µs
		$f_{ADC} = f_{PCLK}/4$		10.5		$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.188	-	0.259	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (2)	Stabilization time	-		14		$1/f_{ADC}$
t_{CONV} (2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 49. R_{AIN} max for f_{ADC} = 14 MHz

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 50. ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.7 V to 3.6 V T_A = -40 to 85 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 19. ADC accuracy characteristics

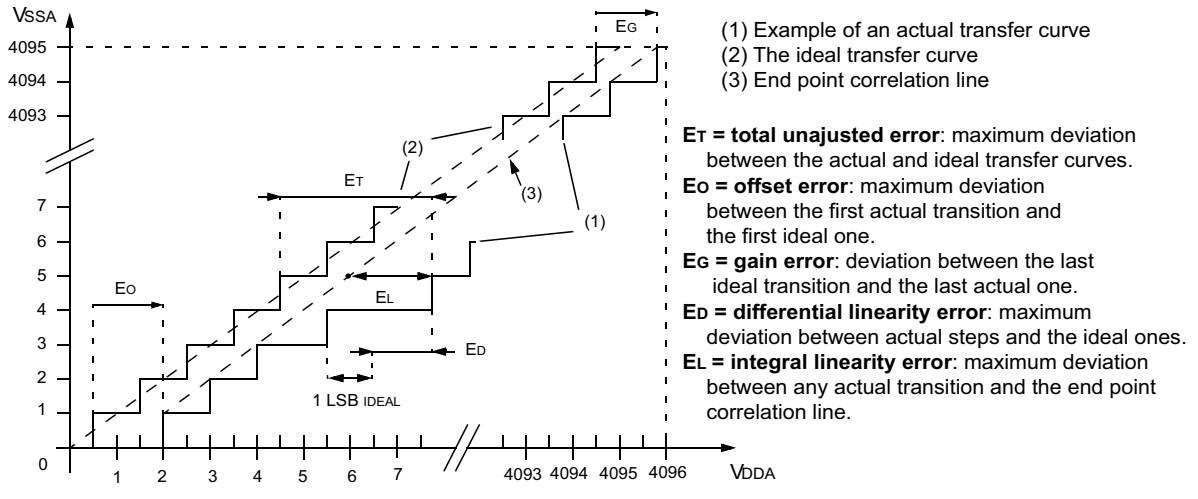
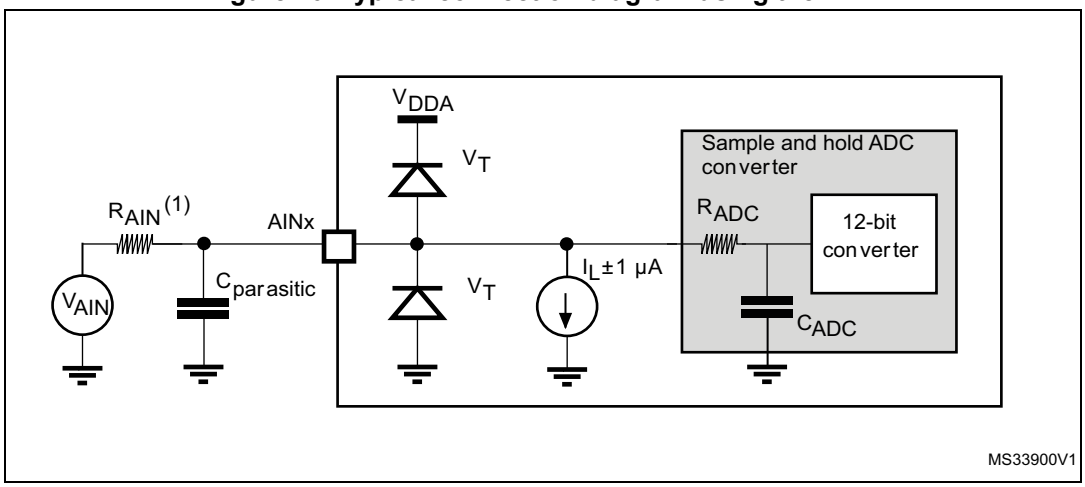


Figure 20. Typical connection diagram using the ADC



1. Refer to *Table 48: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.17 Temperature sensor characteristics

Table 51. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{30}	Voltage at 30 °C (±5 °C)(2)	1.34	1.43	1.52	V
t_{START} (1)	ADC_IN16 buffer startup time	-	-	10	µs
t_{S_temp} (1)	ADC sampling time when reading the temperature	4	-	-	µs

1. Guaranteed by design, not tested in production.
2. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 2: Temperature sensor calibration values*.

6.3.18 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 52. TIMx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	1365	-	µs
	32-bit timer maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	-	s

Table 53. IWDG min/max timeout period at 40 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 54. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.19 Communication interfaces

I^2C interface characteristics

The I2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 55. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in *Table 56* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 19: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 56. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 21. SPI timing diagram - slave mode and CPHA = 0

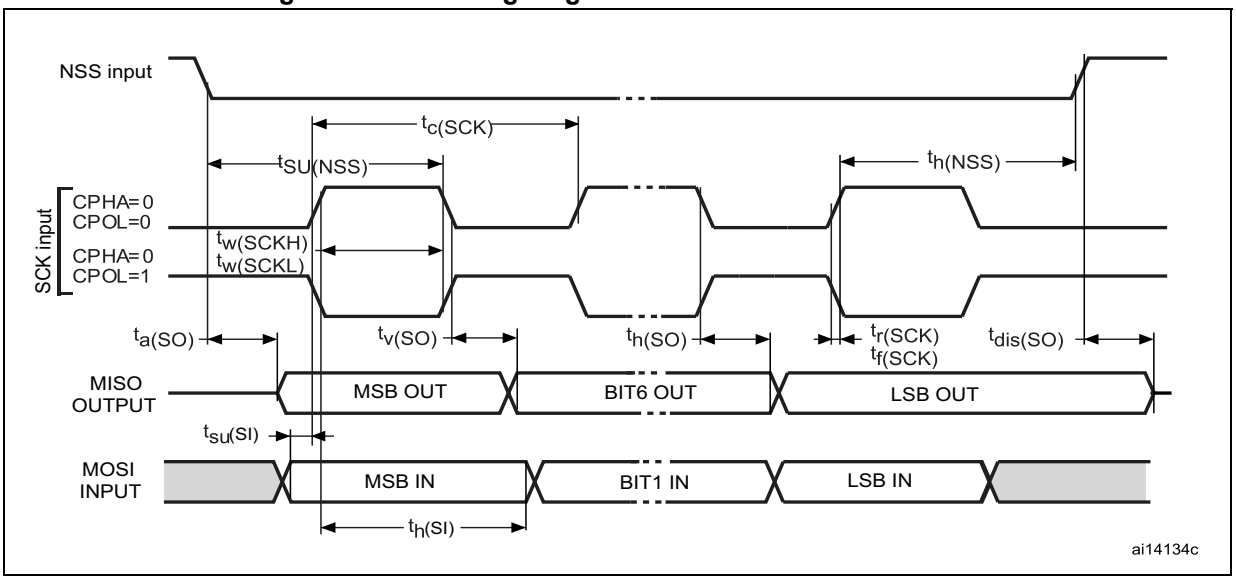
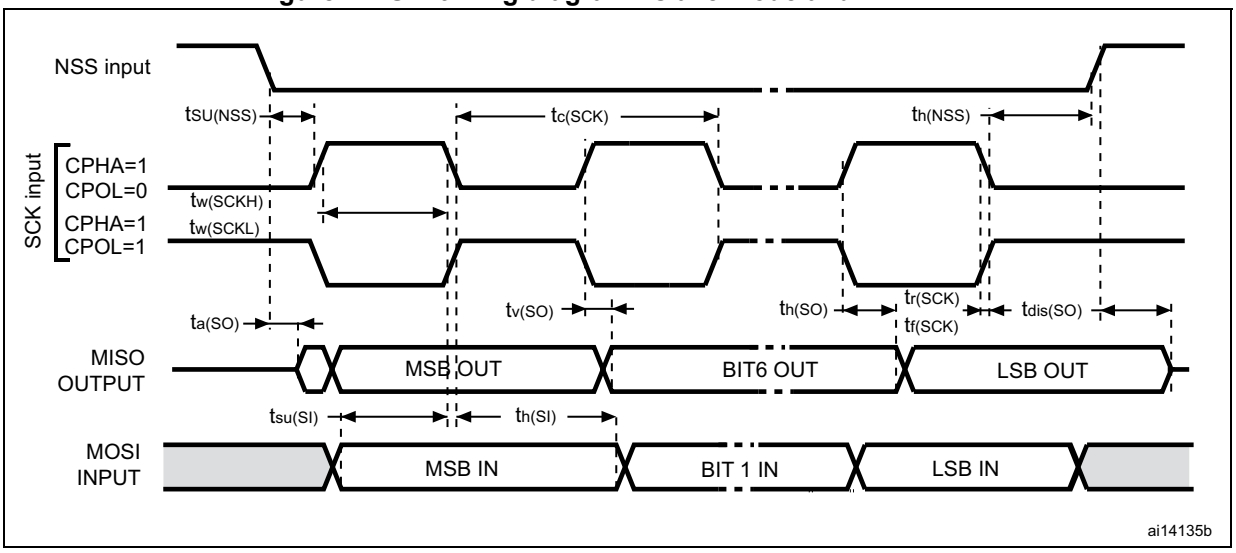
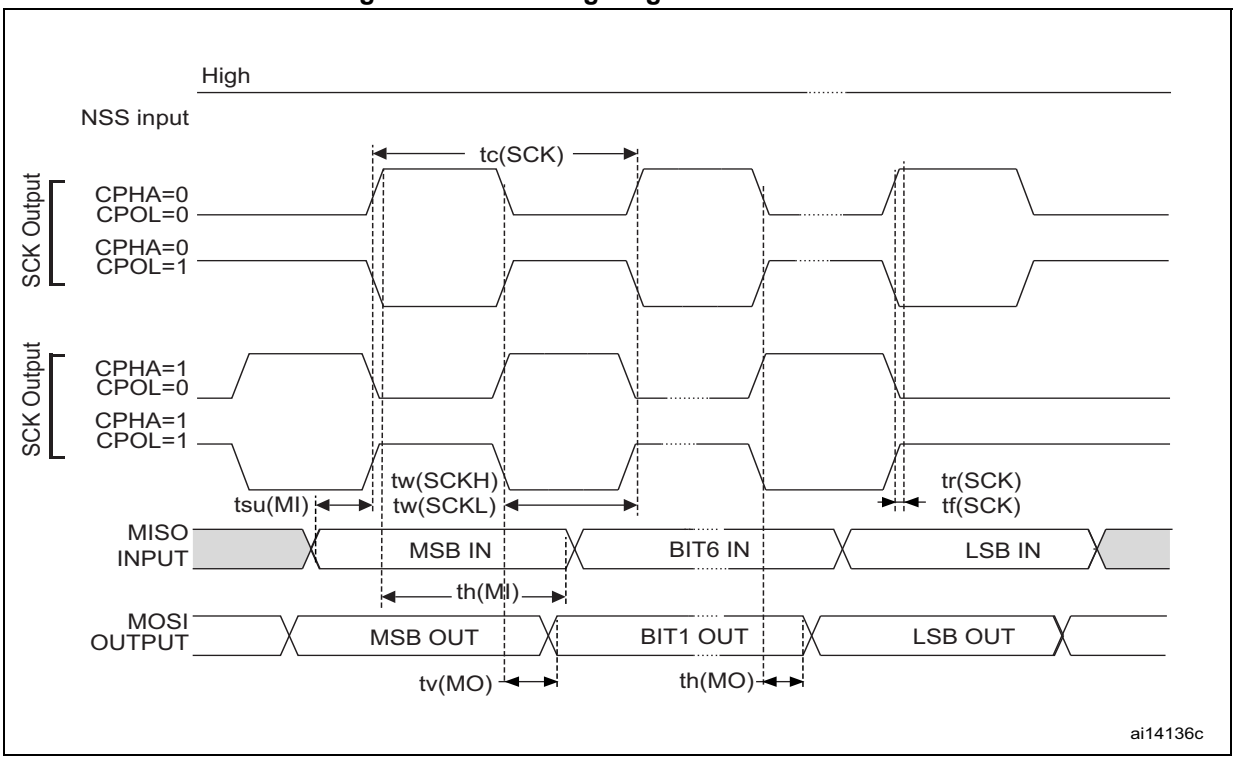


Figure 22. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 23. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

USB characteristics

The STM32F070CB/RB/C6/F6 USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 57. USB electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
V_{DD}	USB transceiver operating voltage	-	3.0(1)	-	3.6	V
$t_{STARTUP}$(2)	USB transceiver startup time	-	-	-	1.0	µs
R_{PUI}	Embedded USB_DP pull-up value during idle	-	1.1	1.26	1.5	kΩ
R_{PUR}	Embedded USB_DP pull-up value during reception	-	2.0	2.26	2.6	
Z_{DRV}(2)	Output driver impedance(3)	Driving high and low	28	40	44	Ω

1. The STM32F070CB/RB/C6/F6 USB functionality is ensured down to 2.7 V, but the USB electrical characteristics are degraded in the 2.7-to-3.0 V voltage range.
2. Guaranteed by design, not tested in production.
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 Device marking

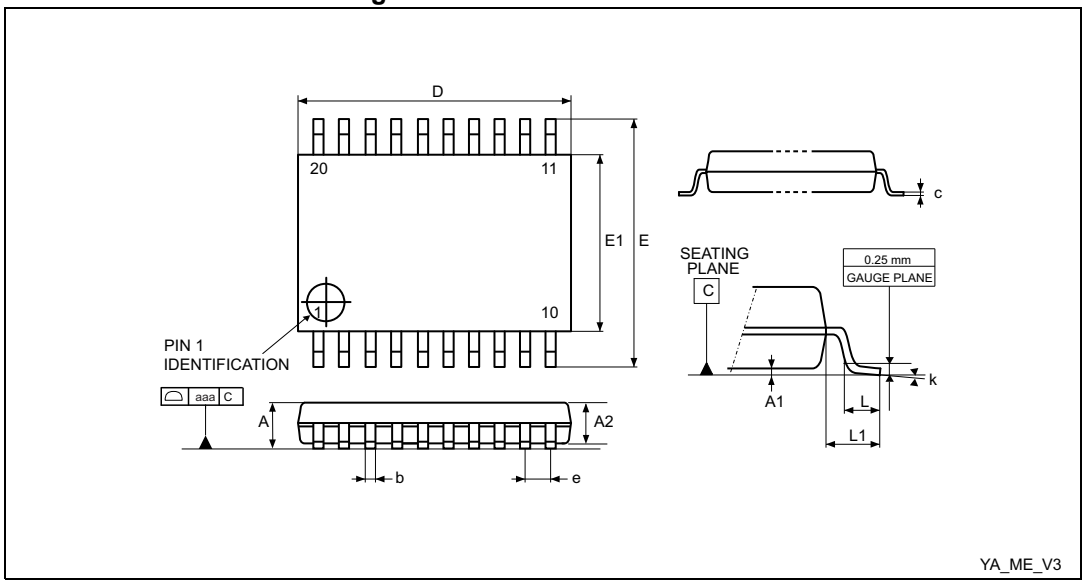
Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 TSSOP20 package information (YA)

TSSOP20 is a 20-lead, 6.5 x 4.4 mm thin small-outline package with 0.65 mm pitch.

Figure 24. TSSOP20 – Outline



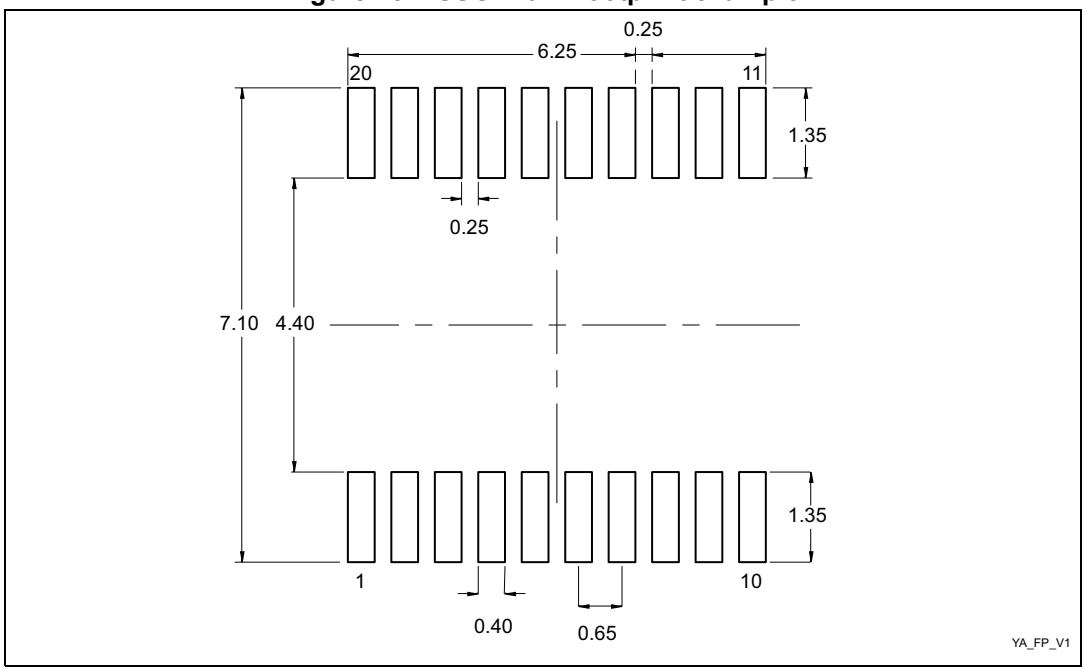
1. Drawing is not to scale.

Table 58. TSSOP20 – Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

Figure 25. TSSOP20 – Footprint example



1. Dimensions are expressed in millimeters.

7.3 LQFP48 package information (5B)

This LQFP is a 48-pin, 7 x 7 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 26. LQFP48 - Outline(15)

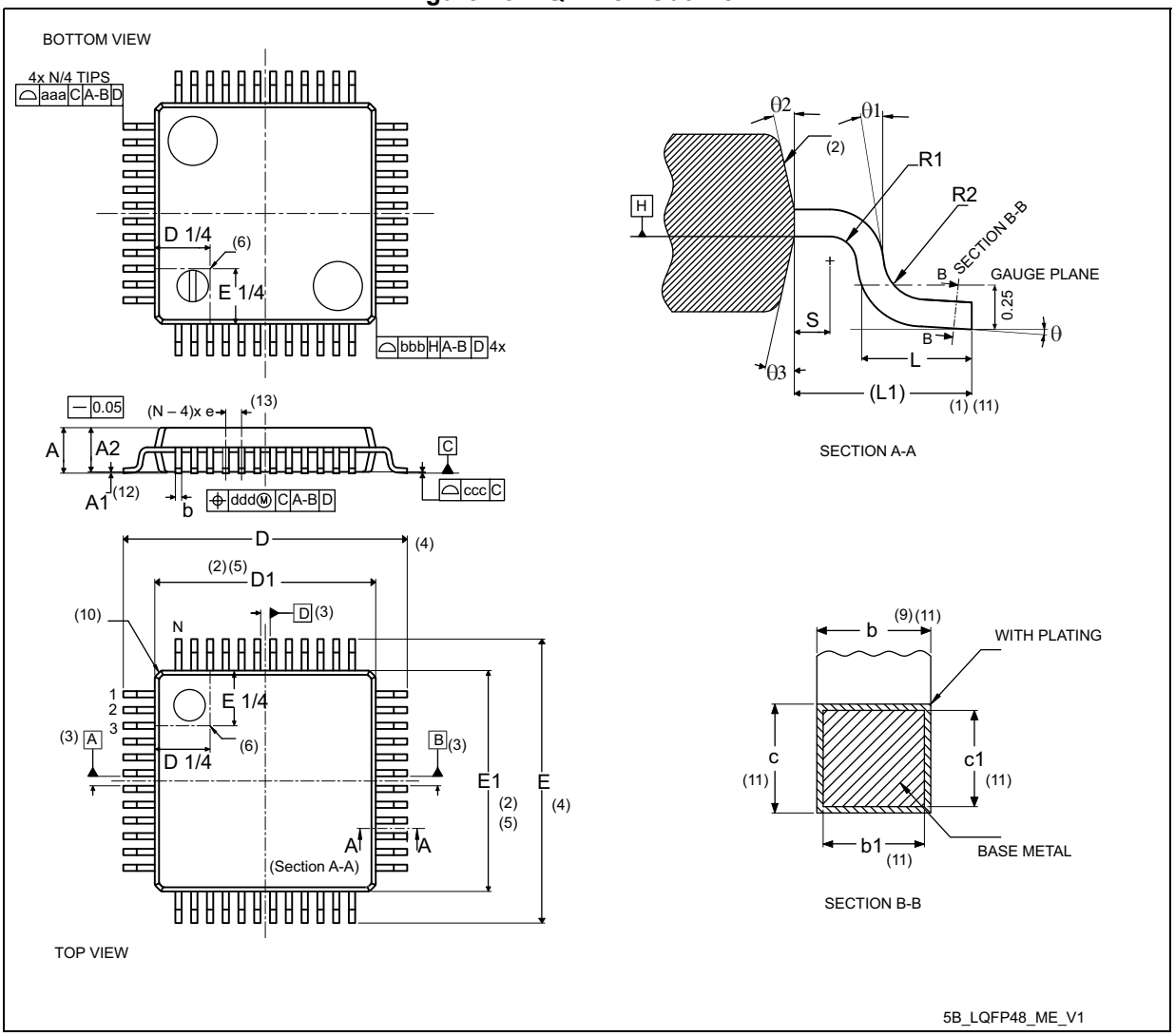


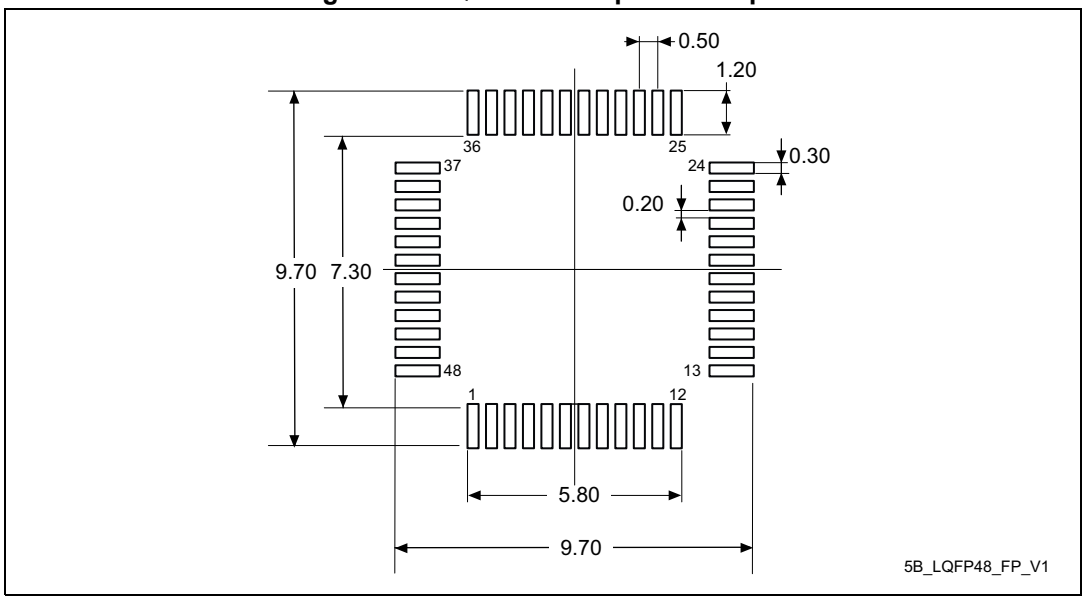
Table 59. LQFP48 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	9.00 BSC			0.3543 BSC		
D1[2][5]	7.00 BSC			0.2756 BSC		
E[4]	9.00 BSC			0.3543 BSC		
E1[2][5]	7.00 BSC			0.2756 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	48					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1][7]	0.20			0.0079		
bbb[1][7]	0.20			0.0079		
ccc[1][7]	0.08			0.0031		
ddd[1][7]	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 27. LQFP48 - Footprint example



1. Dimensions are expressed in millimeters.

7.4 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 28. LQFP64 - Outline(15)

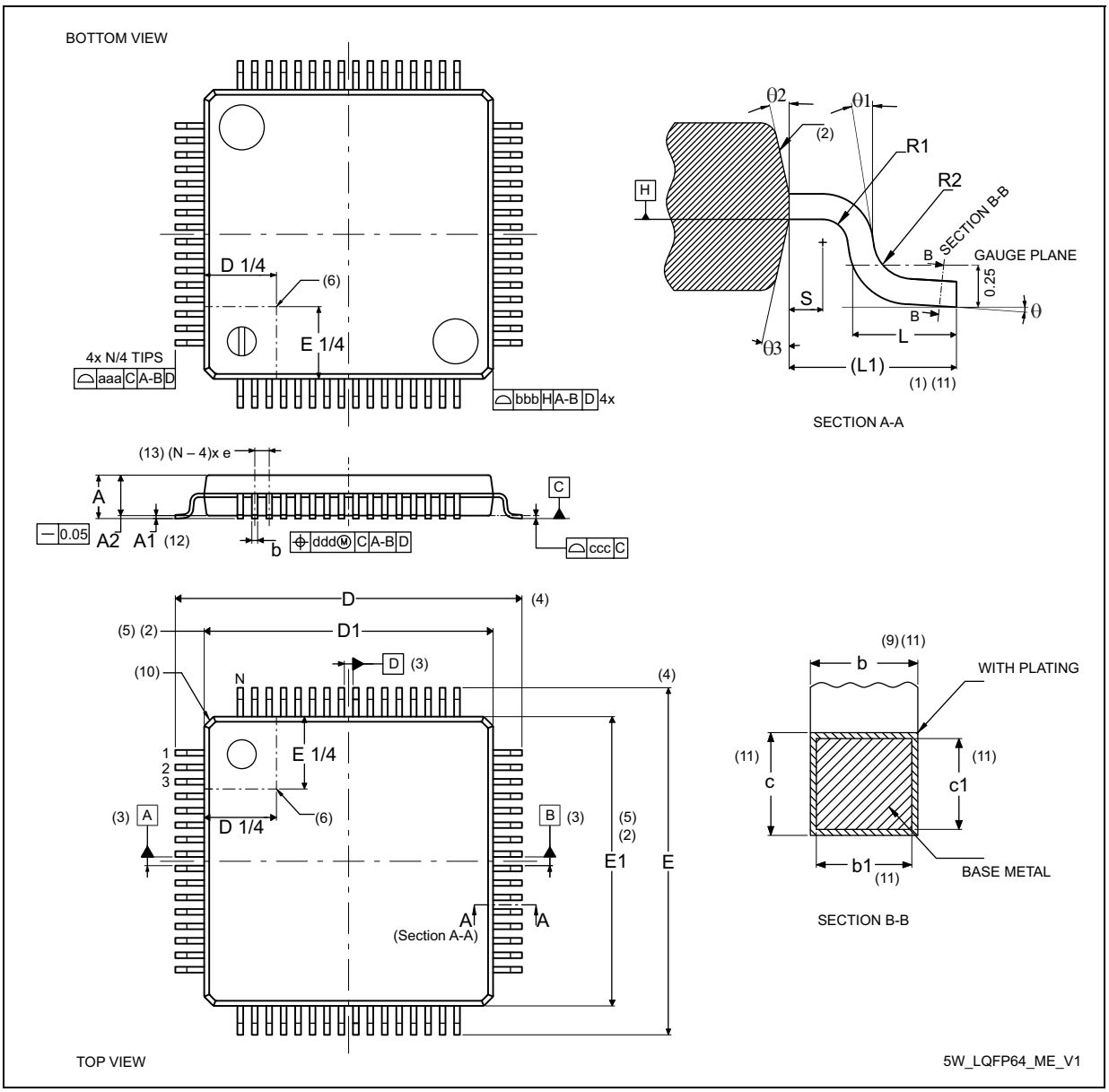


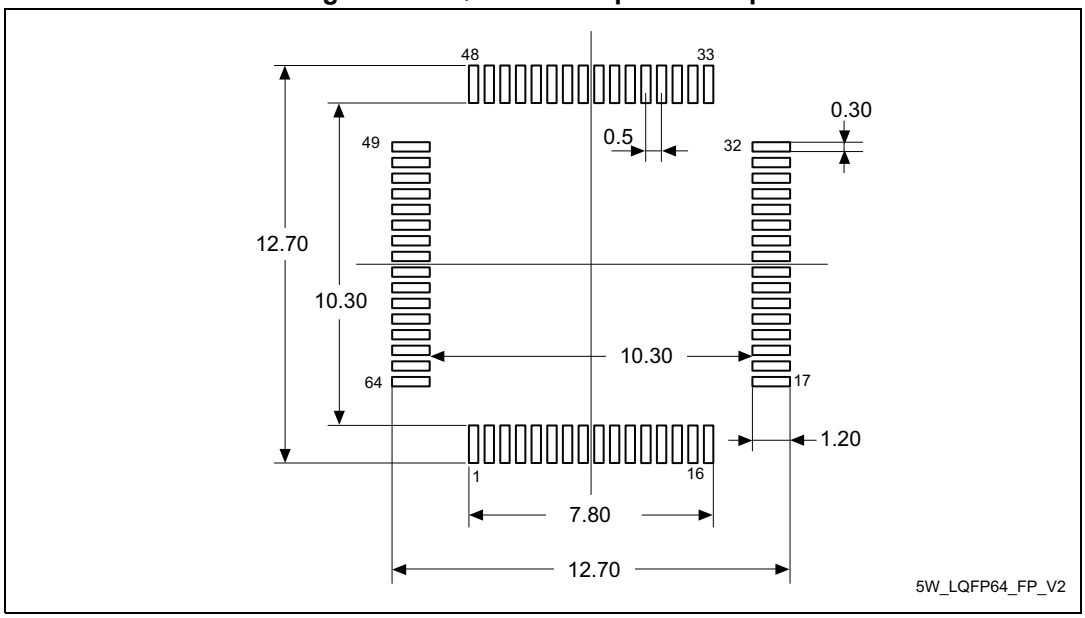
Table 60. LQFP64 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	12.00 BSC			0.4724 BSC		
D1[2][5]	10.00 BSC			0.3937 BSC		
E[4]	12.00 BSC			0.4724 BSC		
E1[2][5]	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	64					
q	0°	3.5°	7°	0°	3.5°	7°
q1	0°	-	-	0°	-	-
q2	10°	12°	14°	10°	12°	14°
q3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 29. LQFP64 - Footprint example



1. Dimensions are expressed in millimeters.

7.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 19: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 61. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_J	**Thermal resistance junction-ambient** LQFP64 - 10 mm x 10 mm	44	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 mm x 7 mm	55	
	Thermal resistance junction-ambient TSSOP20 - 6.5 mm x 6.4 mm	76	

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

8 Ordering information

Example: STM32 F 070 C 6 T 6 x

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

070 = STM32F070xx

Pin count

F = 20 pins

C = 48 pins

R = 64 pins

Code size

6 = 32 Kbyte of flash memory

B = 128 Kbyte of flash memory

Package

P = TSSOP

T = LQFP

Temperature range

6 = –40 to 85 °C

Option

xxx = programmed parts

TR = tape and reel

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on www.st.com for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

10 Revision history

Table 62. Document revision history

Date	Revision	Changes
27-Nov-2014	1	Initial release.
15-Jan-2015	2	Updated the number of SPI in *Features* and *Section: Description*. Updated *Section: Serial peripheral interface (SPI)*. Updated the fourth footnote of *Table: STM32F070xB/i pin definitions*, and added the reference to PB9 pin. Moved the AF3 data to AF4 for PA9 and PA10 pins in *Table: Alternate functions selected through GPIOA_AFR registers for port A*. Added the reference to footnote 1 to AF0 data for PB12, PB13, PB14 and PB15, and to AF5 data for PB9 and PB10 in *Table: Alternate functions selected through GPIOB_AFR registers for port B*. Added the reference to footnote 1 to SPI2 in *Table: STM32F070xB/6 peripheral register boundary addressesF070.*
07-Feb-2016	3	Updated: – Removal of Table 1 from cover page (all part numbers put in the header) – *Table 1: STM32F070CB/RB/C6/F6 family device features and peripheral counts*; number of int. ADC channels corrected – *Figure 1: Block diagram* – *Figure 2: Clock tree* – *Table 7: STM32F70x0 USART implementation* – *Figure 6: STM32F070CB/RB/C6/F6 memory map and added the note related to the start address of the system memory* – *Figure 9: Power supply scheme* – *Section 3.5.1: Power supply schemes* – *Section 3.11: Timers and watchdogs - number of complementary outputs in the table* – *Table 10: STM32F070xB/6 pin definitions - TSSOP20 pinout* correction, pins 10, 15 and 16 – *Table 22: Embedded internal reference voltage*: added tSTART, changed VREFINT and tS_vrefint values and notes – *Table 32: LSE oscillator characteristics* (fLSE = 32.768 kHz) LSEDRV[1:0] values removed (see ref. manual) – *Table 48: ADC characteristics* - tSTAB defined relative to clock frequency; notes 3. and 4. added – *Table 51*: TS characteristics: removed the min. value for t_{START}

Table 62. Document revision history (continued)

Date	Revision	Changes
07-Feb-2016	3	– *Figure 15* and *Figure 16* improved – *Section 7: Package information* name and structure change – *Section 8: Ordering information* renamed from Part numbering; removed undue code sizes
26-Apr-2024	4	– Cover image updated – Updated *Section 1: Introduction*, *Section 3.3: Boot modes*, *Section 3.4: Cyclic redundancy check calculation unit (CRC)*, *Section 4: Pinouts and pin descriptions* (packages reorder from lowest to highest pincount), *Section 7: Package information* (marking information removed, packages reordered from lowest to highest pincount, package references added) – Added *Section 9: Important security notice*