

COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D $T_A = +25^\circ\text{C}$
Q1	30V	60m Ω @ $V_{GS} = 10\text{V}$	3.4A
		100m Ω @ $V_{GS} = 4.5\text{V}$	2.7A
Q2	-30V	95m Ω @ $V_{GS} = -10\text{V}$	-2.8A
		140m Ω @ $V_{GS} = -4.5\text{V}$	-2.3A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

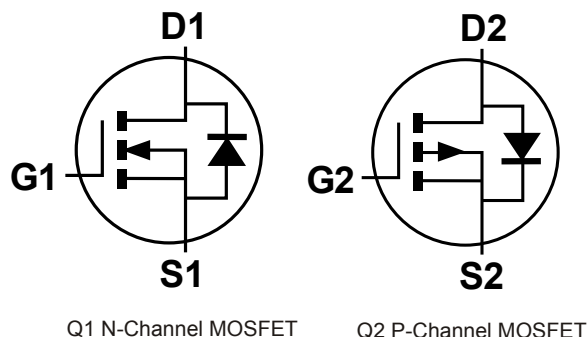
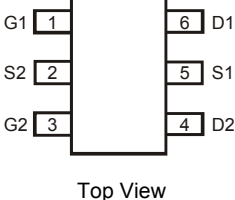
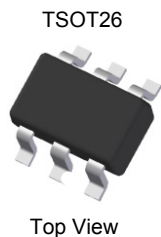
- Backlighting
- DC-DC Converters
- Power management functions

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound.
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish – Matte Tin annealed over Copper leadframe.
Solderable per MIL-STD-202, Method 208 
- Weight: 0.013 grams (approximate)

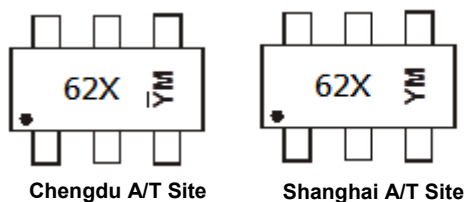


Ordering Information (Note 4)

Part Number	Case	Packaging
DMG6602SVTX-7	TSOT26	3000 / Tape & Reel
DMG6602SVTX-13	TSOT26	10000 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



62X = Product Type Marking Code
 YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 YM = Date Code Marking for CAT (Chengdu Assembly/ Test site)
 Y or Y̅ = Year (ex: A = 2013)
 M = Month (ex: 9 = September)

Date Code Key

Year	2010	2011	2012	2013	2014	2015	2016
Code	X	Y	Z	A	B	C	D

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 5) V _{GS} = 10V	Steady State	T _A = +25°C T _A = +70°C	I _D	3.4 2.7	A
Continuous Drain Current (Note 5) V _{GS} = 4.5V	Steady State	T _A = +25°C T _A = +70°C	I _D	2.7 2.2	A
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	1.5	A
Pulsed Drain Current (Note 6)			I _{DM}	13.0	A

Maximum Ratings – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	-30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 5) V _{GS} = -10V	Steady State	T _A = +25°C T _A = +70°C	I _D	-2.8 -2.4	A
Continuous Drain Current (Note 5) V _{GS} = -4.5V	Steady State	T _A = +25°C T _A = +70°C	I _D	-2.3 -2.1	A
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	-1.5	A
Pulsed Drain Current (Note 6)			I _D	-11.2	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P _D	1.0	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 5)	R _{θJA}	124	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	0.5	1.2	1.8	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	35	60	mΩ	V _{GS} = 10V, I _D = 3.1A
			50	100		V _{GS} = 4.5V, I _D = 2A
			100	200		V _{GS} = 3.3V, I _D = 1.5A
Forward Transfer Admittance	Y _{fs}	—	4	—	S	V _{DS} = 5V, I _D = 3.1A
Diode Forward Voltage	V _{SD}	—	0.8	1	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	234	—	pF	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	42	—		
Reverse Transfer Capacitance	C _{rss}	—	40	—		
Gate Resistance	R _g	—	1.45	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	3.6	—	nC	V _{DS} = 15V, V _{GS} = 4.5V, I _D = 3A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	7.3	—		
Gate-Source Charge	Q _{gs}	—	0.9	—		V _{DS} = 15V, V _{GS} = 10V, I _D = 3A
Gate-Drain Charge	Q _{gd}	—	1.6	—		
Turn-On Delay Time	t _{D(on)}	—	3.6	—	ns	V _{GS} = 10V, V _{DS} = 15V, R _G = 3Ω, R _L = 1.7Ω
Turn-On Rise Time	t _r	—	2.5	—		
Turn-Off Delay Time	t _{D(off)}	—	16	—		
Turn-Off Fall Time	t _f	—	6	—		

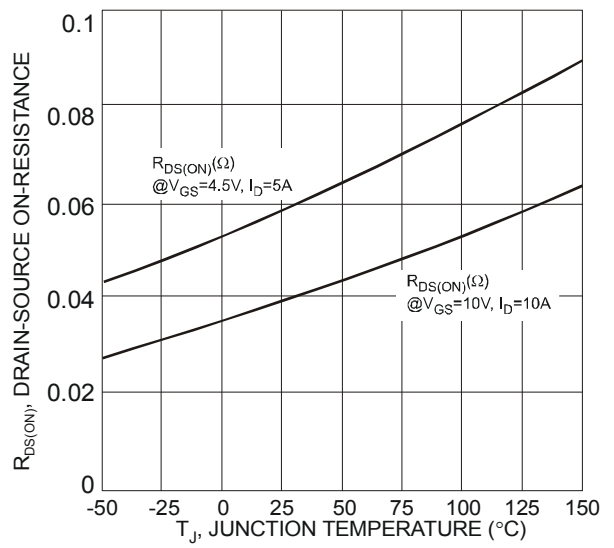
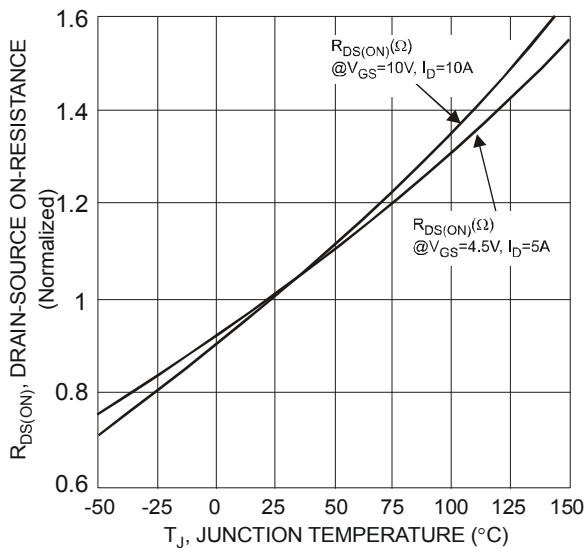
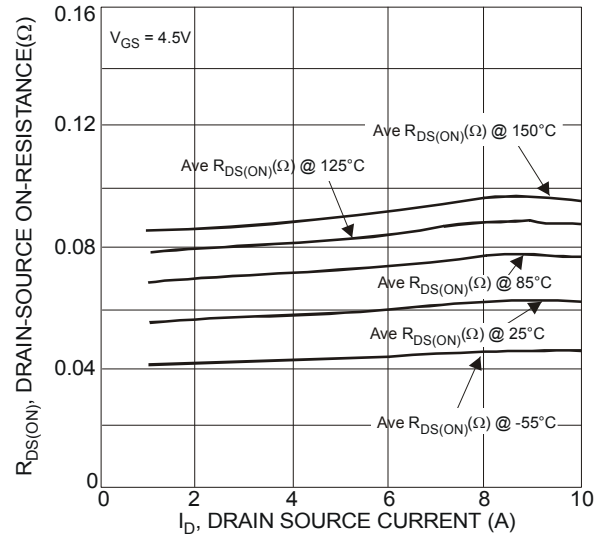
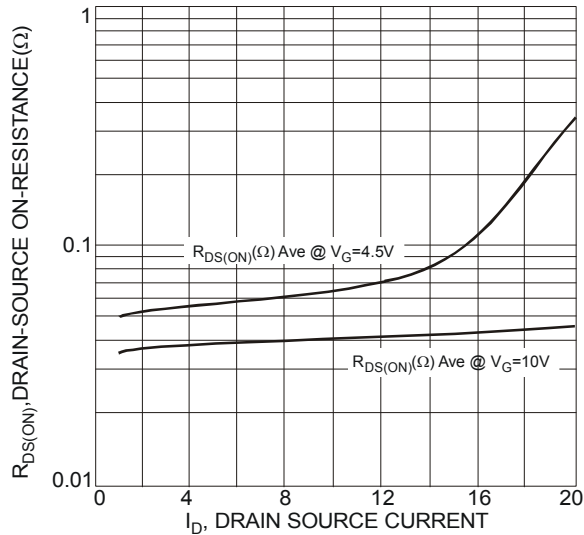
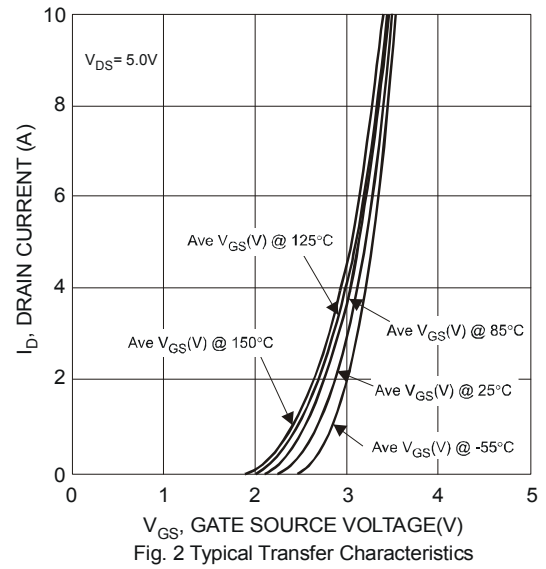
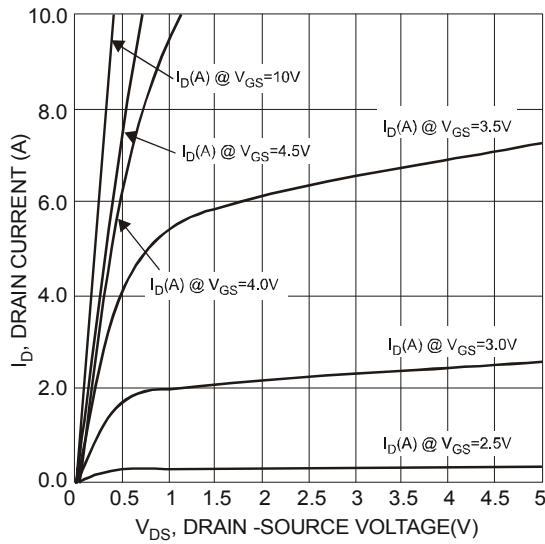
- Notes:
- Device mounted on FR-4 with minimum recommended pad layout, single sided.
 - Repetitive rating, pulse width limited by junction temperature.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

Electrical Characteristics – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-1.0	μA	V _{DS} = -24V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	-0.5	-1.5	-2.2	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	75	95	mΩ	V _{GS} = -10V, I _D = -2.7A
			105	140		V _{GS} = -4.5V, I _D = -2A
			140	200		V _{GS} = -3.3V, I _D = -1.5A
Forward Transfer Admittance	Y _{fs}	—	6	—	S	V _{DS} = -5V, I _D = -2.7A
Diode Forward Voltage	V _{SD}	—	-0.8	-1.0	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	410	—	pF	V _{DS} = -15V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	50	—		
Reverse Transfer Capacitance	C _{rss}	—	45	—		
Gate Resistance	R _g	—	6.2	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = -4.5V)	Q _g	—	3.7	—	nC	V _{DS} = -15V, V _{GS} = -4.5V, I _D = -3A
Total Gate Charge (V _{GS} = -10V)	Q _g	—	7.8	—		
Gate-Source Charge	Q _{gs}	—	1.1	—		
Gate-Drain Charge	Q _{gd}	—	1.3	—		
Turn-On Delay Time	t _{D(on)}	—	3.3	—	ns	V _{GS} = -10V, V _{DS} = -15V, R _G = 6Ω, R _L = 15Ω
Turn-On Rise Time	t _r	—	3.0	—		
Turn-Off Delay Time	t _{D(off)}	—	14	—		
Turn-Off Fall Time	t _f	—	6.8	—		

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

Q1 N-CHANNEL



Q1 N-CHANNEL

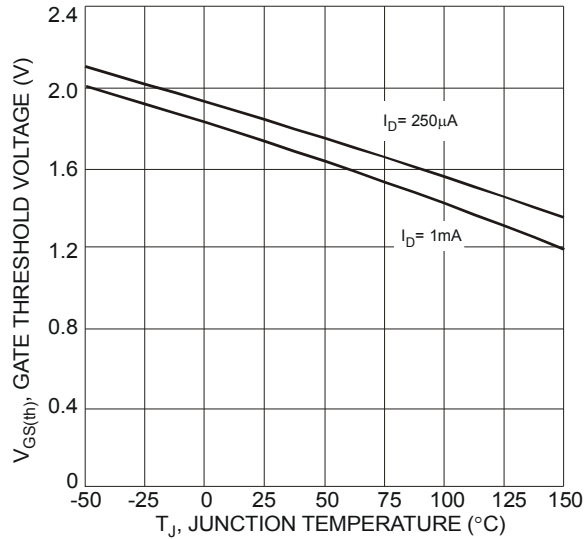


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

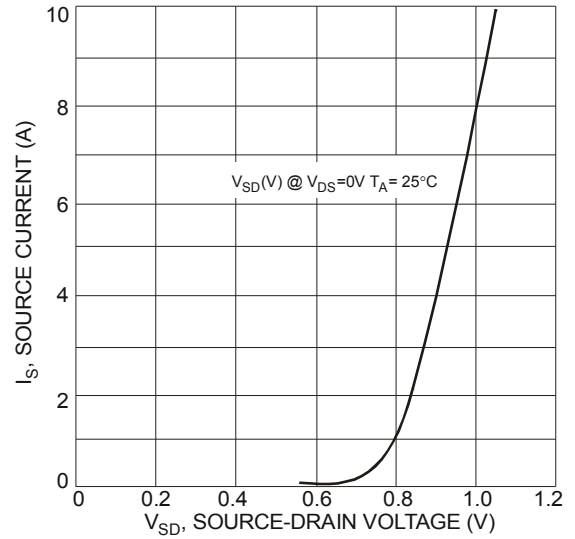


Fig. 8 Diode Forward Voltage vs. Current

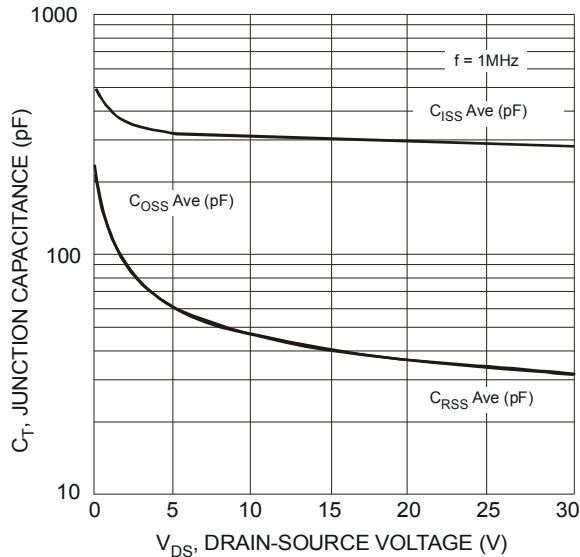


Fig. 9 Typical Junction Capacitance

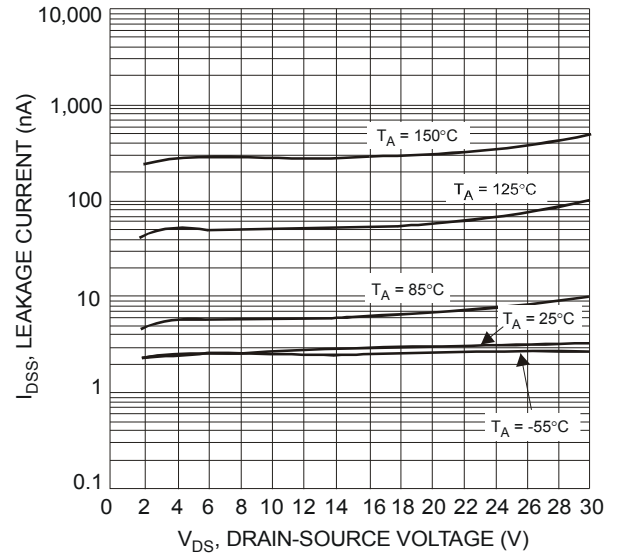


Fig. 10 Typical Drain-Source Leakage Current vs. Voltage

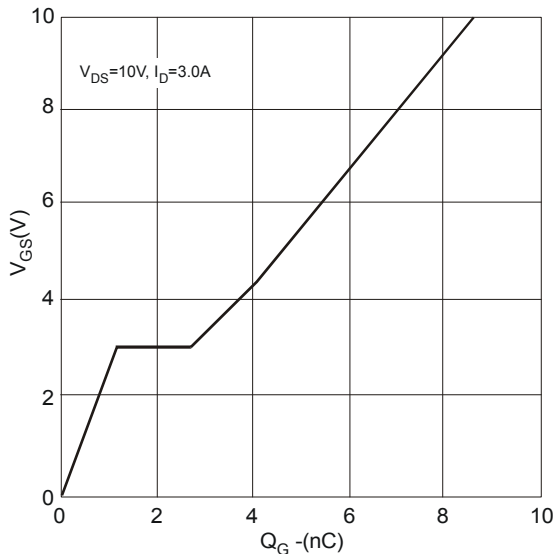


Fig. 11 Gate Charge Characteristics

Q2 P-CHANNEL

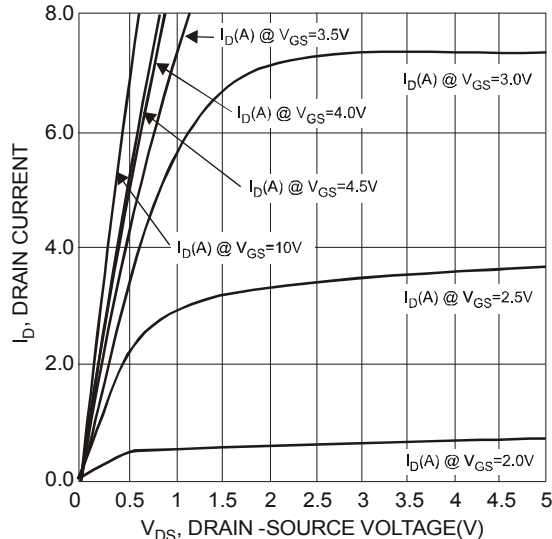


Fig. 12 Typical Output Characteristics

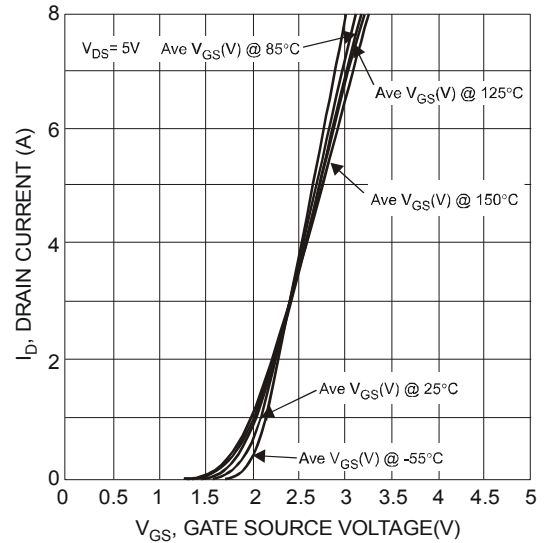


Fig. 13 Typical Transfer Characteristics

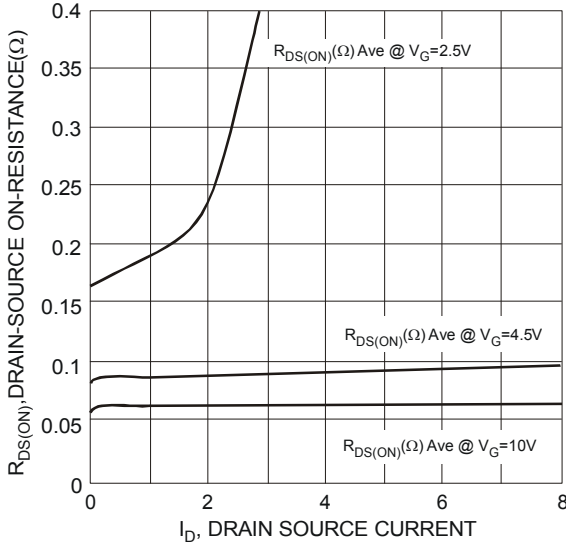


Fig. 14 Typical On-Resistance vs. Drain Current and Gate Voltage

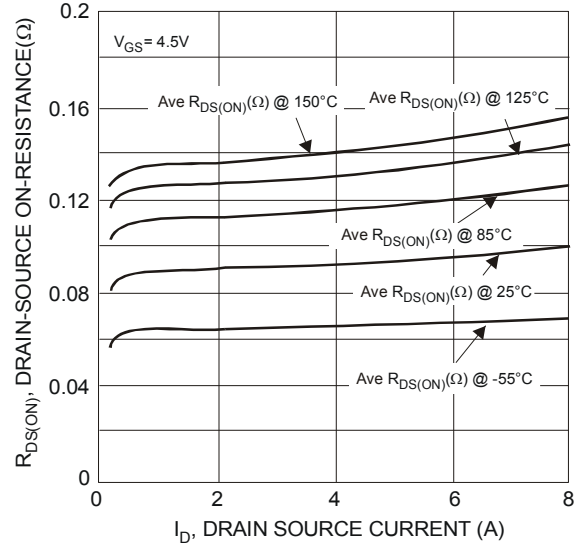


Fig. 15 Typical On-Resistance vs. Drain Current and Temperature

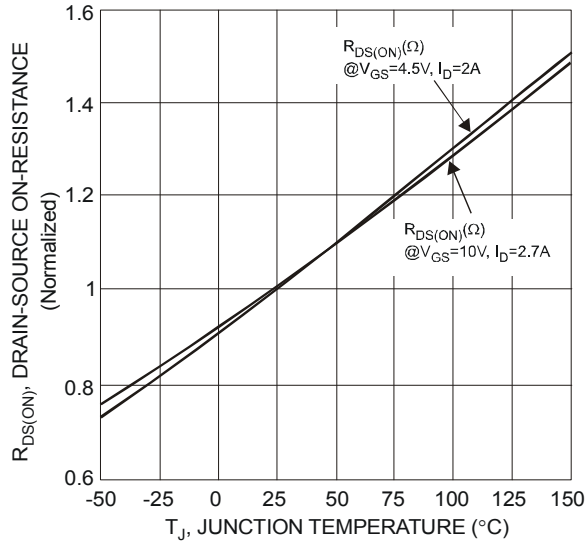


Fig. 16 On-Resistance Variation with Temperature

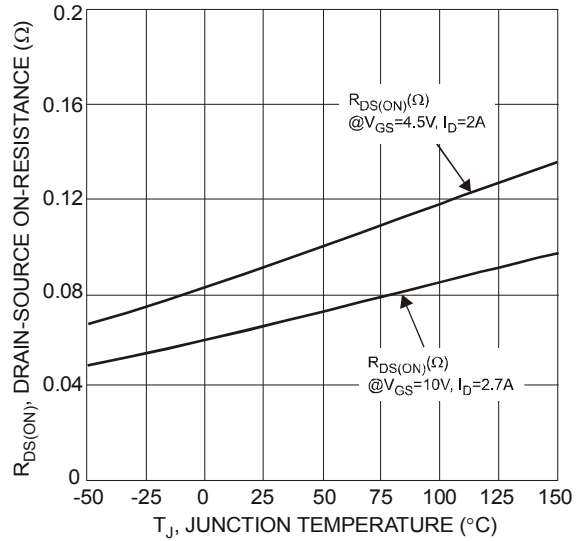


Fig. 17 On-Resistance Variation with Temperature

Q2 P-CHANNEL

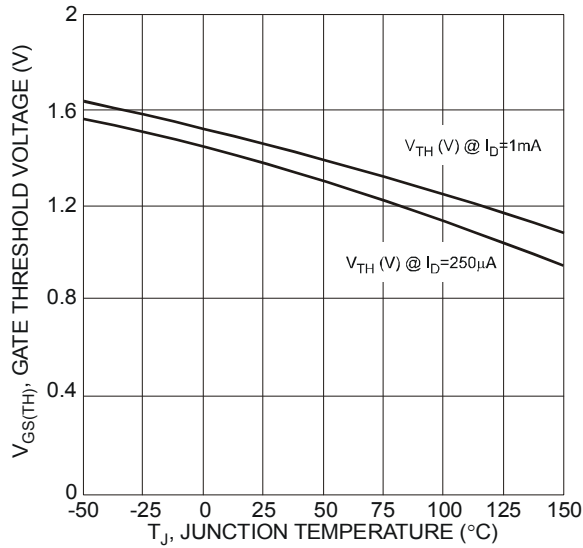


Fig. 18 Gate Threshold Variation vs. Ambient Temperature

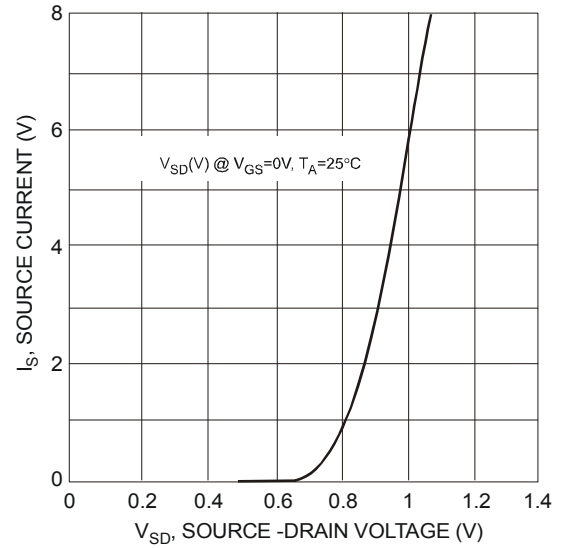


Fig. 19 Diode Forward Voltage vs. Current

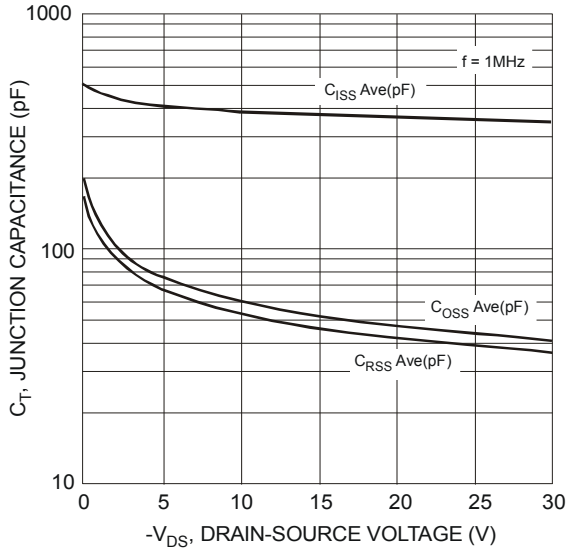


Fig. 20 Typical Junction Capacitance

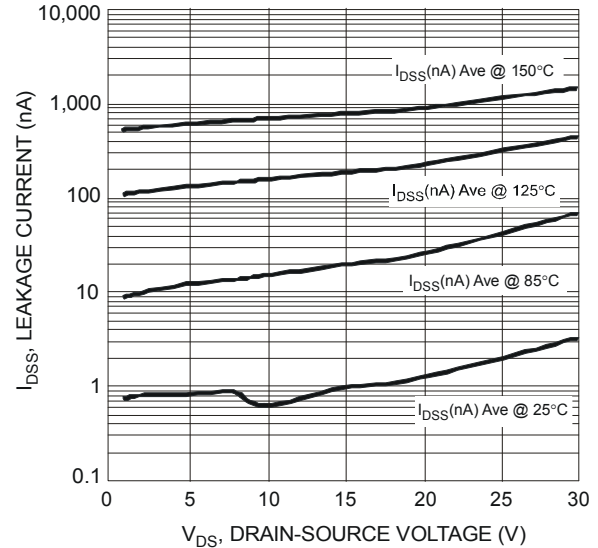


Fig. 21 Typical Drain-Source Leakage Current vs. Voltage

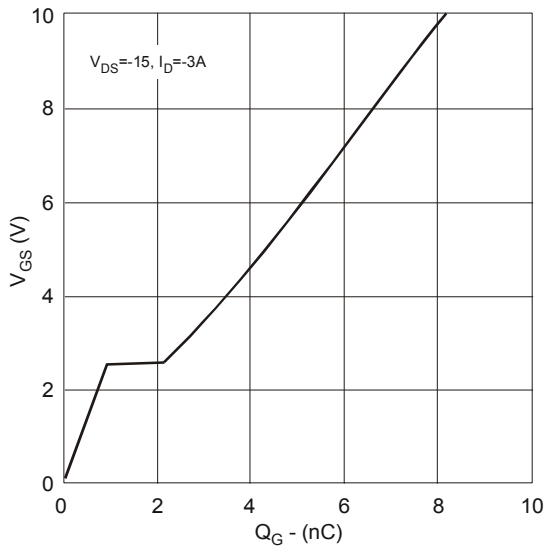
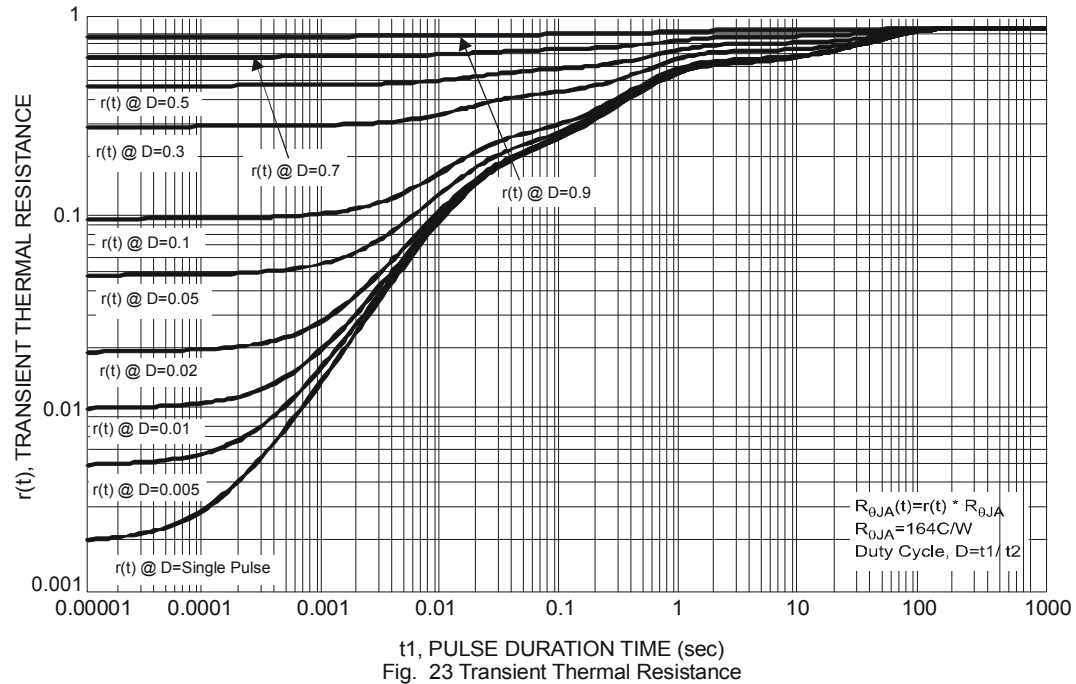
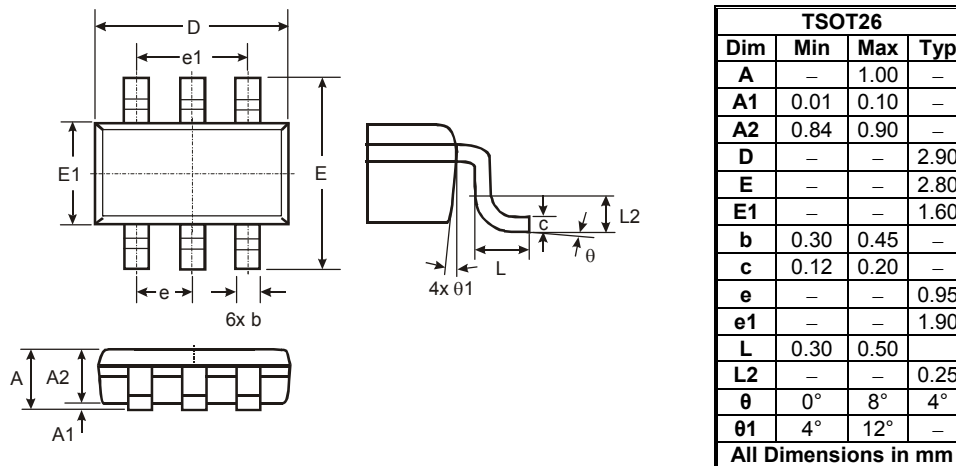


Fig. 22 Gate Charge Characteristics



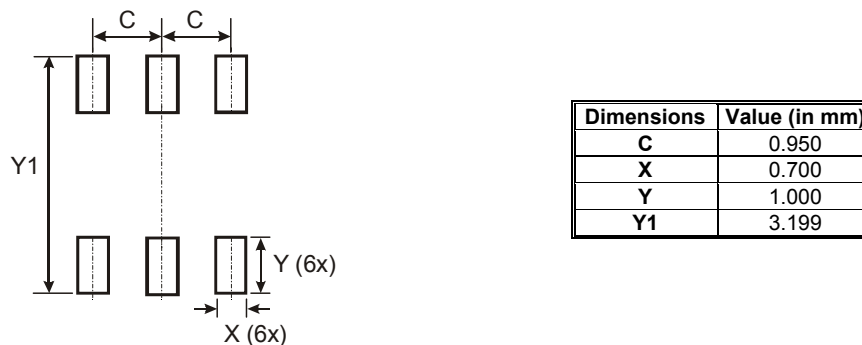
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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