

MOSFET – N-Channel, POWER TRENCH[®], Ultra Thin, 1.5 V

20 V, 9.5 A, 23 mΩ

FDMA410NZT

Description

This Single N-Channel MOSFET has been designed using onsemi's advanced Power Trench process to optimize the $R_{DS(on)}$ @ $V_{GS} = 1.5$ V on special MicroFET™ leadframe.

This design is similar to the FDMA410NZ, however it features our new advanced 0.55 mm max 2 x 2 MLP package technology.

Features

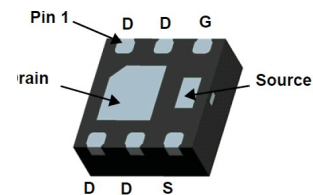
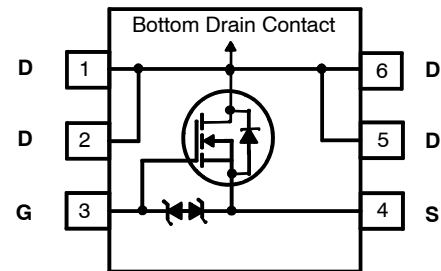
- 0.55 mm max package height MicroFET 2 x 2 mm Package
- Max $R_{DS(on)} = 23$ mΩ at $V_{GS} = 4.5$ V, $I_D = 9.5$ A
- Max $R_{DS(on)} = 29$ mΩ at $V_{GS} = 2.5$ V, $I_D = 8.0$ A
- Max $R_{DS(on)} = 36$ mΩ at $V_{GS} = 1.8$ V, $I_D = 4.0$ A
- Max $R_{DS(on)} = 60$ mΩ at $V_{GS} = 1.5$ V, $I_D = 2.0$ A
- HBM ESD protection level > 1.5 kV (Note 3)
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion
- Mobile Device Switching

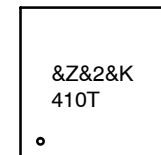
V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
20 V	23 mΩ @ 4.5 V	9.5 A

Ultra Thin N-Channel



UDFN6 2.05x2.05 0.65P
(MicroFET)
CASE 517DT

MARKING DIAGRAM



&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
410T	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMA410NZT

MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V _{DS}	Drain to Source Voltage	20	V
V _{GS}	Gate to Source Voltage	±8	V
I _D	–Continuous, T _A = 25°C (Note 1a)	9.5	A
	–Pulsed (Note 4)	63	
P _D	Power Dissipation, T _A = 25°C (Note 1a)	2.4	W
	Power Dissipation, T _A = 25°C (Note 1b)	0.9	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1b)	145	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping (Qty / Packing) [†]	Pin 1 Orientation
410T	FDMA410NZT	MicroFET 2x2	3000 / Tape & Reel	Top left
410T	FDMA410NZT–F130	MicroFET 2x2	3000 / Tape & Reel	Top right

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	15	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±8 V, V _{DS} = 0 V	–	–	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	0.4	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–3	–	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 4.5 V, I _D = 9.5 A	–	14	23	mΩ
		V _{GS} = 2.5 V, I _D = 8.0 A	–	18	29	
		V _{GS} = 1.8 V, I _D = 4.0 A	–	25	36	
		V _{GS} = 1.5 V, I _D = 2.0 A	–	35	60	
		V _{GS} = 4.5 V, I _D = 9.5 A, T _J = 125°C	–	21	32	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 9.5 A	–	36	–	S

FDMA410NZT

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	–	935	1310	pF
C _{oss}	Output Capacitance		–	122	170	pF
C _{rss}	Reverse Transfer Capacitance		–	84	118	pF
R _g	Gate Resistance	f = 1 MHz	0.1	1.4	3.0	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-on Delay Time	V _{DD} = 10 V, I _D = 9.5 A, V _{GS} = 4.5 V, R _{GEN} = 6 Ω	–	8.5	17	ns
t _r	Rise Time		–	3.0	10	
t _{d(off)}	Turn-off Delay Time		–	27	44	
t _f	Fall Time		–	3.3	10	
Q _g	Total Gate Charge	V _{GS} = 4.5 V, V _{DD} = 10 V, I _D = 9.5 A	–	10	14	nC
Q _{gs}	Gate to Source Charge		–	1.2	–	
Q _{gd}	Gate to Drain “Miller” Charge		–	2.0	–	

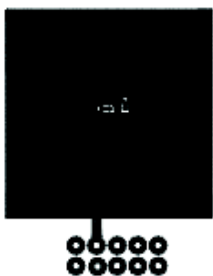
DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	2.0	A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2 A (Note 2)	–	0.7	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 9.5 A, di/dt = 100 A/μs	–	16	30	ns
Q _{rr}	Reverse Recovery Charge		–	4.5	10	nC

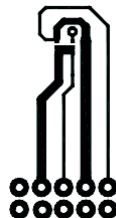
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R_{θJA} is determined by the user's board design.



- a) 52°C/W when mounted on a 1 in² pad of 2 oz copper.



- b) 145°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. Pulsed I_d please refer to Figure 11 SOA curve for more details.

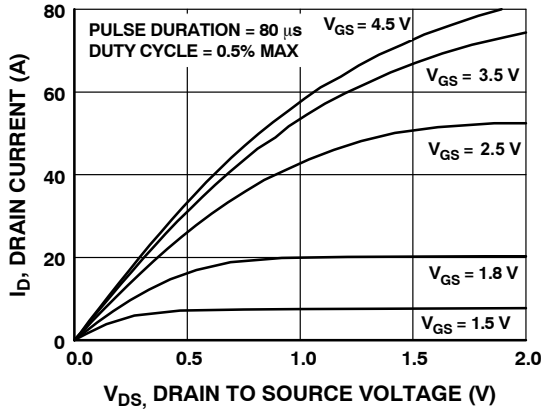
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Figure 1. On Region Characteristics

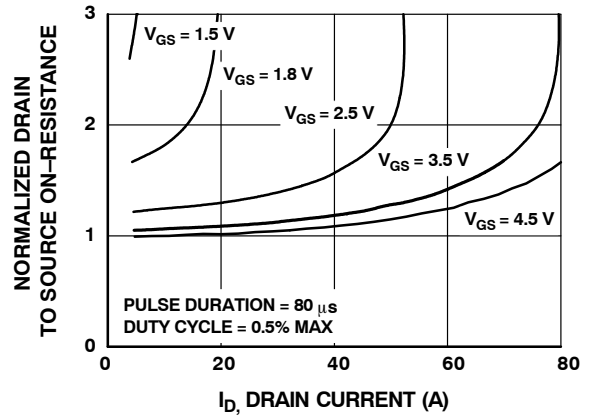


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

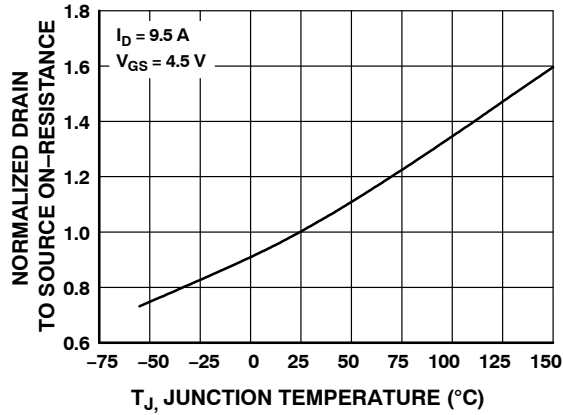


Figure 3. Normalized On Resistance vs. Junction Temperature

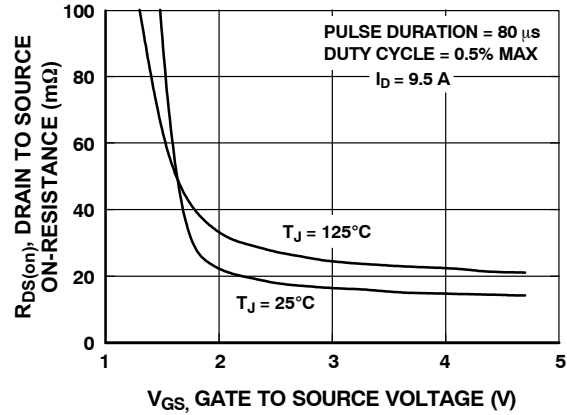


Figure 4. On-Resistance vs. Gate to Source Voltage

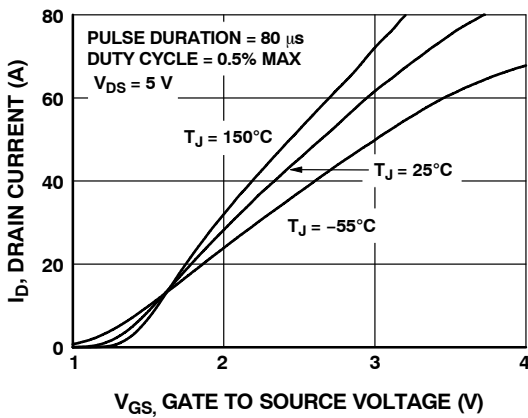


Figure 5. Transfer Characteristics

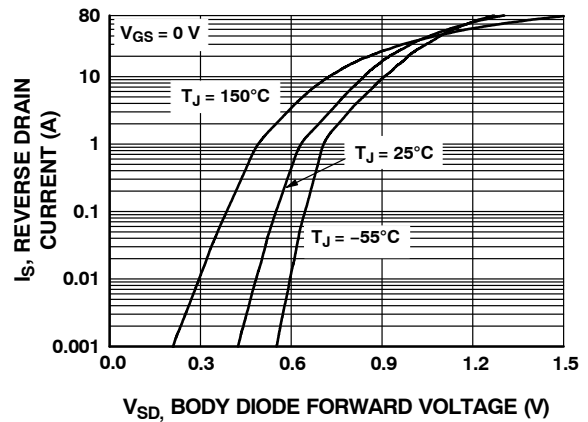


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

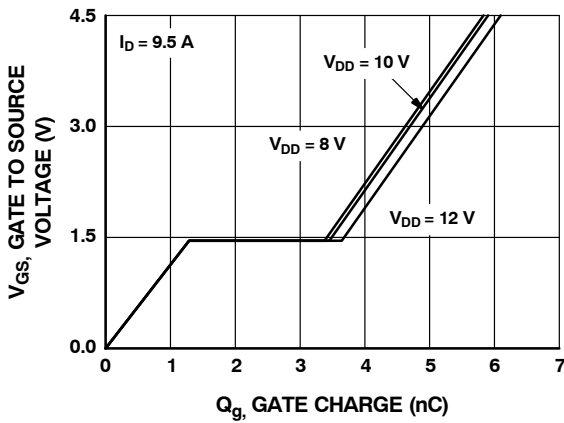


Figure 7. Gate Charge Characteristics

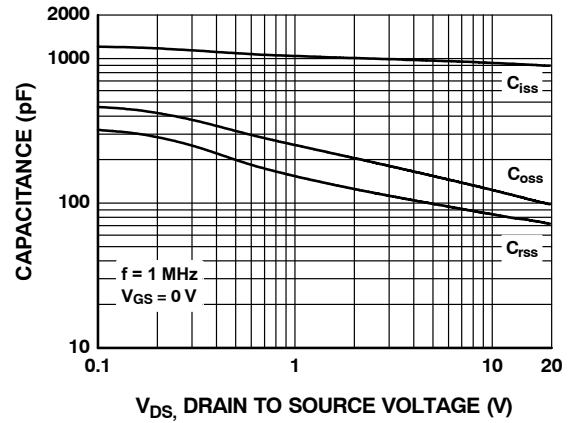


Figure 8. Capacitance vs. Drain to Source Voltage

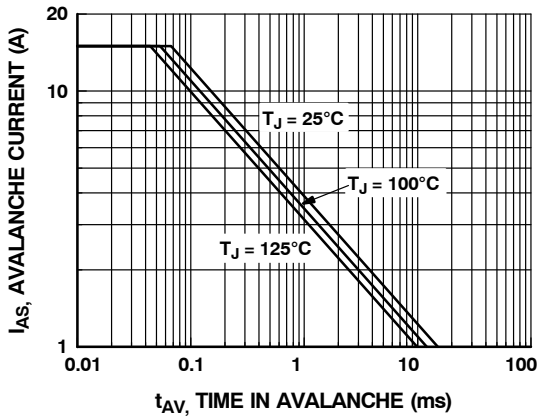


Figure 9. Unclamped Inductive Switching Capability

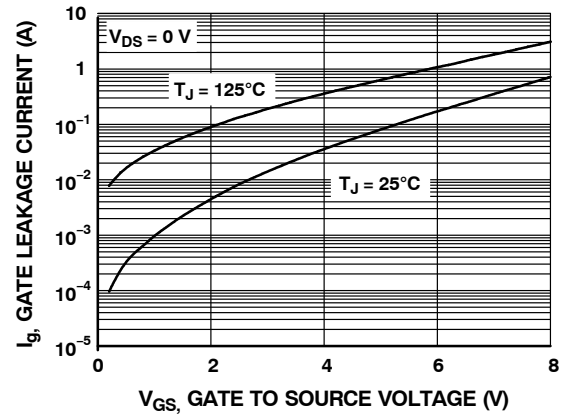


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

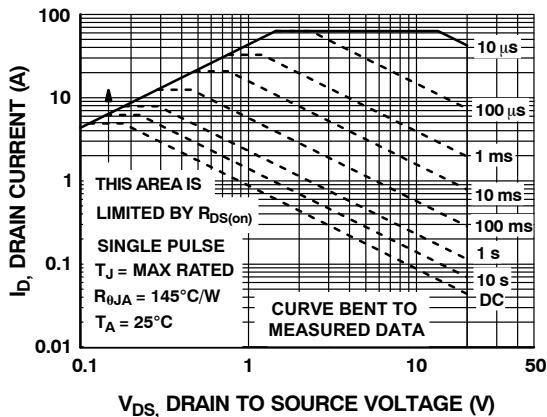


Figure 11. Forward Bias Safe Operating Area

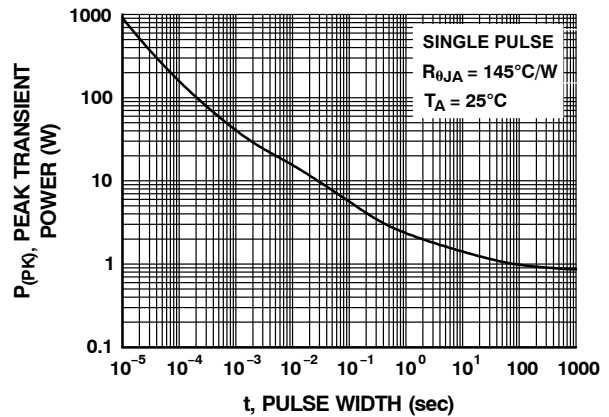


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

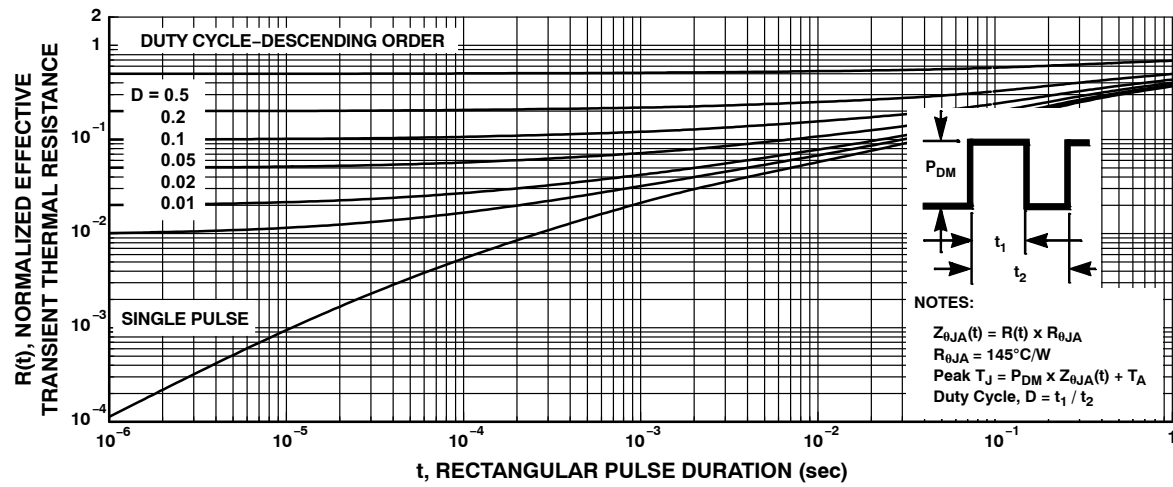
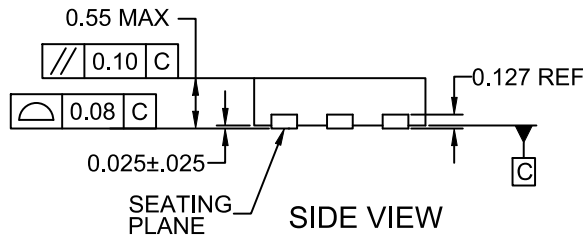
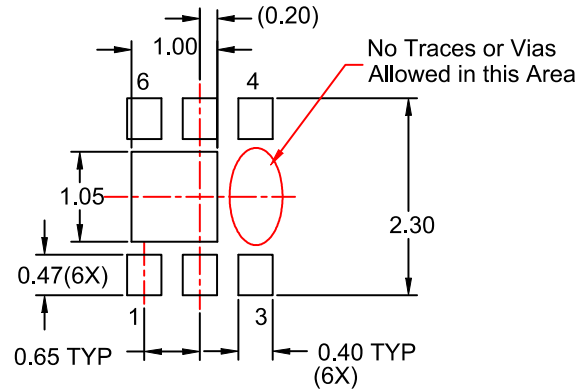
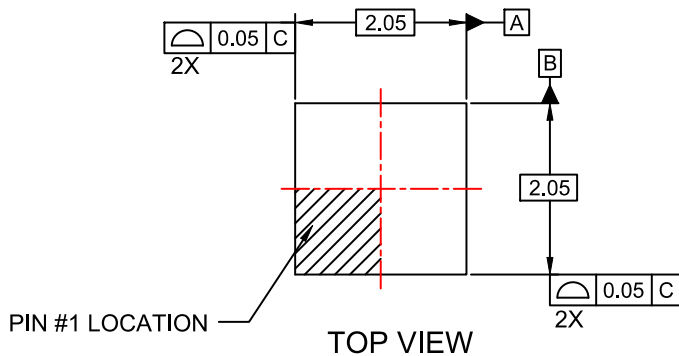


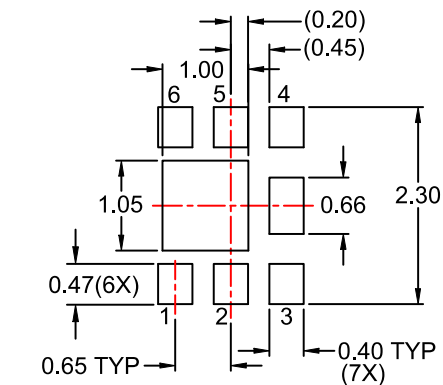
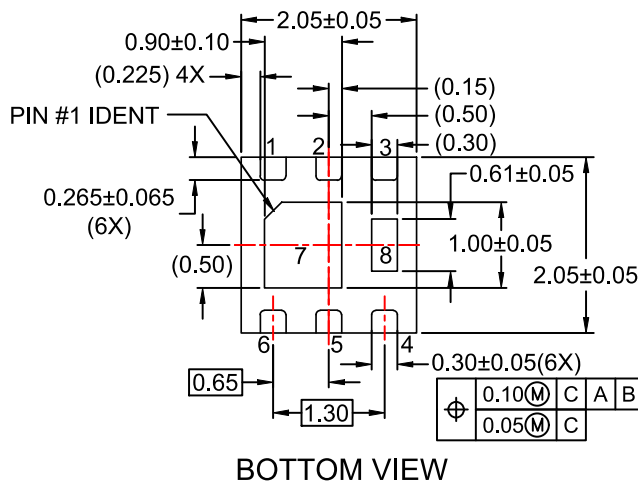
Figure 13. Junction-to-Case Transient Thermal Response Curve

UDFN6 2.05x2.05, 0.65P
CASE 517DT
ISSUE O

DATE 31 OCT 2016



RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

NOTES:

- A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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