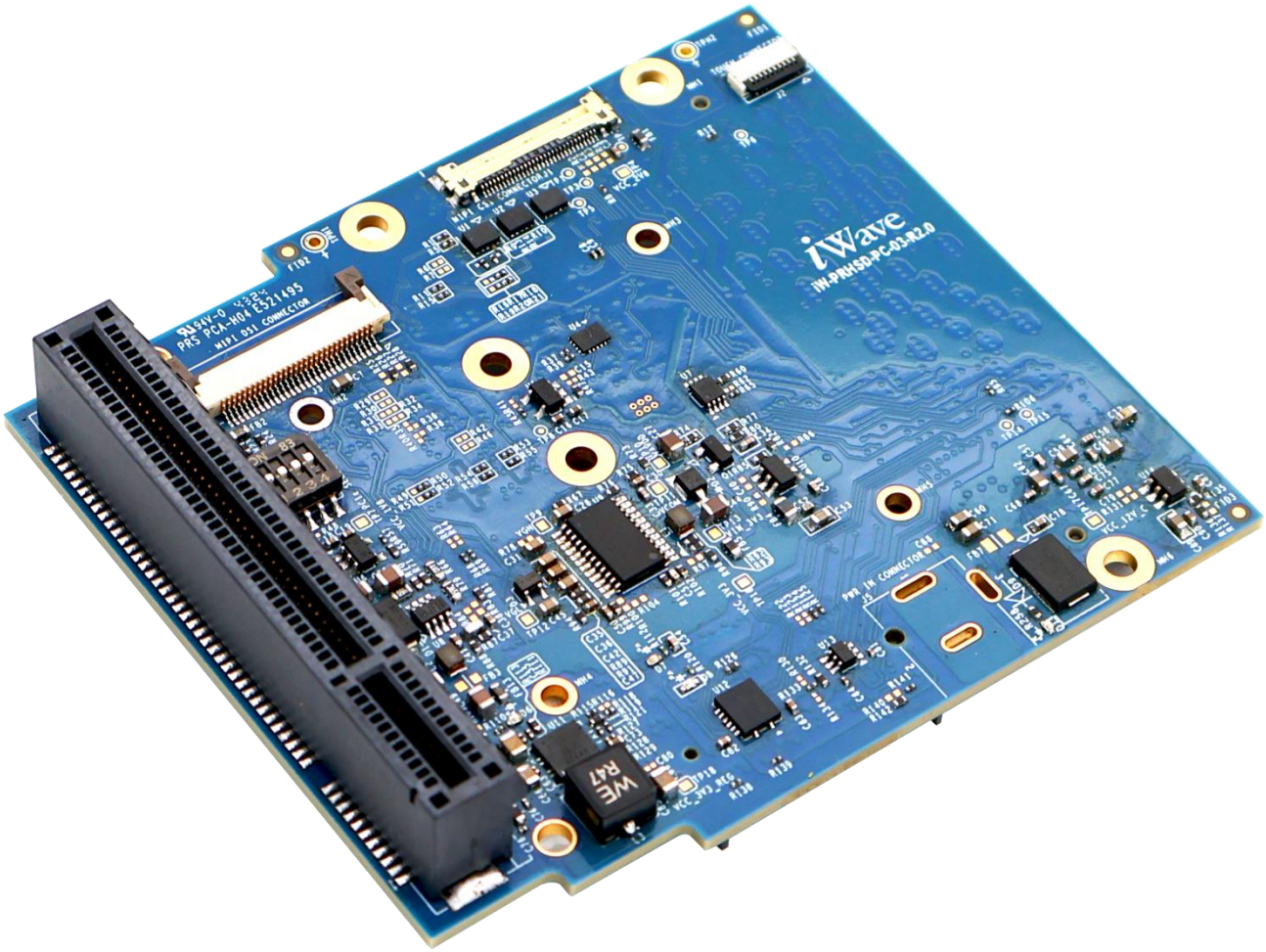
PCIe Gen4/Gen3/Gen2/Gen1 x8 FMC Module Datasheet



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1. INTRODUCTION

1.1 Purpose

This datasheet provides comprehensive technical details for the **PCIe Gen4 x8 FMC Module**, a robust and versatile solution designed and supported by iWave Global. It encompasses information on hardware specifications, software capabilities, and mechanical dimensions, enabling seamless integration into diverse embedded and industrial applications.

1.2 Overview

The PCIe Gen4 x8 FMC Module can be used for quick validation for PCIe Gen4/Gen3/Gen2/Gen1 x8 Root port & End point. Also, this module supports M.2 NVMe PCIe connector, MIPI CSI & MIPI DSI connector.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor Signal
CSI	Camera Serial Interface
DSI	Display Serial Interface
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
HPC	High Pin Count
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
Mbps	Megabits per sec
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
NC	No Connect
NVMe	Non-Volatile Memory Express
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
RX	Receiver
SOM	System On Module
TX	Transmitter
TXVR	Transceiver

Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
Analog	Analog Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
I	Input Signal
IO	Bidirectional Input/output Signal
NA	Not Applicable
NC	Not Connected
O	Output Signal
OC	Open Collector Signal
OD	Open Drain Signal
PD	Pull Down
Power	Power Pin
PU	Pull Up

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.4 References

- Vita 57.1 FMC Specification
- Vita57.4 FMC+ Specification

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the PCIe Gen4 x8 FMC Module features with high level block diagram and detailed information about each block.

2.1 PCIe Gen4 x8 FMC Module Block Diagram

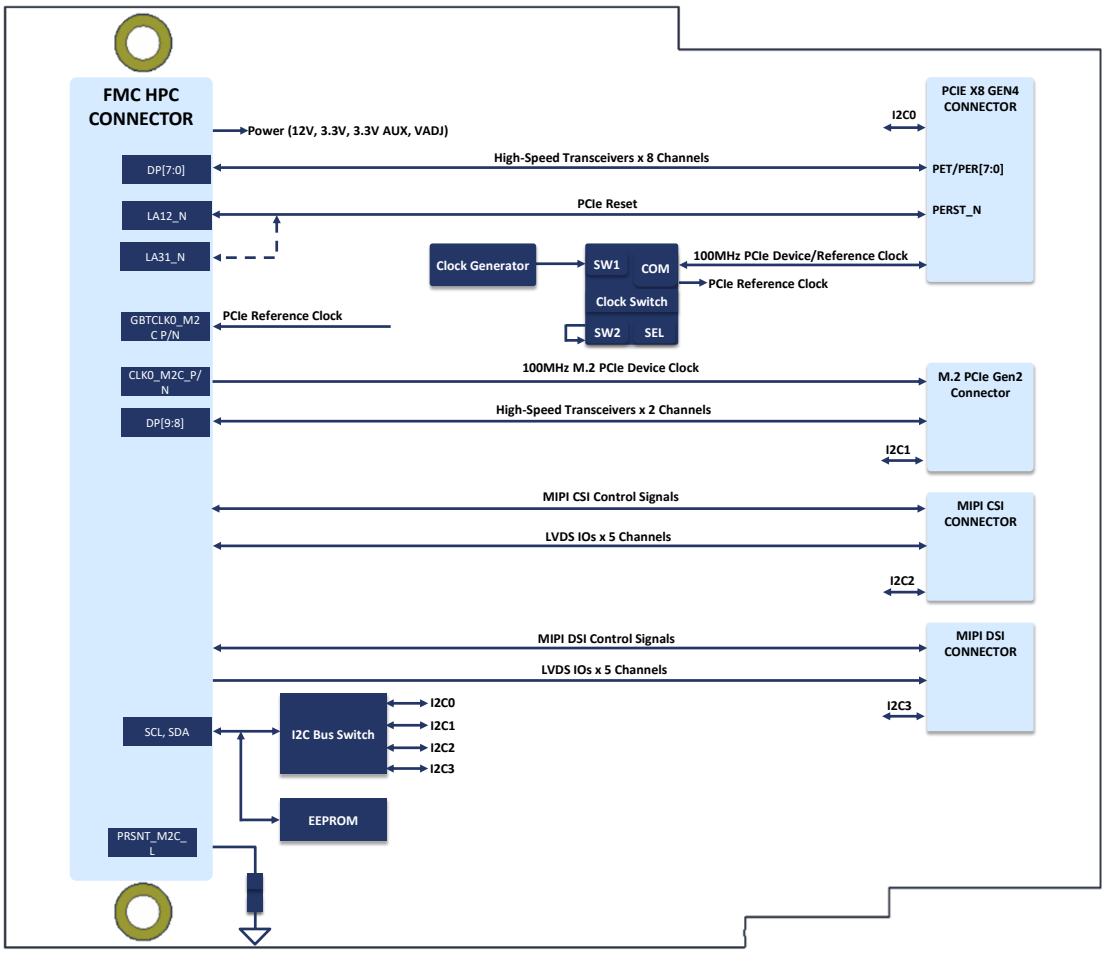

Figure 1: PCIe Gen4 x8 FMC Module Block Diagram

2.2 PCIe Gen4 x8 FMC Module Features

The PCIe Gen4 x8 FMC Module supports the following features through ANSI/VITA 57.1 FMC Connector.

- FMC VITA 57.1 HPC Connector
- PCIe Gen4/Gen3/Gen2/Gen1 x8 Connector
- M.2 Key-M NVMe PCIe Connector
- MIPI CSI Connector
- MIPI DSI Connector
- Touch Connector
- 32Kb EEPROM
- Compatible with FMC+ HSPC Connector

Additional Features

- On-Board PCIe Clock Oscillator and switch to support PCIe Root Port and Endpoint
- 4 Port I2C Bus Switch

General Specification

- 12V, 3.3V, VADJ, 3.3AUX Power: From FMC connector
- Optional 12V Power Jack
- Form Factor: 78.5mm X 69mm

2.3 FMC HPC Connector

The PCIe Gen4 x8 FMC module supports one 400-pin standard FMC VITA 57.1 HPC connector, with 10 High-Speed Transceiver Channels, 22 Differential Signals and 17 Single-Ended Signals, making it capable of handling high-speed serialized signals and suitable for on-module interfaces.

Note: *The PCIe Gen4 x8 FMC module comes with VITA 57.4 FMC+ form factor, which can also support FMC+ HSPC connector.*

This 400Pin FMC HPC Connector (J6) is physically located at the bottom of the module as shown below.

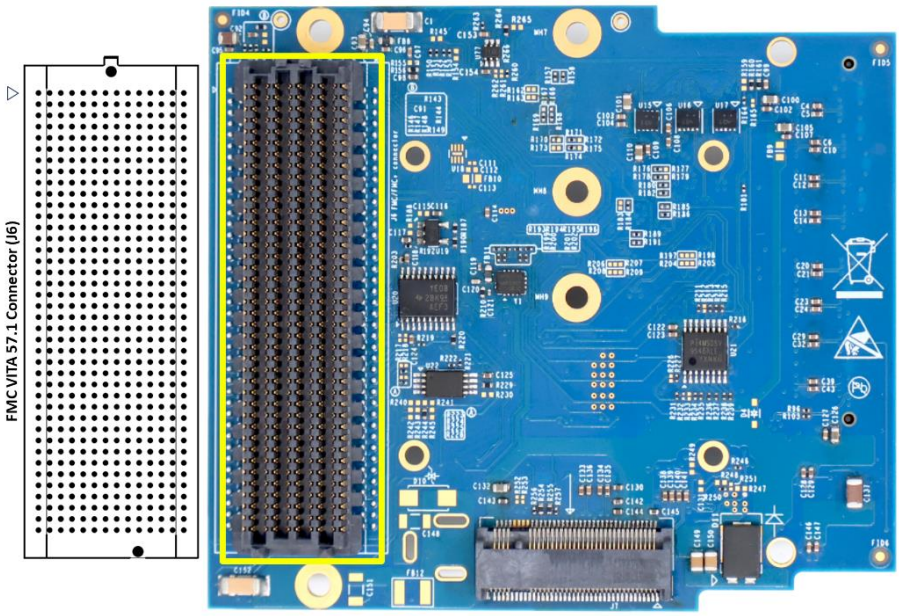

Figure 2: FMC HPC Connector

FMC HPC connector (J6) pin mapping is shown below.

	K	J	H	G	F	E	D	C	B	A
1	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	NC	PRSNT_M2C_L	NC	GND	NC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	NC	GND	NC	GND	NC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	NC	GND	NC	GND	NC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	NC	GND	NC	GND	NC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	NC	GND	LA00_P_CC	GND	NC	GND	DP0_M2C_P	GND	DP2_M2C_P
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	GND	DP2_M2C_N
8	NC	GND	LA02_N	GND	NC	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	NC	GND	LA03_P	GND	NC	LA01_N_CC	GND	DP8_M2C_N	GND
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	GND	DP3_M2C_P
11	NC	GND	LA04_N	GND	NC	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	NC	GND	LA08_P	GND	NC	LA05_N	GND	DP7_M2C_P	GND
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	DP7_M2C_N	GND
14	NC	GND	LA07_N	GND	NC	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	NC	GND	LA12_P	GND	NC	LA09_N	LA10_N	GND	DP4_M2C_N
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	DP6_M2C_P	GND
17	NC	GND	LA11_N	GND	NC	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	NC	GND	LA16_P	GND	NC	LA13_N	LA14_P	GND	DP5_M2C_P
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	GND	DP5_M2C_N
20	NC	GND	LA15_N	GND	NC	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	NC	GND	LA20_P	GND	NC	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	GND	DP1_C2M_P
23	NC	GND	LA19_N	GND	NC	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	NC	GND	LA22_P	GND	NC	LA23_N	GND	DP9_C2M_P	GND
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	DP9_C2M_N	GND
26	NC	GND	LA21_N	GND	NC	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	NC	GND	LA25_P	GND	NC	LA26_N	LA27_N	GND	DP2_C2M_N
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	DP8_C2M_P	GND
29	NC	GND	LA24_N	GND	NC	GND	TCK	GND	DP8_C2M_N	GND
30	GND	NC	GND	LA29_P	GND	NC	TDI	SCL	GND	DP3_C2M_P
31	NC	NC	LA28_P	NC	NC	NC	TDO	SDA	GND	DP3_C2M_N
32	NC	GND	LA28_N	GND	NC	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	NC	TMS	GND	DP7_C2M_N	GND
34	NC	HB15_N	LA30_P	LA31_N	NC	NC	TRST_L	GA0	GND	DP4_C2M_P
35	NC	GND	LA30_N	GND	NC	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	NC	GND	NC	GND	NC	3P3V	GND	DP6_C2M_P	GND
37	NC	NC	NC	NC	NC	NC	GND	12P0V	DP6_C2M_N	GND
38	NC	GND	NC	GND	NC	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

Figure 3: FMC HPC Connector Pin Out

Table 3: FMC HPC Connector Pin Assignment

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
A1	GND	GND	Power	Ground.
A2	DP1_M2C_P	HS_TXVR1_RX_CH1p	O, DIFF	PCIe Lane1 Receive pair positive.
A3	DP1_M2C_N	HS_TXVR1_RX_CH1n	O, DIFF	PCIe Lane1 Receive pair negative.
A4	GND	GND	Power	Ground.
A5	GND	GND	Power	Ground.
A6	DP2_M2C_P	HS_TXVR1_RX_CH2p	O, DIFF	PCIe Lane2 Receive pair positive.
A7	DP2_M2C_N	HS_TXVR1_RX_CH2n	O, DIFF	PCIe Lane2 Receive pair negative.
A8	GND	GND	Power	Ground.
A9	GND	GND	Power	Ground.
A10	DP3_M2C_P	HS_TXVR1_RX_CH3p	O, DIFF	PCIe Lane3 Receive pair positive.
A11	DP3_M2C_N	HS_TXVR1_RX_CH3n	O, DIFF	PCIe Lane3 Receive pair negative.
A12	GND	GND	Power	Ground.
A13	GND	GND	Power	Ground.
A14	DP4_M2C_P	HS_TXVR2_RX_CH0p	O, DIFF	PCIe Lane4 Receive pair positive.
A15	DP4_M2C_N	HS_TXVR2_RX_CH0n	O, DIFF	PCIe Lane4 Receive pair negative.
A16	GND	GND	Power	Ground.
A17	GND	GND	Power	Ground.
A18	DP5_M2C_P	HS_TXVR2_RX_CH1p	O, DIFF	PCIe Lane5 Receive pair positive.
A19	DP5_M2C_N	HS_TXVR2_RX_CH1n	O, DIFF	PCIe Lane5 Receive pair negative.
A20	GND	GND	Power	Ground.
A21	GND	GND	Power	Ground.
A22	DP1_C2M_P	HS_TXVR1_TX_CH1p	I, DIFF	PCIe Lane1 Transmit pair positive.
A23	DP1_C2M_N	HS_TXVR1_TX_CH1n	I, DIFF	PCIe Lane1 Transmit pair negative.
A24	GND	GND	Power	Ground.
A25	GND	GND	Power	Ground.
A26	DP2_C2M_P	HS_TXVR1_TX_CH2p	I, DIFF	PCIe Lane2 Transmit pair positive.
A27	DP2_C2M_N	HS_TXVR1_TX_CH2n	I, DIFF	PCIe Lane2 Transmit pair negative.
A28	GND	GND	Power	Ground.
A29	GND	GND	Power	Ground.
A30	DP3_C2M_P	HS_TXVR1_TX_CH3p	I, DIFF	PCIe Lane3 Transmit pair positive.
A31	DP3_C2M_N	HS_TXVR1_TX_CH3n	I, DIFF	PCIe Lane3 Transmit pair negative.
A32	GND	GND	Power	Ground.
A33	GND	GND	Power	Ground.
A34	DP4_C2M_P	HS_TXVR2_TX_CH0p	I, DIFF	PCIe Lane4 Transmit pair positive.
A35	DP4_C2M_N	HS_TXVR2_TX_CH0n	I, DIFF	PCIe Lane4 Transmit pair negative.
A36	GND	GND	Power	Ground.
A37	GND	GND	Power	Ground.
A38	DP5_C2M_P	HS_TXVR2_TX_CH1p	I, DIFF	PCIe Lane5 Transmit pair positive.
A39	DP5_C2M_N	HS_TXVR2_TX_CH1n	I, DIFF	PCIe Lane5 Transmit pair negative.
A40	GND	GND	Power	Ground.
B1	CLK_DIR	NA	NA	NC.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
B2	GND	GND	Power	Ground.
B3	GND	GND	Power	Ground.
B4	DP9_M2C_P	HS_TXVR3_RX_CH0p	O, DIFF	M.2 PCIe Lane1 Receive pair positive.
B5	DP9_M2C_N	HS_TXVR3_RX_CH0n	O, DIFF	M.2 PCIe Lane1 Receive pair negative.
B6	GND	GND	Power	Ground.
B7	GND	GND	Power	Ground.
B8	DP8_M2C_P	HS_TXVR4_RX_CH1p	O, DIFF	M.2 PCIe Lane0 Receive pair positive.
B9	DP8_M2C_N	HS_TXVR4_RX_CH1n	O, DIFF	M.2 PCIe Lane0 Receive pair negative.
B10	GND	GND	Power	Ground.
B11	GND	GND	Power	Ground.
B12	DP7_M2C_P	HS_TXVR2_RX_CH3p	O, DIFF	PCIe Lane7 Receive pair positive.
B13	DP7_M2C_N	HS_TXVR2_RX_CH3n	O, DIFF	PCIe Lane7 Receive pair negative.
B14	GND	GND	Power	Ground.
B15	GND	GND	Power	Ground.
B16	DP6_M2C_P	HS_TXVR2_RX_CH2p	O, DIFF	PCIe Lane6 Receive pair positive.
B17	DP6_M2C_N	HS_TXVR2_RX_CH2n	O, DIFF	PCIe Lane6 Receive pair negative.
B18	GND	GND	Power	Ground.
B19	GND	GND	Power	Ground.
B20	GBTCLK1_M2C_P	HS_TXVR2_REFCLK_CH0p	O, DIFF	NC Optional PCIe Transceiver Clock Positive.
B21	GBTCLK1_M2C_N	HS_TXVR2_REFCLK_CH0n	O, DIFF	NC Optional PCIe Transceiver Clock Negative.
B22	GND	GND	Power	Ground.
B23	GND	GND	Power	Ground.
B24	DP9_C2M_P	HS_TXVR3_TX_CH1p	I, DIFF	M.2 PCIe Lane1 Transmit pair positive.
B25	DP9_C2M_N	HS_TXVR3_TX_CH1n	I, DIFF	M.2 PCIe Lane1 Transmit pair negative.
B26	GND	GND	Power	Ground.
B27	GND	GND	Power	Ground.
B28	DP8_C2M_P	HS_TXVR3_TX_CH0p	I, DIFF	M.2 PCIe Lane0 Transmit pair positive.
B29	DP8_C2M_N	HS_TXVR3_TX_CH0n	I, DIFF	M.2 PCIe Lane0 Transmit pair negative.
B30	GND	GND	Power	Ground.
B31	GND	GND	Power	Ground.
B32	DP7_C2M_P	HS_TXVR2_TX_CH3p	I, DIFF	PCIe Lane7 Transmit pair positive.
B33	DP7_C2M_N	HS_TXVR2_TX_CH3n	I, DIFF	PCIe Lane7 Transmit pair negative.
B34	GND	GND	Power	Ground.
B35	GND	GND	Power	Ground.
B36	DP6_C2M_P	HS_TXVR2_TX_CH2p	I, DIFF	PCIe Lane6 Transmit pair positive.
B37	DP6_C2M_N	HS_TXVR2_TX_CH2n	I, DIFF	PCIe Lane6 Transmit pair negative.
B38	GND	GND	Power	Ground.
B39	GND	GND	Power	Ground.
B40	RES0	NA	NA	NC.
C1	GND	GND	Power	Ground.
C2	DP0_C2M_P	HS_TXVR1_TX_CH0p	I, DIFF	PCIe Lane0 Transmit pair positive.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
C3	DP0_C2M_N	HS_TXVR1_TX_CH0n	I, DIFF	PCIe Lane0 Transmit pair negative.
C4	GND	GND	Power	Ground.
C5	GND	GND	Power	Ground.
C6	DP0_M2C_P	HS_TXVR1_RX_CH0p	O, DIFF	PCIe Lane0 Receive pair positive.
C7	DP0_M2C_N	HS_TXVR1_RX_CH0n	O, DIFF	PCIe Lane0 Receive pair negative.
C8	GND	GND	Power	Ground.
C9	GND	GND	Power	Ground.
C10	LA06_P	LA06_P	O,1.2V MIPI	MIPI CSI Connector Data Lane3 positive.
C11	LA06_N	LA06_N	O, 1.2V MIPI	MIPI CSI Connector Data Lane3 negative.
C12	GND	GND	Power	Ground.
C13	GND	GND	Power	Ground.
C14	LA10_P	LA10_P	O, 1.2V MIPI	MIPI CSI Connector Data Lane1 positive.
C15	LA10_N	LA10_N	O, 1.2V MIPI	MIPI CSI Connector Data Lane1 negative.
C16	GND	GND	Power	Ground.
C17	GND	GND	Power	Ground.
C18	LA14_P	LA14_P	NA	NC.
C19	LA14_N	LA14_N	NA	NC.
C20	GND	GND	Power	Ground.
C21	GND	GND	Power	Ground.
C22	LA18_P_CC	LA18_P_CC	I, 1.2V MIPI	MIPI DSI Connector Clock positive.
C23	LA18_N_CC	LA18_N_CC	I, 1.2V MIPI	MIPI DSI Connector Clock negative.
C24	GND	GND	Power	Ground.
C25	GND	GND	Power	Ground.
C26	LA27_P	LA27_P	O, VADJ LVCMOS	M.2 PCIe Connector Device Identification (Config).
C27	LA27_N	LA27_N	I, VADJ LVCMOS	Touch panel reset of touch connector.
C28	GND	GND	Power	Ground.
C29	GND	GND	Power	Ground.
C30	SCL	FMC+_SCL	I, 3.3V LVCMOS	I2C Clock
C31	SDA	FMC+_SDA	IO, 3.3V LVCMOS	I2C Data
C32	GND	GND	Power	Ground.
C33	GND	GND	Power	Ground.
C34	GA0	GA0_FMC	I, 3.3V LVCMOS	Geographical address 0. This pin is connected to EEPROM address bit 0.
C35	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
C36	GND	GND	Power	Ground.
C37	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
C38	GND	GND	Power	Ground.
C39	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
C40	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
D1	PG_C2M	FMC+_PG_C2M	I, 3.3V LVCMOS	Power Good signal to Module. This pin is connected to power Enable of on board 3.3V Regulator.
D2	GND	GND	Power	Ground.
D3	GND	GND	Power	Ground.
D4	GBTCLK0_M2C_P	HS_TXVR1_REFCLK_CH0p	O, HCSL	PCIe transceiver reference clock positive.
D5	GBTCLK0_M2C_N	HS_TXVR1_REFCLK_CH0n	O, HSCL	PCIe transceiver reference clock negative.
D6	GND	GND	Power	Ground.
D7	GND	GND	Power	Ground.
D8	LA01_P_CC	LA01_P_CC	O, VADJ LVCMOS	MIPI CSI Connector Vertical video synchronization
D9	LA01_N_CC	LA01_N_CC	O, VADJ LVCMOS	MIPI CSI Connector Horizontal video synchronization
D10	GND	GND	Power	Ground.
D11	LA05_P	LA05_P	NA	NC.
D12	LA05_N	LA05_N	NA	NC.
D13	GND	GND	Power	Ground.
D14	LA09_P	LA09_P	O,1.2V MIPI	MIPI CSI Connector Data Lane0 positive.
D15	LA09_N	LA09_N	O, 1.2V MIPI	MIPI CSI Connector Data Lane0 negative.
D16	GND	GND	Power	Ground.
D17	LA13_P	LA13_P	NA	NC.
D18	LA13_N	LA13_N	NA	NC.
D19	GND	GND	Power	Ground.
D20	LA17_P_CC	LA17_P_CC	I, 1.2V MIPI	MIPI DSI Connector Data Lane1 positive.
D21	LA17_N_CC	LA17_N_CC	I,1.2V MIPI	MIPI DSI Connector Data Lane1 negative.
D22	GND	GND	Power	Ground.
D23	LA23_P	NA	NA	NC.
D24	LA23_N	NA	NA	NC.
D25	GND	GND	Power	Ground.
D26	LA26_P	NA	NA	NC.
D27	LA26_N	LA26_N	I, VADJ LVCMOS	MIPI CSI Connector Flash Enable.
D28	GND	GND	Power	Ground.
D29	TCK	NA	NA	NC.
D30	TDI	TDI	O, 3.3V LVCMOS	Connected to TDO
D31	TDO	TDO	I, 3.3V LVCMOS	Connected to TDI
D32	3P3VAUX	VCC_3V3_AUX	O, 3.3V Power	Auxiliary Supply Voltage.
D33	TMS	NA	NA	NC.
D34	TRST_L	NA	NA	NC.
D35	GA1	GA1_FMC	I, 3.3V LVCMOS	Geographical address1. This pin is connected to EEPROM address bit 1.
D36	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
D37	GND	GND	Power	Ground.
D38	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
D39	GND	GND	Power	Ground.
D40	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
E1	GND	GND	Power	Ground.
E2	HA01_P_CC	NA	NA	NC.
E3	HA01_N_CC	NA	NA	NC.
E4	GND	GND	Power	Ground.
E5	GND	GND	Power	Ground.
E6	HA05_P	NA	NA	NC.
E7	HA05_N	NA	NA	NC.
E8	GND	GND	Power	Ground.
E9	HA09_P	NA	NA	NC.
E10	HA09_N	NA	NA	NC.
E11	GND	GND	Power	Ground.
E12	HA13_P	NA	NA	NC.
E13	HA13_N	NA	NA	NC.
E14	GND	GND	Power	Ground.
E15	HA16_P	NA	NA	NC.
E16	HA16_N	NA	NA	NC.
E17	GND	GND	Power	Ground.
E18	HA20_P	NA	NA	NC.
E19	HA20_N	NA	NA	NC.
E20	GND	GND	Power	Ground.
E21	HB03_P	NA	NA	NC.
E22	HB03_N	NA	NA	NC.
E23	GND	GND	Power	Ground.
E24	HB05_P	NA	NA	NC.
E25	HB05_N	NA	NA	NC.
E26	GND	GND	Power	Ground.
E27	HB09_P	NA	NA	NC.
E28	HB09_N	NA	NA	NC.
E29	GND	GND	Power	Ground.
E30	HB13_P	NA	NA	NC.
E31	HB13_N	NA	NA	NC.
E32	GND	GND	Power	Ground.
E33	HB19_P	NA	NA	NC.
E34	HB19_N	NA	NA	NC.
E35	GND	GND	Power	Ground.
E36	HB21_P	NA	NA	NC.
E37	HB21_N	NA	NA	NC.
E38	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
E39	VADJ	VCC_FMC+_ADJ	I, VADJ Power	Adjustable Voltage from Carrier board to module.
E40	GND	GND	Power	Ground.
F1	PG_M2C	NA	NA	NC.
F2	GND	GND	Power	Ground.
F3	GND	GND	Power	Ground.
F4	HA00_P_CC	NA	NA	NC.
F5	HA00_N_CC	NA	NA	NC.
F6	GND	GND	Power	Ground.
F7	HA04_P	NA	NA	NC.
F8	HA04_N	NA	NA	NC.
F9	GND	GND	Power	Ground.
F10	HA08_P	NA	NA	NC.
F11	HA08_N	NA	NA	NC.
F12	GND	GND	Power	Ground.
F13	HA12_P	NA	NA	NC.
F14	HA12_N	NA	NA	NC.
F15	GND	GND	Power	Ground.
F16	HA15_P	NA	NA	NC.
F17	HA15_N	NA	NA	NC.
F18	GND	GND	Power	Ground.
F19	HA19_P	NA	NA	NC.
F20	HA19_N	NA	NA	NC.
F21	GND	GND	Power	Ground.
F22	HB02_P	NA	NA	NC.
F23	HB02_N	NA	NA	NC.
F24	GND	GND	Power	Ground.
F25	HB04_P	NA	NA	NC.
F26	HB04_N	NA	NA	NC.
F27	GND	GND	Power	Ground.
F28	HB08_P	NA	NA	NC.
F29	HB08_N	NA	NA	NC.
F30	GND	GND	Power	Ground.
F31	HB12_P	NA	NA	NC.
F32	HB12_N	NA	NA	NC.
F33	GND	GND	Power	Ground.
F34	HB16_P	NA	NA	NC.
F35	HB16_N	NA	NA	NC.
F36	GND	GND	Power	Ground.
F37	HB20_P	NA	NA	NC.
F38	HB20_N	NA	NA	NC.
F39	GND	GND	Power	Ground.
F40	VADJ	VCC_FMC+_ADJ	I, VADJ Power	Adjustable Voltage from Carrier board to module.
G1	GND	GND	Power	Ground.
G2	CLK1_M2C_P	NA	NA	NC.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
G3	CLK1_M2C_N	NA	NA	NC.
G4	GND	GND	Power	Ground.
G5	GND	GND	Power	Ground.
G6	LA00_P_CC	LA00_P_CC	NA	NC.
G7	LA00_N_CC	LA00_N_CC	NA	NC.
G8	GND	GND	Power	Ground.
G9	LA03_P	LA03_P	I, VADJ LVCMOS	24MHz Clock to MIPI CSI Connector.
G10	LA03_N	LA03_N	I, VADJ LVCMOS	MIPI CSI Connector Reset.
G11	GND	GND	Power	Ground.
G12	LA08_P	LA08_P	I, 1.2V MIPI	MIPI CSI Connector clock positive.
G13	LA08_N	LA08_N	I, 1.2V MIPI	MIPI CSI Connector clock negative.
G14	GND	GND	Power	Ground.
G15	LA12_P	NA	NA	NC.
G16	LA12_N	LA12_N	IO, VADJ LVCMOS	PCIe Reset.
G17	GND	GND	Power	Ground.
G18	LA16_P	LA16_P	I, 1.2V MIPI	MIPI DSI Connector Data Lane2 positive.
G19	LA16_N	LA16_N	I, 1.2V MIPI	MIPI DSI Connector Data Lane2 negative.
G20	GND	GND	Power	Ground.
G21	LA20_P	LA20_P	NA	NC.
G22	LA20_N	LA20_N	NA	NC.
G23	GND	GND	Power	Ground.
G24	LA22_P	LA22_P	NA	NC.
G25	LA22_N	LA22_N	NA	NC.
G26	GND	GND	Power	Ground.
G27	LA25_P	LA25_P	I, VADJ LVCMOS	MIPI DSI Connector LCD Reset.
G28	LA25_N	LA25_N	O, VADJ LVCMOS	MIPI DSI Touch panel interrupt of touch connector.
G29	GND	GND	Power	Ground.
G30	LA29_P	LA29_P	I, VADJ LVCMOS	PCIe Wake
G31	LA29_N	NA	NA	NC.
G32	GND	GND	Power	Ground.
G33	LA31_P	LA31_P	I, VADJ LVCMOS	MIPI DSI Connector VLED Driver Enable.
G34	LA31_N	LA31_N	I, VADJ LVCMOS	NC Optional PCIe Reset
G35	GND	GND	Power	Ground.
G36	LA33_P	NA	NA	NC.
G37	LA33_N	NA	NA	NC.
G38	GND	GND	Power	Ground.
G39	VADJ	VCC_FMC+_ADJ	I, VADJ Power	Adjustable Voltage from Carrier board to module.
G40	GND	GND	Power	Ground.
H1	VREF_A_M2C	NA	NA	NC

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
H2	PRSNT_M2C_L	FMC+_PR_M2C_L	NA	Module Present Signal. This Pin is connected to GND through 0 ohm.
H3	GND	GND	Power	Ground.
H4	CLK0_M2C_P	CLK0_M2C_P	I,DIFF	M.2 Device Clock Positive.
H5	CLK0_M2C_N	CLK0_M2C_N	I,DIFF	M.2 Device Clock Negative.
H6	GND	GND	Power	Ground.
H7	LA02_P	LA02_P	NA	NC.
H8	LA02_N	LA02_N	NA	NC.
H9	GND	GND	Power	Ground.
H10	LA04_P	LA04_P	NA	NC.
H11	LA04_N	LA04_N	NA	NC.
H12	GND	GND	Power	Ground.
H13	LA07_P	LA07_P	O, 1.2V MIPI	MIPI CSI Connector Data Lane2 positive.
H14	LA07_N	LA07_N	O, 1.2V MIPI	MIPI CSI Connector Data Lane2 negative.
H15	GND	GND	Power	Ground.
H16	LA11_P	LA11_P	I, 1.2V MIPI	MIPI DSI Connector Data Lane0 positive.
H17	LA11_N	LA11_N	I, 1.2V MIPI	MIPI DSI Connector Data Lane0 negative.
H18	GND	GND	Power	Ground.
H19	LA15_P	LA15_P	NA	NC.
H20	LA15_N	LA15_N	NA	NC.
H21	GND	GND	Power	Ground.
H22	LA19_P	LA19_P	I, 1.2V MIPI	MIPI DSI Connector Data Lane3 positive.
H23	LA19_N	LA19_N	I, 1.2V MIPI	MIPI DSI Connector Data Lane3 negative.
H24	GND	GND	Power	Ground.
H25	LA21_P	LA21_P	NA	NC.
H26	LA21_N	LA21_N	NA	NC.
H27	GND	GND	Power	Ground.
H28	LA24_P	NA	NA	NC.
H29	LA24_N	NA	NA	NC.
H30	GND	GND	Power	Ground.
H31	LA28_P	LA28_P	I, VADJ LVCMOS	M.2 PCIe Reset.
H32	LA28_N	LA28_N	I, VADJ LVCMOS	M.2 PCIe Device sleep.
H33	GND	GND	Power	Ground.
H34	LA30_P	LA30_P	I, VADJ LVCMOS	M.2 PCIe Wake.
H35	LA30_N	LA30_N	I, VADJ LVCMOS	I2C Bus Reset.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
H36	GND	GND	Power	Ground.
H37	LA32_P	LA32_P	I, VADJ LVCMOS	MIPI CSI Trigger Enable.
H38	LA32_N	NA	NA	NC.
H39	GND	GND	Power	Ground.
H40	VADJ	VCC_FMC+_ADJ	I, VADJ Power	Adjustable Voltage from Carrier board to module.
J1	GND	GND	Power	Ground.
J2	CLK3_BIDIR_P	NA	NA	NC.
J3	CLK3_BIDIR_N	NA	NA	NC.
J4	GND	GND	Power	Ground.
J5	GND	GND	Power	Ground.
J6	HA03_P	NA	NA	NC.
J7	HA03_N	NA	NA	NC.
J8	GND	GND	Power	Ground.
J9	HA07_P	NA	NA	NC.
J10	HA07_N	NA	NA	NC.
J11	GND	GND	Power	Ground.
J12	HA11_P	NA	NA	NC.
J13	HA11_N	NA	NA	NC.
J14	GND	GND	Power	Ground.
J15	HA14_P	NA	NA	NC.
J16	HA14_N	NA	NA	NC.
J17	GND	GND	Power	Ground.
J18	HA18_P	NA	NA	NC.
J19	HA18_N	NA	NA	NC.
J20	GND	GND	Power	Ground.
J21	HA22_P	NA	NA	NC.
J22	HA22_N	NA	NA	NC.
J23	GND	GND	Power	Ground.
J24	HB01_P	NA	NA	NC.
J25	HB01_N	NA	NA	NC.
J26	GND	GND	Power	Ground.
J27	HB07_P	NA	NA	NC.
J28	HB07_N	NA	NA	NC.
J29	GND	GND	Power	Ground.
J30	HB11_P	NA	NA	NC.
J31	HB11_N	NA	NA	NC.
J32	GND	GND	Power	Ground.
J33	HB15_P	HB15_P	NA	NC.
J34	HB15_N	HB15_N	NA	NC.
J35	GND	GND	Power	Ground.
J36	HB18_P	NA	NA	NC.
J37	HB18_N	NA	NA	NC.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
J38	GND	GND	Power	Ground.
J39	VIO_B_M2C	NA	NA	NC.
J40	GND	GND	Power	Ground.
K1	VREF_B_M2C	NA	NA	NC.
K2	GND	GND	Power	Ground.
K3	GND	GND	Power	Ground.
K4	CLK2_BIDIR_P	NA	NA	NC.
K5	CLK2_BIDIR_N	NA	NA	NC.
K6	GND	GND	Power	Ground.
K7	HA02_P	NA	NA	NC.
K8	HA02_N	NA	NA	NC.
K9	GND	GND	Power	Ground.
K10	HA06_P	NA	NA	NC.
K11	HA06_N	NA	NA	NC.
K12	GND	GND	Power	Ground.
K13	HA10_P	NA	NA	NC.
K14	HA10_N	NA	NA	NC.
K15	GND	GND	Power	Ground.
K16	HA17_P_CC	NA	NA	NC.
K17	HA17_N_CC	NA	NA	NC.
K18	GND	GND	Power	Ground.
K19	HA21_P	NA	NA	NC.
K20	HA21_N	NA	NA	NC.
K21	GND	GND	Power	Ground.
K22	HA23_P	NA	NA	NC.
K23	HA23_N	NA	NA	NC.
K24	GND	GND	Power	Ground.
K25	HB00_P_CC	NA	NA	NC.
K26	HB00_N_CC	NA	NA	NC.
K27	GND	GND	Power	Ground.
K28	HB06_P_CC	NA	NA	NC.
K29	HB06_N_CC	NA	NA	NC.
K30	GND	GND	Power	Ground.
K31	HB10_P	NA	NA	NC.
K32	HB10_N	NA	NA	NC.
K33	GND	GND	Power	Ground.
K34	HB14_P	NA	NA	NC.
K35	HB14_N	NA	NA	NC.
K36	GND	GND	Power	Ground.
K37	HB17_P_CC	NA	NA	NC.
K38	HB17_N_CC	NA	NA	NC.
K39	GND	GND	Power	Ground.
K40	VIO_B_M2C	NA	NA	NC.

2.3.1 PCIe x8 Connector

The PCIe Gen4 x8 FMC module support one PCIe x8 interface through PCIe x8 Connector (J4). Eight high speed transceiver pairs from FMC HPC connector are directly connected to PCIe x8 Connector (J4) connector for PCIe interface. This PCIe x8 connector physically located at the top of the board as shown below.

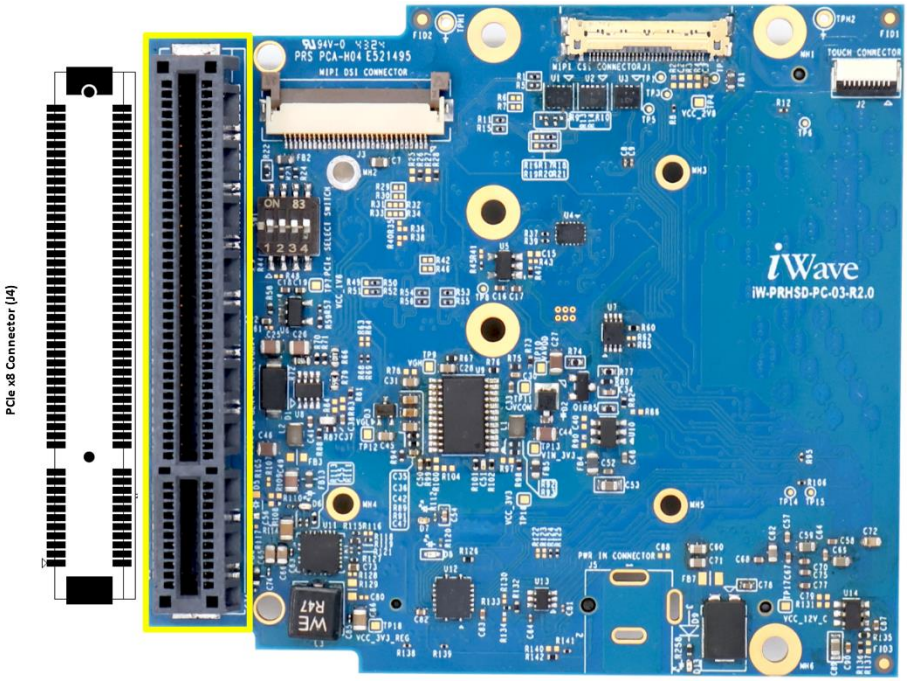

Figure 4: PCIe x 8 Connector

This PCIe Gen4 x8 FMC module supports both PCIe Root Port and PCIe Endpoint Synchronous Mode of operation. To select between PCIe Root port mode and Endpoint mode, the PCIe Mode Select Switch (SW1.1) is utilized. PCIe Root port mode is selected by keeping SW1.1 in the OFF state. In this condition, the on-module clock oscillator will be the source of the clock for the PCIe X8 connector and the GBTCLK0_M2C_P/N pins of FMC Connector. Also power is sourced from FMC connector to PCIe connector.

Similarly, PCIe Endpoint mode is selected by keeping the SW1.1 in the ON state. In this condition, the PCIe reference clock will be sourced from the Host PC via the PCIe X8 connector to the GBTCLK0_M2C_P/N pins of the FMC Connector. Also power is sourced from PCIe connector to on Module peripherals. And Power from FMC connector is cutoff.

The PCIe Mode Select Switch is physically located at the top of PCIe FMC Module as shown below.

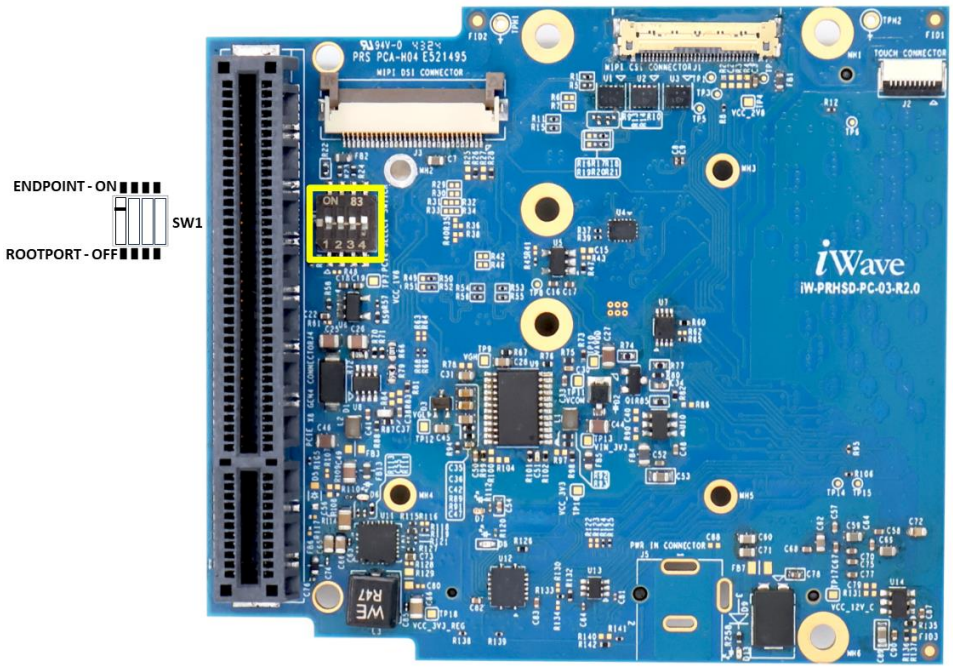

Figure 5: PCIe Mode Select Switch

Table 4: PCIe Mode Select Switch

Switch Position	Switch Mode	SW1.1	SW1.2	SW1.3	SW1.4
	Endpoint	ON	ON	ON	OFF
	Root port	OFF	OFF	OFF	ON

Table 5: PCIe x8 Connector Pin Assignment

PCIe Connector Pin No.	PCIe Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
A1	PRSNT1_N	NA	NA	NA	NA	Default Grounded.
A2	+12V	VCC_12V	NA	NA	12V Power	12V Supply Voltage. Note: 12V is output for Root Port application and input for Endpoint application.
A3	+12V	VCC_12V	NA	NA	12V Power	12V Supply Voltage. Note: 12V is output for Root Port application and input for Endpoint application.
A4	GND	GND	NA	NA	Power	Ground.
A5	JTAG_TCK	NA	NA	NA	NA	NC.
A6	JTAG_TDI	NA	NA	NA	NA	NC.
A7	JTAG_TDO	NA	NA	NA	NA	NC.
A8	JTAG_TMS	NA	NA	NA	NA	NC.
A9	+3_3V	VCC_3V3_PCIe	NA	NA	3.3V Power	3.3V Supply Voltage. Note: 3.3V is output for Root Port application and input for Endpoint application.
A10	+3_3V	VCC_3V3_PCIe	NA	NA	3.3V Power	3.3V Supply Voltage. Note: 3.3V is output for Root Port application and input for Endpoint application.
A11	PERST_N	PCIE_RESET	G16	LA12_N	IO,3.3V LVCMOS	PCIe Reset. Note: This reset signal is output for Root Port application and input for Endpoint application.
A12	GND	GND	NA	NA	Power	Ground.
A13	REFCLK+	PCIe_CLKP	NA	NA	IO, DIFF	100MHz PCIe Reference Clock positive. Note: This 100MHz clock is output for Root Port application and input for Endpoint application.

PCIe Connector Pin No.	PCIe Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
A14	REFCLK-	PCIe_CLKN	NA	NA	IO, DIFF	100MHz PCIe Reference Clock negative. Note: This 100MHz clock is output for Root Port application and input for Endpoint application.
A15	GND	GND	NA	NA	Power	Ground.
A16	PER0P	HS_TXVR1_RX_CH0p	C6	DP0_M2C_P	I, DIFF	PCIe Lane0 Receive pair positive.
A17	PER0N	HS_TXVR1_RX_CH0n	C7	DP0_M2C_N	I, DIFF	PCIe Lane0 Receive pair negative.
A18	GND	GND	NA	NA	Power	Ground.
A19	RSVD2	NA	NA	NA	NA	NC.
A20	GND	GND	NA	NA	Power	Ground.
A21	PER1P	HS_TXVR1_RX_CH1p	A2	DP1_M2C_P	I, DIFF	PCIe Lane1 Receive pair positive.
A22	PER1N	HS_TXVR1_RX_CH1n	A3	DP1_M2C_N	I, DIFF	PCIe Lane1 Receive pair negative
A23	GND	GND	NA	NA	Power	Ground.
A24	GND	GND	NA	NA	Power	Ground.
A25	PER2P	HS_TXVR1_RX_CH2p	A6	DP2_M2C_P	I, DIFF	PCIe Lane2 Receive pair positive.
A26	PER2N	HS_TXVR1_RX_CH2n	A7	DP2_M2C_N	I, DIFF	PCIe Lane2 Receive pair negative.
A27	GND	GND	NA	NA	Power	Ground.
A28	GND	GND	NA	NA	Power	Ground.
A29	PER3P	HS_TXVR1_RX_CH3p	A10	DP3_M2C_P	I, DIFF	PCIe Lane3 Receive pair positive.
A30	PER3N	HS_TXVR1_RX_CH3n	A11	DP3_M2C_N	I, DIFF	PCIe Lane3 Receive pair negative.
A31	GND	GND	NA	NA	Power	Ground.
A32	RSVD4	NA	NA	NA	NA	NC.
A33	RSVD5	NA	NA	NA	NA	NC.
A34	GND	GND	NA	NA	Power	Ground.
A35	PER4P	HS_TXVR2_RX_CH0p	A14	DP4_M2C_P	I, DIFF	PCIe Lane4 Receive pair positive.
A36	PER4N	HS_TXVR2_RX_CH0n	A15	DP4_M2C_N	I, DIFF	PCIe Lane4 Receive pair negative.
A37	GND	GND	NA	NA	Power	Ground.
A38	GND	GND	NA	NA	Power	Ground.
A39	PER5P	HS_TXVR2_RX_CH1p	A18	DP5_M2C_P	I, DIFF	PCIe Lane5 Receive pair positive.

PCIe Connector Pin No.	PCIe Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
A40	PER5N	HS_TXVR2_RX_CH1p	A19	DP5_M2C_N	I, DIFF	PCIe Lane5 Receive pair negative.
A41	GND	GND	NA	NA	Power	Ground.
A42	GND	GND	NA	NA	Power	Ground.
A43	PER6P	HS_TXVR2_RX_CH2p	B16	DP6_M2C_P	I, DIFF	PCIe Lane6 Receive pair positive.
A44	PER6N	HS_TXVR2_RX_CH2n	B17	DP6_M2C_N	I, DIFF	PCIe Lane6 Receive pair negative.
A45	GND	GND	NA	NA	Power	Ground.
A46	GND	GND	NA	NA	Power	Ground.
A47	PER7P	HS_TXVR2_RX_CH3p	B12	DP7_M2C_P	I, DIFF	PCIe Lane7 Receive pair positive.
A48	PER7N	HS_TXVR2_RX_CH3n	B13	DP7_M2C_N	I, DIFF	PCIe Lane7 Receive pair negative.
A49	GND	GND	NA	NA	Power	Ground.
B1	+12V	VCC_12V	NA	NA	12V Power	12V Supply Voltage. Note: 12V is output for Root Port application and input for Endpoint application.
B2	+12V	VCC_12V	NA	NA	12V Power	12V Supply Voltage. Note: 12V is output for Root Port application and input for Endpoint application.
B3	+12V	VCC_12V	NA	NA	12V Power	12V Supply Voltage. Note: 12V is output for Root Port application and input for Endpoint application.
B4	GND	GND	NA	NA	Power	Ground.
B5	SMCLK	NA	NA	NA	NA	NC. Note: This pin is optionally connected to I2C Bus switch port0 through resistor and by default not populated.
B6	SMDAT	NA	NA	NA	NA	NC. Note: This pin is optionally connected to I2C Bus switch port0 through resistor and by default not populated.

PCIe Connector Pin No.	PCIe Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
B7	GND	GND	NA	NA	Power	Ground.
B8	+3_3V	VCC_3V3_PCIe	NA	NA	3.3V Power	3.3V Supply Voltage. Note: 3.3V is output for Root Port application and input for Endpoint application.
B9	JTAG_TRSTN	NA	NA	NA	NA	NC.
B10	+3_3VAUX	NA	NA	NA	NA	NC. This pin is optionally connected to VCC_3V3_PCIe.
B11	WAKE_N	NA	NA	NA	NA	NC. This pin is optionally connected to LA30_P through resistor and by default not populated.
B12	RSVD1	NA	NA	NA	NA	NC.
B13	GND	GND	NA	NA	Power	Ground.
B14	PET0P	HS_TXVR1_TX_CH0p	C2	DP0_C2M_P	O, DIFF	PCIe Lane0 Transmit pair positive.
B15	PET0N	HS_TXVR1_TX_CH0n	C3	DP0_C2M_N	O, DIFF	PCIe Lane0 Transmit pair negative.
B16	GND	GND	NA	NA	Power	Ground.
B17	PRSNT2n_X1	NA	NA	NA	NA	NC
B18	GND	GND	NA	NA	Power	Ground.
B19	PET1P	HS_TXVR1_TX_CH1p	A22	DP1_C2M_P	O, DIFF	PCIe Lane1 Transmit pair positive.
B20	PET1N	HS_TXVR1_TX_CH1n	A23	DP1_C2M_N	O, DIFF	PCIe Lane1 Transmit pair negative
B21	GND	GND	NA	NA	Power	Ground.
B22	GND	GND	NA	NA	Power	Ground.
B23	PET2P	HS_TXVR1_TX_CH2p	A26	DP2_C2M_P	O, DIFF	PCIe Lane2 Transmit pair positive.
B24	PET2N	HS_TXVR1_TX_CH2n	A27	DP2_C2M_N	O, DIFF	PCIe Lane2 Transmit pair negative
B25	GND	GND	NA	NA	Power	Ground.
B26	GND	GND	NA	NA	Power	Ground.
B27	PET3P	HS_TXVR1_TX_CH3p	A30	DP3_C2M_P	O, DIFF	PCIe Lane3 Transmit pair positive.
B28	PET3N	HS_TXVR1_TX_CH2n	A31	DP3_C2M_N	O, DIFF	PCIe Lane3 Transmit pair negative

PCIe Connector Pin No.	PCIe Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
B29	GND	GND	NA	NA	Power	Ground.
B30	RSVD3	NA	NA	NA	NA	NC.
B31	PRSNT2n_X4	NA	NA	NA	NA	NC
B32	GND	GND	NA	NA	Power	Ground.
B33	PET4P	HS_TXVR2_TX_CH0p	A34	DP4_C2M_P	O, DIFF	PCIe Lane4 Transmit pair positive.
B34	PET4N	HS_TXVR2_TX_CH0n	A35	DP4_C2M_N	O, DIFF	PCIe Lane4 Transmit pair negative
B35	GND	GND	NA	NA	Power	Ground.
B36	GND	GND	NA	NA	Power	Ground.
B37	PET5P	HS_TXVR2_TX_CH1p	A38	DP5_C2M_P	O, DIFF	PCIe Lane5 Transmit pair positive.
B38	PET5N	HS_TXVR2_TX_CH1n	A39	DP5_C2M_N	O, DIFF	PCIe Lane5 Transmit pair negative
B39	GND	GND	NA	NA	Power	Ground.
B40	GND	GND	NA	NA	Power	Ground.
B41	PET6P	HS_TXVR2_TX_CH2p	B36	DP6_C2M_N	O, DIFF	PCIe Lane6 Transmit pair positive.
B42	PET6N	HS_TXVR2_TX_CH2n	B37	DP6_C2M_P	O, DIFF	PCIe Lane6 Transmit pair negative
B43	GND	GND	NA	NA	Power	Ground.
B44	GND	GND	NA	NA	Power	Ground.
B45	PET7P	HS_TXVR2_TX_CH3p	B32	DP7_C2M_P	O, DIFF	PCIe Lane7 Transmit pair positive.
B46	PET7N	HS_TXVR2_TX_CH3n	B33	DP7_C2M_N	O, DIFF	PCIe Lane7 Transmit pair negative
B47	GND	GND	NA	NA	Power	Ground.
B48	PRSNT2n_X8	NA	NA	NA	NA	NC
B49	GND	GND	NA	NA	Power	Ground.

2.3.2 M.2 Key-M NVMe Connector

The PCIe Gen4 x8 FMC module support one PCIe x2 interface through M.2 Key-M NVMe Connector (J8). Two high speed transceiver pairs from FMC HPC connector are directly connected to M.2 Key-M connector for PCIe x2 Root port.

This connector physically located at the bottom of the board as shown below.

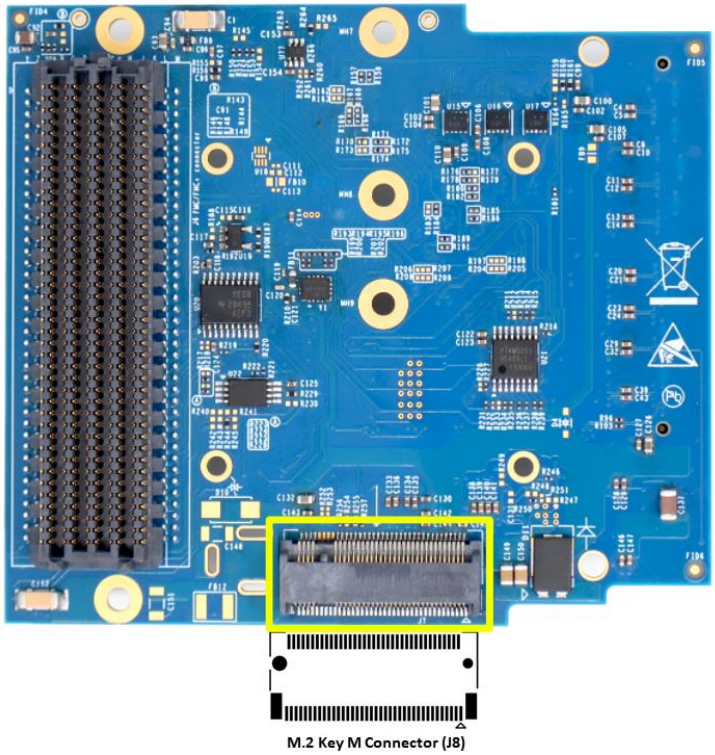

Figure 6: M.2 Key-M NVMe Connector

Note: The PCIe Gen4 x8 FMC module also supports PCIe x4 interface optionally through M.2 Key-M NVMe Connector(J8), when VITA 57.4 FMC+ connector is mounted

Table 6: M.2 Key M Connector Pin Assignment

M.2 Connector Pin No	M.2 Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
1	CONFIG_3	NA	NA	NA	NA	This pin is connected to Ground.
2	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.
3	GND	GND	NA	NA	Power	Ground.
4	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.
5	PERn3	HS_TXVR3_RX_CH3n	Z13	DP11_M2C_N	I, DIFF	M.2 PCIe Lane3 Receive pair negative Note: This lane is only supported when FMC+ Conn. is mounted.
6	N/A1	NA	NA	NA	NA	NC.
7	PERp3	HS_TXVR3_RX_CH3p	Z12	DP11_M2C_P	I, DIFF	M.2 PCIe Lane3 Receive pair positive Note: This lane is only supported when FMC+ Conn. is mounted.
8	N/A2	NA	NA	NA	NA	NC.
9	GND	GND	NA	NA	Power	Ground.
10	DAS/DSS	NA	NA	NA	NA	This pin is connected to M.2 LED.
11	PETn3	HS_TXVR3_TX_CH3n	Y27	DP11_C2M_N	O, DIFF	M.2 PCIe Lane3 Transmit pair negative Note: This lane is only supported when FMC+ Conn. is mounted.
12	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.
13	PETp3	HS_TXVR3_TX_CH3p	Y26	DP11_C2M_P	O, DIFF	M.2 PCIe Lane3 Transmit pair positive Note: This lane is only supported when FMC+ Conn. is mounted.
14	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.
15	GND	GND	NA	NA	Power	Ground.
16	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.

M.2 Connector Pin No	M.2 Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
17	PERn2	HS_TXVR3_RX_CH2n	Y11	DP10_M2C_N	I, DIFF	M.2 PCIe Lane2 Receive pair negative Note: This lane is only supported when FMC+ Conn. is mounted.
18	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.
19	PERp2	HS_TXVR3_RX_CH2p	Y10	DP10_M2C_P	I, DIFF	M.2 PCIe Lane2 Receive pair positive Note: This lane is only supported when FMC+ Conn. is mounted.
20	N/A3	NA	NA	NA	NA	NC.
21	CONFIG_0	NA	NA	NA	NA	Configuration 0. This pin is connected to Ground.
22	N/A4	NA	NA	NA	NA	NC.
23	PETn2	HS_TXVR3_TX_CH2n	Z25	DP10_C2M_N	O, DIFF	M.2 PCIe Lane2 Transmit pair negative Note: This lane is only supported when FMC+ Conn. is mounted.
24	N/A5	NA	NA	NA	NA	NC.
25	PETp2	HS_TXVR3_TX_CH2p	Z24	DP10_C2M_P	O, DIFF	M.2 PCIe Lane2 Transmit pair positive Note: This lane is only supported when FMC+ Conn. is mounted.
26	N/A6	NA	NA	NA	NA	NC.
27	GND	GND	NA	NA	Power	Ground.
28	N/A7	NA	NA	NA	NA	NC.
29	PERn1	HS_TXVR3_RX_CH1n	B5	DP9_M2C_N	I, DIFF	M.2 PCIe Lane1 Receive pair negative.
30	N/A8	NA	NA	NA	NA	NC.
31	PERp1	HS_TXVR3_RX_CH1p	B4	DP9_M2C_P	I, DIFF	M.2 PCIe Lane1 Receive pair positive.
32	N/A9	NA	NA	NA	NA	NC.
33	GND	GND	NA	NA	Power	Ground.
34	N/A10	NA	NA	NA	NA	NC.
35	PETn1	HS_TXVR3_TX_CH1n	B25	DP9_C2M_N	O, DIFF	M.2 PCIe Lane1 Transmit pair negative
36	N/A11	NA	NA	NA	NA	NC.
37	PETp1	HS_TXVR3_TX_CH1p	B24	DP9_C2M_P	O, DIFF	M.2 PCIe Lane1 Transmit pair positive.

M.2 Connector Pin No	M.2 Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
38	DEVSLP	M.2 _DEVSLP	H32	LA28_N	IO,3V3 LVCMOS	M.2 Device Sleep.
39	GND	GND	NA	NA	Power	Ground.
40	SMB_CLK	I2C0_SD3_SCL	NA	NA	NA	This pin is connected to I2C Bus Switch Port 3
41	SATA-B+/PERn0	HS_TXVR3_RX_CH0n	B9	DP8_M2C_N	I, DIFF	M.2 PCIe Lane0 Receive pair negative.
42	SMB_DATA	I2C0_SD3_SDA	NA	NA	NA	This pin is connected to I2C Bus Switch Port 3.
43	SATA-B-/PERp0	HS_TXVR3_RX_CH0p	B8	DP8_M2C_P	I, DIFF	M.2 PCIe Lane0 Receive pair positive.
44	ALERT#	NA	NA	NA	NA	NC.
45	GND	GND	NA	NA	Power	Ground.
46	N/A15	NA	NA	NA	NA	NC.
47	SATA-A-/PETn0	HS_TXVR3_TX_CH0n	B29	DP8_C2M_N	O, DIFF	M.2 PCIe Lane0 Transmit pair negative.
48	N/A16	NA	NA	NA	NA	NC.
49	SATA-A+/PETp0	HS_TXVR3_TX_CH0p	B28	DP8_C2M_P	O, DIFF	M.2 PCIe Lane0 Transmit pair positive.
50	PERST#	LA28_P	H31	LA28_P	O,3V3 LVCMOS/ 10K PU	M.2 PCIe reset This signal is connected through Level Translator
51	GND	GND	NA	NA	Power	Ground.
52	CLKREQ#	NA	NA	NA	NA	NC.
53	REFCLKN	CLK0_M2C_N	H5	CLK0_M2C_N	O, DIFF	M.2 PCIe Device Clock negative
54	PEWAKE#	LA30_P	H34	LA30_P	O,3V3 LVCMOS/ 10K PU	M.2 PCIe wake. This signal is connected through Level Translator
55	REFCLKP	CLK0_M2C_P	H4	CLK0_M2C_P	O, DIFF	M.2 PCIe Device Clock positive
56	MFG1	NA	NA	NA	NA	NC.
57	GND	GND	NA	NA	Power	Ground.
58	MFG2	NA	NA	NA	NA	NC.
59	M1	NA	NA	NA	NA	NC.
60	M2	NA	NA	NA	NA	NC.
61	M3	NA	NA	NA	NA	NC.
62	M4	NA	NA	NA	NA	NC.
63	M5	NA	NA	NA	NA	NC.
64	M6	NA	NA	NA	NA	NC.
65	M7	NA	NA	NA	NA	NC.
66	M8	NA	NA	NA	NA	NC.
67	N/A17	NA	NA	NA	NA	NC.

M.2 Connector Pin No	M.2 Connector Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
68	SUSCLK	NA	NA	NA	NA	NC
69	CONFIG_1	LA27_P	C26	LA27_P	O,3V3 LVCMOS	M.2 Config. This signal is connected through Level Translator
70	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.
71	GND	GND	NA	NA	Power	Ground.
72	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.
73	GND	GND	NA	NA	Power	Ground.
74	3.3V	VCC_3V3_PCIe	NA	NA	3.3V Power	Supply Voltage.
75	CONFIG_2	NA	NA	NA	NA	This pin is connected to Ground.

2.3.3 MIPI CSI Connector

The PCIe Gen4 x8 FMC Module supports MIPI CSI connector to support MIPI interface. Four lane MIPI CSI interface signals from FMC HPC connector are used for MIPI CSI interface.

Supported Camera Module: LI-IMX274-MIPI-M12 from Leopard Imaging Inc

Cable Part Number: FAW-1233-01 from Leopard Imaging Inc

MIPI CSI connector (J1) is physically located on top of the board as shown below.

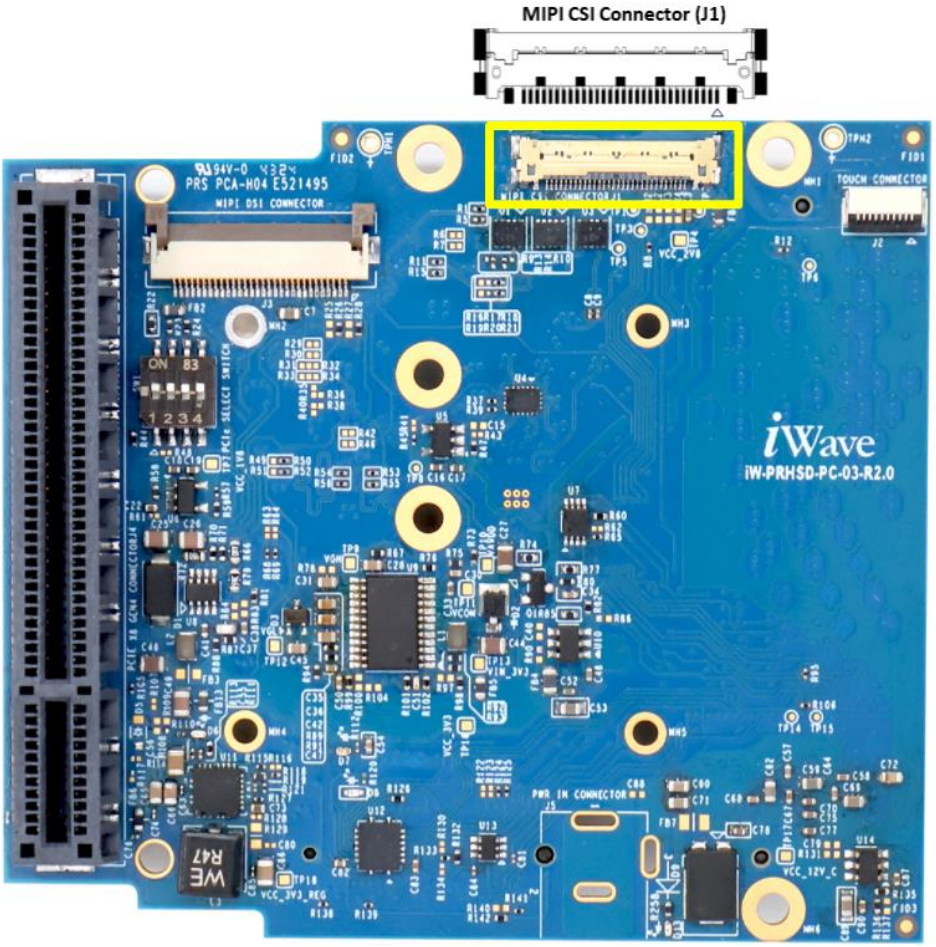

Figure 7: MIPI CSI Connector

Table 7: MIPI CSI Connector Pin Assignment

Pin No	Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
1	3V3	VCC_3V3	NA	NA	3.3V Power	3.3V Supply Voltage.
2	3V3	VCC_3V3	NA	NA	3.3V Power	3.3V Supply Voltage.
3	3V3	VCC_3V3	NA	NA	3.3V Power	3.3V Supply Voltage.
4	5V0	NA	NA	NA	NA	NC.
5	V_2.8V	VCC_2V8	NA	NA	2.8V Power	2.8V Supply Voltage.
6	V_1.8V	VCC_1V8	NA	NA	1.8V Power	1.8V Supply Voltage.
7	V_1.2V	VCC_1V2	NA	NA	1.2V Power	1.2V Supply Voltage.

Pin No	Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
8	V_1.2V	VCC_1V2	NA	NA	1.2V Power	1.2V Supply Voltage.
9	TX1_GPIO1	NA	NA	NA	NA	NC.
10	TEST1	LA01_P_CC	D8	LA01_P_CC	I,1.8V LVCMOS	Camera Vertical Sync.
11	TX1_GPIO2	NA	NA	NA	NA	NC.
12	TEST2	LA01_N_CC	D9	LA01_P_CC	I,1.8V LVCMOS	Camera Horizontal Sync.
13	TEST3	LA32_P	H37	LA32_P	O,1.8V LVCMOS	Camera Trigger Enable.
14	FLASH_EN	LA26_N	D27	LA26_N	O,1.8V LVCMOS	Camera Flash Enable.
15	CAM_TMP	LA03_P	G9	LA03_P	O, 1.8V LVCMOS	24MHz Input clock to Camera Module.
16	CAM_RST	LA03_N	G10	LA03_N	O,1.8V LVCMOS/10K PU	Camera Reset.
17	CAM_SDA	I2C0_MIPIC_SDA	NA	NA	IO,1.8V LVCMOS /4.7K PU	I2C Data for Camera. This signal is connected from the I2C Bus Switch port 2.
18	CAM_SCL	I2C0_MIPIC_SCL	NA	NA	O,1.8V LVCMOS /4.7K PU	I2C Clock for Camera. This signal is connected from the I2C Bus Switch port2.
19	TEST4	NA	NA	NA	NA	NC.
20	MIPI_D2N	LA07_N	H14	LA07_N	I, 1.2V MIPI	MIPI_CSI DATA Lane2 Negative. This pin is optionally connected to LA00_N_CC and LA11_N through resistors and by default not populated.
21	MIPI_D2P	LA07_P	H13	LA07_P	I, 1.2V MIPI	MIPI_CSI DATA Lane2 Positive. This pin is optionally connected to LA00_P_CC through resistor and by default not populated.
22	MIPI_D0N	LA09_N	D15	LA09_N	I, 1.2V MIPI	MIPI_CSI DATA Lane0 Negative. This pin is optionally connected to LA04_N through resistor and by default not populated.

Pin No	Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
23	MIPI_D0P	LA09_P	D14	LA09_P	I, 1.2V MIPI	MIPI_CSI DATA Lane0 Positive. This pin is optionally connected to LA04_P through resistor and by default not populated.
24	MIPI_CN	LA08_N	G13	LA08_N	O, 1.2V MIPI	MIPI_CSI Clock Negative. This pin is optionally connected to LA06_N and LA18_N_CC through resistors and by default not populated.
25	MIPI_CP	LA08_P	G12	LA08_P	O, 1.2V MIPI	MIPI_CSI Clock Positive. This pin is optionally connected to LA06_P and LA18_P_CC through resistors and by default not populated.
26	GND	GND	NA	NA	Power	Ground.
27	MIPI_D1N	LA10_N	C15	LA10_N	I, 1.2V MIPI	MIPI_CSI DATA Lane1 Negative. This pin is optionally connected through resistors and by default not populated.
28	MIPI_D1P	LA10_P	C14	LA10_P	I, 1.2V MIPI	MIPI_CSI DATA Lane1 Positive. This pin is optionally connected through resistors and by default not populated.
29	MIPI_D3N	LA06_N	C11	LA06_PN	I, 1.2V MIPI	MIPI_CSI DATA Lane3 Negative. This pin is optionally connected through resistors and by default not populated.
30	MIPI_D3P	LA06_P	C10	LA06_P	I, 1.2V MIPI	MIPI_CSI DATA Lane3 Positive. This pin is optionally connected through resistors and by default not populated.

2.3.4 MIPI DSI Connector

The PCIe Gen4 x8 FMC Module supports MIPI DSI connector to support MIPI DSI interface. Four lane MIPI DSI interface signals from FMC HPC connector are used for MIPI DSI interface.

Supported MIPI Display: R070C019MICV01 & WF70A8TYAHMNGB

MIPI DSI connector (J3) is physically located on top of the board as shown below.

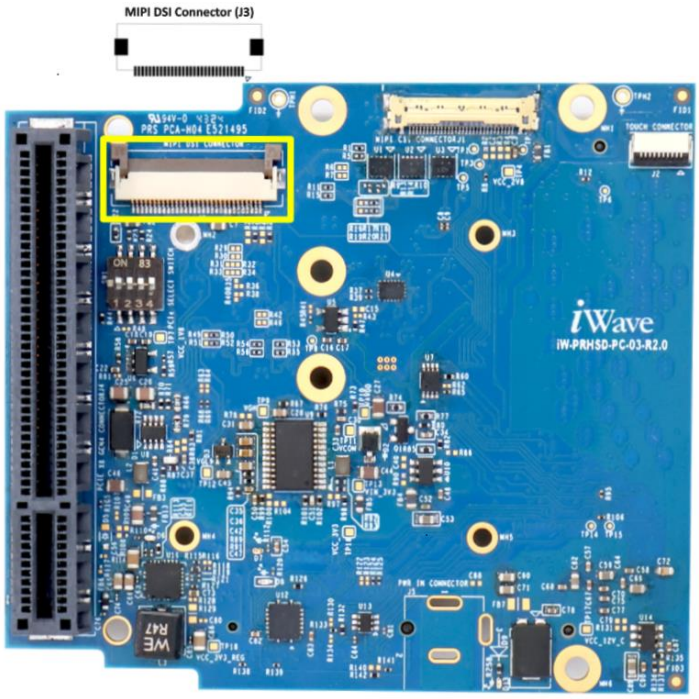

Figure 8: MIPI DSI Connector

Table 8: Default MIPI DSI Connector Pin Assignment

Pin No	Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
1	VLED+	VLED+	NA	NA	Power	Display backlight positive voltage.
2	VLED+	VLED+	NA	NA	Power	Display backlight positive voltage.
3	VGH	VGH	NA	NA	18V Power	18V Supply voltage for Display circuit.
4	VGL	VGL	NA	NA	-6V Power	-6V Supply voltage for Display Circuit
5	UPDN	UPDN	NA	NA	10K PD	UPDN Control signal.
6	SHLR	SHLR	NA	NA	1.8V 10K PU	SHLR
7	VLED-	VLED-	NA	NA	Power	Display backlight negative voltage.

Pin No	Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
8	VLED-	VLED-	NA	NA	Power	Display backlight negative voltage.
9	AVDD	AVDD	NA	NA	9V, Power	9V Supply voltage for Display circuit.
10	GND	GND	NA	NA	Power	Ground.
11	D3P	LA19_P	H22	LA19_P	O, 1.2V MIPI	MIPI_DSI DATA Lane3 Positive. This pin is optionally connected to LA15_P and LA09_P through resistors and by default not populated.
12	D3N	LA19_N	H23	LA19_N	O, 1.2V MIPI	MIPI_DSI DATA Lane3 Negative. This pin is optionally connected to LA15_N and LA09_N through resistors and by default not populated.
13	GND	GND	NA	NA	Power	Ground.
14	D2P	LA16_P	G18	LA16_P	O, 1.2V MIPI	MIPI_DSI DATA Lane2 Positive. This pin is optionally connected to LA02_P through resistor and by default not populated.
15	D2N	LA16_N	G19	LA16_N	O, 1.2V MIPI	MIPI_DSI DATA Lane2 Negative This pin is optionally connected to LA02_N through resistor and by default not populated.
16	GND	GND	NA	NA	Power	Ground.
17	CLKP	LA18_P_CC	C22	LA18_P_CC	O, 1.2V MIPI	MIPI_DSI Clock Positive. This pin is optionally connected to LA12_P and LA21_P through resistors and by default not populated.
18	CLKN	LA18_N_CC	C23	LA18_N_CC	O, 1.2V MIPI	MIPI_DSI Clock Negative. This pin is optionally connected to LA12_N and LA21_N through resistors and by default not populated.
19	GND	GND	NA	NA	Power	Ground.
20	D1P	LA17_P_CC	D20	LA17_P_CC	O, 1.2V MIPI	MIPI_DSI DATA Lane1 Positive. This pin is optionally connected to LA14_P and LA20_P through resistors and by default not populated.

Pin No	Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
21	D1N	LA17_N_CC	D21	LA17_N_CC	O, 1.2V MIPI	MIPI_DSI DATA Lane1 Negative. This pin is optionally connected to LA14_N and LA20_N through resistors and by default not populated.
22	GND	GND	NA	NA	Power	Ground.
23	D0P	LA11_P	H16	LA11_P	O, 1.2V MIPI	MIPI_DSI DATA Lane0 Positive. This pin is optionally connected to LA13_P, LA22_P and HB15_P through resistors and by default not populated.
24	D0N	LA11_N	H17	LA11_N	O, 1.2V MIPI	MIPI_DSI DATA Lane0 Negative. This pin is optionally connected to LA13_N, LA22_N and HB15_N through resistors and by default not populated.
25	GND	GND	NA	NA	Power	Ground.
26	STBYB	DSI_STANDBY	NA	NA	10K, PU.	DSI Standby.
27	RESET	LA25_P	G27	LA25_P	O, 1.8V/ 10K PU	Display reset.
28	VDD	VCC_1V8	NA	NA	1.8V Power	1.8V Supply voltage for Display Circuit.
29	VDD	VCC_1V8	NA	NA	1.8V Power	1.8V Supply voltage for Display Circuit.
30	VCOMIN	VCOM	NA	NA	3.3V, Power	3.3V Supply voltage for Display Circuit.

2.3.5 MIPI DSI Touch Connector

The PCIe Gen4 x8 FMC Module supports MIPI DSI touch connector to support touch display.

Supported MIPI Displays Part Number: WF70A8TYAHMNGB & R070C019MICV01

MIPI DSI touch connector (J2) is physically located on top of the board as shown below.

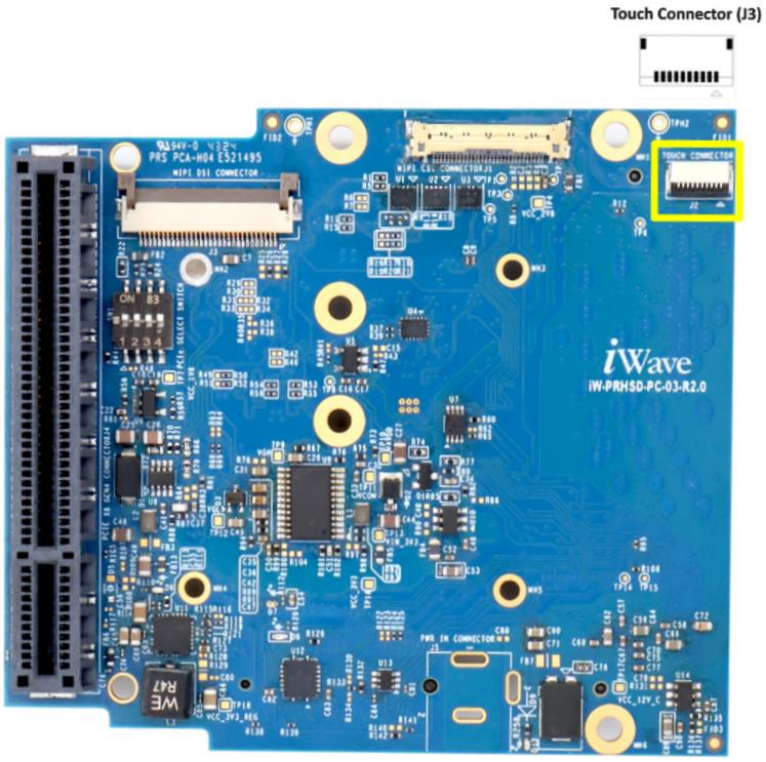

Figure 9: MIPI DSI Touch Connector

Table 9: MIPI Touch Connector Pin Assignment

Pin No	Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
1	VSS	GND	NA	NA	Power	Ground.
2	VCC	VCC_3V3	NA	NA	3.3V, Power	3.3V Supply voltage for Touch Connector.
3	SCL	I2C0_MIPID_SCL	NA	NA	O, 3.3V I2C/ 4.7K PU	I2C Clock to DSI from I2C Bus Switch Port 1.
4	NC1	NC	NA	NA	NA	NA
5	SDA	I2C0_MIPID_SDA	NA	NA	IO,3.3V I2C/ 4.7K PU	I2C Data to DSI from I2C Bus Switch Port 1.
6	NC2	NC	NA	NA	NA	NA

Pin No	Pin Name	Signal Name	FMC Connector Pin No.	FMC Connector Pin Name	Signal Type/ Termination	Description
7	RST	LA27_N	C27	LA27_N	O, 3.3V/ 10K PU	Touch reset.
8	NC3	NC	NA	NA	NA	NA
9	INT	LA25_N	G28	LA25_N	I,3.3V	Touch Interrupt.
10	VSS	GND	NA	NA	Power	Ground.

2.3.6 4 Port I2C Bus Switch

The PCIe Gen4 x8 FMC Module supports 4port I2C Bus switch for the I2C expansion. I2C interface pins (SCL & SDA) of the FMC HPC connector is connected to On-Module I2C peripherals through this I2C Bus switch other than EEPROM. For EEPROM, I2C interface pins are directly connected from FMC HPC connector.

The below table provide details about 4port I2C Switch connection to each ON-Module Peripherals.

Table 10: I2C Bus Switch

I2C Bus Switch Port Number	Connected to Peripherals
Port0	NC. Note: Optionally connected to SMBUS pins of PCIe x8 connector through resistors and by default not populated.
Port1	I2C pins of MIPI DSI Touch Connector
Port2	I2C pins of MIPI CSI Connector.
Port3	SMBUS pins of M.2 Key-M Connector

2.3.7 Clock Oscillator

This FMC module supports both PCIe Root port and PCIe Endpoint Mode of operation. For Root port application on-module clock oscillator will be the source of the clock for the PCIe X8 connector and the GBTCLK0_M2C_P/N pins of FMC Connector. The PCIe Gen4 x8 FMC module supports below mentioned clock flow in Root port configuration.

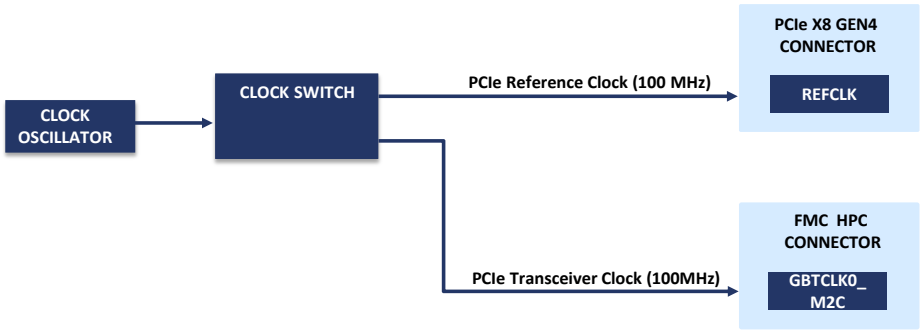

Figure 10: Clock for Root Port Application

For Endpoint application, the 100MHz PCIe reference clock will be sourced from the Host PC via the PCIe X8 connector to the GBTCLK0_M2C_P/N pins of the FMC Connector. The FMC module supports below mentioned clock flow in Endpoint configuration.

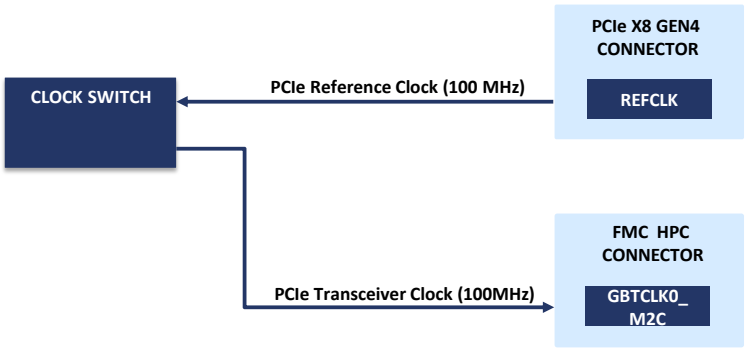

Figure 11: Clock for Endpoint Application

2.3.8 EEPROM

The PCIe Gen4 x8 FMC Module supports EEPROM “M24C32-RDW6TP” to store FMC FRU details. This EEPROM is interfaced to SCL & SDA pins of the FMC HPC connector. Also, its I2C address setting pins A0 & A1 is connected to FMC HPC connector pins GA1 & GA0 respectively and A2 is fixed to ‘0’ in FMC Module.

Table 11: EEPROM Address Configuration

Address Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	1	0	1	0	A2	A1	A0	R/W
Bit Logic Level	1	0	1	0	0	GA0	GA1	R/W

Bit Logic Level -1 : High
Bit Logic Level -0 : Low

3. TECHNICAL SPECIFICATION

This section provides detailed information about the PCIe Gen4 x8 FMC Module technical specification with Electrical and Environmental characteristics.

3.1 Power Input Requirement

By default, The PCIe Gen4 x8 FMC Module is designed to work with power from FMC HPC Connector. The below table provides the Power Input Requirement of PCIe FMC Module.

Table 12: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)
1	VCC_FMC+_ADJ	0	VADJ	1.8[1]
2	VCC_3V3	3.15	3.3	3.45
3	3P3VAUX	3.15	3.3	3.45
4	VCC_12V	11.75	12	12.25

[1]VADJ Maximum is limited to 1.8V since the control signals of MIPI interface is 1.8V

***Important Note:** While using PCIe as Endpoint and connected to external PCIe Host (Root port), make sure that the SW1.1 is turned ON.*

The PCIe Gen4 x8 FMC Module is also has option to connect external power supply through Power Jack (J5) and by default not populated. This connector is physically placed at the top of the board as shown below.

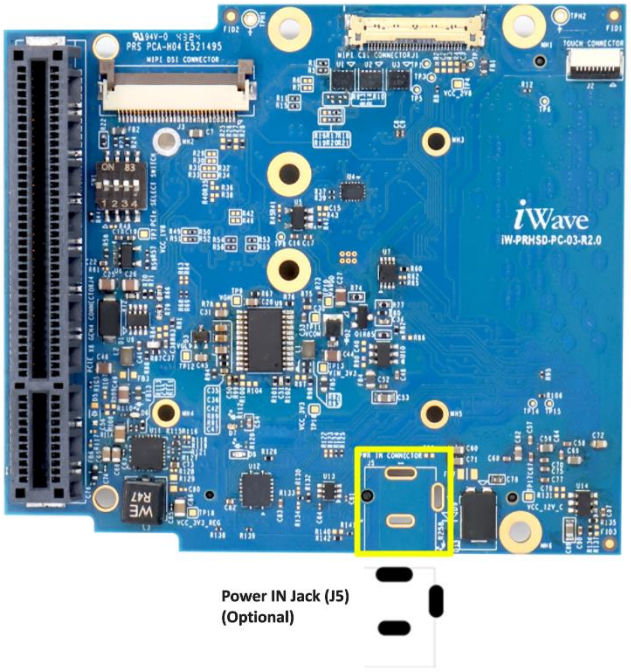

Figure 12: Power IN Jack (Optional)

3.2 Power LEDs

The PCIe Gen4 x8 FMC Module comes with power LEDs to indicate the FMC input powers from FMC connector to module. Power LEDs are provided for VCC_12V, VCC_3V3 and VCC_3V3_PCIe power rails. These LEDs are physically placed at the top of the board as shown below.

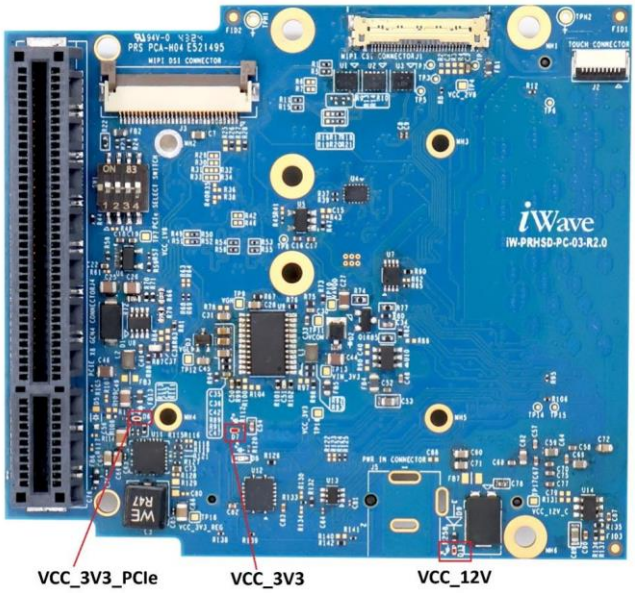

Figure 13: Power LEDs

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of PCIe Gen4 x8 FMC Module.

Table 13: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave only guarantees the component selection for the given operating temperature.

3.3.2 RoHS Compliance

The PCIe Gen4 x8 FMC Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

The PCIe Gen4 x8 FMC Module is sensitive to electrostatic discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 PCIe FMC Module Mechanical Dimensions

The PCIe Gen4 x8 FMC Module PCB form factor is 78.5mm X 69mm and Board mechanical dimension is shown below.

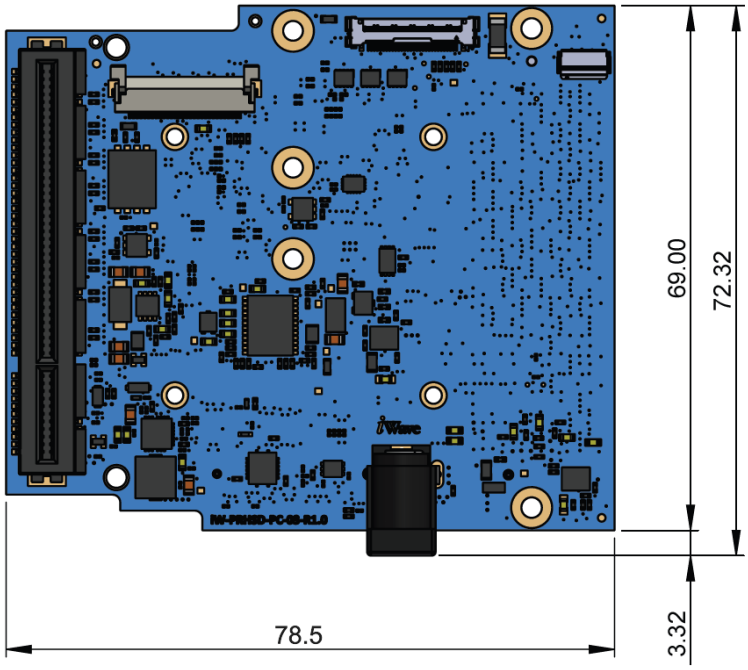

Figure 14: PCIe FMC Module Mechanical dimension – Top View

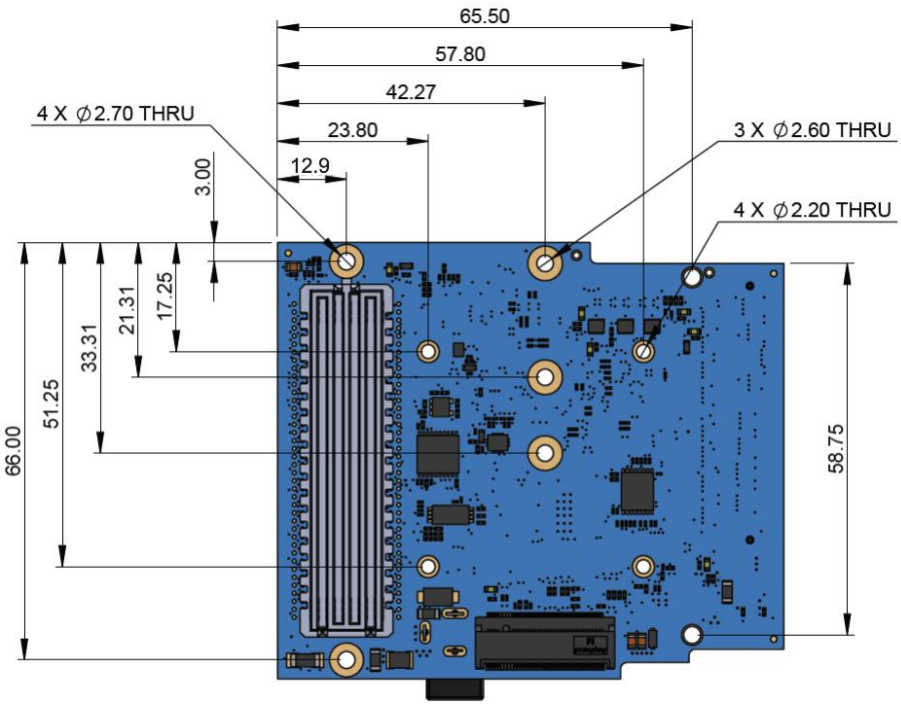

Figure 15: PCIe FMC Module Mechanical dimension – Bottom View

The PCIe Gen4 x8 FMC Module PCB thickness is 1.6mm±0.1mm, top side maximum height component is PCIex8 Connector (11.00mm) and bottom side maximum height component is FMC Connector (7.1mm). Please refer the below figure for height details of the PCIe FMC Module.

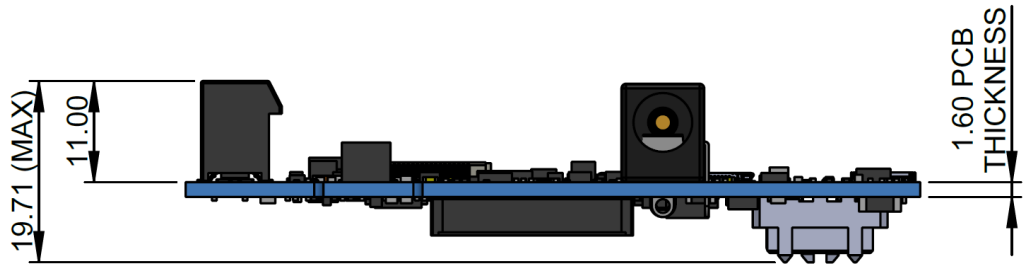

Figure 16: PCIe FMC Module Mechanical dimension – Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for PCIe Gen4 x8 FMC Module.

Table 14: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iG-FMC-PCIe08-I2	PCIe Gen4 x8 FMC Module Refer below **Table 15** for MIPI configuration.	Industrial
iG-FMC-PCIe08-I3	PCIe Gen4 x8 FMC Module. Refer below **Table 15** for MIPI configuration.	Industrial
iG-C40-PCIe08-C3	PCIe x8 Goldfinger to Goldfinger Cross cable (40cm length) for PCIe Endpoint testing.	Commercial

Note: The PCIe x8 connector enables the PCIe Gen4 x8 FMC Module to connect to any root port host system at 16 GT/s (Gen4).

4.1 MIPI Configuration

Table 15: MIPI Configuration for Product Part Number iG-FMC-PCIe08-I2 & iG-FMC-PCIe08-I3

Below shown the 4 Lane MIPI CSI and DSI Configuration for Product Part Number **iG-FMC-PCIe08-I2** & **iG-FMC-PCIe08-I3**.

Connector Pin No.	Pin Name	Pin Description	MIPI Configuration for Product Part Number	
MIPI CSI Connector (J1)			**iG-FMC-PCIe08-I2**	**iG-FMC-PCIe08-I3**
25	MIPI_CP	MIPI_CSI Clock Positive	LA08_P	LA06_P
24	MIPI_CN	MIPI_CSI Clock Negative	LA08_N	LA06_N
23	MIPI_D0P	MIPI_CSI DATA Lane0 Positive	LA09_P	LA09_P
22	MIPI_D0N	MIPI_CSI DATA Lane0 Negative	LA09_N	LA09_N
28	MIPI_D1P	MIPI_CSI DATA Lane1 Positive	LA10_P	LA10_P
27	MIPI_D1N	MIPI_CSI DATA Lane1 Negative	LA10_N	LA10_N
21	MIPI_D2P	MIPI_CSI DATA Lane2 Positive	LA07_P	LA07_P
20	MIPI_D2N	MIPI_CSI DATA Lane2 Negative	LA07_N	LA07_N
30	MIPI_D3P	MIPI_CSI DATA Lane3 Positive	LA06_P	LA08_P
29	MIPI_D3N	MIPI_CSI DATA Lane3 Negative	LA06_N	LA08_N
MIPI DSI Connector (J3)			**iG-FMC-PCIe08-I2**	**iG-FMC-PCIe08-I3**
17	CLKP	MIPI_DSI Clock Positive	LA18_P_CC	LA12_P
18	CLKN	MIPI_DSI Clock Negative	LA18_N_CC	LA12_N
23	D0P	MIPI_DSI DATA Lane0 Positive	LA11_P	LA13_P
24	D0N	MIPI_DSI DATA Lane0 Negative	LA11_N	LA13_N
20	D1P	MIPI_DSI DATA Lane1 Positive	LA17_P_CC	LA14_P
21	D1N	MIPI_DSI DATA Lane1 Negative	LA17_N_CC	LA14_N
14	D2P	MIPI_DSI DATA Lane2 Positive	LA16_P	LA16_P
15	D2N	MIPI_DSI DATA Lane2 Negative	LA16_N	LA16_N
11	D3P	MIPI_DSI DATA Lane3 Positive	LA19_P	LA15_P
12	D3N	MIPI_DSI DATA Lane3 Negative	LA19_N	LA15_N

5. APPENDIX

5.1 Root Port Connection

Refer Table 4 in the PCIe x8 Connector section and change the Config Switch (SW1) settings to Rootport mode. Insert the FMC Module in the development kit and insert the PCIe NVMe module as shown below.

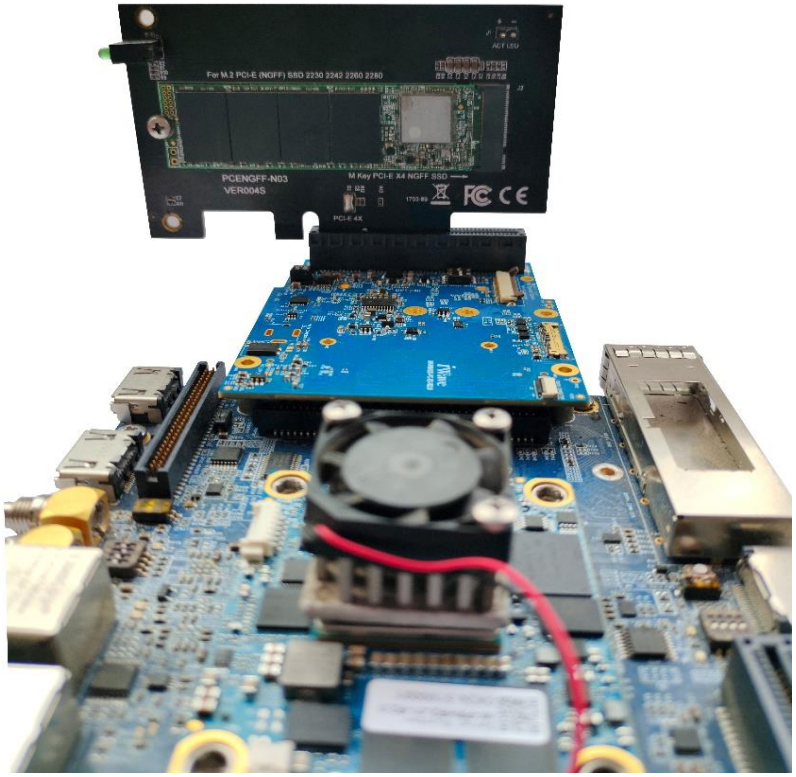

Figure 17: PCIe Root Port Connection

5.2 Endpoint Connection to Host PC

Refer Table 4 in the PCIe x8 Connector section and change the Config Switch (SW1) settings to End Point mode.

1. Insert the PCIe Gen4 x8 FMC module into development kit as shown below.

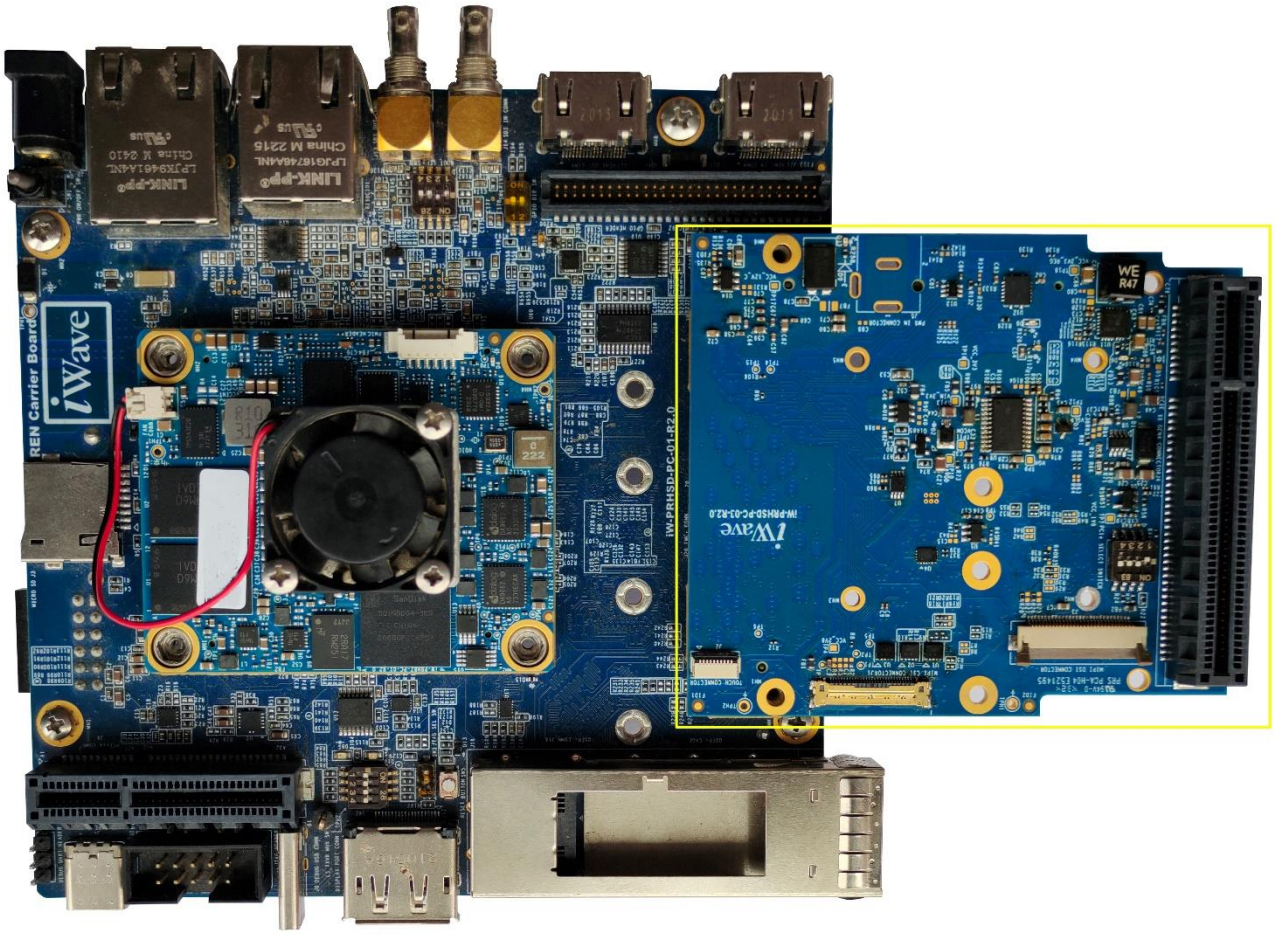

Figure 18: Inserting FMC Module in Development Kit

2. Insert the PCIe x8 Cable to the PCIe x8 connector in the PCIe Gen4 x8 FMC Module as shown below.

Figure 19: PCIe x8 Cable insertion into FMC Module

3. Insert the other end of the PCIe x8 cable to the Host PC's PCIe slot as shown below.

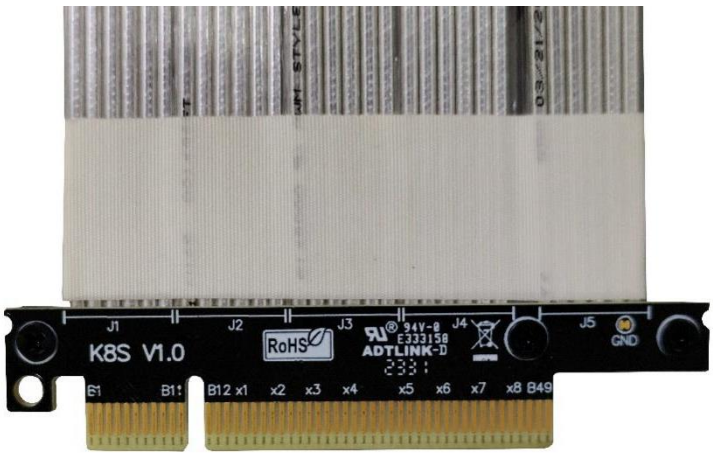

Figure 20: PCIe Cable End

Figure 21: PCIe Endpoint Setup (Host PC to Development Kit)

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mktg@iwave-global.com

iWave
Bangalore, India

iWave USA
Campbell, California

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