

MOSFET – N-Channel, POWER TRENCH[®]

100 V

FDT3612

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 3.7 A, 100 V
 - ♦ $R_{DS(ON)} = 120\text{ m}\Omega$ @ $V_{GS} = 10\text{ V}$
 - ♦ $R_{DS(ON)} = 130\text{ m}\Omega$ @ $V_{GS} = 6\text{ V}$
- Fast Switching Speed
- Low Gate Charge (14 nC Typ)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package.
- This is a Pb-Free Device

Applications

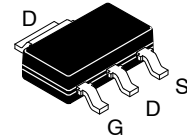
- DC/DC Converter
- Power Management

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current		A
	– Continuous (Note 1a)	3.7	
	– Pulsed	20	
P_D	Maximum Power Dissipation		W
	(Note 1a)	3.0	
	(Note 1b)	1.3	
	(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to $+150$	$^\circ\text{C}$

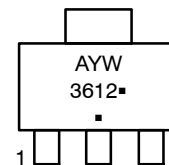
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DSS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	120 m Ω @ 10 V	3.7 A
	130 m Ω @ 6 V	



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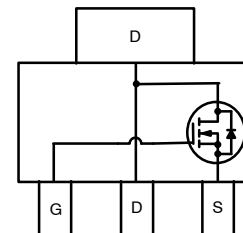
MARKING DIAGRAM



A	= Assembly Location
Y	= Year
W	= Work Week
3612	= Specific Device Code
■	= Pb-Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]
FDT3612	SOT-223 (Pb-Free)	4000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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DRAIN-SOURCE AVALANCHE RATINGS (Note 2)

W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 50\text{ V}$, $I_D = 3.7\text{ A}$	–	–	90	mJ
I_{AR}	Drain-Source Avalanche Current		–	–	3.7	A

OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	106	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$	–	–	10	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	-100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	2.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	-6	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.7\text{ A}$	–	88	120	m Ω
		$V_{GS} = 6\text{ V}$, $I_D = 3.5\text{ A}$	–	94	130	
		$V_{GS} = 10\text{ V}$, $I_D = 3.7\text{ A}$, $T_J = 125^\circ\text{C}$	–	170	245	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 10\text{ V}$	10	–	–	A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 3.7\text{ A}$	–	11	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	–	632	–	pF
C_{oss}	Output Capacitance		–	40	–	pF
C_{rss}	Reverse Transfer Capacitance		–	20	–	pF

SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn – On Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$	–	8.5	17	ns
t_r	Turn – On Rise Time		–	2	4	ns
$t_{d(off)}$	Turn – Off Delay Time		–	23	37	ns
t_f	Turn – Off Fall Time		–	4.5	9	ns
Q_g	Total Gate Charge	$V_{DS} = 50\text{ V}$, $I_D = 3.7\text{ A}$, $V_{GS} = 10\text{ V}$	–	14	20	nC
Q_{gs}	Gate-Source Charge		–	2.4	–	nC
Q_{gd}	Gate-Drain Charge		–	3.8	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

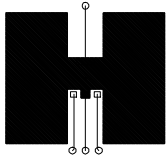
I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	2.5	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.5 A (Note 2)	–	0.75	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

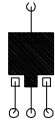
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NOTES:

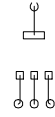
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42°C/W when
mounted on a 1 in²
pad of 2 oz copper.



b. 95°C/W when
mounted on a 0.0066
in² pad of 2 oz copper.



c. 110°C/W when
mounted on a minimum
pad.

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%.

TYPICAL CHARACTERISTICS

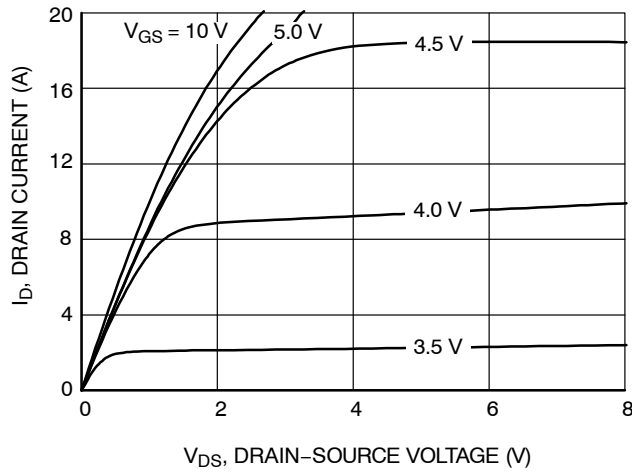


Figure 1. On-Region Characteristics

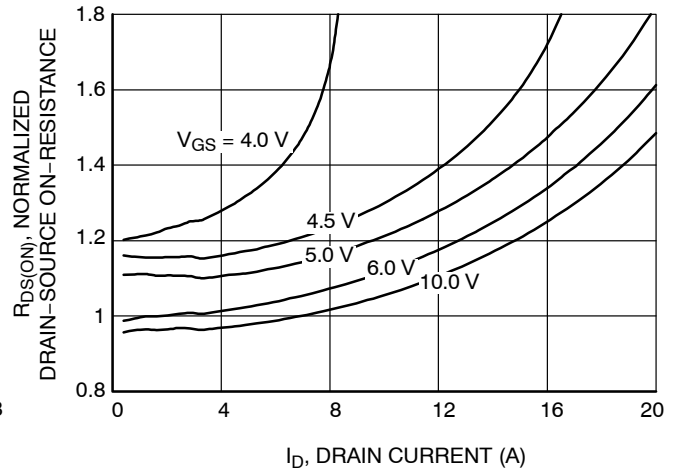


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

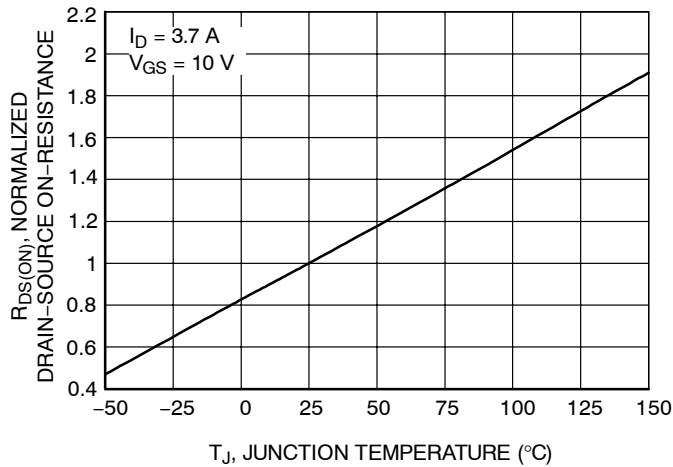


Figure 3. On-Resistance Variation with Temperature

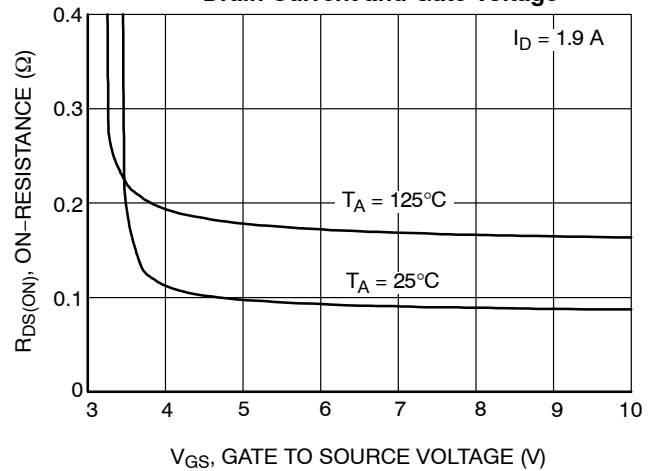


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

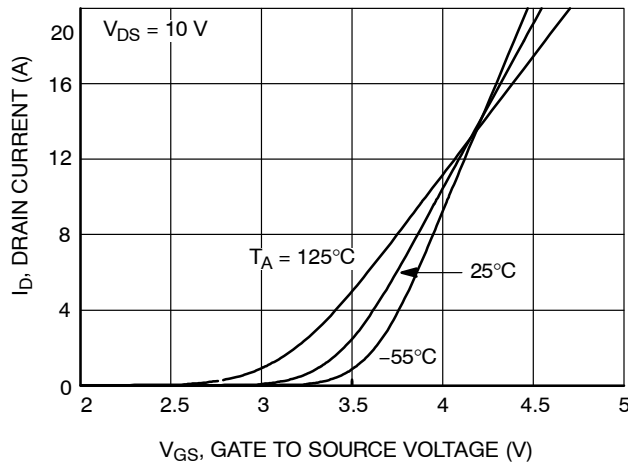


Figure 5. Transfer Characteristics

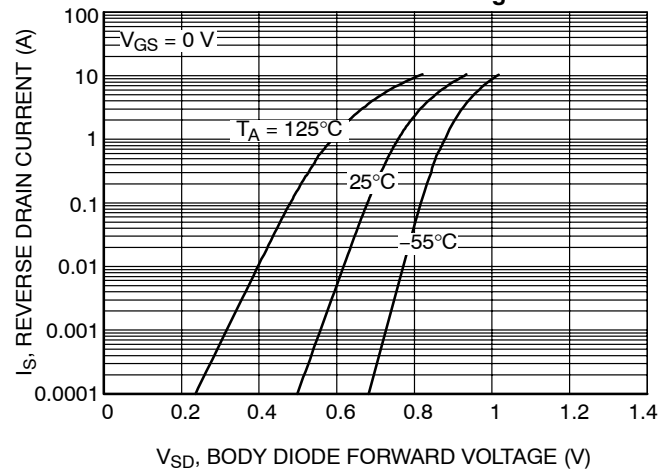


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

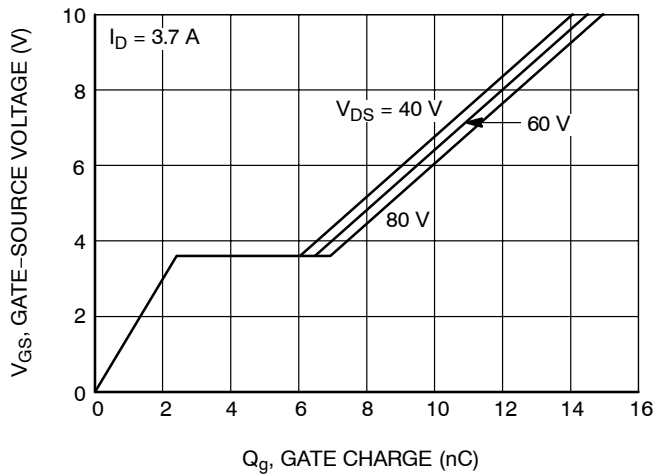


Figure 7. Gate Charge Characteristics

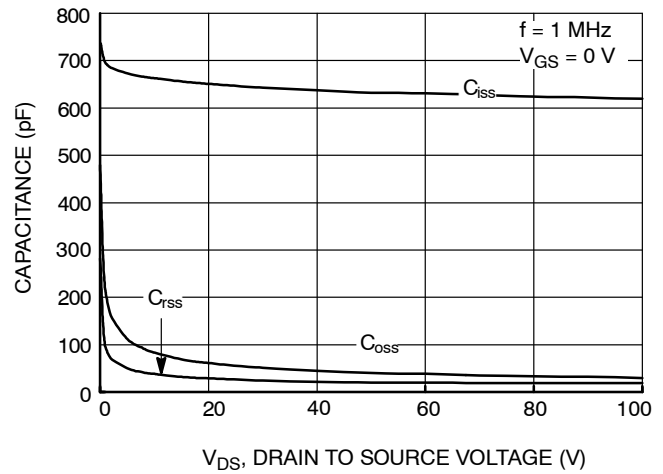


Figure 8. Capacitance Characteristics

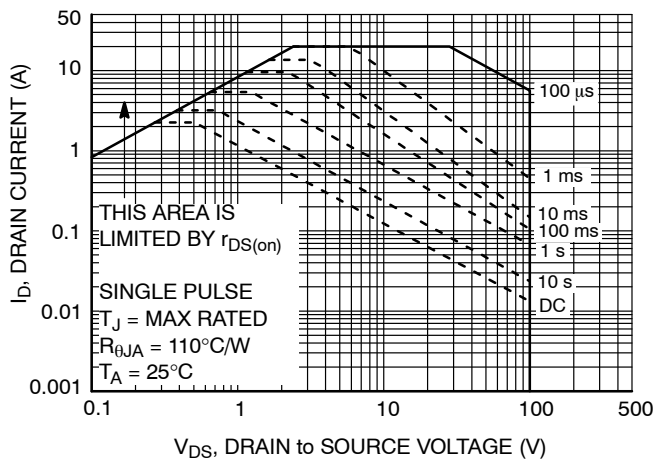


Figure 9. Maximum Safe Operating Area

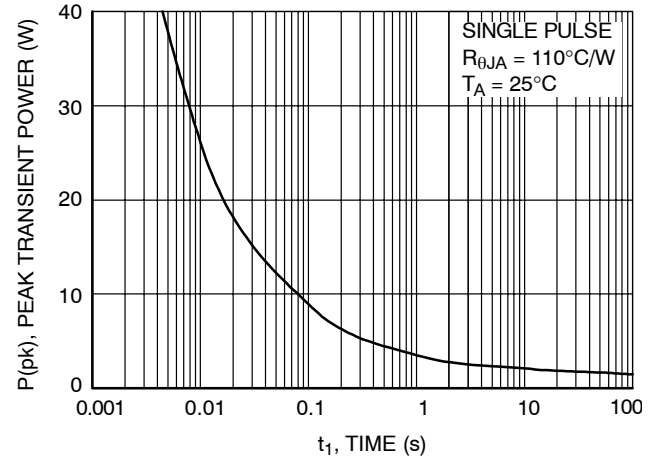


Figure 10. Single Pulse Maximum Power Dissipation

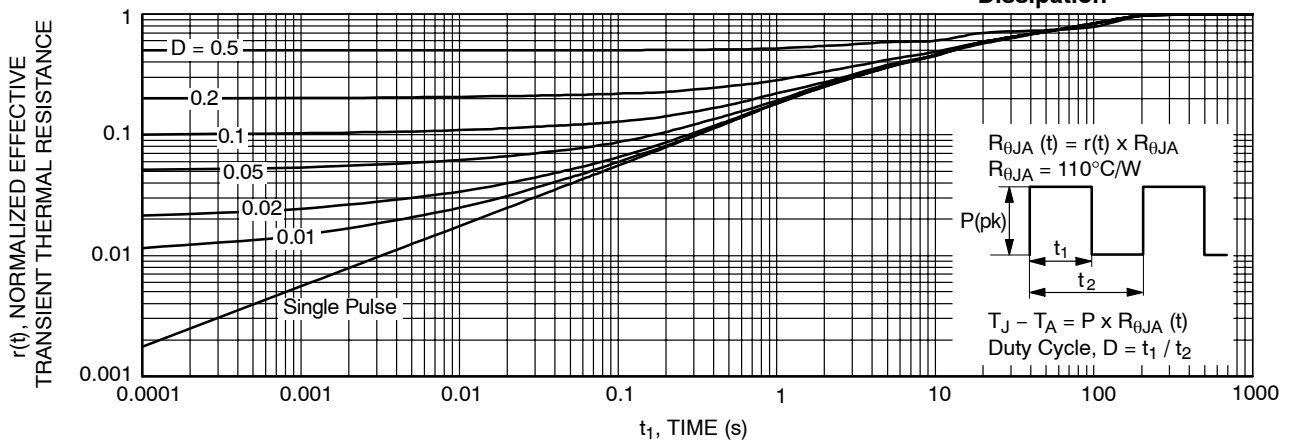
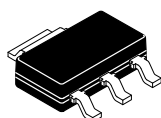


Figure 11. Transient Thermal Response Curve

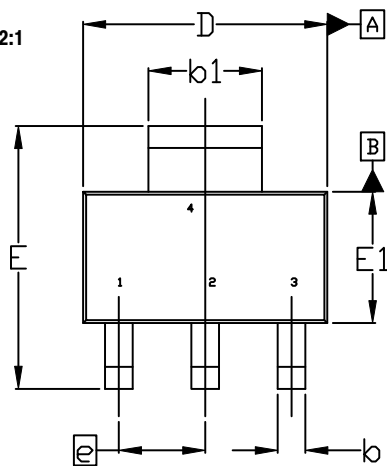
Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.



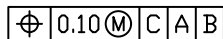
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DATE 13 MAY 2020

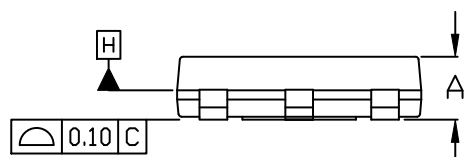
SCALE 2:1



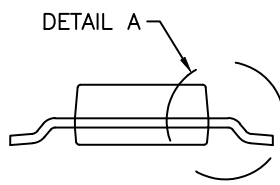
TOP VIEW



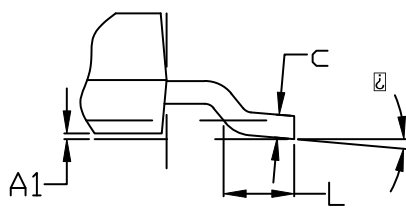
NOTE 7



SIDE VIEW

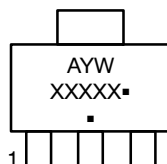


END VIEW



DETAIL A

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb-Free Package

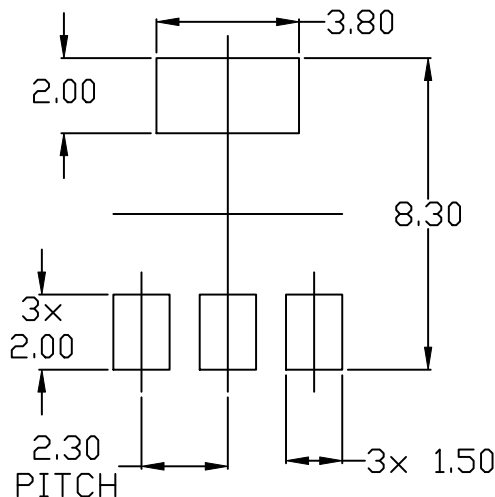
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
⌀	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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