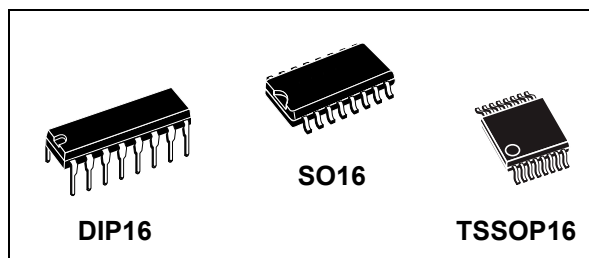


8-bit SIPO shift latch register (3-state)

Datasheet - production data



Applications

- Automotive
- Industrial
- Computer
- Consumer

Description

The M74HC4094 device is a high speed CMOS 8-bit SIPO shift latch register fabricated with silicon gate C²MOS technology. It consists of an 8-bit shift register and an 8-bit latch with 3-state output buffer. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage (QS) can be used to cascade several devices.

Data on the QS output is transferred to a second output (QS') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch, which latches data on the negative going transition of the STROBE input signal. When the STROBE input is held high, data propagates through the latch to a 3-state output buffer. This buffer is enabled when OUTPUT ENABLE input is taken high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features

- High speed: $f_{MAX} = 80 \text{ MHz (typ.)}$ at $V_{CC} = 6 \text{ V}$
- Low power dissipation:
 $I_{CC} = 4 \mu\text{A (max.)}$ at $T_A = 25^\circ\text{C}$
- High noise immunity:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min.)}$
- Symmetrical output impedance:
 $|I_{OH}| = I_{OL} = 4 \text{ mA (min.)}$
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range:
 $V_{CC} \text{ (opr.)} = 2 \text{ V to } 6 \text{ V}$
- Pin and function compatible with 74 series 4094
- ESD performance
 - CDM: 1 kV
 - HBM: 2 kV
 - MM: 200 V

Table 1. Device summary

Order code	Temperature range	Package	Packaging	Marking
M74HC4094RM13TR	-55/+125 °C	SO16	Tape and reel	74HC4094
M74HC4094YRM13TR ⁽¹⁾	-40/+125 °C	SO16 (automotive grade)		HC4094
M74HC4094TTR	-55/+125 °C	TSSOP16		
M74HC4094YTTR ⁽¹⁾	-40/+125 °C	TSSOP16 (automotive grade)		
M74HC4094B1R	-55/+125 °C	DIP16	Tube	M74HC4094B1

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent are ongoing.

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1 Pin information

Figure 1. Pin connection and IEC logic symbols

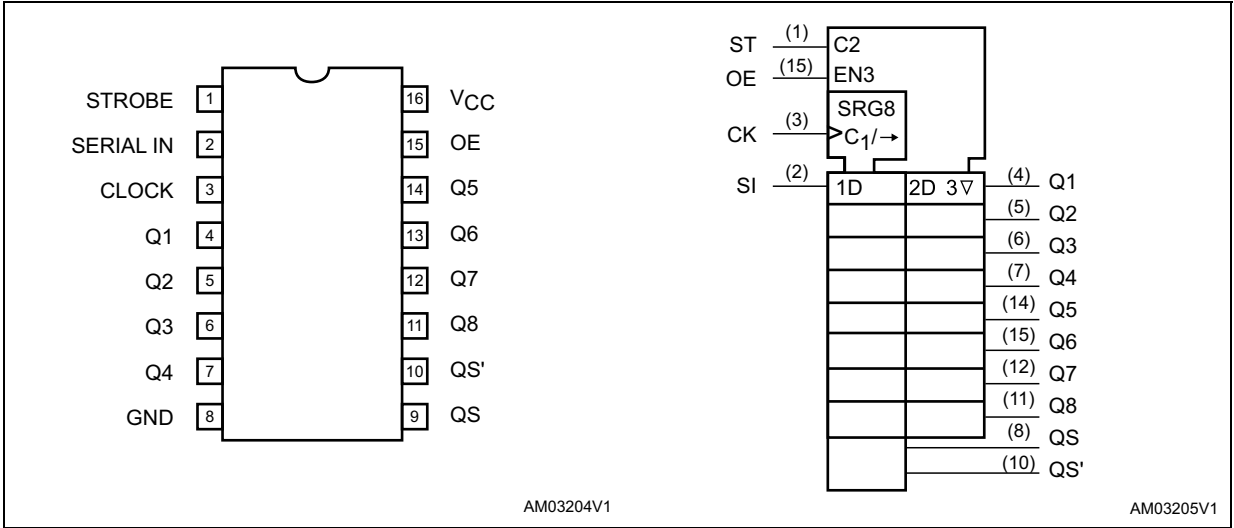
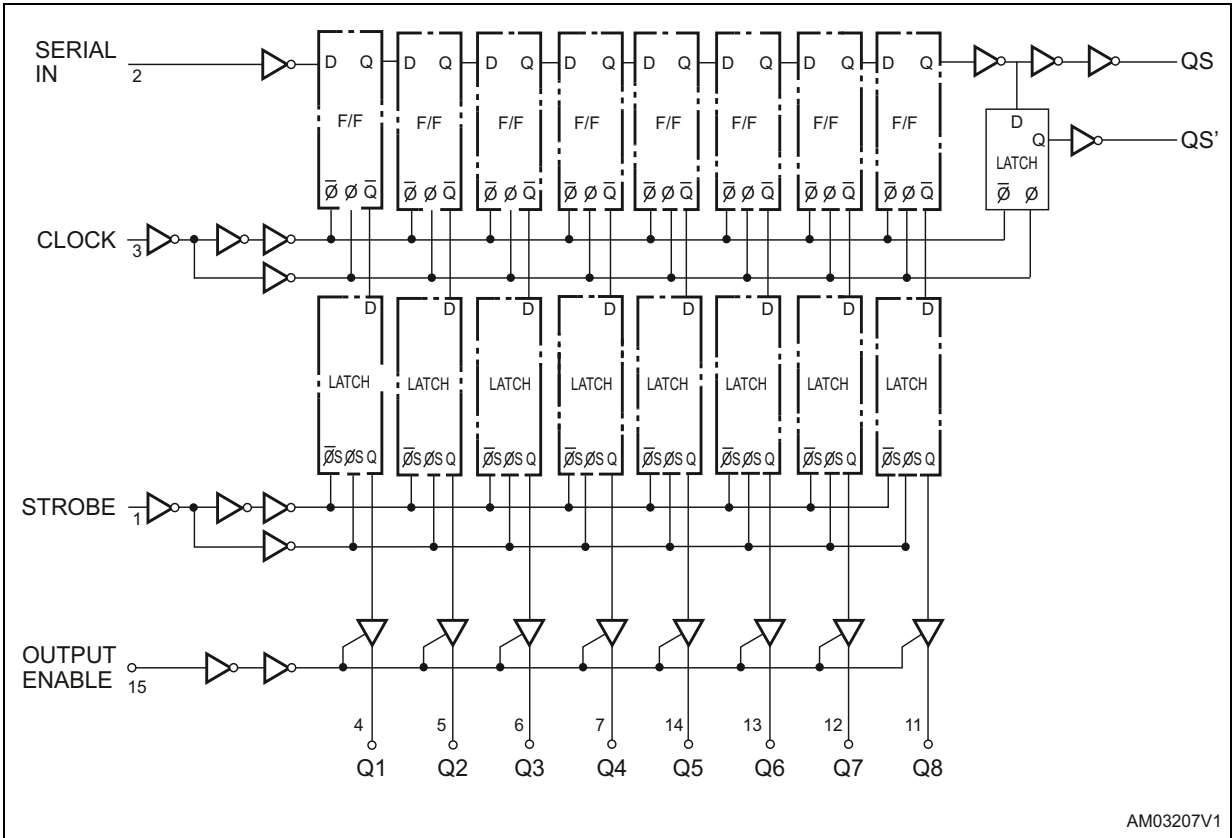


Table 2. Pin description

Pin no	Symbol	Name and function
1	STROBE	Strobe input
2	SERIAL IN	Serial input
3	CLOCK	Clock input
4, 5, 6, 7, 14, 13, 12, 11	Q1 to Q7	Parallel outputs
9, 10	QS, QS'	Serial outputs
15	OE	Output enable input
8	GND	Ground (0 V)
16	V _{CC}	Positive supply voltage

2 Functional description

Figure 2. Logic diagram



1. This logic diagram has not be used to estimate propagation delays.

Table 3. Truth table⁽¹⁾

CK	OE	ST	SI	Parallel outputs		Serial outputs	
				Q1	Qn	QS	QS'
	H	H	L	L	Qn-1	Q7	NC
	H	H	H	H	Qn-1	Q7	NC
	H	L	X	NC	NC	Q7	NC
	L	X	X	Z	Z	Q7	NC
	H	X	X	NC	NC	NC	QS
	L	X	X	Z	Z	NC	QS

1. X: don't care
Z: high impedance
NC: no change.

Figure 3. Input and output equivalent circuit

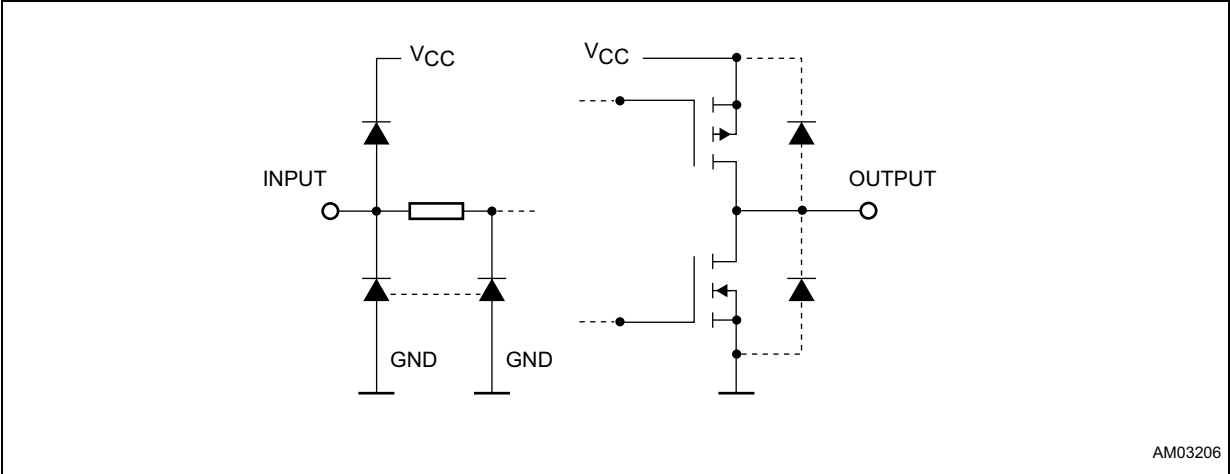
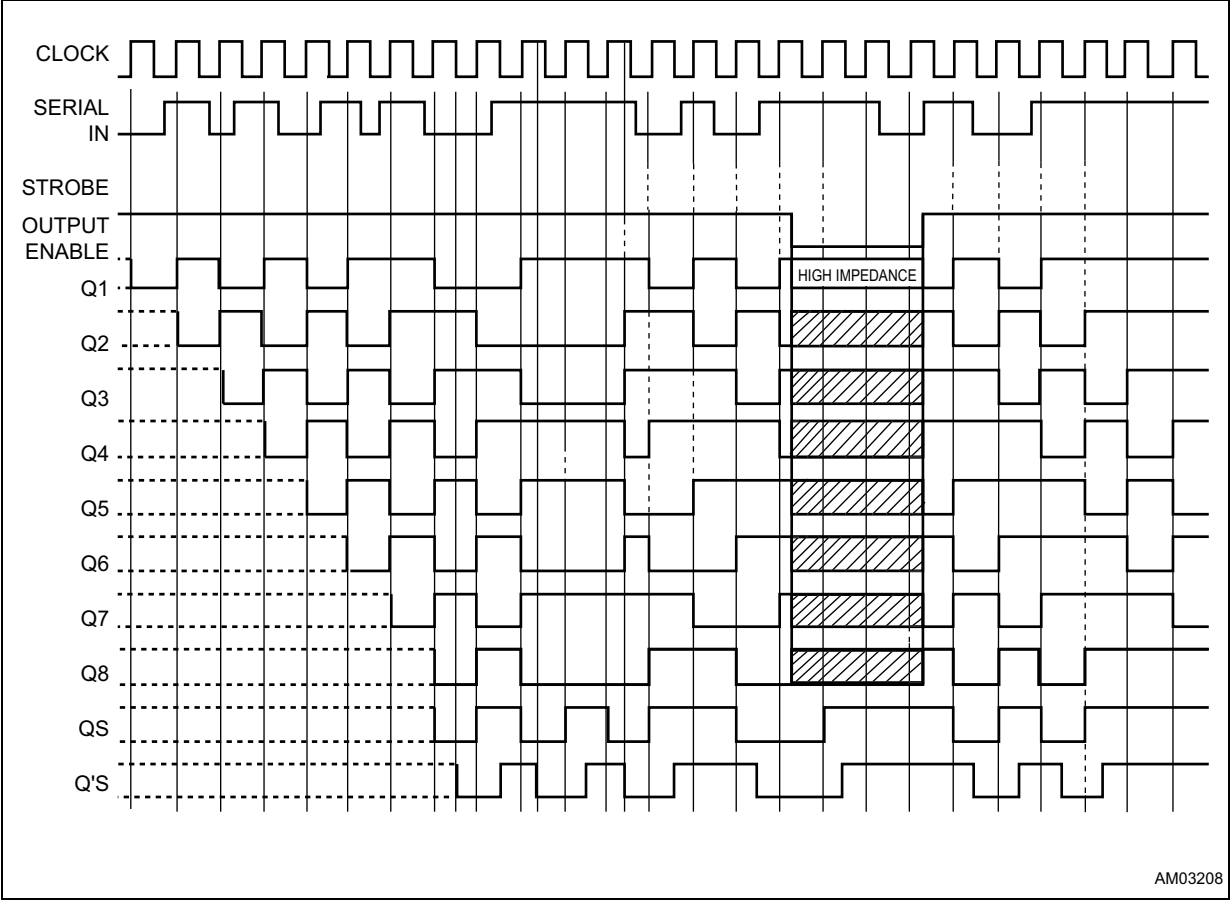


Figure 4. Timing chart



3 Electrical description

Table 4. Absolute maximum ratings⁽¹⁾

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	± 20	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 50	mA
P_D	Power dissipation	500 ⁽²⁾	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec.)	300	°C

1. Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
2. 500 mW at 65 °C; derate to 300 mW by 10 mW/°C from 65 °C to 85 °C.

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		2 to 6	V
V_I	Input voltage		0 to V_{CC}	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-55 to 125	°C
t_r, t_f	Input rise and fall time	$V_{CC} = 2.0 \text{ V}$	0 to 1000	ns
		$V_{CC} = 4.5 \text{ V}$	0 to 500	ns
		$V_{CC} = 6.0 \text{ V}$	0 to 400	ns

Table 6. DC specifications

Symbol	Parameter	Test condition		Value								Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High level input voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low level input voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High level output voltage	2.0	I _O = -20 μA	1.9	2.0		1.9		1.9		V	
		4.5	I _O = -20 μA	4.4	4.5		4.4		4.4			
		6.0	I _O = -20 μA	5.9	6.0		5.9		5.9			
		4.5	I _O = -4.0 mA	4.18	4.31		4.13		4.10			
		6.0	I _O = -5.2 mA	5.68	5.8		5.63		5.60			
V _{OL}	Low level output voltage	2.0	I _O = 20 μA		0.0	0.1		0.1		0.1	V	
		4.5	I _O = 20 μA		0.0	0.1		0.1		0.1		
		6.0	I _O = 20 μA		0.0	0.1		0.1		0.1		
		4.5	I _O = 4.0 mA		0.17	0.26		0.33		0.40		
		6.0	I _O = 5.2 mA		0.18	0.26		0.33		0.40		
I _I	Input leakage current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{OZ}	High impedance output leakage current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.5		±5		±10	μA	
I _{CC}	Quiescent supply current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

Table 7. AC electrical characteristics ($C_L = 50$ pF, input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test condition		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} , t _{THL}	Output transition time	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			7	13		16		20	
t _{PLH} , t _{PHL}	Propagation delay time (CLOCK - Qn)	2.0			92	200		250		300	ns
		4.5			26	40		50		60	
		6.0			20	34		43		51	
t _{PLH} , t _{PHL}	Propagation delay time (CLOCK - QS, QS')	2.0			65	150		190		225	ns
		4.5			19	30		38		45	
		6.0			15	26		32		38	
t _{PLH} , t _{PHL}	Propagation delay time (STROBE - Qn)	2.0			75	160		200		240	ns
		4.5			20	32		40		48	
		6.0			16	27		34		41	
t _{PZL} , t _{PZH}	High impedance output enable time	2.0			58	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
t _{PHZ} , t _{PLZ}	High impedance output disable time	2.0			35	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
f _{MAX}	Maximum clock frequency	2.0		6	16		4.8		4		MHz
		4.5		30	66		24		20		
		6.0		35	80		28		24		
t _{W(H)} , t _{W(L)}	Minimum pulse width	2.0			17	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t _{W(L)}	Minimum pulse width	2.0			28	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t _s	Minimum set-up time (SERIAL INPUT)	2.0			30	75		95		110	ns
		4.5			7	15		19		22	
		6.0			5	13		16		19	

Table 7. AC electrical characteristics ($C_L = 50$ pF, input $t_r = t_f = 6$ ns) (continued)

Symbol	Parameter	Test condition		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _s	Minimum set-up time (STROBE)	2.0			45	100		125		145	ns
		4.5			10	20		25		29	
		6.0			8	17		21		25	
t _h	Minimum hold time (SI, ST)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	

Table 8. Capacitive characteristics

Symbol	Parameter	Test condition		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input capacitance	5.0			5	10		10		10	pF
C _{PD}	Power dissipation capacitance ⁽¹⁾	5.0			140						pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to [Figure 5: Test circuit](#)). Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per flip-flop).

Figure 5. Test circuit

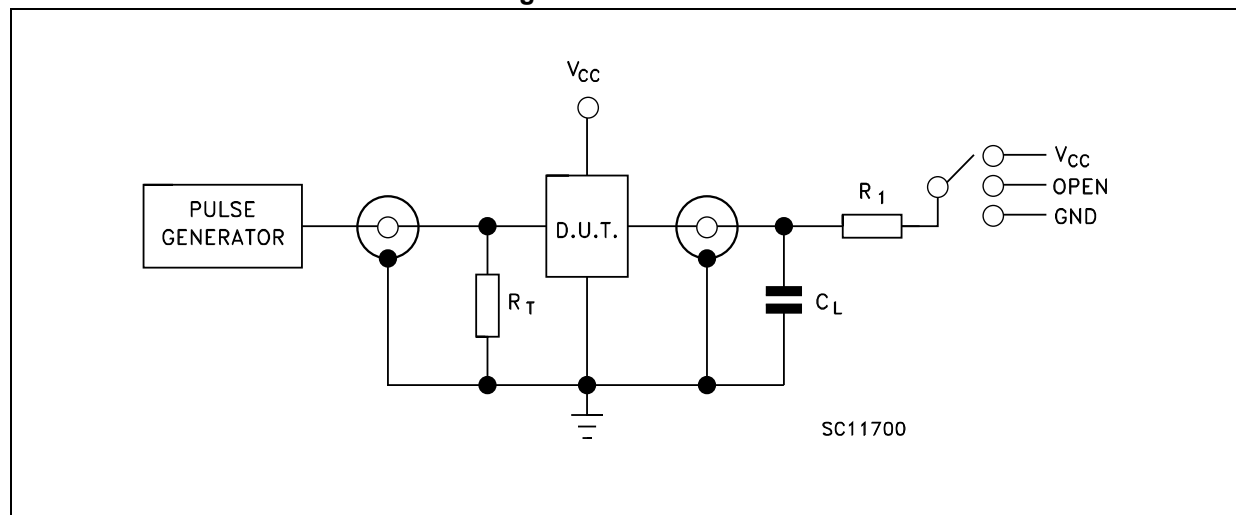


Table 9. Propagation delay time configuration

Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_{CC}
t_{PZH} , t_{PHZ}	GND

Note: $C_L = 50\text{ pF}/150\text{ pF}$ or equivalent (includes jig and probe capacitance).
 $R_1 = 1\text{ K}\Omega$ or equivalent.
 $R_T = Z_{OUT}$ of pulse generator (typically $50\ \Omega$).

Figure 6. Waveform 1 - propagation delay times, minimum pulse width (CLOCK), setup and hold times (CLOCK) (f = 1 MHz; 50% duty cycle)

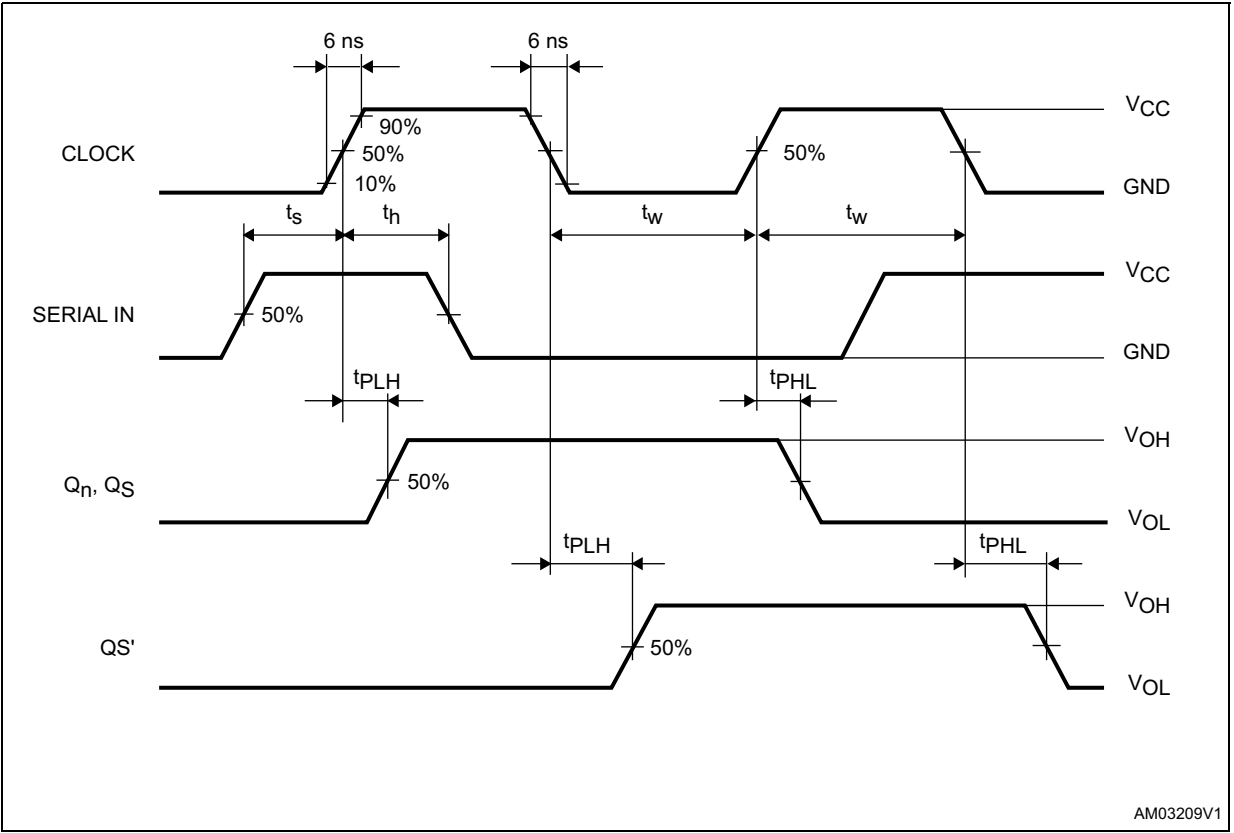


Figure 7. Waveform 2 - propagation delay times, minimum pulse width (STROBE), setup and hold times (STROBE) ($f = 1\text{ MHz}$; 50% duty cycle)

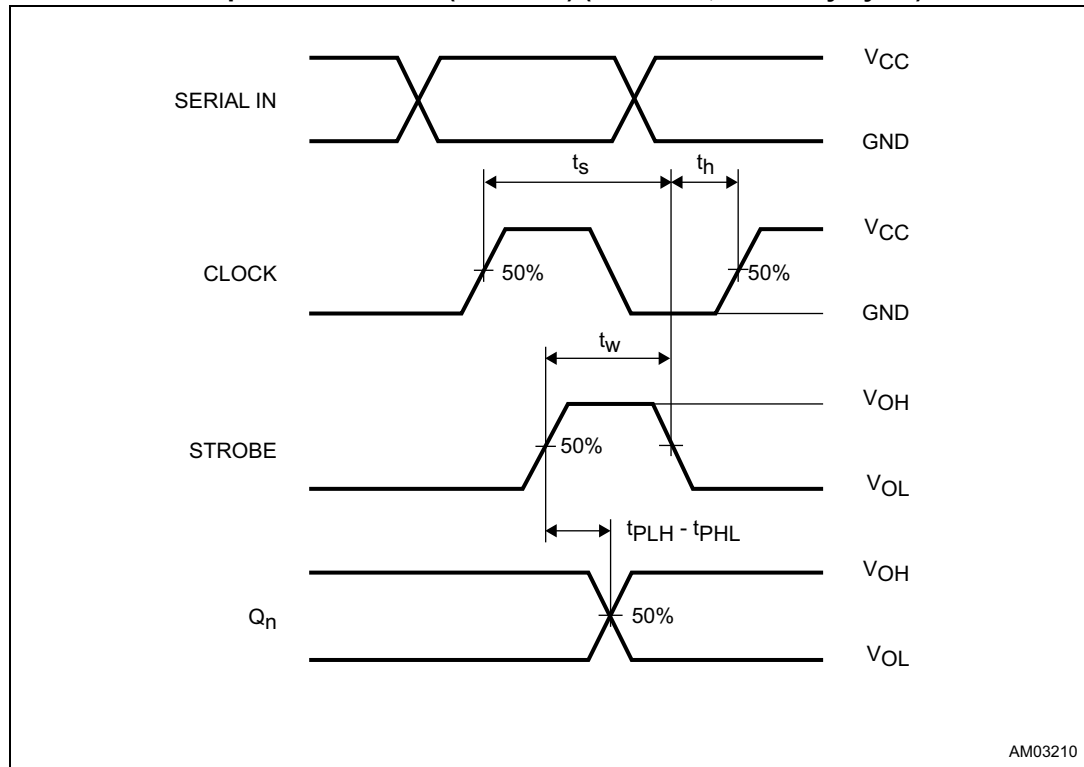
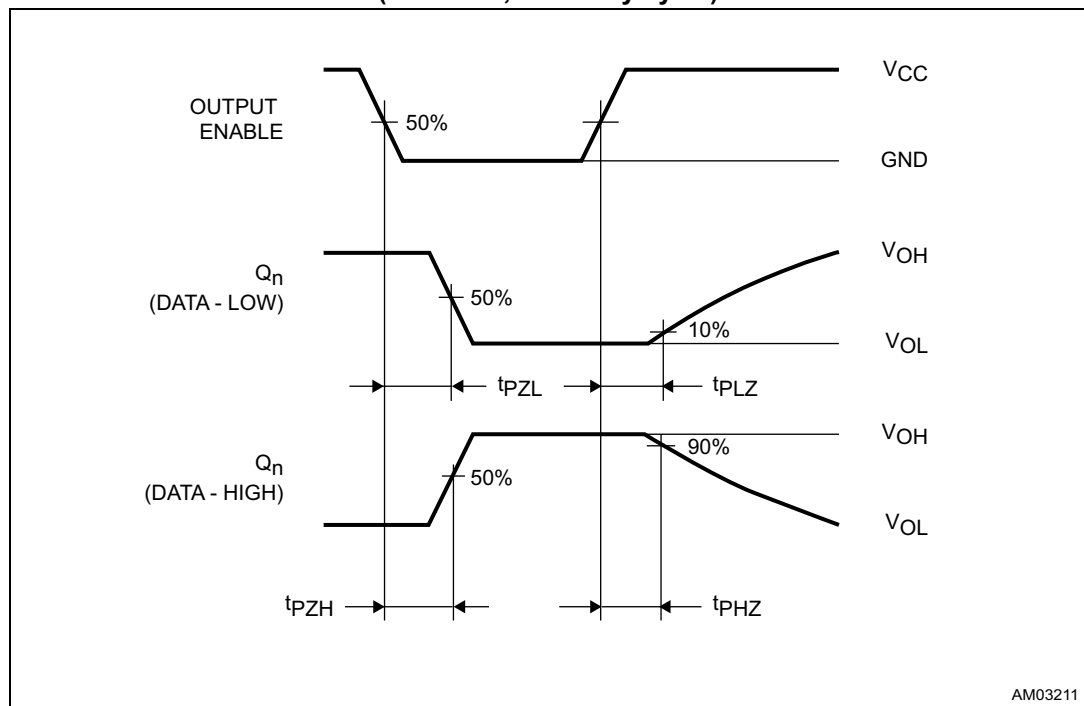


Figure 8. Waveform 3 - OUTPUT ENABLE and DISABLE times ($f = 1\text{ MHz}$; 50% duty cycle)



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DIP16 package information

Figure 9. DIP16 (0.25) package mechanical drawing

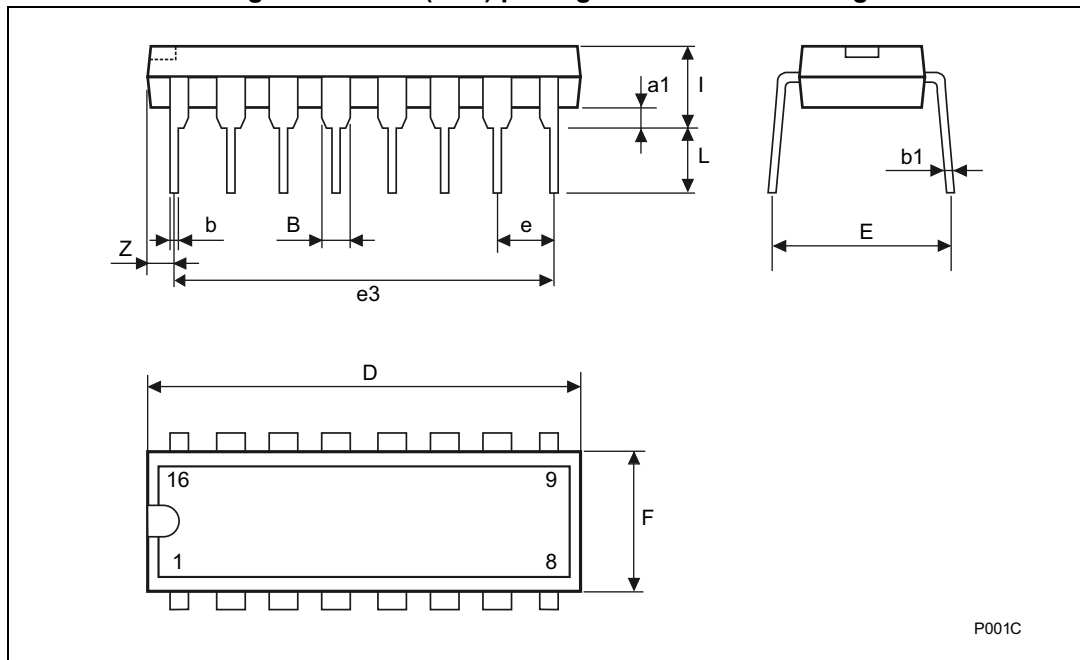


Table 10. DIP16 (0.25) package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

4.2 SO16 package information

Figure 10. SO16 package mechanical drawing

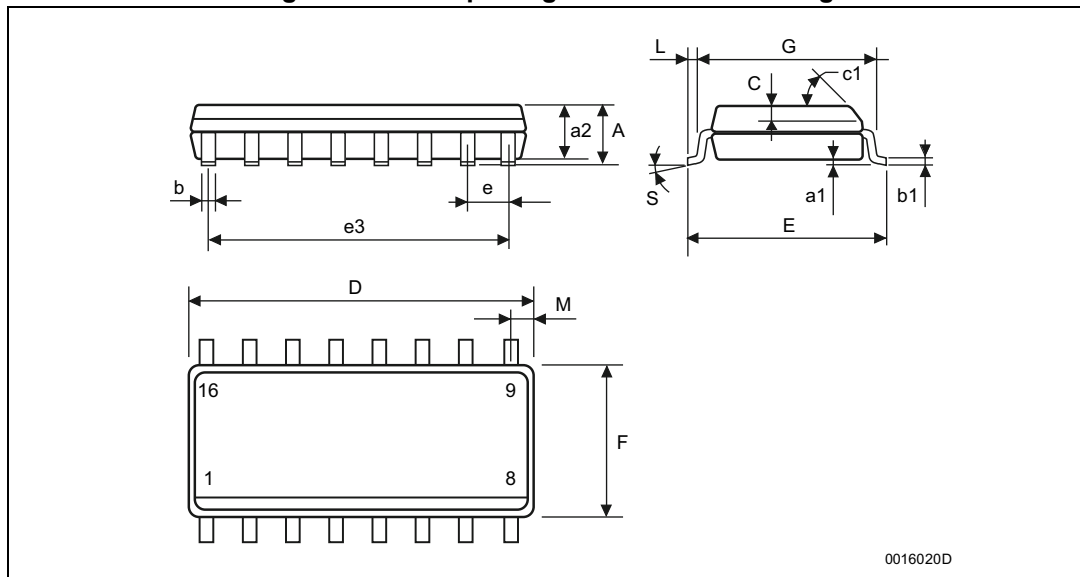


Table 11. SO16 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.004		0.008
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					

4.3 TSSOP16 package information

Figure 11. TSSOP16 package mechanical drawing

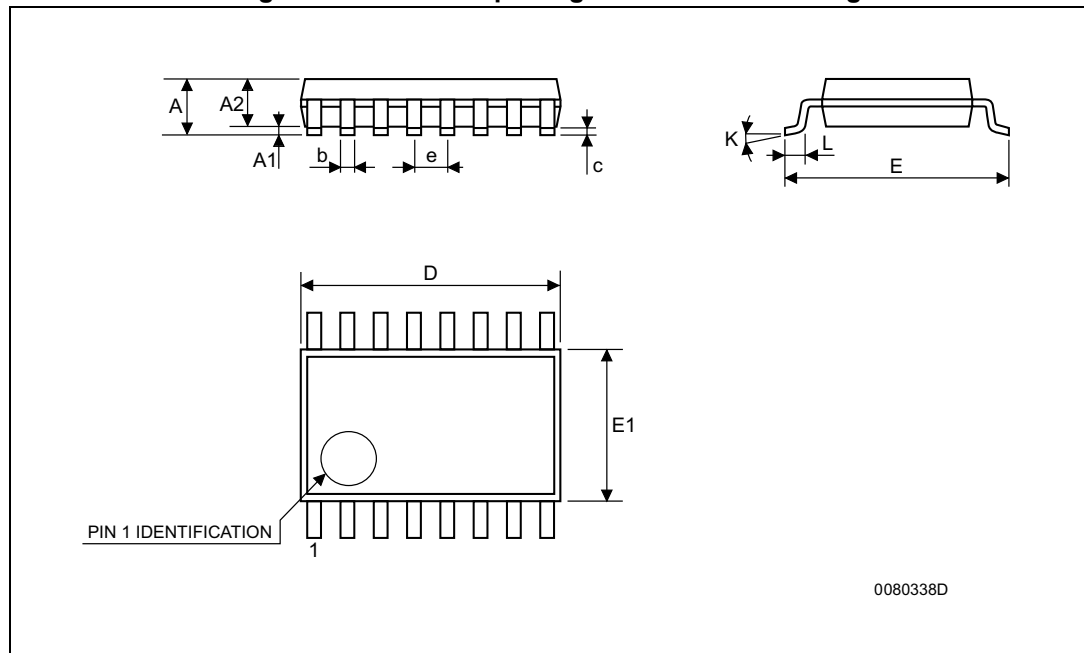


Table 12. TSSOP16 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5.5	.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

5 Ordering information

Table 13. Order codes

Order code	Temperature range	Package	Packaging	Marking
M74HC4094RM13TR	-55/+125 °C	SO16	Tape and reel	74HC4094
M74HC4094YRM13TR ⁽¹⁾	-40/+125 °C	SO16 (automotive grade)		
M74HC4094TTR	-55/+125 °C	TSSOP16		HC4094
M74HC4094YTTR ⁽¹⁾	-40/+125 °C	TSSOP16 (automotive grade)		
M74HC4094B1R	-55/+125 °C	DIP16	Tube	M74HC4094B1

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent are ongoing.

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
15-Apr-2013	3	Added Applications to page 1. Updated Table 1 (updated data, removed M74HC4094M1R order code, added M74HC4094RM13TR, M74HC4094YRM13TR, M74HC4094TTR, and M74HC4094YTTR order code, temperature range, marking, updated package and packaging). Redrawn Figure 1 to Figure 4 and Figure 6 to Figure 8. Moved Figure 1 to page 3. Added Contents. Added titles to Section 1 to Section 6 (reformatted Section 1 and Section 2). Added title to Table 9. Added cross-reference to note 1. below Table 8. Added ECOPACK text to Section 4, reformatted Section 4 (reversed order of figures and tables, added titles to Table 10 to Table 12 and Figure 9 to Figure 12). Added Table 14. Minor corrections throughout document.
12-Aug-2013	4	Features: added ESD data Table 1: updated marking of automotive order codes. Added Section 5: Ordering information

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