iSSI20R02H, iSSI20R03H, iSSI20R11H, iSSI30R11H, iSSI30R12H
Infineon's coreless-transformer advanced solid-state isolators

Features

- Solid-state isolators using Infineon's coreless-transformer technology
- No isolated gate bias supply required for gate driving
- Perfect match for CoolMOS™, OptiMOS™, and TRENCHSTOP™ IGBT
- Low power, large input voltage range from 2.6 V to 3.5 V (internally clamped)
- High-impedance, CMOS input (buffered variants)
- High output voltage up to 18 V - no series or parallel configuration required for powerful gate driving
- High output peak current of 175 µA (direct drive variants) or 400 mA (buffered variants)
- Fast turn-off for safe switches' SOA operation
- Temperature sensor and current sensor protection inputs
- Latch-off in case of a failure event (overcurrent or over-temperature)
- Dynamic Miller clamping protection
- Wide-body package with high creepage and clearance for UL 1577 and reinforced isolation according to IEC 60747-17 (planned)

Potential applications

- Solid-state relay AC and DC applications
- Electro-mechanical relay replacements
- Programmable logic control, industrial automation, and controls
- Smart building and home automation systems (thermostat, lighting, heating control)
- Instrumentation equipment

PG-DSO-8-66

PG-DSO-16-33

Product validation

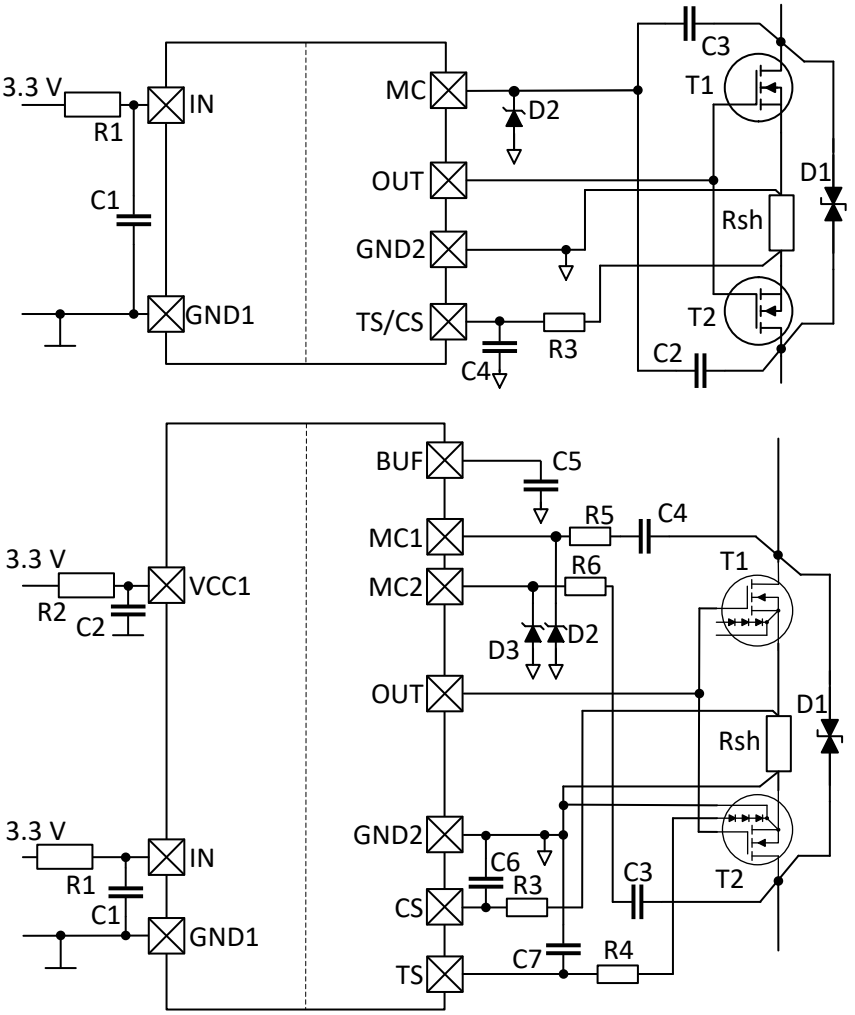
Qualified for industrial applications according to relevant tests of JEDEC47/20/22.

Description

The Infineon SSI solid-state isolator family provides powerful energy transmission over a galvanic isolation barrier to drive the gates of MOS-controlled power transistors, such as CoolMOS™, OptiMOS™, TRENCHSTOP™ IGBT, or CoolSiC™. The output side of the Infineon SSI solid-state isolator family does not require a dedicated voltage supply to drive the power transistor's gate. The output side offers advanced control functions such as fast turn-on, fast turn-off, overcurrent protection and over-temperature protection to easily and safely build up solid-state relays for various applications. The Infineon SSI family includes iSSI30R12H which is tailored for CoolMOS™ S7 T-sense power MOSFETs offering an integrated temperature sensor. Other parts of the family are for use with external PTC resistors. The Infineon SSI family offers precise protection functions for building cost effective systems. The input side of the isolator is 3.3 V compatible and operates with a supply current of typically 16 mA.

The variants iSSI20R02H, iSSI20R03H, and iSSI20R11H come in a DSO-8-66 package while iSSI30R11H and iSSI30R12H come in a DSO-16-33 package.

The isolation is IEC 60747-17 (planned) certified for reinforced isolation and UL 1577 compliant.



Product type	Protection features	Fast turn-on	Certification	Marking	Package
iSSI20R02H	OCP or OTP (PTC), DMC	No	IEC 60747-17, UL1577	I20R02	PG-DSO-8-66
iSSI20R03H	OCP, OTP (PTC)	No	IEC 60747-17, UL1577	I20R03	PG-DSO-8-66
iSSI20R11H	OCP or OTP (PTC)	Yes	IEC 60747-17, UL1577	I20R11	PG-DSO-8-66
iSSI30R11H	OCP, OTP (PTC), DMC	Yes	IEC 60747-17, UL1577	I30R11	PG-DSO-16-33
iSSI30R12H	OCP, OTP (diode), DMC	Yes	IEC 60747-17, UL1577	I30R12	PG-DSO-16-33

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1 Block diagrams

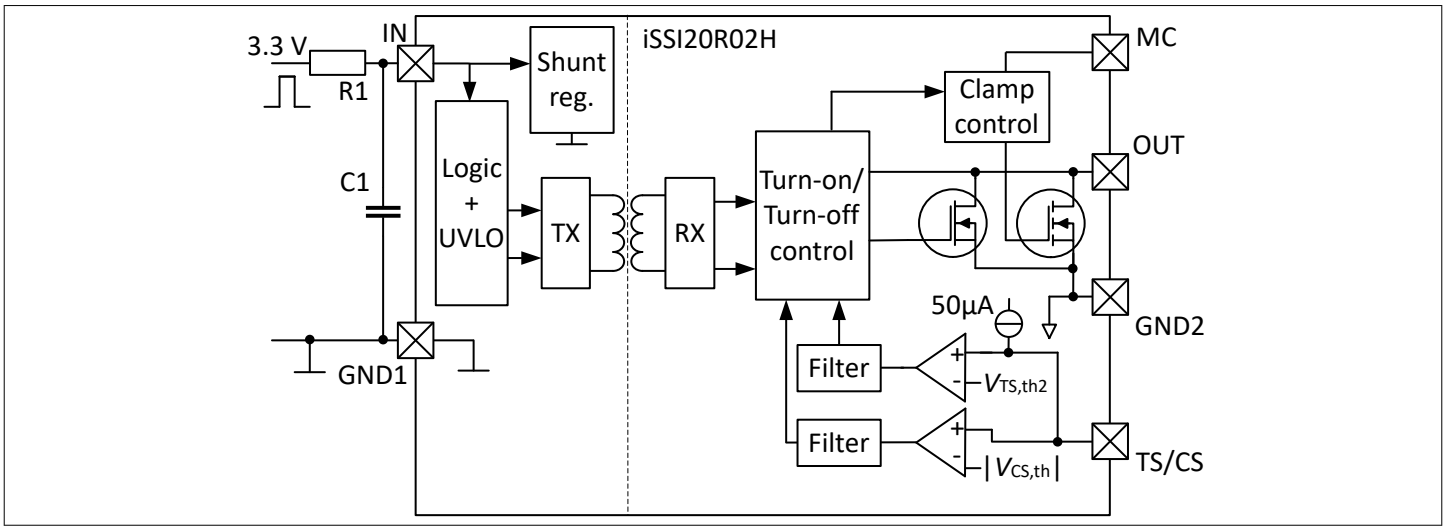


Figure 1 Block diagram of iSSI20R02H

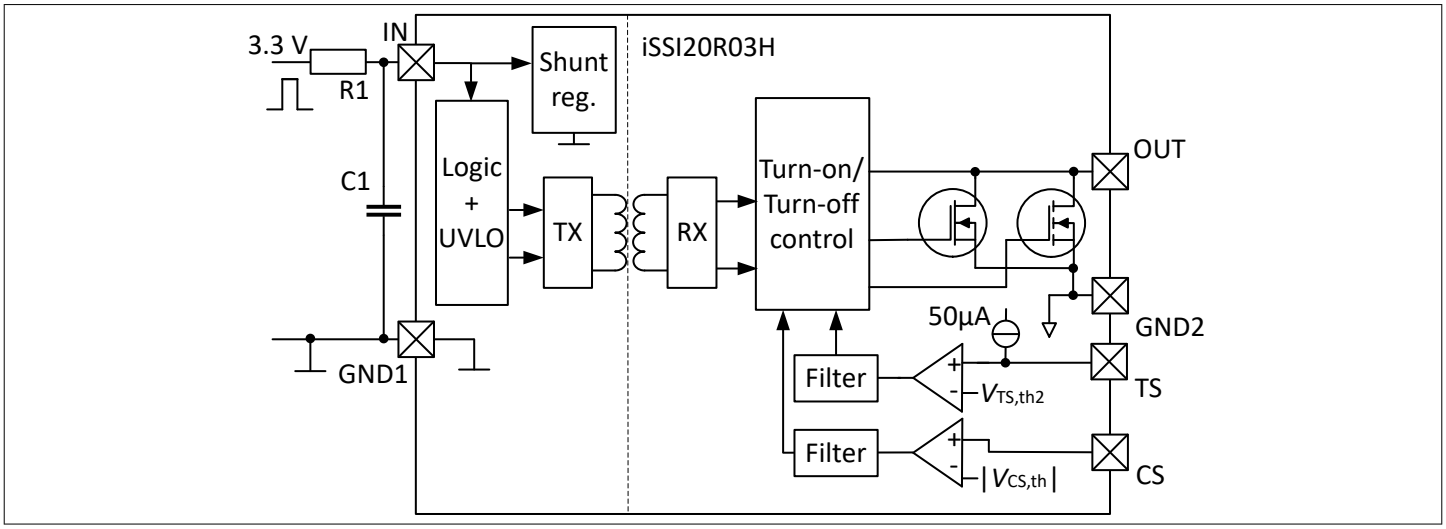


Figure 2 Block diagram of iSSI20R03H

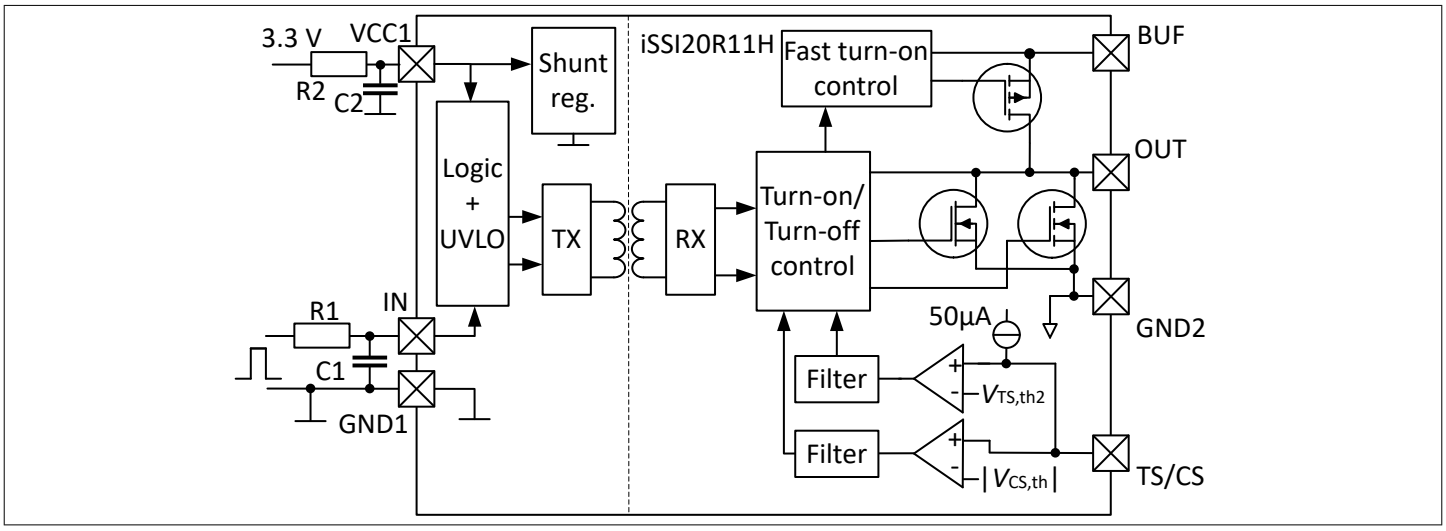


Figure 3 Block diagram of iSSI20R11H

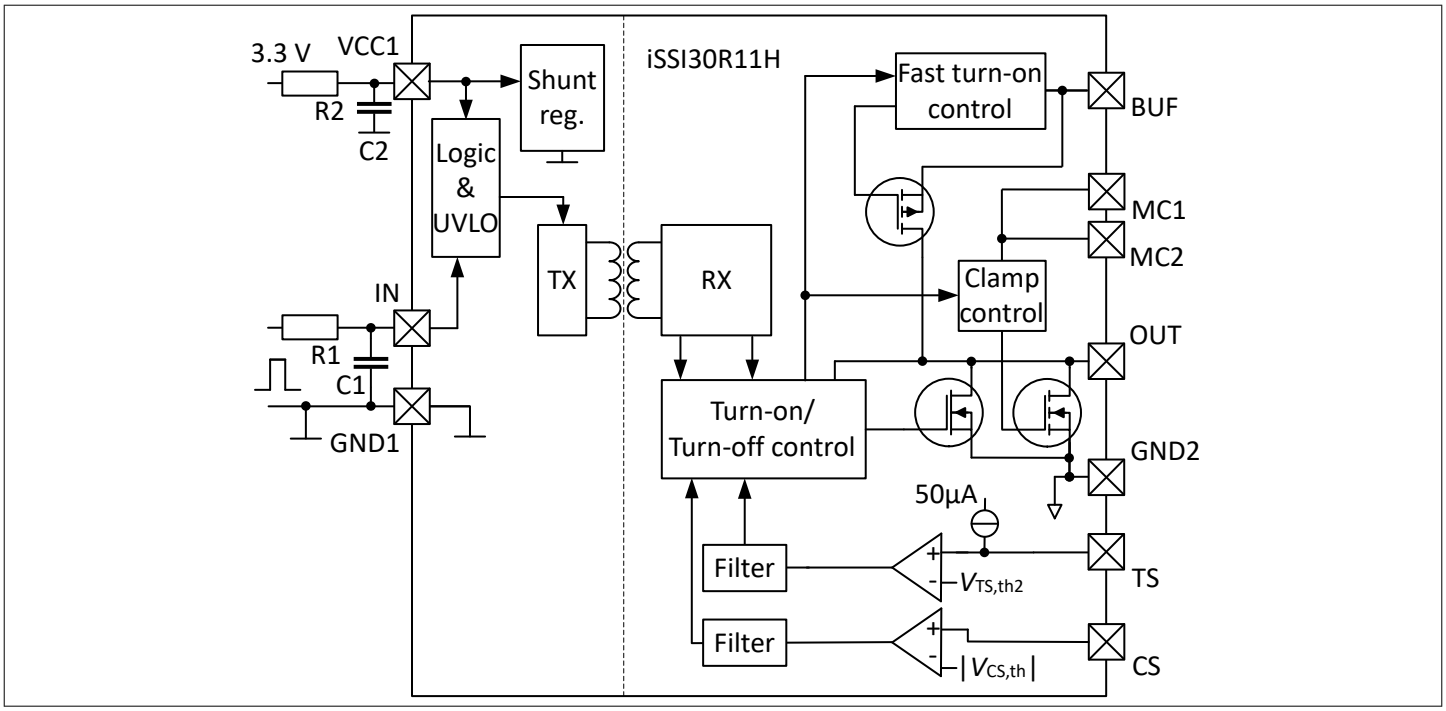


Figure 4 Block diagram of iSSI30R11H

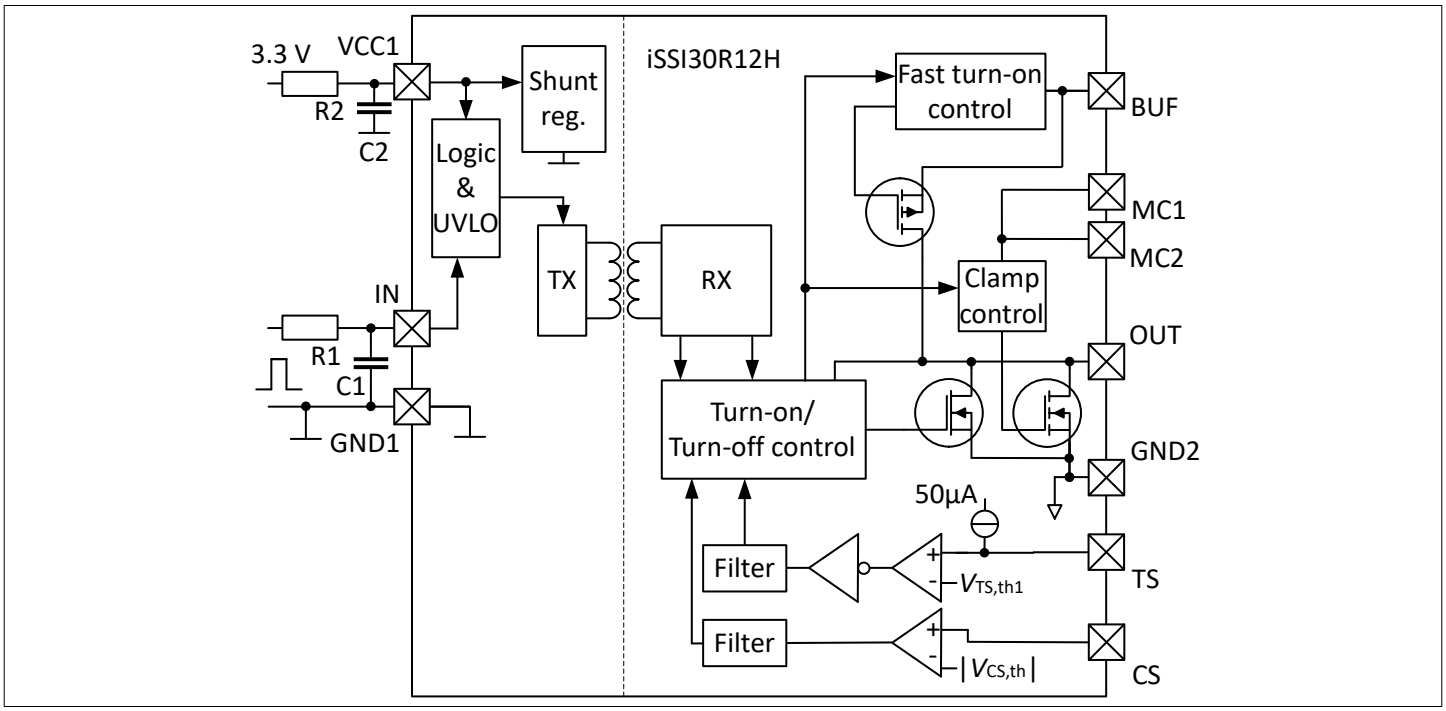


Figure 5 Block diagram of iSSI30R12H

2 Pin configuration

2.1 Pin configuration

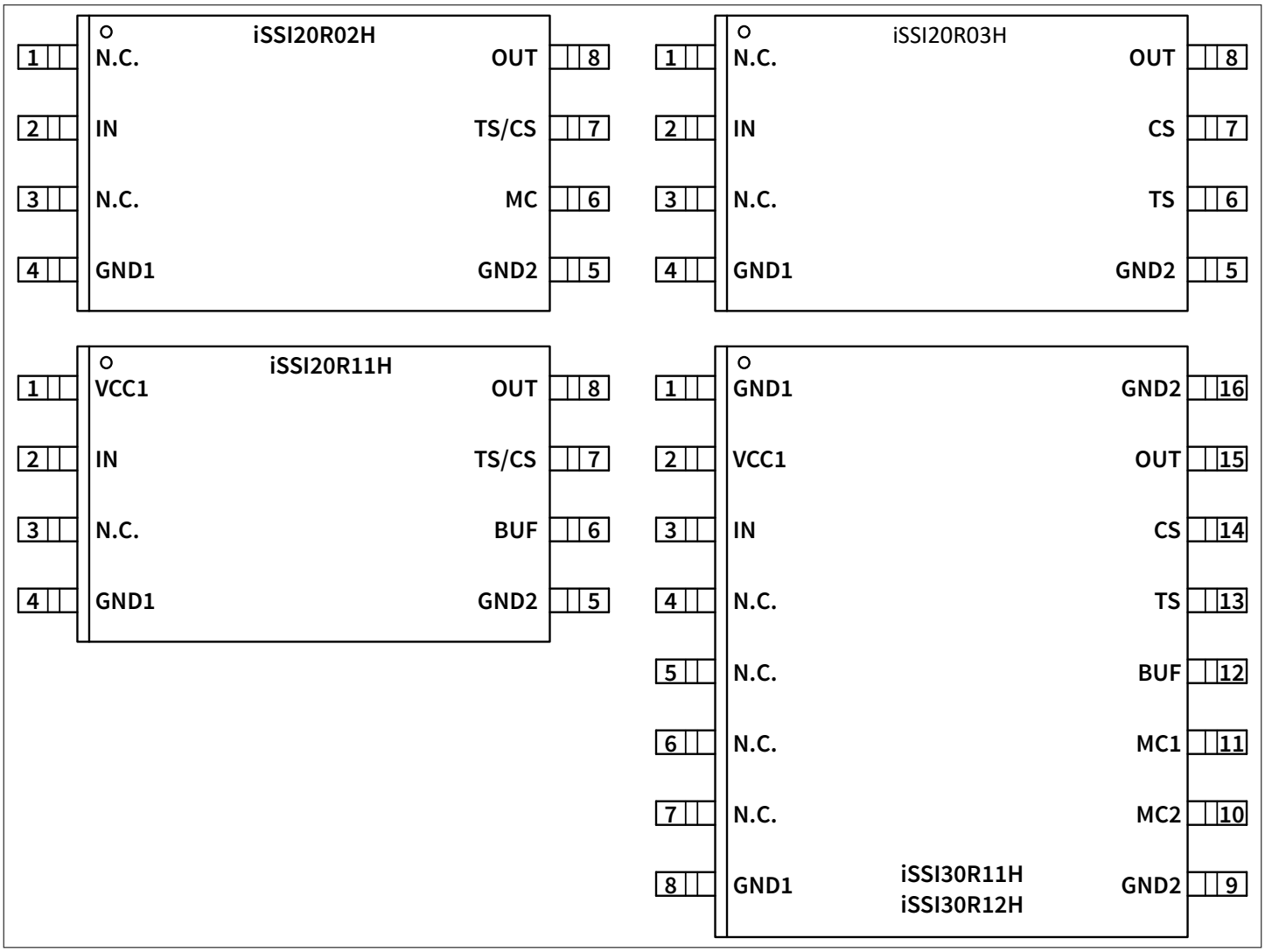


Figure 6 Pin configuration of Infineon SSI family

Table 1 Pin configuration for iSSI20R02H

Pin no.	Pin name	Pin type	Function
1	*N.C.*	-	Not connected
2	*IN*	PWR	Supply and non-inverting control input
3	*N.C.*	-	Not connected
4	*GND1*	PWR	Reference of control side
5	*GND2*	PWR	Reference of output side
6	*MC*	I	Miller clamp input
7	*TS/CS*	I/O	Output for temperature sensor bias current and input for sensed signal
8	*OUT*	O	Gate drive output

Table 2 Pin configuration for iSSI20R03H

Pin no.	Pin name	Pin type	Function
1	*N.C.*	-	Not connected
2	*IN*	PWR	Supply and non-inverting control input
3	*N.C.*	-	Not connected
4	*GND1*	PWR	Reference of control side
5	*GND2*	PWR	Reference of output side
6	*TS*	I/o	Output for temperature sensor bias current and input for temperature signal
7	*CS*	I	Input for current-sense signal
8	*OUT*	O	Gate drive output

Table 3 Pin configuration for iSSI20R11H

Pin no.	Pin name	Pin type	Function
1	*VCC1*	PWR	Supply input
2	*IN*	I	Non-inverting control input
3	*N.C.*	-	Not connected
4	*GND1*	PWR	Reference of control side
5	*GND2*	PWR	Reference of output side
6	*BUF*	I/O	Output for buffer charges and input for fast turn-on
7	*TS/CS*	I/O	Output for temperature sensor bias current and input for sensed signal
8	*OUT*	O	Gate drive output

Table 4 Pin configuration for iSSI30R11H and iSSI30R12H

Pin no.	Pin name	Pin type	Function
1	*GND1*	PWR	Reference of control side
2	*VCC1*	PWR	Supply input
3	*IN*	I	Non-inverting control input
4	*N.C.*	-	Not connected
5	*N.C.*	-	Not connected
6	*N.C.*	-	Not connected
7	*N.C.*	-	Not connected
8	*GND1*	PWR	Reference of control side
9	*GND2*	PWR	Reference of output side
10	MC2	I	Dynamic Miller clamp input 1
11	MC1	I	Dynamic Miller clamp input 2
12	*BUF*	I/O	Output for buffer charges and input for fast turn-on

(table continues...)

Table 4 (continued) Pin configuration for iSSI30R11H and iSSI30R12H

Pin no.	Pin name	Pin type	Function
13	*TS*	I/O	Output for temperature sensor bias current and input for sensed signal
14	*CS*	I	Input for current sense signal
15	*OUT*	O	Gate drive output
16	*GND2*	PWR	Reference of output side

2.2 Pin description

- *VCC1*: Supply of input side; best operated with 3.3 V; can be shorted to terminal *IN*; referenced to GND1.
- *IN*: Logic input for variants iSSI20R11H, iSSI30R11H and iSSI30R12H, can be shorted to *VCC1*. It is the input supply pin for variants iSSI20R02H and iSSI20R03H. Pin is referenced to *GND1*
- *GND1:* Reference pin for *VCC1* and *IN*.
- *GND2*: Reference pin for *MC*, *MC1*, *MC2*, *CS*, *TS*, *TS/CS*, *OUT* and *BUF*.
- *MC*, *MC1*, *MC2*: Input pins for dynamic Miller clamp. Keep these pins unconnected for deactivating the dynamic Miller clamp. Referenced to *GND2*.
- *CS*: Current sense input. When unused, it is recommended to connect to *GND2*. Referenced to *GND2*.
- *TS*: Temperature sense input. When unused, it is recommended for variant iSSI30R12H to let the pin float and for all other variants, it is recommended to connect to *GND2*. Referenced to *GND2*.
- *TS/CS*: Pin can be used either as temperature sense input or as current sense input. When unused, it is recommended to connect to *GND2*. Referenced to *GND2*.
- *OUT*: Gate drive output. Referenced to *GND2*.
- *BUF*: Gate drive buffer. Typically, a capacitor is connected to implement the fast turn-on feature. Referenced to *GND2*.

3 Electrical characteristics and parameters

3.1 Absolute maximum ratings

Table 5 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output offset voltage	V_{OFFSET}	-1200	–	1200	V	$V_{offset} = \|V_{GND1} - V_{GND2}\|$ [1]
Input supply voltage	V_{IN} V_{VCC1}	-10	-	4.25	V	iSSI20R02H, iSSI20R03H iSSI20R11H, iSSI30R11H, iSSI30R12H
Input logic voltage (terminal IN)	$V_{IN,logic}$	-10	-	15	V	Reference to GND1
Output voltage at terminal OUT	V_{OUT}	-0.3		20	V	[2]
Voltage at terminal MC	V_{MC}	-0.3		3.6	V	[2]
Voltage at terminals TS, CS or TS/CS (static)	V_{TS}, V_{CS} $V_{TS/CS}$	-1.2		4	V	[2]
Voltage at terminals CS, TS and TS/CS (positive signals, dynamic)	$V_{pin,dyn}$	0	-	6	V	[2] $0 < I_{pin,dyn} < 10$ mA, $t_p < 2$ µs, $d < 0.001$
Voltage at terminals CS, TS and TS/CS (negative signals, dynamic)	$V_{pin,dyn}$	-2	-	0	V	[2] $0 > I_{pin,dyn} > -10$ mA, $t_p < 2$ µs, $d < 0.001$
Voltage at terminal BUF	V_{BUF}	-0.3		20	V	[2]
Input supply current	I_{IN} I_{VCC1}	0	-	120	mA	iSSI20R02H, iSSI20R03H iSSI20R11H, iSSI30R11H, iSSI30R12H
Current at terminal OUT (static)	I_{OUT}	-10		10	mA	Output deactivated
Current at terminal OUT (dynamic)	$I_{OUT,dyn}$	-100	-	100	mA	Output deactivated; $t_p < 10$ µs for negative current pulses; $t_p <$ 1 µs for positive current pulses
Current at terminal MC (static)	I_{MC}	-6		6	mA	[2]
Current at terminal MC (dynamic)	$I_{MC,dyn}$	-100		100	mA	$t_p < 1$ µs; $d < 1\%$
Current at terminal TS	I_{TS}	-1		1	mA	[2]
Current at terminal CS or TS/CS	I_{CS}, $I_{TS/CS}$	-1		1	mA	[2]
Current at terminal BUF (static)	I_{BUF}	-10		10	mA	
Current at terminal BUF (dynamic)	$I_{BUF,dyn}$	-1		1	A	$t_p < 1$ µs
Power dissipation input part	P_{DIN}			200	mW	$T_A = 85$°C [3] [4]
Power dissipation output part	P_{DOUT}			4.5	mW	$T_A = 85$°C [5] [6]
Thermal resistance junction-to-ambient	R_{THJA}			140 96	K/W	$T_A = 85$°C, PG DSO-8-66, 2s2p footprint only $T_A = 85$°C, PG DSO-16-33, 2s2p footprint only

(table continues...)

Table 5 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Characterization parameter junction-to-package top	Ψ_{Jtop}			39.77 35.30	K/W	T_A = 85°C, PG-DSO-8-66, 2s2p footprint only T_A = 85°C, PG-DSO-16-33, 2s2p footprint only
ESD robustness - human body model	$\lvert V_{ESD,HBM}\rvert$	2			kV	7)
ESD robustness - charged device model	*ESD,CDM*	–	–	TC 1000	–	8)
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{ST}	-55		150	°C	
Maximum switching frequency	f_{SW}	-	-	2	kHz	C_{Load} = 100 pF, V_{IN} = 3.3 V, V_{VCC1} = 3.3 V (where appropriate)

1) For functional operation only
2) Reference to GND2.
3) PG-DSO-8-66: derating of power above T_j = 122°C with 7.14 mW/°C, layout 2s2p (JESD 51-5 / JESD 51-7).
4) PG-DSO-16-33: derating of power above T_j = 130.8°C with 10.42 mW/°C, layout 2s2p (JESD 51-5 / JESD 51-7).
5) PG-DSO-8-66: derating of power above T_j = 149.3°C with 7.14 mW/°C, layout 2s2p (JESD 51-5 / JESD 51-7).
6) PG-DSO-16-33: derating of power above T_j = 149.5°C with 10.42 mW/°C, layout 2s2p (JESD 51-5 / JESD 51-7).
7) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
8) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = highest test condition passed according to AEC-Q100-011 Rev D).

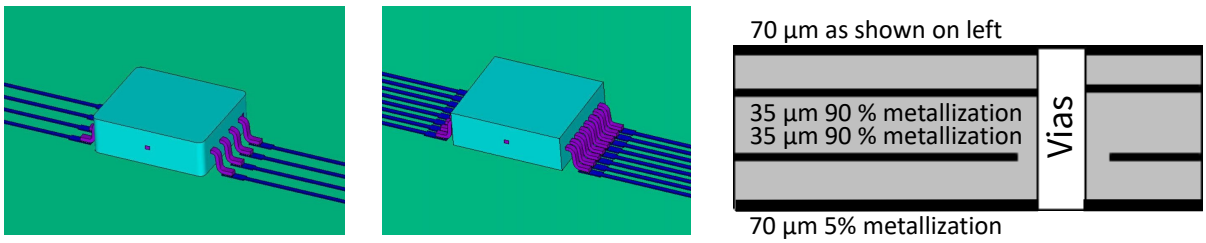


Figure 7 Thermal reference design

3.2 Operating parameters

Table 6 Operating parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input supply voltage (terminal VCC1 (or IN if VCC1 is absent))	V_{VCC1}	2.85	3.3	3.5	V	–
Voltage at terminals TS, CS, or TS/CS (static)	V_{TS}, V_{CS} $V_{TS/CS}$	-0.5		2.7	V	1)

(table continues...)

Table 6 (continued) Operating parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External input supply capacitance including tolerances of the capacitor	$C_{VCC1,ext}$	-	-	4.7	nF	
External capacitance at terminal TS including tolerances of the capacitor (variant iSSI30R12H)	$C_{TS,ext}$	-	-	1.5	nF	
Ambient temperature	T_A	-40	–	125	°C	–
Junction temperature	T_J	-40	–	125	°C	–
Common-mode transient immunity	$\|dv_{CM}/dt\|$			200	V/ns	

1) Reference to GND2

3.3 Electrical characteristics

The minimum and maximum electrical characteristics include the spread of values over supply voltages and temperatures within the operating parameters. Electrical characteristics are tested in production at T_A = 25°C and the default load at terminal OUT is 100 pF. Typical values represent the median values measured at supply voltage V_{IN} = 3.3 V (or V_{VCC1} = 3.3 V where applicable) and T_A = 25°C. Minimum and maximum characteristics are verified by characterization/design. All voltages are referenced to their respective GND (GND1 for input side pins and GND2 for output side pins). This is valid for all electrical characteristics unless specified otherwise.

3.3.1 IC Supply

Table 7 IC Supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO threshold input side (power up)	V_{UVLOH1}	2.7	2.775	2.85	V	
UVLO threshold input side (power down)	V_{UVLOL1}	2.6	2.68	2.75	V	Reference to GND1
UVLO hysteresis input side	V_{HYS1}	89	-	-	mV	*1)* V_{UVLOH1}- V_{UVLOL1}
Supply current input side at terminal IN (or VCC1 where available)	I_{IN}	14	16	19	mA	V_{IN} = 3.3 V, I_{OUT} = 0
Standby input supply current at terminal VCC1	$I_{IN,STBY}$	-	1.4	2.5	mA	V_{VCC1} = 3.3 V, V_{IN} = 0
Integrated supply bias resistance	$R_{VCC1,bias}$	2.45		7.14	Ω	
Reverse supply resistance	$R_{VCC1,rev}$ $R_{IN,rev}$	1 0.17	-	-	MΩ	iSSI30R11H and iSSI30R12H, V_{test} = -2.5 V iSSI20R02H, iSSI20R03H, iSSI20R11H, V_{test} = -2.5 V
Off-time before turn-on	$t_{OFF,IN}$ $t_{OFF,VCC1}$	25	-	-	µs	*1)* V_{IN} < V_{UVLOL1} (or V_{VCC1} < V_{UVLOL1} where applicable)

1) Parameter is not subject to production test - verified by design/characterization.

3.3.2 Logic input (iSSI20R11H, iSSI30R11H, iSSI30R12H)

Table 8 Logic input (iSSI20R11H, iSSI30R11H, iSSI30R12H)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IN logic low input threshold voltage	V_{IL}	1.0	1.2	-	V	Reference to GND1
IN logic high input threshold voltage	V_{IH}		2.1	2.3	V	
IN logic low/high hysteresis	$V_{IN,HYS}$	0.7			V	
IN logic pull down resistor	$R_{IN,PD}$	200	-	-	kΩ	V_{IN} = 2.5 V
Off-time before turn-on	$t_{OFF,IN}$	25	-	-	µs	1) V_{VCC1} = 3.3 V, V_{IN} < $V_{IL,min}$

1) Parameter is not subject to production test - verified by design/characterization.

3.3.3 Gate drive

Table 9 Gate drive

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output voltage	V_{OUT}	10	15	20	V	1) V_{IN} = 3.3 V, I_{OUT} = 0
Output voltage	V_{OUT}	10	13	16	V	1) V_{IN} = 2.6 V, I_{OUT} = 0
Short circuit output current (iSSI20R02H, iSSI20R03H)	I_{OUT}	100	175	-	µA	V_{IN} = 3.3 V, V_{OUT} = 0
Short circuit output current (iSSI20R11H, iSSI30R11H, iSSI30R12H)	I_{OUT}	150	325	550	µA	V_{IN} = 3.3 V, V_{OUT} = 0
Turn-off current	$I_{off,sat}$	50	160	270	mA	2) V_{IN} = 0 V, V_{OUT} = 5 V
Fast turn-off transistor saturation current	$I_{off,fast,sat}$	488	-	-	mA	2) V_{IN} = 3.3 V, V_{CS} = 0.3 V, V_{OUT} = 5 V
High-level output resistance	R_{OH}	60	110	155	kΩ	V_{IN} = 3.3 V, ΔV_{OUT} = 1 V, iSSI20R02H, iSSI20R03H
High-level output resistance	R_{OH}	48	95	135	kΩ	V_{IN} = 3.3 V, ΔV_{OUT} = 1 V, iSSI20R11H, iSSI30R11H, iSSI30R12H
Low-level output resistance	R_{OL}	5	8.5	12	Ω	V_{VCC1} = 0, V_{OUT} < 0.5 V
Turn-on propagation delay terminal IN and VCC1 (where applicable) to terminal OUT or BUF (where applicable)	t_{PDON}	-	-	20	µs	V_{IN} = 3.3 V, V_{VCC1} = 3.3 V (where applicable), no load
Turn-off propagation delay	t_{PDOFF}	0.3	3	6	µs	V_{IN} = 0, no load, V_{VCC1} = 3.3 V (where applicable)

(table continues...)

Table 9 (continued) Gate drive

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise time	t_r, $t_{r,BUF}$	-	8	15	µs	V_{VCC1} = 3.3 V (where appropriate), V_{IN} = 3.3 V, no load
Fall time	t_f	-	1.9	4	µs	Supply at VCC1: V_{VCC1} = 3.3 V, V_{IN} ≤ 1 V, C_{BUF} = 3 nF, no load Supply at IN: V_{IN} ≤ 2.6 V
Fall time	t_f	1	3.2	6.5	µs	Supply at VCC1: V_{VCC1} = 3.3 V, V_{IN} ≤ 1 V, C_L = 10 nF Supply at IN: V_{IN} ≤ 2.6 V, C_L = 10 nF

1) Reference to GND2.
2) Parameter is not subject to production test - verified by design/characterization.

3.3.4 Fast turn-on (iSSI20R11H, iSSI30R11H, iSSI30R12H)

Table 10 Fast turn-on (iSSI20R11H, iSSI30R11H, iSSI30R12H)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fast turn-on threshold (power up)	$V_{BUF,th}$	10.0	10.4	10.8	V	*1)*
Fast turn-on saturation current	$I_{on,fast,sat}$	232	400	-	mA	*2)* V_{OUT} = 5 V, V_{BUF} = 10.4 V
Resistance between terminal BUF and OUT after fast turn-on	$R_{BUF-OUT}$	300	500	-	kΩ	*2)*
Fast turn-on propagation delay input-to-output	$t_{PDON,fast}$	-	5	-	ms	*2)* C_{BUF} = 33 nF, C_{OUT} = 5.6 nF, V_{OUT} = 1 V
Fast turn-on rise time	$t_{r,fast}$	-	530	1000	ns	*2)* C_{BUF} = 48 nF, C_{OUT} = 10 nF

1) Reference to GND2.
2) Parameter is not subject to production test - verified by design/characterization.

3.3.5 Dynamic Miller clamping

Table 11 Dynamic Miller clamping

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Dynamic Miller clamp saturation current	I_{CLAMP}	500	1700	-	mA	*1)* V_{MC} = 2.5 V; V_{OUT} = 3 V
Low-level output resistance during dynamic Miller clamping	$R_{OL,MC}$	0.7	1.5	3.5	Ω	V_{MC} = 2.5 V, I_{OUT} = 10 mA
Input resistance terminal MC	R_{MC}	400	500	600	Ω	V_{VCC1} = 0, V_{MC} = 0.5 V

1) Parameter is not subject to production test - verified by design/characterization.

3.3.6 Over-temperature protection

Table 12 Over-temperature protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Temperature sense comparator threshold (iSSI30R12H)	$V_{TS,th1}$	1.056	1.095	1.120	V	[1] V_{IN} = 3.3 V
Temperature sense comparator threshold (other variants)	$V_{TS,th2}$	190	200	210	mV	[1] V_{IN} = 3.3 V
Temperature sense bias current (terminals TS and TS/CS)	$I_{TS,bias}$ $I_{TS/CS,bias}$	40	50	60	µA	V_{IN} = V_{VCC1} = 3.3 V
Temperature sense protection propagation delay	$t_{PD,TS}$	-	-	5	µs	V_{IN} = 3.3 V, C_{Load} ≤ 100 pF, V_{TS} = $V_{TS,th2}$ -20 mV (iSSI30R12H), V_{TS} = $V_{TS,th1}$ +20 mV (other variants)
Temperature sense filter time	$t_{TS,filter}$	1.9 0.12	2.7 0.15	3.5 0.175	µs	[2] V_{VCC1} = 3.3 V, V_{TS} = $V_{TS,th2}$ -20 mV (iSSI30R12H), V_{VCC1} = 3.3 V, V_{TS} = $V_{TS,th1}$ +20 mV (other variants)
Fast turn-off fall time after OTP trigger	$t_{f,TS}$	-	-	725	ns	[2] C_{OUT} = 28 nF, V_{OUT} = 12 V

1) Reference to GND2.
2) Parameter is not subject to production test - verified by design/characterization.

3.3.7 Overcurrent protection

Table 13 Overcurrent protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overcurrent comparator shut down threshold	$\|V_{CS,th}\|$	185	200	215	mV	[1] V_{VCC1} = 3.3 V; Output is active;
Overcurrent shut-down delay	$t_{CS,off}$	-	0.6	1	µs	V_{CS} = 300 mV, V_{OUT} = 2.5 V
Overcurrent filter time	$t_{CS,filter}$	120	150	175	ns	[2] $\|v_{CS}\|$ = 0.3 V
Fast turn-off fall time after OCP trigger	$t_{f,CS}$	-	-	725	ns	[2] C_{OUT} = 28 nF, V_{OUT} = 12 V, $\|dv_{CS}/dt\|$ > 480 mV/µs

1) Reference to GND2.
2) Parameter is not subject to production test - verified by design/characterization.

4 Insulation and safety-related specification

4.1 Safety-limiting values

Note: safety-limiting values define the operating conditions under which the isolation barrier can be guaranteed to stay unaffected. This corresponds with the maximum allowed junction temperature, as temperature-induced failures might cause significant overheating and eventually damage the isolation barrier.

Parameter	Symbol	Value	Unit	Note or condition
iSSI20R02H, iSSI20R03H, iSSI20R11H				
Maximum ambient safety temperature	T_S	150	°C	
Safety input power dissipation	P_S	200	mW	Derating required above T_A = 122°C with 7.14 mW/°C, T_J = 150 °C
Safety input supply current	I_{SI}	50	mA	Derating required above T_A = 122 °C with 1.8 mA/°C, T_J = 150 °C
Safety output power dissipation	P_{SO}	4.5	mW	Derating required above T_A = 149.4°C with 7.14 mW/°C, T_J = 150 °C
iSSI30R11H, iSSI30R12H				
Maximum ambient safety temperature	T_S	150	°C	
Safety input power dissipation	P_{SI}	200	mW	Derating required above T_A = 130.8°C with 10.42 mW/°C, T_J = 150 °C
Safety input supply current	I_{SI}	50	mA	Derating required above T_A = 130.8 °C with 2.6 mA/°C, T_J = 150 °C
Safety output power dissipation	P_{SO}	4.5	mW	Derating required above T_A = 149.5°C with 10.42 mW/°C, T_J = 150 °C

4.2 Reinforced insulation according to IEC 60747-17 (planned)

Parameter	Symbol	Value	Unit	Note or condition
External clearance	*CLR*	>8	mm	Shortest distance in air from any input pin to any output pin according to IEC 60664-1[1)]
External creepage	*CRP*	>8	mm	Shortest distance over package surface from any input pin to any output pin according to IEC 60664-1[1)]
Comparative tracking index	*CTI*	>400	V	According to IEC 60112
Material group		II		According to IEC 60112
Pollution degree		2		According to IEC 60664-1
Overvoltage category (According to IEC 60664-1)		I - IV I - IV I - III I-II		Rated mains voltage ≤ 150 V (rms) Rated mains voltage ≤ 300 V (rms) Rated mains voltage ≤ 600 V (rms) Rated mains voltage ≤ 1000 V (rms)
Climatic category		40/125/21		

Parameter	Symbol	Value	Unit	Note or condition
Input-to-output isolation according to UL1577 Ed. 5				
Input-to-output isolation voltage	V_{ISO}	5700	V_{rms}	$V_{TEST} = V_{ISO}$ for t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ for t = 1 s (100% productive tests)
Input-to-output isolation according to IEC 60747-17 (planned)				
Maximum rated transient isolation voltage	V_{IOTM}	8000	V_{pk}	$V_{TEST} = V_{IOTM}$ for t_{ini} = 60 s (type test and sample test) $V_{TEST} = 1.2 \times V_{IOTM}$ for t_{ini} = 1 s (routine test)
Maximum rated repetitive peak isolation voltage	V_{IORM}	1200	V_{pk}	According to Time Dependent Dielectric Breakdown (TDDB) test
Apparent charge	q_{PD}	<5	pC	Method (b1) (routine test and type test pre-conditioning) $V_{PD(ini),b} = 1.2 \times V_{IOTM}$ for t_{ini} = 1 s $V_{PD(m)} = 1.875 \times V_{IORM}$ for t_m = 1 s Method (a) (type test, subgroup 1 final measurements) $V_{PD(ini),a} = V_{IOTM}$ for t_{ini} = 60 s $V_{PD(m)} = 1.6 \times V_{IORM}$ for t_m = 10 s[3]
Impulse voltage	V_{IMP}	8000	V_{pk}	
Maximum surge isolation voltage	V_{IOSM}	11000	V_{pk}	$V_{TEST} \geq 1.3 \times V_{IMP}$ (type test)[4]
Isolation resistance	R_{IO}	$>10^{12}$	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 25 °C[5]
Isolation resistance	R_{IO}	$>10^{11}$	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 125 °C[5]
Isolation resistance	R_{IO_S}	$>10^{9}$	Ω	V_{IO} = 500 V_{dc} for t = 60 s, $T_S = T_A$ = 150 °C[5]
Isolation capacitance	C_{IO}	1.9	pF	f = 1 MHz[5]

1) Creepage and clearance requirements depend on the application and related end-equipment isolation standard. Care should be taken to keep the required creepage and clearance value on printed-circuit-board level.

2) Safety certification pending.

3) The partial discharge voltage $V_{PD(m)}$ applied during productive tests is greater (tbd $V_{pk} > 1.875 \times V_{IORM}$) to include the F_4 factor (1.1) required by end-equipment standards IEC 60664-1, IEC 62368-1, IEC 60950 ($V_{PD(m)} = F_1 \times F_2 \times F_3 \times F_4 \times V_{IORM} = 1.875 \times F_4 \times V_{IORM}$). The F_3 factor (1.25) is also considered for further stress of the insulation.

4) The surge test is performed in insulation oil to determine the intrinsic surge immunity of the insulation barrier.

5) The parameters apply to the product converted in a two terminals device with all terminals on side 1 connected together and all terminals on side 2 connected together.

5 Timing diagrams

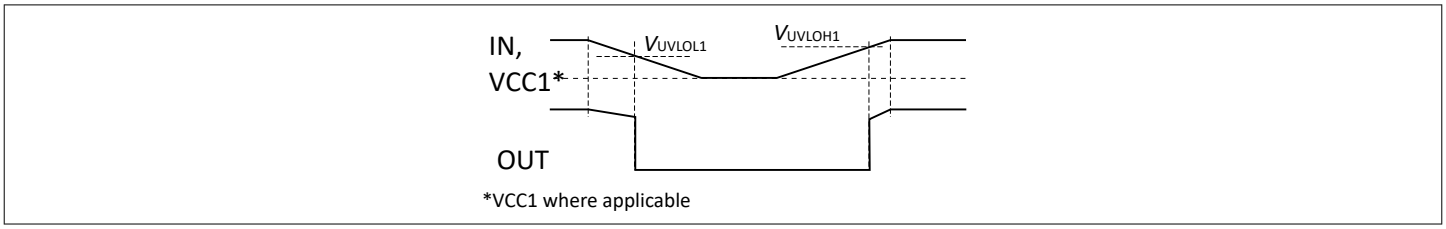


Figure 8 UVLO behavior

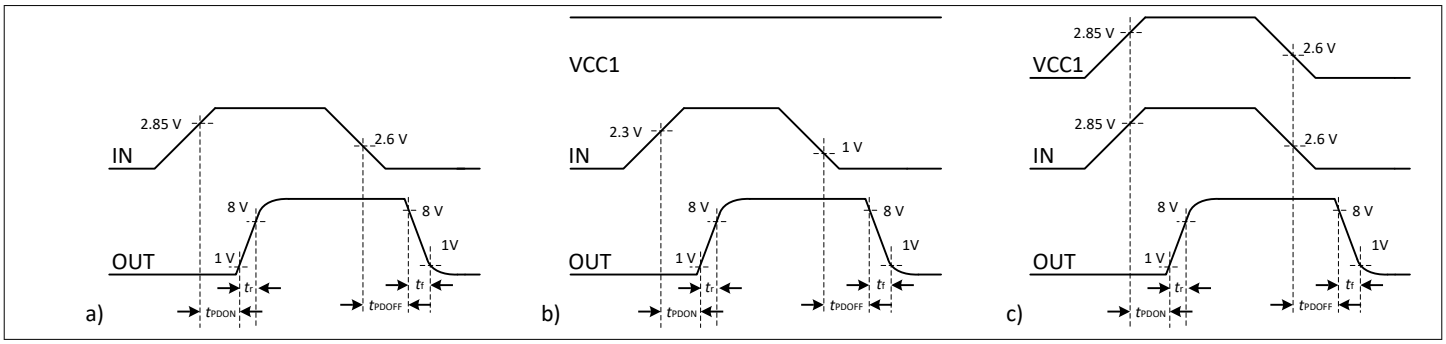


Figure 9 Direct gate drive turn-on and turn-off propagation delay, rise and fall time: a) direct drive turn-on for variants iSSI20R02H and iSSI20R03H, b) separate *VCC1* and *IN* using no buffer capacitor, c) *VCC1* and *IN* shorted using no buffer capacitor

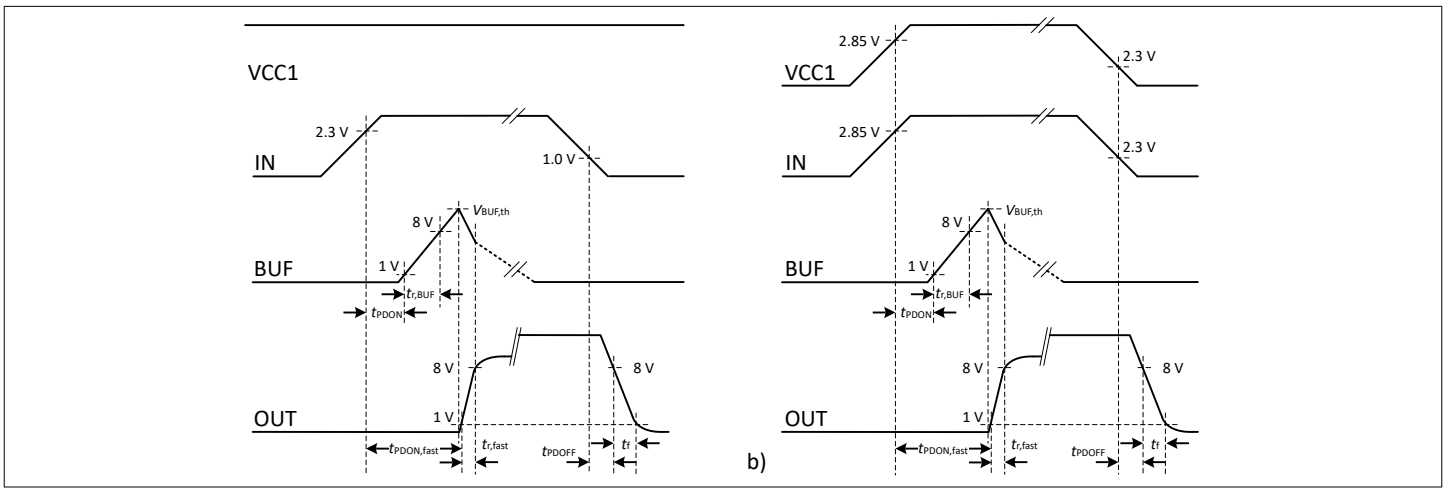


Figure 10 Fast turn-on timing using a buffer capacitor: a) separate *VCC1* and *IN*, b) *VCC1* and *IN* shorted

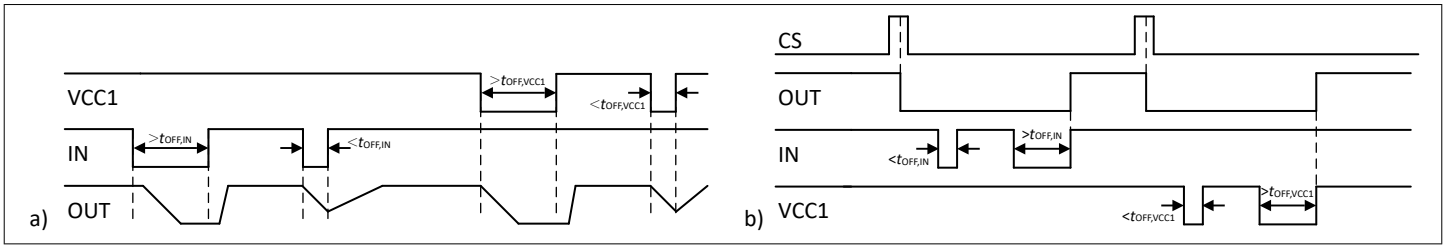


Figure 11 a) Off-time before turn-on, b) off-time after protection (example of overcurrent protection)

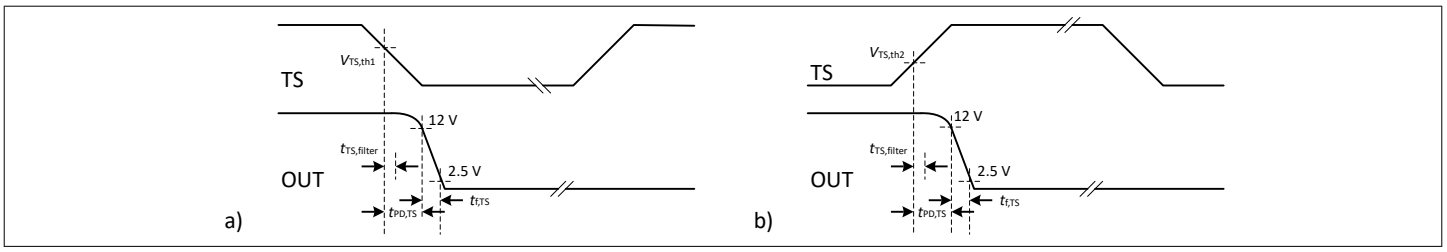


Figure 12 Over-temperature protection timing: a) iSSI30R12H, b) others

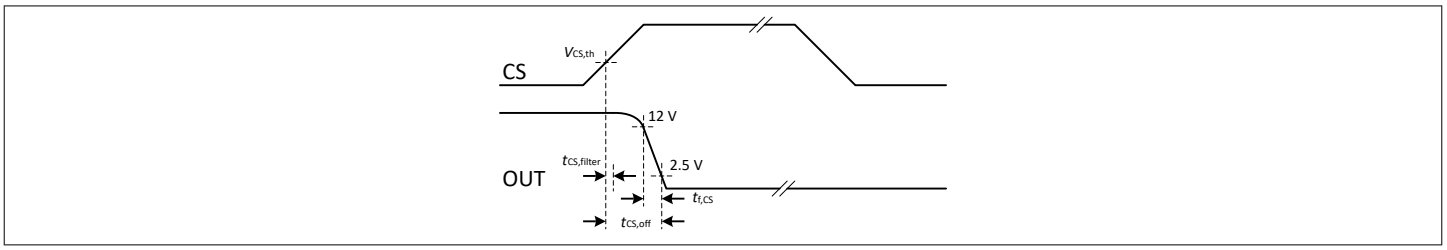


Figure 13 Overcurrent protection timing

6 Functional description

6.1 Input side

6.1.1 Input side supply

The input side of the Infineon SSI family is 3.3 V compatible and operates best with an input voltage tolerance of 5%. The power-up under-voltage threshold voltage is V_{UVLOH1}. It ensures sufficient output voltage for operating the output. The power-down under-voltage threshold is V_{UVLOL1}. The integrated supply is based on a shunt regulator that emulates a diode structure to simplify designs. The device can then be supplied even by any voltage rail that exceeds the operating range by using a current limiting resistor placed in series to the supply terminal *IN* or *VCC1* (where applicable). If no suitable resistor in series to terminal *VCC1* is used for current limitation, then staying within the operating parameters is recommended to avoid unnecessary power dissipation in the IC.

The input side of the IC contains an integrated power supply buffer capacitor. External buffer capacitors for the supply voltage are not necessary, but possible. Such external buffer capacitors should not exceed $C_{VCC1,ext}$.

In addition, the Infineon SSI family provides a strong reverse bias capability for the supply terminals *IN* or *VCC1* (where applicable). This enables all variants to operate in differential operation with respect to their terminals *IN* and *GND1*.

A minimum off-time $t_{OFF,IN}$ or $t_{OFF,VCC1}$ is required between the turn-off and turn-on signals to establish a defined "off"-state on the output side of the isolator.

Variants iSSI20R02H and iSSI20R03H use the supply terminal *IN* to perform the reset procedure after the output side latch-off procedure of the protection functions. Variants iSSI20R11H, iSSI30R11H, and iSSI30R12H can perform this reset at either at terminal *VCC1* or at terminal *IN*. In any case of reset of any variant, ensure that the reset time is larger than $t_{OFF,IN}$or $t_{OFF,VCC1}$ before turning on again after a protection event.

6.1.2 Logic input

Variants iSSI20R11H, iSSI30R11H, and iSSI30R12H offer separate supply and control terminals. The control logic thresholds V_{IL} and V_{IH} at terminal *IN* are 3.3 V CMOS compliant and can be controlled directly from standard CMOS logic outputs. Please note that the signal level at terminal *IN* can be substantially higher than the supply voltage at terminal *VCC1*. For example, it is possible to apply signals on 5 V level while V_{VCC1} = 3.3 V. The output acts in phase with the input control signal at terminal *IN*. Before turning on, a minimum off-time $t_{OFF,IN}$ has to be considered for resetting the output side. If the equivalent MOSFET's input capacitance is larger than 100 pF longer off-times than $t_{OFF,IN}$ might be needed.

A new reset procedure has to be performed after a protection triggered turn-off. Variants iSSI20R11H, iSSI30R11H, and iSSI30R12H can perform this reset at either at terminal *VCC1* or at terminal *IN*. In any case of reset of any variant, ensure that the reset time is larger than $t_{OFF,IN}$ before turning on again after a protection event.

Applications using the variants iSSI20R11H, iSSI30R11H, and iSSI30R12H can use these isolators with externally shorted terminals *VCC1* and *IN*. In this case, all operating guidelines of variants iSSI20R02H and iSSI20R03H apply.

6.2 Output side

6.2.1 Direct gate drive

Terminal *OUT* is the gate drive output. The output voltage V_{OUT} is sufficient to drive CoolMOS™, OptiMOS™, or TRENCHSTOP™ IGBT without additional, external buffers. Variants iSSI20R02 and iSSI20R03 provide the short circuit output current I_{OUT} directly to the gate. This enables a quick turn-on of MOS-controlled power transistor. Variants iSSI20R11H and iSSI30R1xH can be used in direct drive mode, as well, if the buffer capacitor is not connected.

6.2.2 Fast turn-on feature

Variants iSSI20R11H, iSSI30R11H, and iSSI30R12H provide the fast turn-on feature that further enforces the turn-on current by accumulating charge in an external buffer capacitor at terminal *BUF*. The accumulated charge is released to terminal *OUT*, if the voltage at terminal *BUF* equal or higher than the buffer threshold voltage $V_{BUF,th}$ and a turn-on condition is given on the control side.

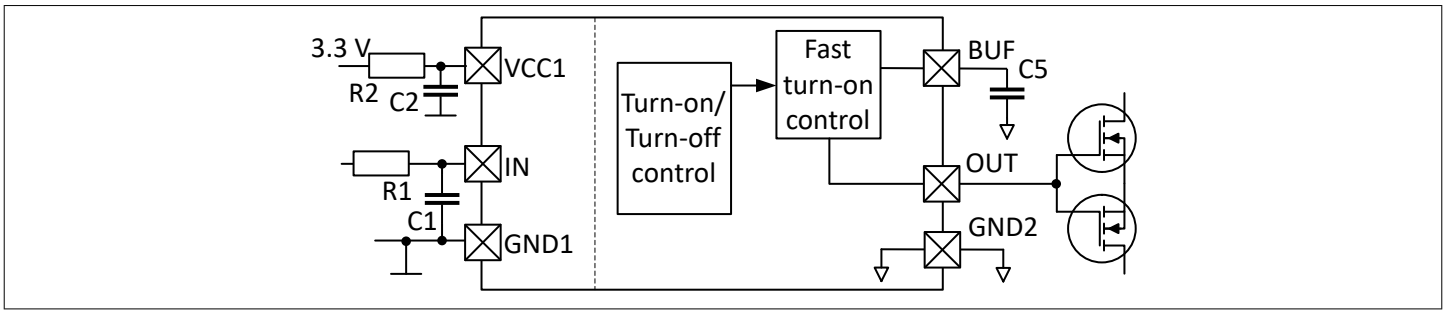


Figure 14 Fast turn-on feature of iSSI20R11H, iSSI30R11H, and iSSI30R12H

6.2.3 Normal turn-off

The normal turn-off feature is implemented in all variants. A turn-off signal from the input side activates the integrated depletion FET. The depletion FET discharges the gate node of the operated power transistor. The Infineon SSI family's sink saturation current $I_{off,sat}$ is dimensioned to discharge CoolMOS™ S7 transistors within a few microseconds.

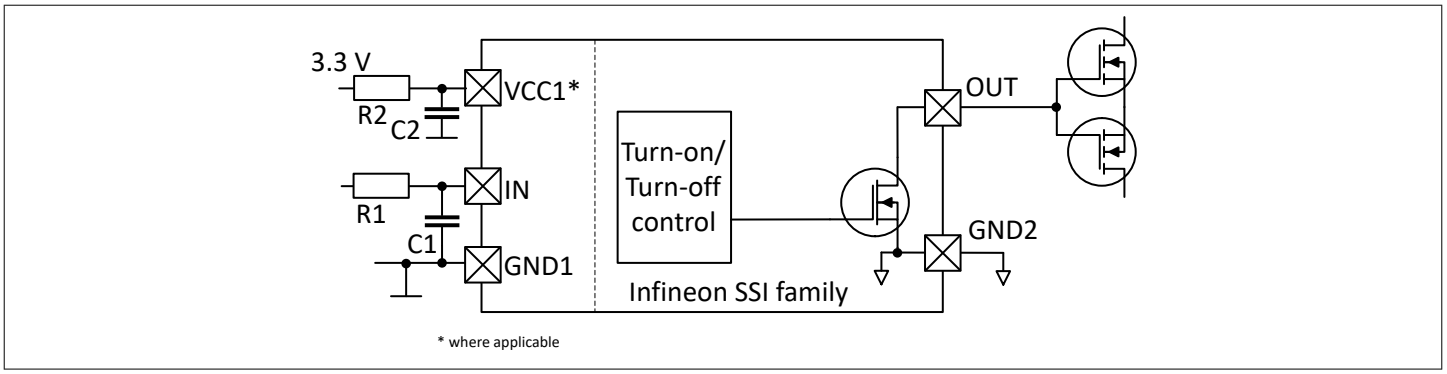


Figure 15 Normal turn-off

6.2.4 Fast turn-off

Overcurrent or over-temperature events trigger the fast turn-off feature of the Infineon SSI family. The fast turn-off enables the Infineon SSI family to shut down the power transistors inside their safe operating area particularly under high load operations. The Infineon SSI family's fast turn-off sink saturation current $I_{off,fast,sat}$ is dimensioned to discharge CoolMOS™ S7 transistors faster than a normal turn-off.

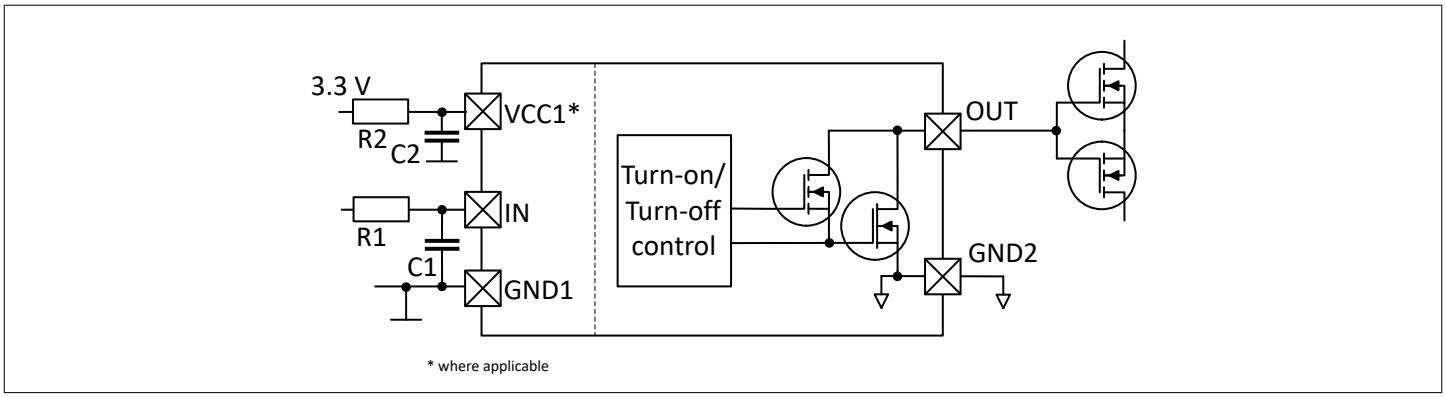


Figure 16 Fast turn-off

6.2.5 Dynamic Miller clamping (DMC)

The dv/dt applied by the connected AC voltage creates capacitive displacement currents through the parasitic capacitances of a power transistor. This can lead to parasitic turn-on of the power switch by increasing the voltage at the gate node of the power switch during its "off"-state. Three major effects can cause dv/dt to occur in installations:

- surge voltages
- fast electric transients (burst)
- dv/dt of line voltage

  The dv/dt of line voltage results in a relatively slow dv/dt of 320 V * 2*π * 50 Hz ~ 100 V/ms in 230 V a.c. grids. Many power transistors are robust, by default, against parasitic turn-on under this condition. Surge voltages and fast electric transients result in a much faster dv/dt and power transistors benefit from the dynamic Miller clamping feature.

The dynamic Miller clamping feature ensures that the power switch stays in the “off” state. It is activated by connecting the power switch's drain to terminal *MC*, *MC1*, or *MC2* respectively with a suitable capacitor. The dv/dt appearing at the drain also injects a current into the related terminals *MC*x and activates of the dynamic Miller clamp FET.

Voltage clamping elements at the Miller clamping terminals may be needed to stay within the absolute maximum ratings.

6.2.6 Overcurrent protection

Overcurrent protection detects excessive, positive and negative current through the power transistor and uses the voltage drop at an external shunt resistor to trigger a comparator with a fixed threshold $|V_{CS,th}|$ at terminal *CS* or *TS/CS*. Please note that $V_{CS,th}$ can be positive or negative. Once triggered, the protection reacts quickly and is able to turn off, for example, CoolMOS™ IPT60R022S7 in very short time. Thus, it is able to support the AC-15 system tests according to IEC 60947-5-1 under appropriate operating conditions. The integrated noise filter has a filter time of $t_{CS,filter}$ and can be backed up by an external RC-filter. However, it is recommended to have as little external filtering as possible to get a quick reaction time in case of overcurrent.

The triggering of the overcurrent protection leads to the latched turn-off of the power switch with a sinking current of $I_{off,\,fast,sat}$.

Terminal *TS/CS* sources a bias current for temperature sensing in iSSI20R02H and iSSI20R11H. As the current sensing shunt is usually very low-resistive, the effect of the biasing current $I_{TS/CS,bias}$ with respect to the shunt signal can be neglected.

The dimensioning of the shunt follows this equation: $R_{sh} = \frac{|V_{CS,\,th}|}{I_{pk,\,max}}$

6.2.7 Over-temperature protection

The over-temperature protection of the Infineon SSI family offers two options to protect against excessive temperatures of the driven power transistor:

- Protection by reading a PTC resistor(iSSI20R02H, iSSI20R03H, iSSI20R11H, and iSSI30R11H)
- Protection by reading the threshold voltage of one or several diodes in series (iSSI30R12H, best matching with CoolMOS™ S7 with temperature sense)

The Infineon SSI family products provide a constant bias current $I_{TS,bias}$ or $I_{TS/CS,bias}$, respectively, for the two types of temperature sensors listed above. The constant current generates a temperature dependent voltage at the temperature sensor. The sensor voltage is connected to terminal *TS* or TS/CS, and the terminal voltage is compared to the threshold $V_{TS,th1}$ (iSSI30R12H) or $V_{TS,th2}$ (other variants). The integrated comparator includes a noise filter of duration $t_{TS,filter}$ for safe detection of the sensor signal that can be complemented by an external RC-filter. The capacitive portion of the external filter must be below the maximum value of $C_{TS,ext}$ in combination with iSSI30R12H. The resistive portion of the filter influences the trigger temperature of the sensor, because the resistor adds a positive offset voltage to the temperature dependent voltage of the sensor. This influence can also be used to actively tune the protection feature for individual requirements. When using the over-temperature protection together with the over-current protection for example with iSSI30R11H, both sensing signals need to reference to GND2.

The triggering of the over-temperature protection leads to the latched turn-off of the power switch with a sinking current of $I_{off, fast,sat}$.

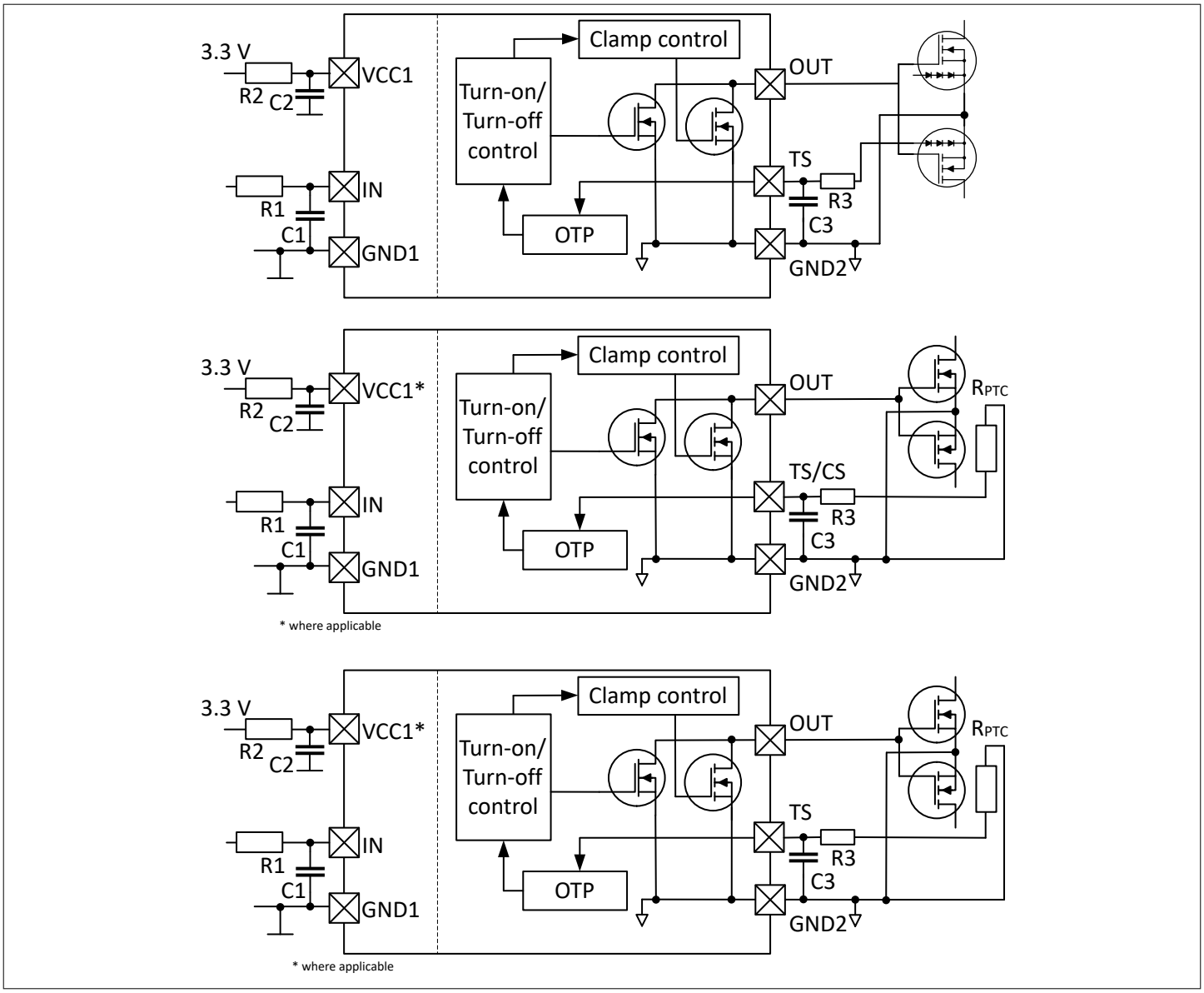


Figure 17 **Schematic examples of the over-temperature protection circuit for variant iSSI30R12H (top), variants iSSI20R02H and iSSI20R11H (middle), and variants iSSI20R03H and iSSI30R11H (bottom)**

7 Application information

Infineon is providing this information as a courtesy only and without acknowledging any legal obligation. Information in the following application chapters is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Adaptation of the supply voltage

The Infineon SSI-family is best operated from a voltage source of 3.3 V. This allows a direct supply from a microcontroller. Please note that normally the pull-down device of general purpose I/O-terminals or high current terminals is stronger than the pull-up device. Thus, it is better to use the pull-down device to control the voltage supply of the Infineon SSI as it is displayed in the figure below.

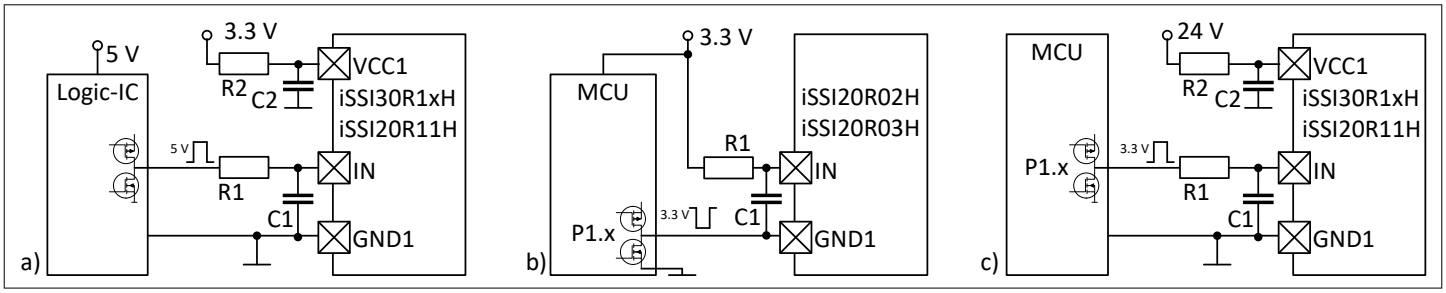


Figure 18 Examples of application relevant control options

The left part in the figure shows the option of using a logic -IC that is supplied with 5 V. Therefore, the logic-IC provides a control signal with 5 V, too, while Infineon SSI is supplied with 3.3 V. This simplifies the interfacing as no downward-level-shifters are required.

The middle part depicts a simple option for the supply scheme for iSSI20R02H, iSSI20R03H and iSSI20R11H. Terminal *IN* is connected to 3.3V and terminal GND1 is connected to the driving port of the microcontroller. The Infineon SSI's output is inverted to the control signal at *IN*. This option requires ports that are able to sink at least the maximum value of I_{IN}, otherwise the effective supply voltage V_{IN} - V_{GND1} may not reach 3.3 V and the IC can stay in the under-voltage lockout mode.

Option c) connects the supply terminal *VCC1* to a higher voltage than 3.3 V, for example 24 V. In these cases, resistor R2 acts as a current limiting resistor. The value for the current limit is the typical value of I_{VCC1}. This results in a limiting resistor value of

$$R2 = \frac{V_{\text{supply}} - V_{\text{VCC1, op, max}}}{I_{\text{VCC1, typ}}} = \frac{24\ \text{V} - 3.5\ \text{V}}{16\ \text{mA}} = 1281\ \Omega \quad (1)$$

A selection of R2 = 1.3 kΩ is sufficient. Of course, worst-case conditions and tolerances of the supply voltage V_{supply} need to be considered, too. It is easy to understand that the solution using a current limiting resistor is not efficient as the resistor might dissipate noticeable power . Dimensioning R2 according to the maximum supply current $I_{VCC1,max}$ yields in higher losses inside the IC. Particularly when operating several Infineon SSI isolators, it is often more efficient to place a DC/DC-converter with a low-tolerance output voltage of 3.3 V instead of using a current limiting resistor for each Infineon SSI.

Very simple microcontroller have often no high current I/O-terminals. In such cases, an interface inverter is a solution for driving iSSI20R02H and iSSI20R03H. Such options using small-signal FETs are given in this figure.

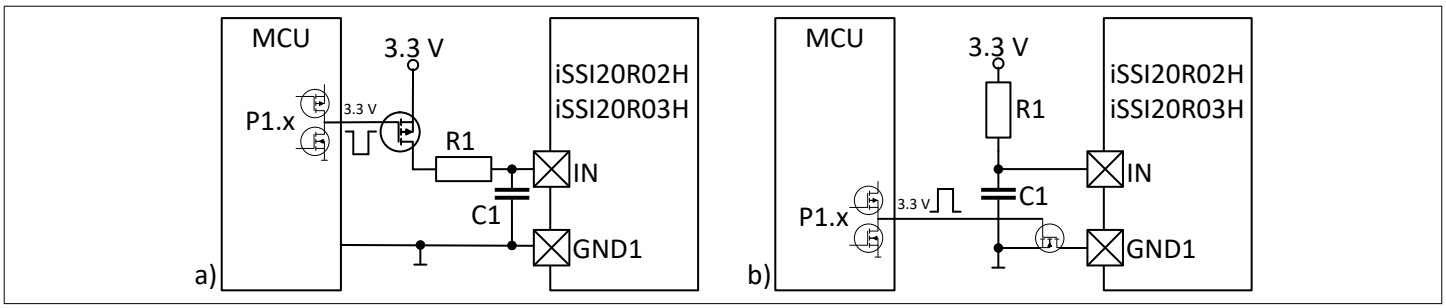


Figure 19 Interfacing with an inverter circuit

7.2 Grounding reference of current and temperature sensor signals

The two sensor signals of the current sensor (shunt) and the temperature sensor have to refer to a single ground reference. It is good engineering to refer the overall ground to one of the sensors.

The left part shows an AC-switch configuration using, for example, two MOSFETs with an integrated temperature sensor and with a shunt resistor for the instantaneous current measurement. The current measurement is more time critical compared to the temperature sensing as it needs to react within a few hundreds of nanoseconds. Therefore, one of the shunt terminals is taken as the reference of the sensor signals. The example utilizes the upper terminal of the shunt resistor R_{Sh} as the reference GND2. Direct connection of PCB traces from terminal *GND2* to the shunt and parallel routing of the current sense signal and its reference GND2 is mandatory to achieve smallest signal distortion and filtering effort.

It is recommended to place the shunt in closest proximity to T1 in order to keep the stray inductance L_σ as small as possible. Any stray inductance of the layout is of course detrimental for the temperature sense voltage v_{TS} signal quality. However, the temperature sensing can be filtered easier because the thermal capacity of the switch allows temperature increases only in the range of hundreds of microseconds or even more. It is important in an AC-switch configuration that the temperature sensor of T2 is not connected. In case of paralleling several MOSFETs, the temperature sensor of only one MOSFET has to be connected

Please note that the gate voltage of T1 $v_{G,T1}$ is directly referenced to GND2 while the gate voltage of T2 $v_{G,T2}$ is lowered by means of the shunt voltage v_{Sh}.

The right part of the figure below depicts the option of using a PTC resistor as a temperature sensor element. All aspects for placing and routing the current sensor signals apply in the same way. The PTC resistor requires a good thermal coupling to the source pad of T1. The stray inductance L_σ is still active, but the good thermal coupling is a superior target to achieve than the minimization of the stray inductance.

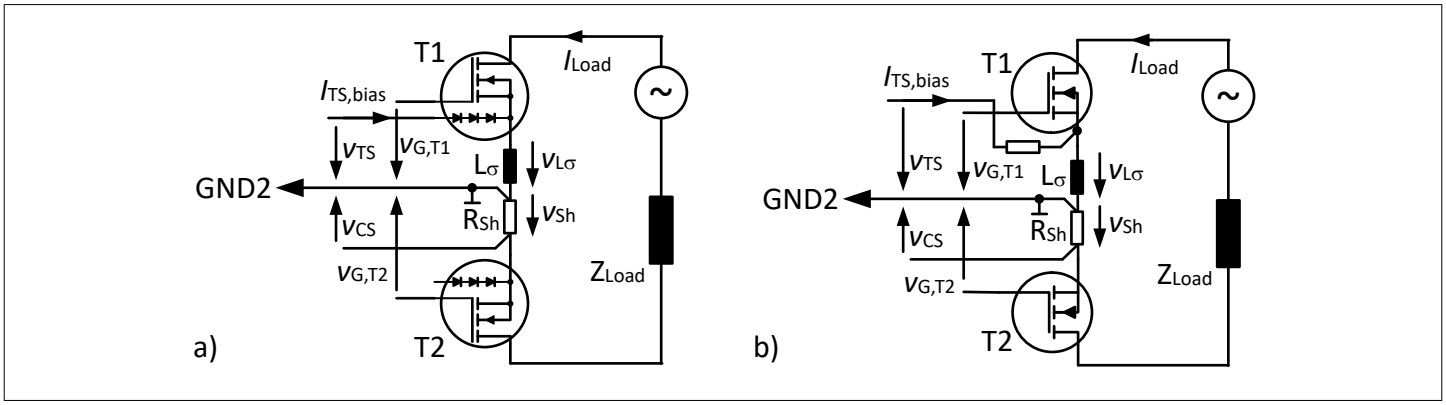


Figure 20 Grounding scheme for AC-switch with integrated temperature sensor (a) and with PTC temperature sensor (b)

In DC-switch configurations, all aspects for placing and routing the current sensor and the temperature sensor signals apply in the same way as for AC-switch configurations.

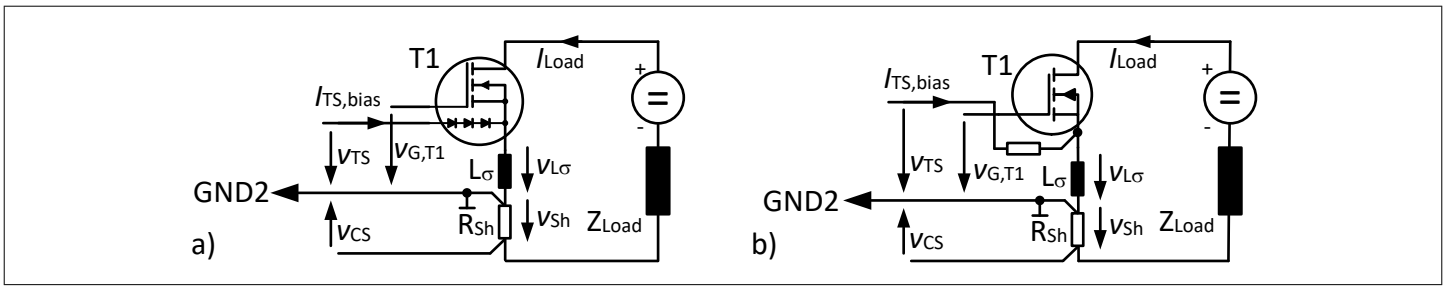


Figure 21 **Grounding scheme for DC-switch with integrated temperature sensor (a) and with PTC temperature sensor (b)**

7.3 Fast turn-on using iSSI20R11H and iSSI30R1xH

The fast turn-on feature enables high-current high-voltage solid-state relays because it allows an amplified turn-on gate current that charges the gate capacitance much faster beyond the Miller voltage level. The fast turn-on saturation current $I_{on,fast,sat}$ of the integrated driving FETs is more than 1000 times higher compared to the direct drive output current I_{OUT} , when keeping terminal BUF unconnected. Please see also the chapter "Fast turn-on" in "Functional description" for more information. The fast turn-on feature should be used in particular in systems where high inrush currents require extremely short turn-on times.

The calculation of the buffer capacitor is simple, but yet essential to ensure a proper dimensioning of the fast turn-on. Take the example of a solid-state relay using two 22 mΩ CoolMOS™ in an a.c.-switch configuration (common-source). The gate voltage after the fast turn-on procedure is proposed to be in the range of 7 V to 8 V. The minimum fast turn-on comparator threshold $V_{BUF,th,min}$.

As there is only one MOSFET of an a.c. configuration in blocking mode while the other MOSFET is in zero-voltage mode, the gate charge is derived graphically in the way as explained in figure below.

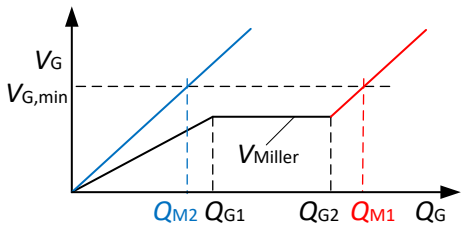


Figure 22 **Gate charge construction for a.c. switch configuration (common source)**

In an a.c. configuration of the switching transistor, there is always one switch that is in blocking mode. The other switching transistor is in freewheeling mode as its body diode or freewheeling diode is in forward bias. Therefore, only one transistor passes the Miller effect. The black/red graph shows a typical curve of the gate voltage V_G as a function of the gate charge Q_G for a MOSFET that is switched under voltage of - for example - 2/3 of the breakdown voltage. The blue curve is the gate charge of a MOSFET under zero-voltage condition (V_{DS} = 0). The blue curve has usually the same slope as the red branch.

The minimum capacitance $C_{BUF,min}$ to be connected to terminal *BUF* is

$$C_{\mathrm{BUF,\,min}} = 1.2 \cdot \frac{Q_{\mathrm{M1}} + Q_{\mathrm{M2}}}{V_{\mathrm{BUF,\,th,\,min}} - V_{\mathrm{G,\,min}}} \quad (2)$$

with Q_{M1} and Q_{M2} being the related gate charges at the end of the fast turn-on when reaching $V_{G,min}$, $V_{BUF,th,min}$ being the minimum fast turn-on comparator threshold voltage and $V_{G,min}$ being the minimum gate-source voltage $V_{GS,min}$ of the switching transistors. A safety factor of 1.2 covers the gate charge tolerance of the switching transistors.

For a.c. switch using two CoolMOS™ IPT60R022S7, a drain-source voltage of 300 V, and a minimum gate-source voltage $V_{G,min}$ = 7 V, the minimum buffer capacitance $C_{BUF,min}$ yields in:

$$C_{\mathrm{BUF,\,min}} = 1.2 \cdot \frac{100\ \mathrm{nC} + 70\ \mathrm{nC}}{10\ \mathrm{V} - 7\ \mathrm{V}} = 68\ \mathrm{nF} \tag{3}$$

7.4 Using the overcurrent protection

The overcurrent protection is designed to react fast on the detection of excessive current using a shunt. This chapter explains how to use this feature for the example of a relay that is able to operate AC-15 loads.

The AC-15 test is a generic test for electromechanical relays and for solid-state relays. Its test scheme is shown in the figure below. It brings demanding requirements for the dimensioning of the overcurrent protection. The protection should not trigger during the first interval of the AC-15 test when a load current of 10 x of the nominal current is applied to the device under test followed by the interval t_2 - t_1 with nominal load current.

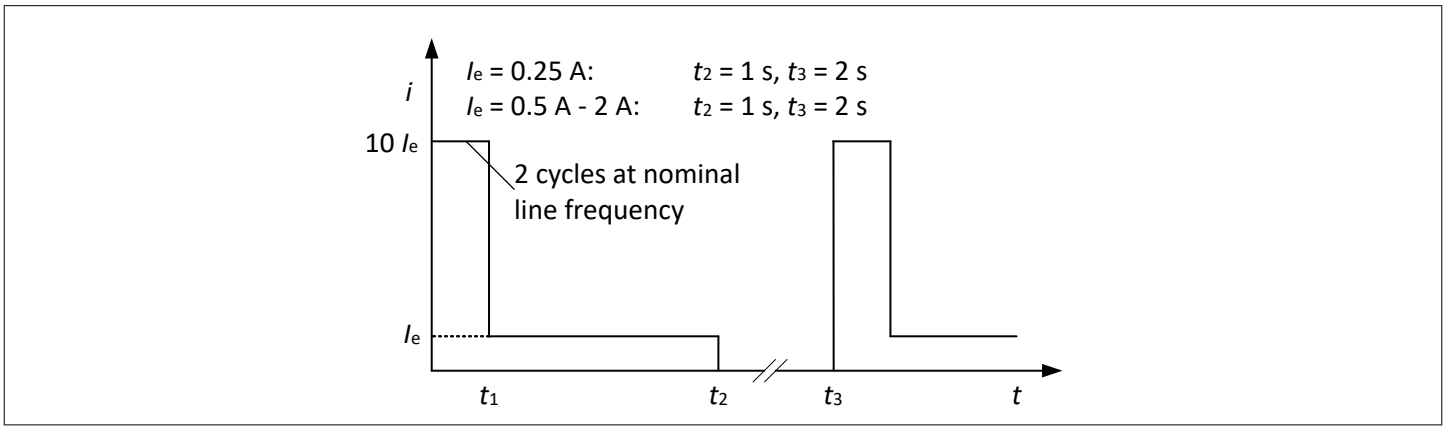


Figure 23 AC-15 test (source: IEC 60947-1:2021)

In addition, there are test requirements for the power factor at make and break for various conditions and tests. The power factor itself does not influence the current amplitude and is therefore not considered. This is an example for the shunt calculation for use in a solid-state relay with a current rating of 2 A supporting AC-15 tests.

The maximum load current in the AC-15 test is 10 x the nominal and might appear at the maximum tolerated grid voltage which is 10% above nominal.

$$I_{\mathrm{pk,\,max}} = 1.1 \cdot \sqrt{2} \cdot 2\ \mathrm{A} \cdot 10 = 31.1\ \mathrm{A\ peak} \tag{4}$$

The worst-case analysis needs a margin of the target protection trigger current with respect to the calculated value $I_{pk,max}$,max. The target protection trigger current is selected for $I_{pk,trig}$ = 32 A peak. The overcurrent protection comparator is tolerated with +/- 15mV around the typical value of $v_{CS,th}$ and an offset of 10 mV according to the figure below. Together with the assumed overdrive of the comparator of 20 mV, the minimum and maximum trigger currents are

$$\begin{aligned} I_{\mathrm{pk,\,trig,\,min}} &= I_{\mathrm{pk,\,trig}} \frac{v_{\mathrm{CS,\,th,\,min}} + 10\ \mathrm{mV} + 20\ \mathrm{mV}}{v_{\mathrm{CS,\,th,\,typ}} + 20\ \mathrm{mV}} = 31.27\ \mathrm{A\ peak} \\ I_{\mathrm{pk,\,trig,\,max}} &= I_{\mathrm{pk,\,trig}} \frac{v_{\mathrm{CS,\,th,\,max}} + 10\ \mathrm{mV} + 20\ \mathrm{mV}}{v_{\mathrm{CS,\,th,\,typ}} + 20\ \mathrm{mV}} = 35.64\ \mathrm{A\ peak} \end{aligned} \tag{5}$$

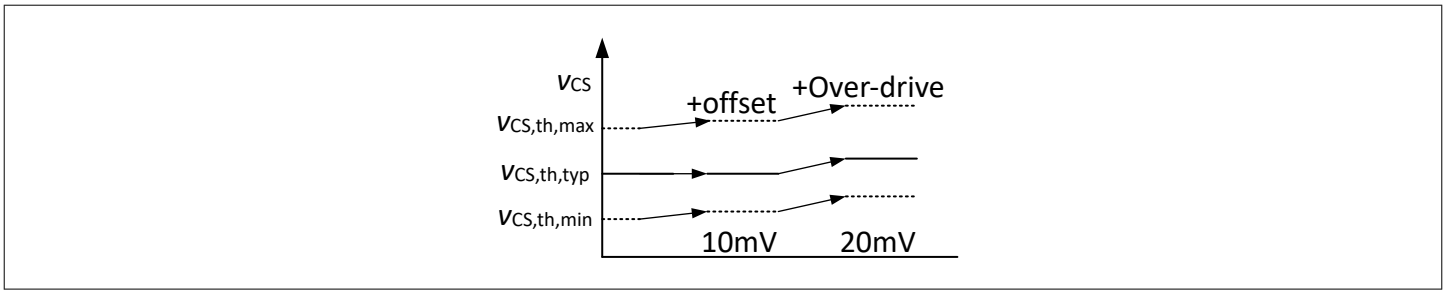


Figure 24 Worst-case current sense trigger thresholds

The dimensioning of the minimum shunt resistance follows this equation using the lowest trigger threshold including offset and overdrive and the maximum peak trigger current $I_{pk,trig,max}$

$$R_{Sh,\,max} = \frac{\upsilon_{CS,\,th,\,min} + 10\ mV + 20\ mV}{I_{pk,\,trig,\,max}} = \frac{215\ mV}{35.64\ A} = 6.033\ m\Omega \quad (6)$$

The above equation results in a selected resistance of R_{Sh} = 6 mΩ.

7.5 Using the dynamic Miller clamping

Connecting a capacitor between the input terminals *MC, MC1* or *MC2* and the drain terminals of the switching transistor activates the dynamic Miller clamping feature that is available in variants iSSI20R02H and iSSI30R1xH. Let terminals *MC, MC1* or *MC2* float to deactivate the feature. The dynamic Miller clamp reinforces the strong, yet limited pull-down capability of Infineon SSI in case that high dv_{DS}/dt events occur at the switched transistors. This is in particular important during off-state, if fast electric transients (bursts) occur. Even though there is usually no dedicated gate resistor in use, transients might lead to a parasitic turn-on of the switched transistor by pulling the gate higher than its gate-source threshold voltage.

The dimensioning of the coupling capacitors considers the fastest occurring dv_{DS}/dt-rates that appear in the application. In a.c. applications, bursts according to IEC 61000-4-4 can be a reference that specifies very steep pulses. However, the resulting pulses that stress the device-under-test have a lower amplitude and slope due to the cabling inductance and capacitance. An assumption for dv_{DS}/dt can be, for example, 10 V/ns and the coupling capacitance may be 1 pF. Please note that one of the two capacitors is shorted bypassed to GND2 by the related switched transistor in parallel. Thus, the only one capacitor is coupling the dv_{DS}/dt signal.

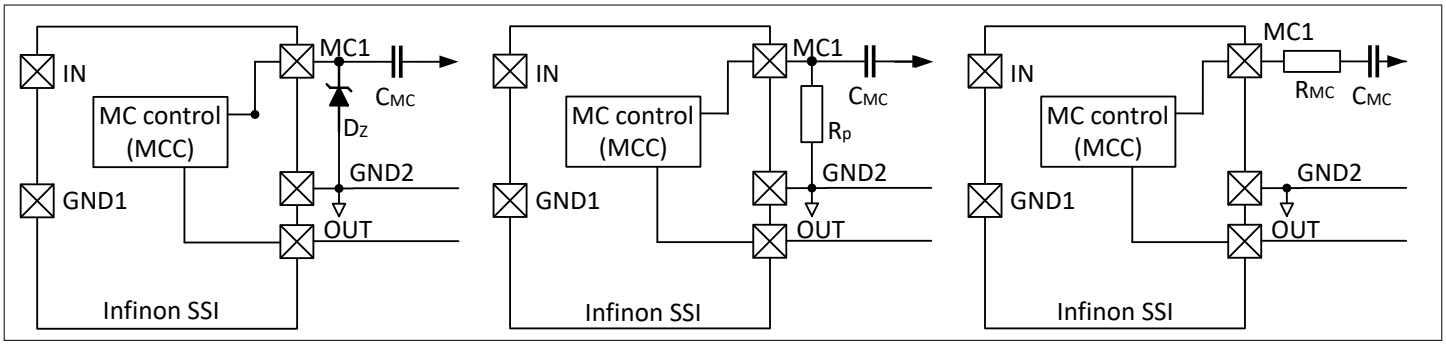


Figure 25 Dynamic Miller clamp options with zener diode (left), parallel resistor (middle) and series resistor (right)

In the above mentioned example, the coupled capacitive current into terminal *MC* is 10 V/ns * 1 pF = 10 mA. This would generate a voltage at terminal *MC* of 10 mA * R_{MC} = 5 V. Even though the static absolute maximum voltage rating at *MC* is v_{MC} = 3.6 V, the dynamic current $I_{MC,dyn}$ for sporadic events (duty cycle < 1%, pulse duration < 1 µs) that is injected into this terminal can be applied for pulsed stress. Therefore, clamping elements, such a 3.3 V clamping zener diode at terminal *MC* to reduce voltages above the zener voltage might not be needed. However, special needs

to be taken at the evaluation of the highest dv/dt in systems. Other clampings options are a resistor between terminal *MC* and *GND2* that would take a portion of the coupled capacitive current or applying a series resistor that generates enough voltage to keep the limits according to the figure above.

7.6 Inductive energy clamping methods

Solid-state relays are often used in combination with loads that have an inductive portion. The inductive portion generates an over-voltage, if the isolator's output is turned off. The amplitude of the over-voltage can exceed the switching transistor's maximum breakdown voltage. Therefore, a clamping element is needed to limit the drain-source voltage of the switching transistor. Various options are possible:

- TVS (transient voltage suppressor) diodes,
- varistors,
- snubbers and
- others

Special care is required for the dimensioning and selection of the related components depending on the application's operating range. For example, two or even more TVS diodes can be required to fulfill the datasheet of the clamping element. Also combinations of the above mentioned options can help for a optimized clamping solution.

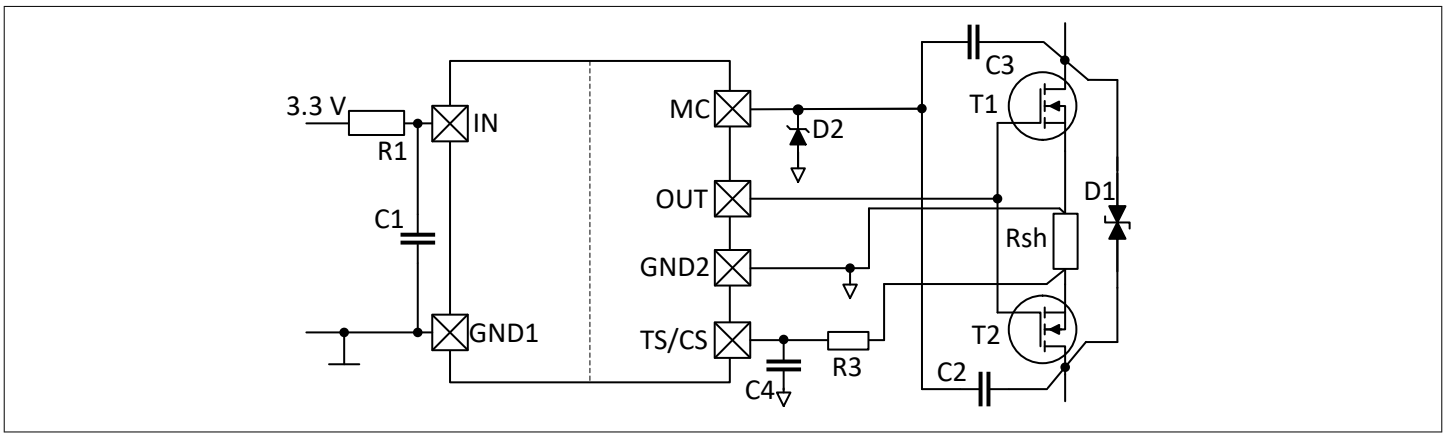


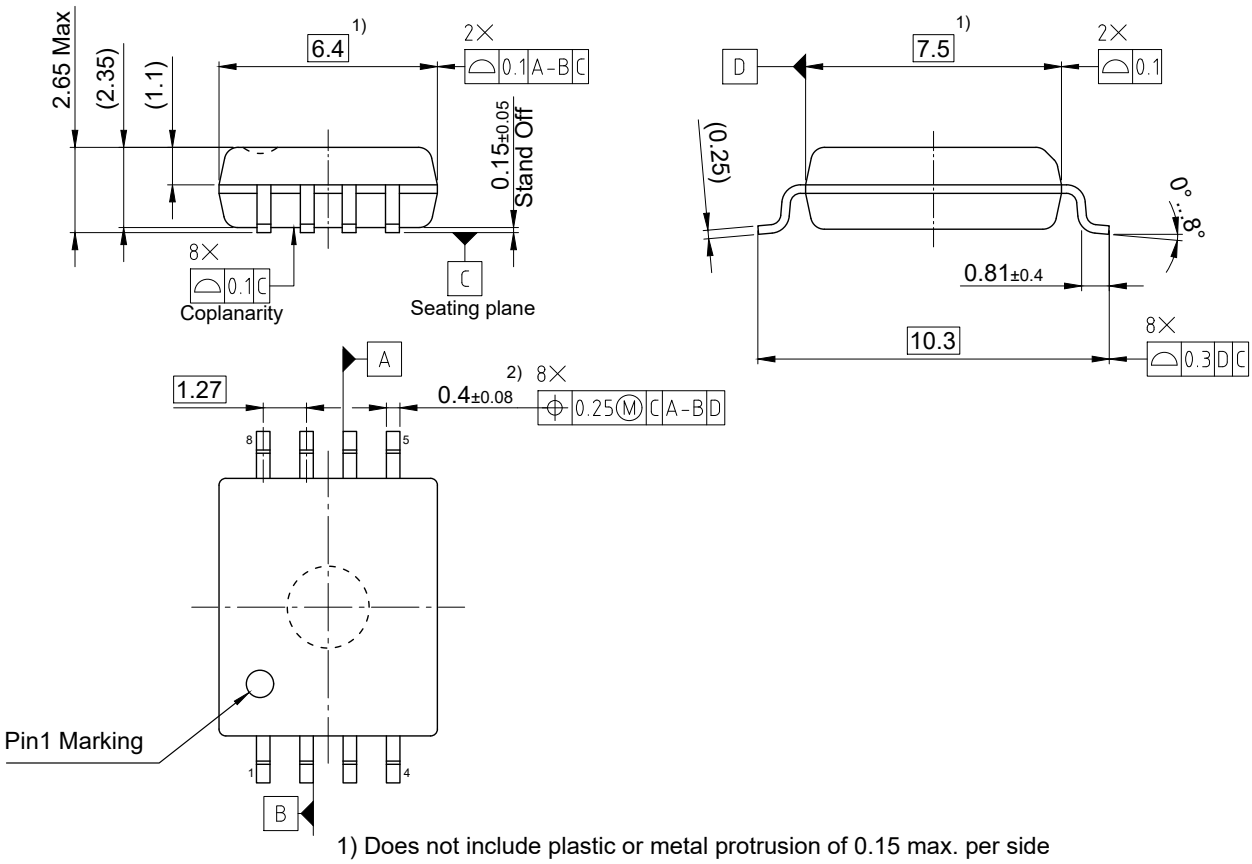
Figure 26 Example of a drain-to-drain TVS-diode D1 as a clamping element in an AC-switch configuration using iSSI20R02H

8 Related products

Product group	Product name	Description
Infineon SSI solid-state isolators	Eval-iSSI30R12H	600 V, 22 mΩ solid-state relay featuring over-temperature protection, overcurrent protection, dynamic miller clamping and fast turn-on
CoolMOS™ S7 discrete MOSFETs	IPT60R065S7	600 V, 65 mΩ MOSFET in TO-leadless (HSOF-8)
	IPT60R040S7	600 V, 40 mΩ MOSFET in TO-leadless (HSOF-8)
	IPT60R022S7	600 V, 22 mΩ MOSFET in TO-leadless (HSOF-8)
	IPQC60R040S7	600 V, 40 mΩ MOSFET in QDPAK bottom-side cooled package (HDSOP)
	IPQC60R017S7	600 V, 17 mΩ MOSFET in QDPAK bottom-side cooled package (HDSOP)
	IPQC60R010S7	600 V, 10 mΩ MOSFET in QDPAK bottom-side cooled package (HDSOP)
	IPDQ60R010S7	600 V, 10 mΩ MOSFET in QDPAK top-side cooled package (HDSOP)
	IPDQ60R017S7	600 V, 17 mΩ MOSFET in QDPAK top-side cooled package (HDSOP)
	IPDQ60R022S7	600 V, 22 mΩ MOSFET in QDPAK top-side cooled package (HDSOP)
	IPDQ60R040S7	600 V, 40 mΩ MOSFET in QDPAK top-side cooled package (HDSOP)
	IPDQ60R065S7	600 V, 65 mΩ MOSFET in QDPAK top-side cooled package (HDSOP)
OptiMOS™ Linear FET, discrete MOSFETs	IPT008N06NM5LF	60 V, 0.8 mΩ MOSFET in TO-leadless (HSOF-8)
	IPT013N08NM5LF	80 V, 1.3 mΩ MOSFET in TO-leadless (HSOF-8)
	IPB017N10N5LF	100 V, 1.7 mΩ MOSFET in D2PAK 7pin (TO-263 7pin)
	IPB020N10N5LF	100 V, 2.0 mΩ MOSFET in D2PAK 7pin (TO-263 7pin)
	IPB033N10N5LF	100 V, 3.3 mΩ MOSFET in D2PAK (PG-TO263-3)
	IPB048N15N5LF	150 V, 4.8 mΩ MOSFET in D2PAK (PG-TO263-3)
	IPB083N15N5LF	150 V, 8.3 mΩ MOSFET in D2PAK (PG-TO263-3)
	IPB110N20N3LF	200 V, 11 mΩ MOSFET in D2PAK (PG-TO263-3)

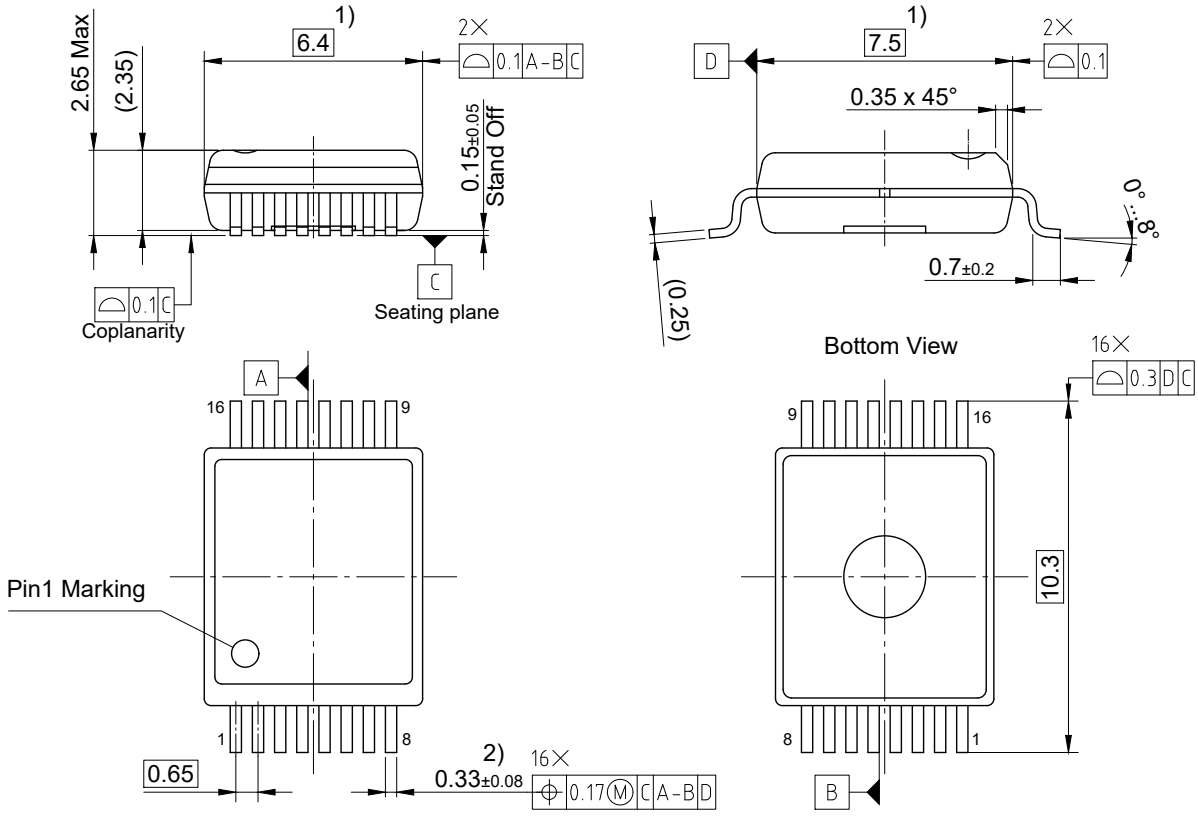
9 Package dimensions

9.1 Package outline



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1mm total in excess of lead width
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 27 PG-DSO-8-66



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 28 PG-DSO-16-33

Revision history

Document version	Date of release	Description of changes
v1.00	2024-01-29	• Initial release
v1.10	2024-08-28	• Short circuit output current value for iSSI20R02H and iSSI20R03H update • Certification information update (UL certification) • Term “iSSI” replace with “Infineon SSI” • Timing diagrams update

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