

PESD5V5V1BCSF

Ultra low clamping bidirectional ESD protection diode

4 July 2022 **Product data sheet**

1. General description

Ultra low clamping bidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a leadless ultra small DSN0603-2 (SOD962) Surface-Mounted Device (SMD) package.

2. Features and benefits

- Bidirectional ESD protection of one line
- Ultra small leadless package with a height of 0.3 mm
- IEC 61000-4-5 (surge): I_{PP} = 8 A average measured
- Very low clamping voltage: V_{CL}= 8.5 V typ at 16 A for a TLP pulse
- Ultra low leakage current: I_{RM} = 1 nA
- ESD protection up to 20 kV

3. Applications

ESD surge protection for:

- Very sensitive interface lines
- Generic interface lines

in portable electronics communication, consumer and computing devices

4. Quick reference data

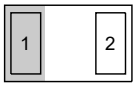
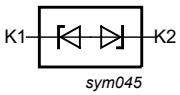
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1]	-	-	7.1	A
V_{CL}	clamping voltage	I_{PP} = 16 A; t_p = 100 ns; T_{amb} = 25 °C	[2]	-	8.5	-	V

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DSN0603-2 (SOD962-2)**	
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V5V1BCSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V5V1BCSF	F8

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1]	-	7.1	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-40	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-	20	kV
		IEC 61000-4-2; air discharge	[2]	-	20	kV

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.

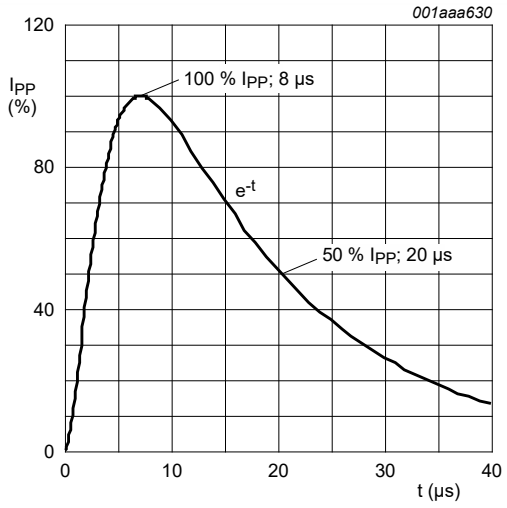


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

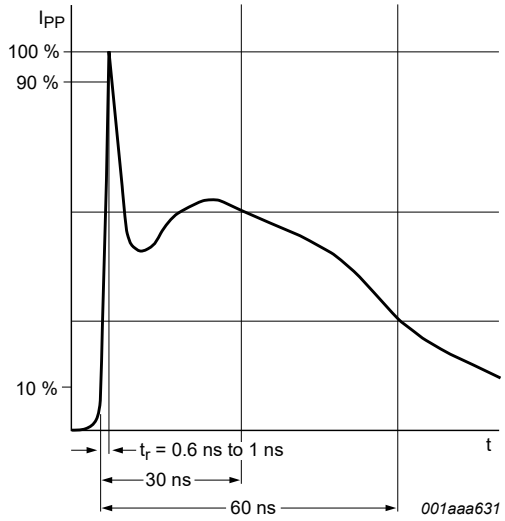


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
V_h	holding voltage	I_T = 5 mA; T_{amb} = 25 °C		4.5	-	8	V
V_{t1}	trigger voltage	T_{amb} = 25 °C	[1]	-	8.2	-	V
I_{RM}	reverse leakage current	V_{RWM} = 5.5 V; T_{amb} = 25 °C		-	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	8	10	pF
V_{CL}	clamping voltage	I_{PPM} = 7.1 A; t_p = 8/20 µs; T_{amb} = 25 °C	[2]	-	8.1	-	V
		I_{PP} = 8 A; t_p = 100 ns; T_{amb} = 25 °C	[1]	-	7.1	-	V
		I_{PP} = 16 A; t_p = 100 ns; T_{amb} = 25 °C	[1]	-	8.5	-	V
R_{dyn}	dynamic resistance	I_R = 10 A; T_{amb} = 25 °C	[1]	-	0.19	-	Ω

[1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.
[2] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.

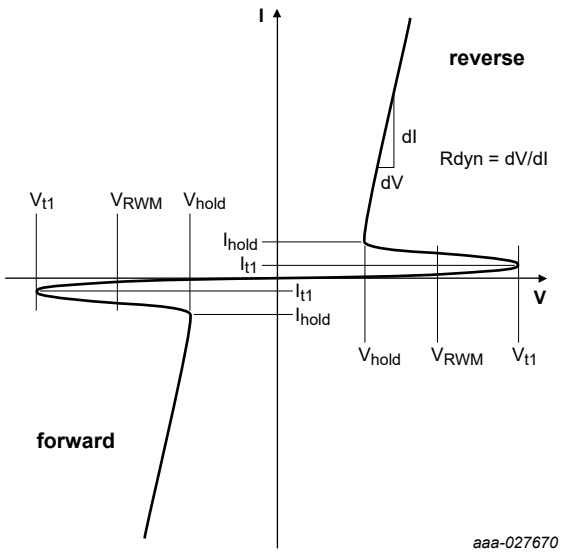


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

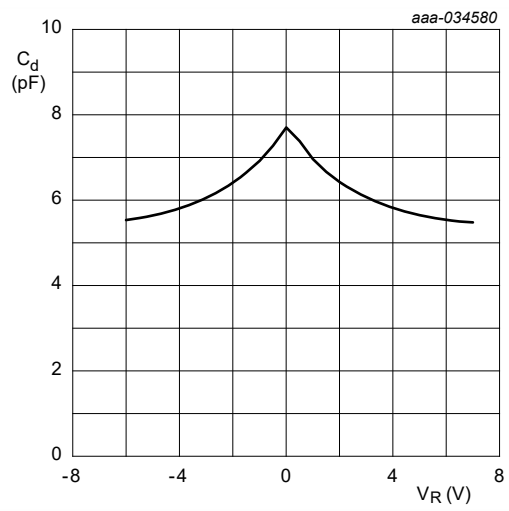
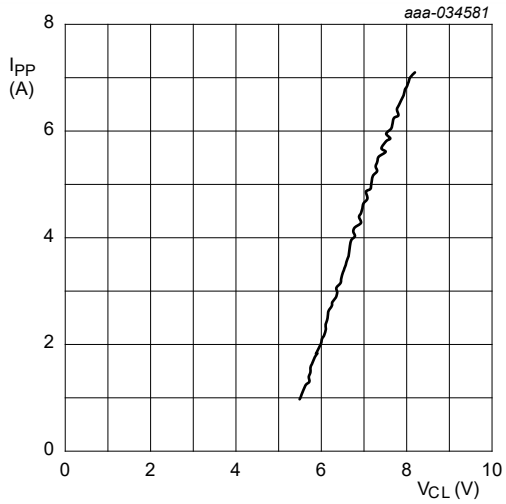


Fig. 4. Capacitance as a function of reverse standoff voltage; typical values

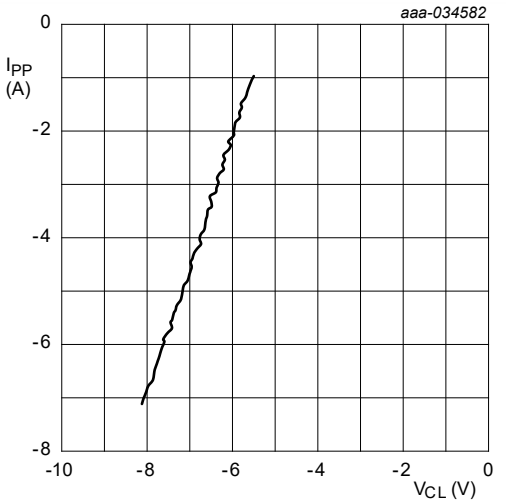
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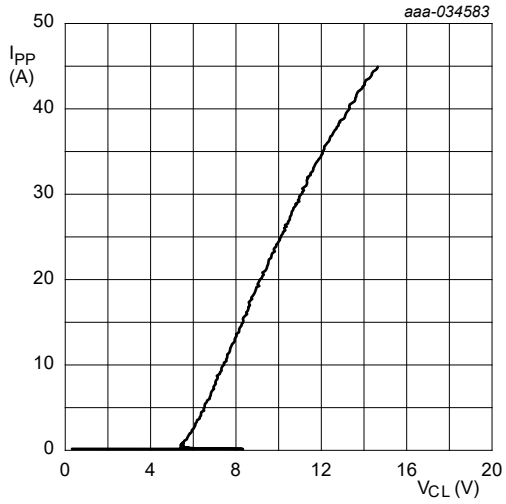
IEC 61000-4-5; t_p = 8/20 µs; positive pulse

Fig. 5. Dynamic resistance with positive clamping; typical values



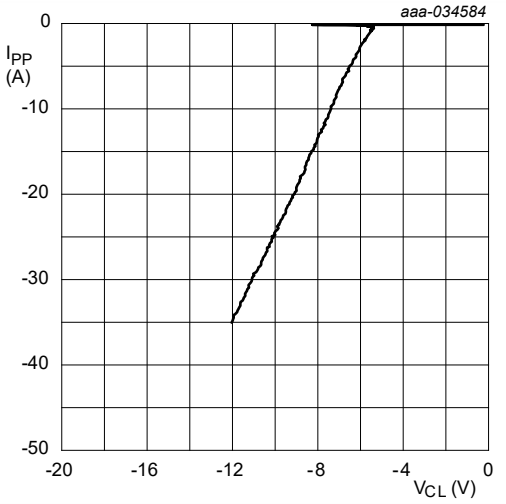
IEC 61000-4-5; t_p = 8/20 µs; negative pulse

Fig. 6. Dynamic resistance with negative clamping; typical values



Transmission Line Pulse (TLP);
t_p = 100 ns; t_r = 1 ns

Fig. 7. Dynamic resistance with positive clamping; typical values



Transmission Line Pulse (TLP);
t_p = 100 ns; t_r = 1 ns

Fig. 8. Dynamic resistance with negative clamping; typical values

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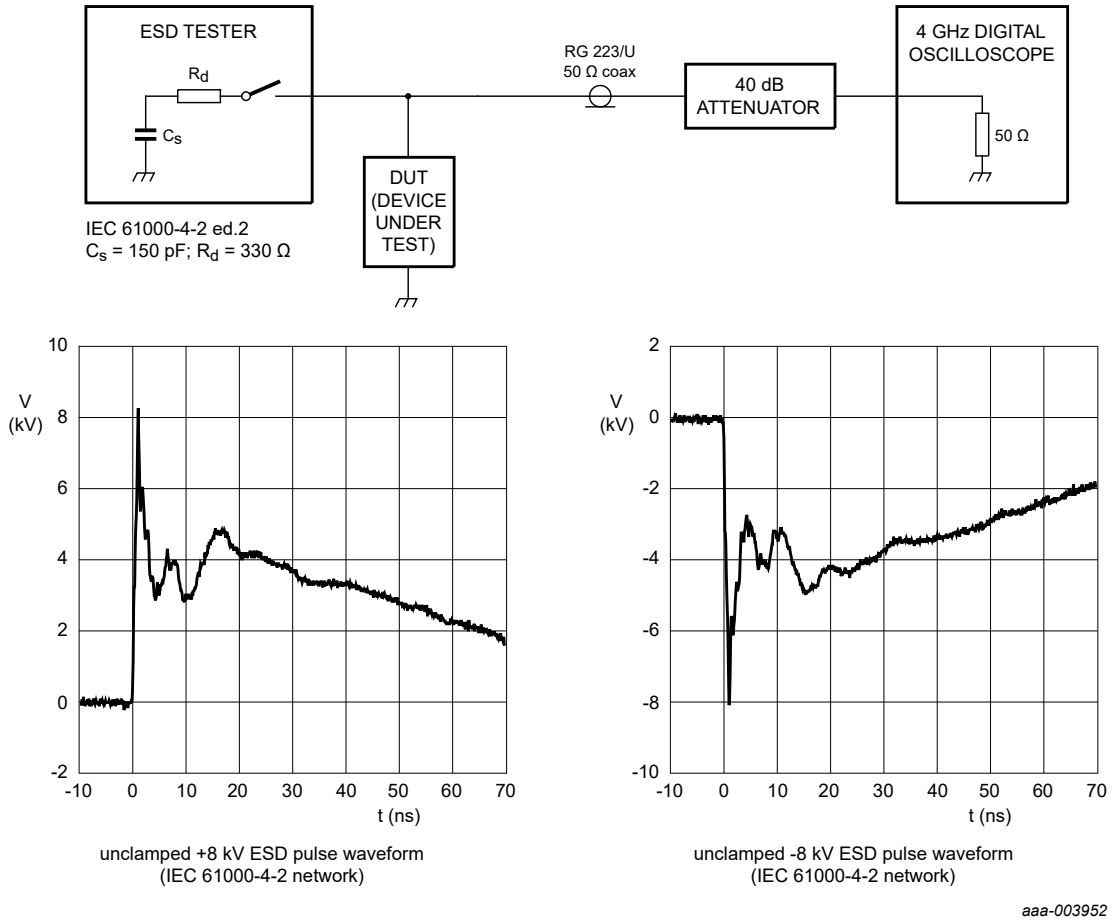


Fig. 9. ESD clamping test setup and waveforms

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10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

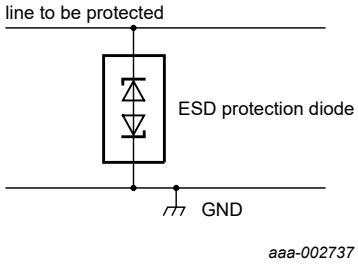


Fig. 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

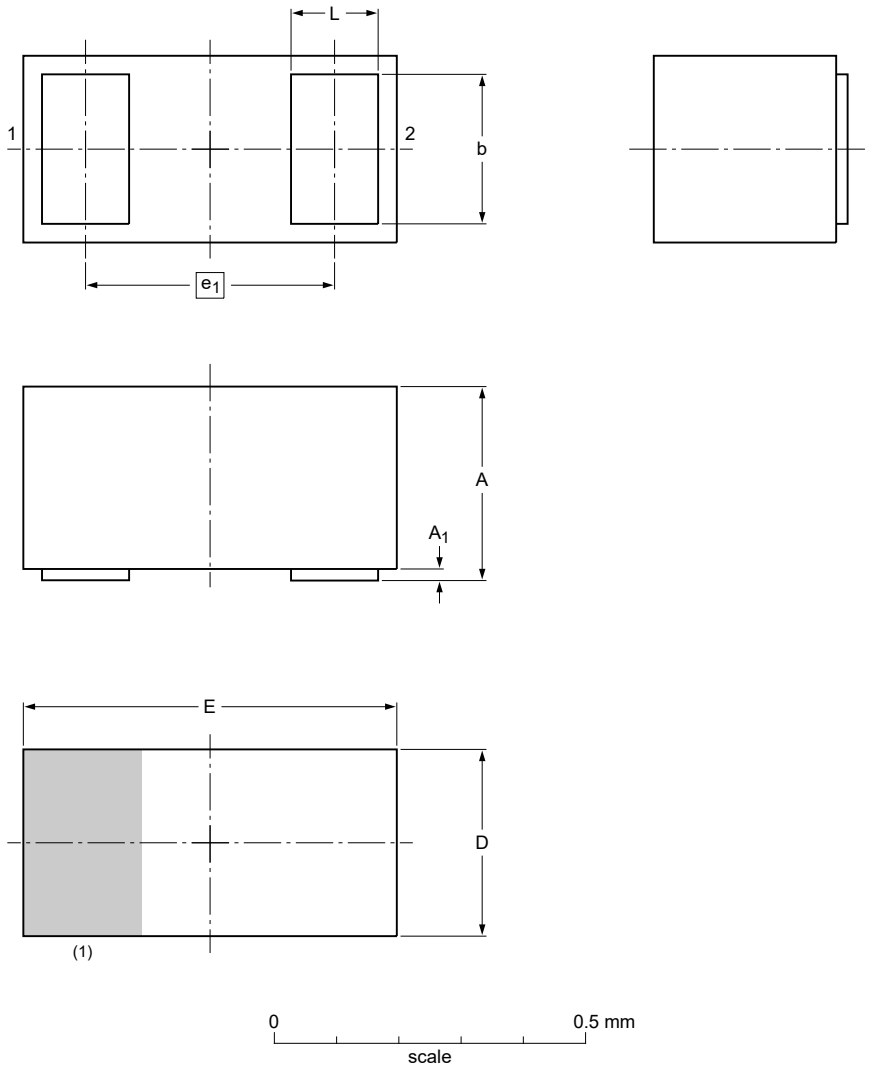
1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

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11. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm **SOD962-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e_1	L
mm	max	0.32	0.03	0.25	0.325	0.625		0.15
	nom						0.4	
	min	0.28		0.23	0.275	0.575		0.13

Note
1. The marking bar indicates the cathode.

sod962-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD962-2						~~13-07-12~~ 13-07-17

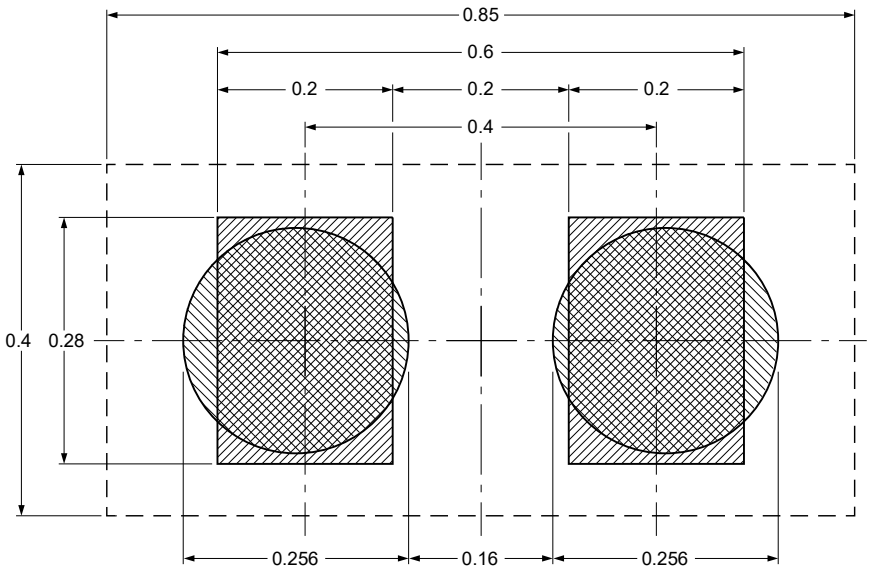
Fig. 11. Package outline DSN0603-2 (SOD962-2)

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12. Soldering

Footprint information for reflow soldering of leadless ultra small package; 2 terminals **SOD962-2**



recommended stencil thickness: 0.1 mm

occupied area

solder paste

solder lands

Dimensions in mm

Issue date ~~16-02-01~~ 20-09-15

sod962-2_fr

Fig. 12. Reflow soldering footprint for DSN0603-2 (SOD962-2)

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13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V5V1BCSF v.1	20220704	Product data sheet	-	-

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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Contents

1. General description....1
2. Features and benefits....1
3. Applications....1
4. Quick reference data....1
5. Pinning information....2
6. Ordering information....2
7. Marking....2
8. Limiting values....3
9. Characteristics....4
10. Application information....7
11. Package outline....8
12. Soldering....9
13. Revision history....10
14. Legal information....11

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