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# MAX96737

# Single GMSL2 Serializer with Dual-OLDI Input and Optional HDCP

## General Description

The MAX96737 convert single or dual OLDI input port data to single GMSL2 high-speed serial link protocol. They also send and receive side-channel and peripheral control data, enabling full-duplex, single-wire, transmission of video and bidirectional data over cables up to 15m in length.

The GMSL2 link operates at a fixed rate of 3Gbps or 6Gbps in the forward direction and 187.5Mbps in reverse.

All products in the MAX96737 family support single GMSL2 PHY operation with 1x4 or 1x8 ganged mode OLDI inputs. Maximum PCLK is up to 160MHz with a 1x4 input and up to 215MHz with a 1x8 input, depending on the product option.

MAX96737 variants supporting HDCP add HDCP v1.4 encryption on the GMSL links, with on-chip secure key storage and a state machine for HDCP authentication and link monitoring.

The GMSL2 concurrent control channel operates at 9.6kbps to 1Mbps in UART-to-UART and up to 1Mbps in $I^2C$-to-$I^2C$ mode with clock stretching. Using the control channel, a microcontroller can program serializer, deserializer, and peripheral device registers from either end of the link at any time, independent of video timing. An additional pass-through I2C/UART channel and a 50MHz SPI channel are provided for peripheral control.

A single, forward path $I^2S$ audio channel is supported. Reverse audio is not supported.

Operation is specified over the automotive ambient temperature range of -40°C to +105°C. The devices are AEC-Q100 qualified and are available in a compact, 56-pin, 8mm x 8mm TQFN package with exposed pad.

## Applications

- Center Console Touch-Panel Displays
- Digital Instrument Clusters and Head-Up Displays
- Rear-Seat and Passenger Infotainment Displays

## Benefits and Features

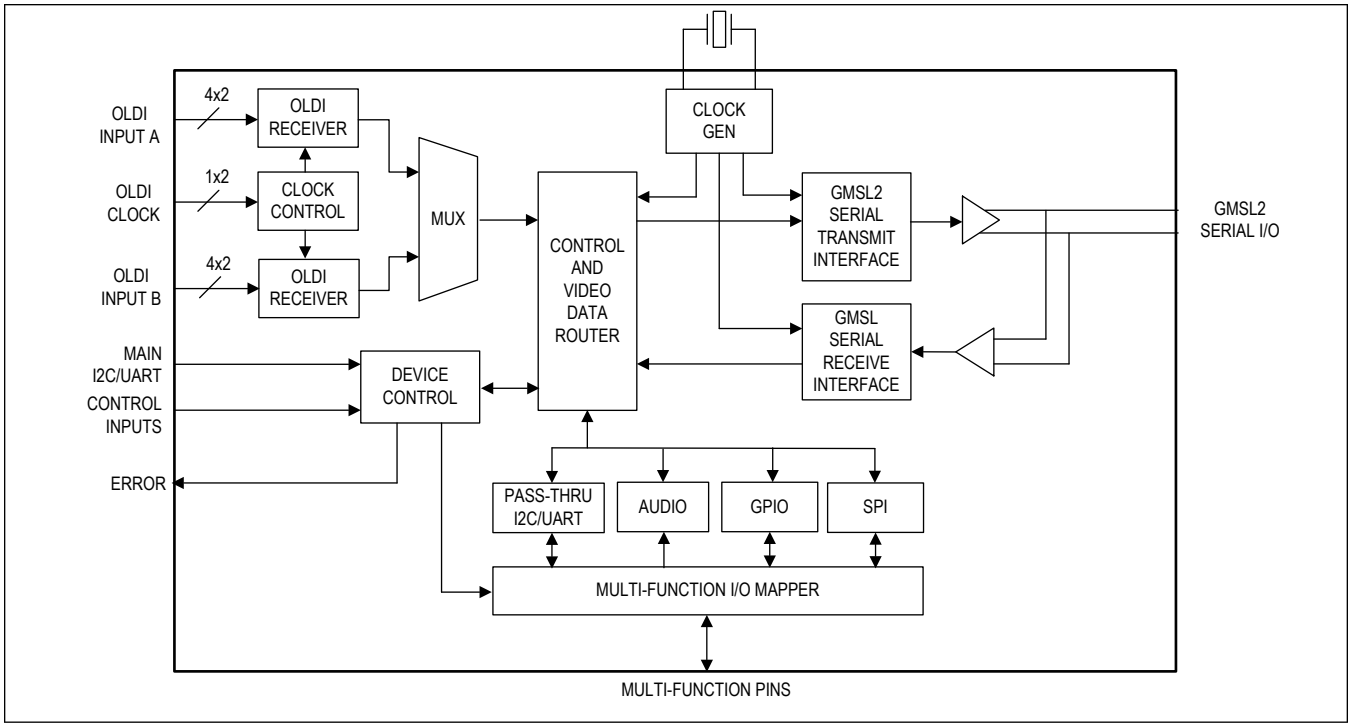
- 1x4, 2x4, and 1x8 OLDI Input Ports
- 3Gbps or 6Gbps GMSL2 Forward Data Rates for System and Power Flexibility
- 187.5Mbps Reverse GMSL2 Data Rate
- Ideal for High-Resolution Entry-Level and Mid-Range Video Applications
  - Up to 2880x1080/60Hz Over a Single Link
- Uses Low-Cost 50Ω Coax or 100Ω STP Cables
- HDCP 1.4 Encryption on GMSL Links (MAX96737 variants supporting HDCP only)
- SPI Interface for remote peripheral control
- Forward $I^2S$ Audio Channel
- GMSL Line-Fault Monitor
- Tracks Spread Spectrum on OLDI Input
- ASIL-Relevant Functional Safety Features
  - 16-bit CRC Protection of Control-Channel Data ($I^2C$, UART, SPI, GPIO, Audio)
  - Optional 32-Bit Video Line CRC
  - Retransmission of All Control-Channel Data ($I^2C$, UART, SPI, GPIO, Audio) Upon Error Detection
  - Video Watermark Generation and Detection
- Continuous Link Margin Monitoring and Optimization
  - Continuous Adaptive Equalization Allows 15m Coax Cable with Multiple In-Line Connectors
  - Forward and Reverse Channel PRBS Generator and Checker for BER Testing of Serial I/O Links
  - Eye-Opening Monitor for Continuous Link Margin Diagnosis
- Concurrent Control Channel for Device Configuration and Communicating with Remote Peripherals
  - Main $I^2C$/UART, Two Pass-Through $I^2C$/UART, SPI, and Tunneled or Register-Programmable GPIO
  - Up To 18 Programmable GPIOs
  - Two Hardware-Programmable Device Addresses
  - Sleep Mode with Register State Retention

***Ordering Information appears at end of datasheet.***



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## Simplified Block Diagram



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## Absolute Maximum Ratings

(All voltages with respect to ground.) .....

$V_{DDIO}$ ..... -0.3V to +3.9V
$V_{DD18}$ ..... -0.3V to +2.0V
$V_{DD}$ ..... -0.3V to +2.0V
CAP_VDD ..... -0.3V to +1.2V
SIO_ (Active State) (Note 1)..... ($V_{DD18}$ - 1.1V) to $V_{DD18}$
SIO_ (Inactive State) (Note 1) ..... -0.3V to +1.1V
DA/B_, CKA/B_ ..... -0.3V to +1.35V
XRES, X2 ..... -0.3V to ($V_{DD18}$ + 0.3V)
All Other Pins (Note 2) ..... -0.3V to ($V_{DDIO}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70ºC) TQFN (Multilayer board, derate 40mW/ºC above +70ºC) .....2200mW
Storage Temperature Range .....-40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

**Note 1:** Active state means the device is powered up and not in sleep or power-down mode. Inactive means the device is not powered up, or is powered up in sleep or power-down mode.

**Note 2:** Specified maximum voltage or 3.9V, whichever is lower.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### 56-Pin TQFN

| | |
|---|---|
| Package Code | T5688+6 |
| Outline Number | 21-0135 |
| Land Pattern Number | 90-100041 |
| **Thermal Resistance, Four-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 25°C/W |
| Junction to Case ($\theta_{JC}$) | 1°C/W |

### 56-Pin TQFN-SW (Side-wettable)

| | |
|---|---|
| Package Code | T5688Y+6 |
| Outline Number | 21-100046 |
| Land Pattern Number | 90-100048 |
| **Thermal Resistance, Four-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 25°C/W |
| Junction to Case ($\theta_{JC}$) | 1°C/W |

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

## Electrical Characteristics

($V_{DD18}$ = 1.7V to 1.9V, $V_{DD}$ = 0.95V to 1.05V or 1.14V to 1.26V, $V_{DDIO}$ = 1.7V to 1.9V or 3.0V to 3.6V, $T_A$ = -40°C to +105°C, EP connected to PCB ground, typical values are at $V_{DD18}$ = $V_{DDIO}$ = 1.8V, $V_{DD}$ = 1.0V, $T_A$ = 25°C, unless otherwise noted. (Note 3))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD CHANNEL SERIAL OUTPUTS (SIO_)—SEE Figure 1** | | | | | | |
| Output Voltage Swing (Single-Ended) | $V_O$ | $R_L$ = 100Ω ±1%, ($V_{OH}$-$V_{OL}$) for both outputs | 300 | 400 | 500 | mV |
| Output Voltage Swing (Differential) | $V_{ODT}$ | $R_L$ = 100Ω ±1%, peak-to-peak differential voltage | 600 | 800 | 1000 | mVp-p |

## Electrical Characteristics (continued)

($V_{DD18}$ = 1.7V to 1.9V, $V_{DD}$ = 0.95V to 1.05V or 1.14V to 1.26V, $V_{DDIO}$ = 1.7V to 1.9V or 3.0V to 3.6V, $T_A$ = -40°C to +105°C, EP connected to PCB ground, typical values are at $V_{DD18}$ = $V_{DDIO}$ = 1.8V, $V_{DD}$ = 1.0V, $T_A$ = 25°C, unless otherwise noted. (Note 3))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Change in $V_{OD}$ Between Complementary Output States | $\Delta V_{OD}$ | $R_L$ = 100Ω ±1%, $\lvert V_{OD(H)} - V_{OD(L)} \rvert$ | | | 25 | mV |
| Differential Output Offset Voltage | $V_{OS}$ | $R_L$ = 100Ω ±1%, offset voltage in each output state | $V_{DD18}$ - 0.65 | $V_{DD18}$ - 0.45 | $V_{DD18}$ - 0.25 | V |
| Change in $V_{OS}$ Between Complementary Output States | $\Delta V_{OS}$ | $R_L$ = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)} \rvert$ | | | 25 | mV |
| Termination Resistance (Internal) | $R_T$ | Any pin to $V_{DD18}$ | 50 | 55 | 60 | Ω |
| **DC ELECTRICAL CHARACTERISTICS / OLDI RECEIVER** | | | | | | |
| Common-Mode Input Voltage | $V_{CM}$ | | 0.6 | | 1.4 | V |
| Differential Input Voltage | $V_{DIFF}$ | | 150 | | 500 | mV |
| Input Differential Termination Resistance | $R_{TERM}$ | | 85 | 110 | 135 | Ω |
| Input Current | $I_{IN}$ | $V_{IN}$ = 0.35V to 1.65V, both inputs at same voltage | | | +/-25 | µA |
| Power-down Mode Input Current | | $V_{IN}$ = TBDV to TBDV, both inputs at same voltage | | | +/-TBD | uA |
| Sleep Mode Input Current | | $V_{IN}$ = TBDV to TBDV, both inputs at same voltage | | | +/-TBD | uA |
| **DC ELECTRICAL CHARACTERISTICS / I/O PINS** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{DDIO}$ | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.3 x $V_{DDIO}$ | V |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = -4mA | $V_{DDIO}$ - 0.4 | | | V |
| Low-Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 4mA | | | 0.4 | V |
| Input Current | $I_{IN}$ | All pullup/pulldown devices disabled. $V_{IN}$ = 0V to $V_{DDIO}$ | | | 1 | µA |
| Input Capacitance | $C_{IN}$ | | | 3 | | pF |
| Internal Pullup/Pulldown Resistance | $R_{IN}$ | 40kΩ enabled | | 40 | | kΩ |
| | | 1MΩ enabled | | 1 | | MΩ |
| **DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{DDIO}$ | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.3 x $V_{DDIO}$ | V |

## Electrical Characteristics (continued)

($V_{DD18}$ = 1.7V to 1.9V, $V_{DD}$ = 0.95V to 1.05V or 1.14V to 1.26V, $V_{DDIO}$ = 1.7V to 1.9V or 3.0V to 3.6V, $T_A$ = -40°C to +105°C, EP connected to PCB ground, typical values are at $V_{DD18}$ = $V_{DDIO}$ = 1.8V, $V_{DD}$ = 1.0V, $T_A$ = 25°C, unless otherwise noted. (Note 3))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Low-Level Open-Drain Output Voltage | $V_{OL}$ | $I_{OL}$ = 4mA | | | 0.4 | V |
| Input Current | $I_{IN}$ | All pullup/pulldown devices disabled. $V_{IN}$ = 0V to $V_{DDIO}$ | | | 1 | µA |
| Input Capacitance | $C_{IN}$ | | | 3 | | pF |
| Internal Pullup Resistance | $R_{PU}$ | 40kΩ enabled | | 40 | | kΩ |
| | | 1MΩ enabled | | 1 | | MΩ |
| **DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{DDIO}$ | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.3 x $V_{DDIO}$ | V |
| Input Current | $I_{IN}$ | $V_{IN}$ = 0V to $V_{DDIO}$ | | | 6 | µA |
| Input Capacitance | $C_{IN}$ | | | 3 | | pF |
| Internal Pulldown Resistance | $R_{PD}$ | | | 1 | | MΩ |
| **DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS** | | | | | | |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = -4mA | $V_{DDIO}$ - 0.4 | | | V |
| Low-Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 4mA | | | 0.4 | V |
| **DC ELECTRICAL CHARACTERISTICS / LINE-FAULT DETECTION INPUTS (LMN_)** | | | | | | |
| Open Pin Voltage | $V_{O0}$ | LMN2 | | 1.25 | | V |
| | $V_{O1}$ | LMN3 | | 0.75 | | |
| **DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (CRYSTAL) (X1/OSC, X2)** | | | | | | |
| X1 Input Capacitance | $C_{IN_X1}$ | | | 3 | | pF |
| X2 Input Capacitance | $C_{IN_X2}$ | | | 1 | | pF |
| Internal X2 Limit Resistor | $R_{LIM}$ | | | 1.2 | | kΩ |
| Internal Feedback Resistor | $R_{FB}$ | | | 10 | | kΩ |
| Transconductance | $g_m$ | | | 28 | | mA/V |
| **DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED)** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | 0.9 | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.4 | V |
| Input Impedance | $R_{IN}$ | | | 10 | | kΩ |
| X1 Input Capacitance | $C_{IN_X1}$ | | | 3 | | pF |

## Electrical Characteristics (continued)

($V_{DD18}$ = 1.7V to 1.9V, $V_{DD}$ = 0.95V to 1.05V or 1.14V to 1.26V, $V_{DDIO}$ = 1.7V to 1.9V or 3.0V to 3.6V, $T_A$ = -40°C to +105°C, EP connected to PCB ground, typical values are at $V_{DD18}$ = $V_{DDIO}$ = 1.8V, $V_{DD}$ = 1.0V, $T_A$ = 25°C, unless otherwise noted. (Note 3))

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS / 1x104MHz 3Gbps** | | | | | | | |
| Supply Current | $I_{DD}$ | 3Gbps link, dual OLDI input, 1920x720 video with 95MHz PCLK | $V_{DD18}$ | | TBD | TBD | mA |
| | | | $V_{DD}$, on-chip regulator disabled | | TBD | TBD | |
| | | | $V_{DD}$, on-chip regulator enabled | | TBD | TBD | |
| **DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS / 1x160MHz 6Gbps** | | | | | | | |
| Supply Current | $I_{DD}$ | 6Gbps link, dual OLDI input, 1920x1080 video with 148.5MHz PCLK | $V_{DD18}$ | | 115 | TBD | mA |
| | | | $V_{DD}$, on-chip regulator disabled | | 90 | TBD | |
| | | | $V_{DD}$, on-chip regulator enabled | | 85 | TBD | |
| **DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS / 1x215MHz 6Gbps** | | | | | | | |
| Supply Current | $I_{DD}$ | 2560x1080/60Hz uncompressed video over single 6Gbps link, 198MHz PCLK, no HDCP | $V_{DD18}$ | | TBD | TBD | mA |
| | | | $V_{DD}$, on-chip regulator disabled | | TBD | TBD | |
| | | | $V_{DD}$, on-chip regulator enabled | | TBD | TBD | |
| **DC ELECTRICAL CHARACTERISTICS / $V_{DDIO}$ Currents** | | | | | | | |
| Maximum $V_{DDIO}$ Supply Current | $I_{DDIO}$ | Per toggling GPIO, $C_L$ = 20pF | $V_{DDIO}$ at 1.9V | | 44 | | µA/MHz |
| | | | $V_{DDIO}$ at 3.6V | | 81 | | |
| **DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENTS** | | | | | | | |
| Maximum Power-Down Current | $I_{DD}$ | $V_{DDIO}$ at 3.6V | $T_A$ = +25ºC | | TBD | | µA |
| | | | $T_A$ = +105ºC | | TBD | | |
| | | $V_{DD18}$ at 1.9V | $T_A$ = +25ºC | | TBD | | |
| | | | $T_A$ = +105ºC | | TBD | | |
| | | $V_{DD}$ at 1.26V | $T_A$ = +25ºC | | TBD | | |
| | | | $T_A$ = +105ºC | | TBD | | |
| **DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENTS** | | | | | | | |
| Maximum Sleep Current | $I_{DD}$ | $V_{DDIO}$ at 3.6V | $T_A$ = +25ºC | | TBD | | µA |
| | | | $T_A$ = +105ºC | | TBD | | |
| | | $V_{DD18}$ at 1.9V | $T_A$ = +25ºC | | TBD | | |
| | | | $T_A$ = +105ºC | | TBD | | |
| | | $V_{DD}$ at 1.26V | $T_A$ = +25ºC | | TBD | | |
| | | | $T_A$ = +105ºC | | TBD | | |
| **AC ELECTRICAL CHARACTERISTICS / FORWARD CHANNEL SWITCHING CHARACTERISTICS** | | | | | | | |
| Serial Output Rise Time | $t_R$ | 20% to 80%, $V_O$ = 400mV, $R_L$ = 100Ω ±1% | | | 50 | | ps |

## Electrical Characteristics (continued)

($V_{DD18}$ = 1.7V to 1.9V, $V_{DD}$ = 0.95V to 1.05V or 1.14V to 1.26V, $V_{DDIO}$ = 1.7V to 1.9V or 3.0V to 3.6V, $T_A$ = -40°C to +105°C, EP connected to PCB ground, typical values are at $V_{DD18}$ = $V_{DDIO}$ = 1.8V, $V_{DD}$ = 1.0V, $T_A$ = 25°C, unless otherwise noted. (Note 3))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial Output Fall Time | $t_F$ | 80% to 20%, $V_O$ = 400mV, $R_L$ = 100Ω ±1% | | 50 | | ps |
| Total Serial Output Jitter | $t_{TSOJ}$ | PRBS7, single-ended or differential output | | 0.15 | | UI (p-p) |
| Deterministic Serial Output Jitter | $t_{DSOJ}$ | PRBS7, single-ended or differential output | | 0.10 | | UI (p-p) |
| Lock Time | $t_{LOCK}$ | From power-up, one-shot reset, or rising edge of PWDNB to rising edge of LOCK Figure 2 | | 25 | | ms |
| Maximum Video Initialization Time | $t_{VIDEOSTART}$ | Time from video applied to input to when the first video packet appears at GMSL2 outputs, assuming link is already established Figure 3 | | TBD | | ms |
| Maximum Video Latency | $t_{VL}$ | Time from OLDI pixel input to SIO_ output in GMSL2 packet Figure 4 | | TBD | | s |
| PWDNB Hold Time | $t_{HOLD_PWDNB}$ | The minimum duration PWDNB must be held LOW to reset the chip. | | 1 | | µs |
| **AC ELECTRICAL CHARACTERISTICS / OLDI RECEIVER (Note 4)** | | | | | | |
| Clock Frequency | $F_{RCLKIN}$ | | 6.45 | | 160 | MHz |
| Data Rate | | Per active lane | | | 1120 | Mbps |
| Data-to-Clock Skew Tolerance | $t_{RSKM}$ | (Note 5) [[Figure x]] | 0.3 | | | UI |
| Gang-Mode Clock Skew Tolerance | | (Note 6) [[Figure x]] | TBD | | | UI |
| **AC ELECTRICAL CHARACTERISTICS / I²C/UART PORT TIMING** | | | | | | |
| Output Fall Time | $t_F$ | 70% to 30%, $C_L$ = 20pF to 100pF, 1kΩ pullup to $V_{DDIO}$ (Note 4) | 20 x $V_{DDIO}$/5.5V | | 150 | ns |
| I²C/UART Wake Time | | From power-up, or rising edge of PWDNB to local register access. For remote register access, I²C/UART Wake Time is the same as Lock Time ($t_{LOCK}$). | | 3 | TBD | ms |
| **AC ELECTRICAL CHARACTERISTICS / I²C TIMING - See Figure 5** | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | Low $f_{SCL}$ range: (I²C MST_BT = 010, I²C SLV_SH = 10) | 9.6 | | 100 | kHz |
| | | Mid $f_{SCL}$ range: (I²C MST_BT = 101, I²C SLV_SH = 01) | 100 | | 400 | |
| | | High $f_{SCL}$ range: (I²C MST_BT = 111, I²C SLV_SH = 00) | 400 | | 1000 | |
| Start Condition Hold Time | $t_{HD:STA}$ | $f_{SCL}$ range, low | 4 | | | µs |
| | | $f_{SCL}$ range, mid | 0.6 | | | |
| | | $f_{SCL}$ range, high | 0.26 | | | |

## Electrical Characteristics (continued)

($V_{DD18}$ = 1.7V to 1.9V, $V_{DD}$ = 0.95V to 1.05V or 1.14V to 1.26V, $V_{DDIO}$ = 1.7V to 1.9V or 3.0V to 3.6V, $T_A$ = -40°C to +105°C, EP connected to PCB ground, typical values are at $V_{DD18}$ = $V_{DDIO}$ = 1.8V, $V_{DD}$ = 1.0V, $T_A$ = 25°C, unless otherwise noted. (Note 3))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Low Period of SCL Clock | $t_{LOW}$ | $f_{SCL}$ range, low | 4.7 | | | µs |
| | | $f_{SCL}$ range, mid | 1.3 | | | |
| | | $f_{SCL}$ range, high | 0.5 | | | |
| High Period of SCL Clock | $t_{HIGH}$ | $f_{SCL}$ range, low | 4 | | | µs |
| | | $f_{SCL}$ range, mid | 0.6 | | | |
| | | $f_{SCL}$ range, high | 0.26 | | | |
| Repeated Start Condition Setup Time | $t_{SU:STA}$ | $f_{SCL}$ range, low | 4.7 | | | µs |
| | | $f_{SCL}$ range, mid | 0.6 | | | |
| | | $f_{SCL}$ range, high | 0.26 | | | |
| Data Hold Time | $t_{HD:DAT}$ | $f_{SCL}$ range, low | 0 | | | ns |
| | | $f_{SCL}$ range, mid | 0 | | | |
| | | $f_{SCL}$ range, high | 0 | | | |
| Data Setup Time | $t_{SU:DAT}$ | $f_{SCL}$ range, low | 250 | | | ns |
| | | $f_{SCL}$ range, mid | 100 | | | |
| | | $f_{SCL}$ range, high | 50 | | | |
| Setup Time for Stop Condition | $t_{SU:STO}$ | $f_{SCL}$ range, low | 4 | | | µs |
| | | $f_{SCL}$ range, mid | 0.6 | | | |
| | | $f_{SCL}$ range, high | 0.26 | | | |
| Bus Free Time | $t_{BUF}$ | $f_{SCL}$ range, low | 4.7 | | | µs |
| | | $f_{SCL}$ range, mid | 1.3 | | | |
| | | $f_{SCL}$ range, high | 0.5 | | | |
| Data Valid Time | $t_{VD:DAT}$ | $f_{SCL}$ range, low | | | 3.45 | µs |
| | | $f_{SCL}$ range, mid | | | 0.9 | |
| | | $f_{SCL}$ range, high | | | 0.45 | |
| Data Valid Acknowledge Time | $t_{VD:ACK}$ | $f_{SCL}$ range, low | | | 3.45 | µs |
| | | $f_{SCL}$ range, mid | | | 0.9 | |
| | | $f_{SCL}$ range, high | | | 0.45 | |
| Pulse Width of Spikes Suppressed | $t_{SP}$ | $f_{SCL}$ range, low | | | 50 | ns |
| | | $f_{SCL}$ range, mid | | | 50 | |
| | | $f_{SCL}$ range, high | | | 50 | |
| Capacitive Load On Each Bus Line | $C_B$ | (Note 4) | | | 100 | pF |
| **AC ELECTRICAL CHARACTERISTICS / SPI MASTER - See Figure 6 (Note 7)** | | | | | | |
| Operating Frequency | $f_{MCK}$ | (Note 4) | 0.588 | | 50 | MHz |
| SCLK Period | $t_{MCK}$ | | | $1/f_{MCK}$ | | ns |
| SCLK Output Pulse-Width High/Low | $t_{MCH}$, $t_{MCL}$ | $C_L$ = 5pF, (Note 4) | $t_{MCK}/2$ - 3.4 | $t_{MCK}/2$ | | ns |

## Electrical Characteristics (continued)

($V_{DD18}$ = 1.7V to 1.9V, $V_{DD}$ = 0.95V to 1.05V or 1.14V to 1.26V, $V_{DDIO}$ = 1.7V to 1.9V or 3.0V to 3.6V, $T_A$ = -40°C to +105°C, EP connected to PCB ground, typical values are at $V_{DD18}$ = $V_{DDIO}$ = 1.8V, $V_{DD}$ = 1.0V, $T_A$ = 25°C, unless otherwise noted. (Note 3))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| MOSI Data Output Delay | $t_{MOD}$ | After SCLK falling edge (Note 4) | -2.3 | | 2.3 | ns |
| MISO Input Setup Time | $t_{MIS}$ | Before programmed sampling edge, (Note 4) | 13.5 | | | ns |
| MISO Input Hold Time | $t_{MIH}$ | After programmed sampling edge, (Note 4) | -2 | | | ns |
| **AC ELECTRICAL CHARACTERISTICS / SPI SLAVE - See Figure 7 (Note 7)** | | | | | | |
| Operating Frequency | $f_{SCK}$ | (Note 4) | | | 50 | MHz |
| SCLK Period | $t_{SCK}$ | | | $1/f_{SCK}$ | | ns |
| MISO Data Output Delay | $t_{SOD}$ | After SCLK falling edge (Note 4) | 2.0 | | 11.3 | ns |
| MOSI Input Setup Time | $t_{SIS}$ | Before SCLK rising edge, (Note 4) | 5 | | | ns |
| MOSI Input Hold Time | $t_{SIH}$ | After SCLK rising edge, (Note 4) | 3 | | | ns |
| **AC ELECTRICAL CHARACTERISTICS / I²S/TDM SLAVE TIMING (Note 4) - See Figure 9** | | | | | | |
| WS Frequency | $f_{WS}$ | | 8 | | 192 | kHz |
| Sample Word Length | $n_{WS}$ | | 8 | | 32 | Bits |
| SCK Frequency | $f_{SCK}$ | $f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$ | 0.512 | | 49.152 | MHz |
| SD, WS Setup Time | $t_{SAS}$ | | 4 | | | ns |
| SD, WS Hold Time | $t_{SAH}$ | | 4 | | | ns |
| **AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL)(X1/OSC, X2) (Note 4)** | | | | | | |
| Frequency | $f_{XTAL}$ | | | 25 | | MHz |
| Frequency Stability + Frequency Tolerance | $f_{TN}$ | | | | ±200 | ppm |
| **AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1/OSC, X2 UNCONNECTED) (Note 4)** | | | | | | |
| Frequency | $f_{REF}$ | | | 25 | | MHz |
| Frequency Stability + Frequency Tolerance | $f_{TN}$ | | | | ±200 | ppm |
| Input Jitter | | 6Gbps/187.5Mbps, sinusoidal jitter < 1MHz (falling edge), downstream deserializer using crystal reference. | | | 600 | ps p-p |
| Input Duty Cycle | $t_{DUTY}$ | | 40 | | 60 | % |
| Input Fall Time | $t_F$ | 80% to 20% | | | 4 | ns |
| **AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK OUTPUT (RCLKOUT)** | | | | | | |
| Frequency | $f_{REFOUT}$ | Crystal or reference clock input, $f_{REF}$ / 1 | | 25 | | MHz |
| | | Crystal or reference clock input, $f_{REF}$ / 2 | | 12.5 | | |
| | | Crystal or reference clock input, $f_{REF}$ / 4 | | 6.25 | | |
| Rise Time | $t_R$ | 20% to 80%, $C_L$ = 10pF, 25MHz divided by 1, 2, or 4, (Note 4, Note 8) | | | 4 | ns |

## Electrical Characteristics (continued)

($V_{DD18}$ = 1.7V to 1.9V, $V_{DD}$ = 0.95V to 1.05V or 1.14V to 1.26V, $V_{DDIO}$ = 1.7V to 1.9V or 3.0V to 3.6V, $T_A$ = -40°C to +105°C, EP connected to PCB ground, typical values are at $V_{DD18}$ = $V_{DDIO}$ = 1.8V, $V_{DD}$ = 1.0V, $T_A$ = 25°C, unless otherwise noted. (Note 3))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Fall Time | $t_F$ | 80% to 20%, $C_L$ = 10pF, 25MHz divided by 1, 2, or 4, (Note 4, Note 8) | | | 4 | ns |
| Jitter | $t_J$ | $C_L$ = 10pF, rising or falling edge, $f_{REFOUT}$ = 12.5MHz | | 260 | | $ps_{(P-P)}$ |
| **ESD PROTECTION** | | | | | | |
| SIO__ | $V_{ESD}$ | Human Body Model (HBM), $R_D$ = 1.5kΩ, $C_S$ = 100pF | | ±8 | | kV |
| | | ISO10605, $R_D$ = 330Ω, $C_S$ = 150pF, contact discharge, coax configuration | | ±6 | | |
| | | ISO10605, $R_D$ = 330Ω, $C_S$ = 150pF, contact discharge, STP configuration | | ±4 | | |
| | | ISO10605, $R_D$ = 330Ω, $C_S$ = 150pF, air discharge | | ±8 | | |
| | | AEC-Q100-011 Rev-C1, Charged Device Model (CDM) | | 750 | | V |
| All Other Pins | $V_{ESD}$ | Human Body Model (HBM), $R_D$ = 1.5kΩ, $C_S$ = 100pF | | ±4 | | kV |
| | | AEC-Q100-011 Rev-C1, Charged Device Model (CDM) | | 750 | | V |

**Note 5:** Skew between clock and data. No clock spread spectrum. Includes skew between clock and 8 data lanes if 1 clock is used in ganged input mode. Skew is the total of all deterministic and random skews, including clock alignment to the mean bit position, bit position error, complementary signal pair skew, other deterministic skews, and jitter. When analyzing, the instrument external clock must use bandwidth filtering appropriate for the pixel clock. Refer to [[LVDS Receiver Input Skew Margin]].

**Note 3:** Limits are 100% tested at $T_A$ = +105°C unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

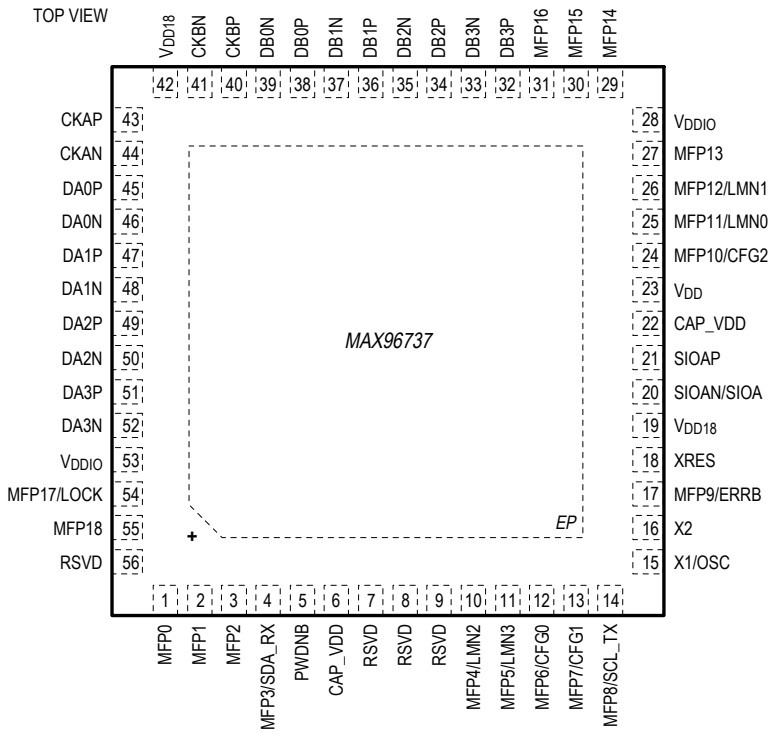
**Note 4:** Not production tested. Guaranteed by design.

**Note 6:** Skew tolerance between clocks if 2 clocks are used in ganged input mode. Not applicable if HS/VS/DE is used for alignment. HS/VS/DE would need to be available on both ports and serializer programmed to perform alignment using HS/VS/DE.

**Note 7:** Measured at 50MHz. For $V_{DDIO}$ = 1.7V–2.24V, SPI_SPEED[1:0] = 00 and for $V_{DDIO}$ = 2.25V–3.6V, SPI_SPEED[1:0] = 01.

**Note 8:** MFP pin speed configured based on VDDIO:
TTS = 01 for $V_{DDIO}$ < 3V
TTS = 10 for $V_{DDIO}$ ≥ 3V
See Table 13 for details regarding output speed programming.

## Pin Configuration




## Pin Descriptions

| PIN | NAME | FUNCTION MODE | FUNCTION |
|---|---|---|---|
| | | GMSL2 | |
| **GMSL2 SERIAL LINK** | | | |
| 20 | SIOAN/SIOA | SIOAN<br>SIOA | SIOAN: GMSL2 Inverted Twisted-Pair Serial-Data Input/Output.<br>SIOA: GMSL2 Coax Serial-Data Input/Output.<br>State of CFG2 on power-up determines configuration. |
| 21 | SIOAP | SIOAP | SIOAP: GMSL2 Link-A Noninverted Coax/Twisted-Pair Serial-Data Output. State of CFG2 on power-up determines configuration. |
| **OLDI INTERFACE** | | | |
| 32 | DB3P | DB3P | OLDI Port-B Data Lane 3 Noninverted Input |
| 33 | DB3N | DB3N | OLDI Port-B Data Lane 3 Inverted Input |
| 34 | DB2P | DB2P | OLDI Port-B Data Lane 2 Noninverted Input |
| 35 | DB2N | DB2N | OLDI Port-B Data Lane 2 Inverted Input |
| 36 | DB1P | DB1P | OLDI Port-B Data Lane 1 Noninverted Input |
| 37 | DB1N | DB1N | OLDI Port-B Data Lane 1 Inverted Input |

| PIN | NAME | FUNCTION MODE | FUNCTION |
|---|---|---|---|
| | | GMSL2 | |
| 38 | DB0P | DB0P | OLDI Port-B Data Lane 0 Noninverted Input |
| 39 | DB0N | DB0N | OLDI Port-B Data Lane 0 Inverted Input |
| 40 | CKBP | CKBP | OLDI Port-B Clock Lane Noninverted Input |
| 41 | CKBN | CKBN | OLDI Port-B Clock Lane Inverted Input |
| 43 | CKAP | CKAP | OLDI Port-A Clock Lane Noninverted Input |
| 44 | CKAN | CKAN | OLDI Port-A Clock Lane Inverted Input |
| 45 | DA0P | DA0P | OLDI Port-A Data Lane 0 Noninverted Input |
| 46 | DA0N | DA0N | OLDI Port-A Data Lane 0 Inverted Input |
| 47 | DA1P | DA1P | OLDI Port-A Data Lane 1 Noninverted Input |
| 48 | DA1N | DA1N | OLDI Port-A Data Lane 1 Inverted Input |
| 49 | DA2P | DA2P | OLDI Port-A Data Lane 2 Noninverted Input. |
| 50 | DA2N | DA2N | OLDI Port-A Data Lane 2 Inverted Input |
| 51 | DA3P | DA3P | OLDI Port-A Data Lane 3 Noninverted Input |
| 52 | DA3N | DA3N | OLDI Port-A Data Lane 3 Inverted Input |
| **MULTIFUNCTION PINS (*Denotes default state after power-up. ♦Input read or output write by register programming only.)** | | | |
| 1 | MFP0 | GPI*<br>RCLKOUT<br>SCLK<br>SD<br>(HS)<br>GPIO0 | GPI: General Purpose Input with internal 1MΩ pulldown to ground.<br><br>RCLKOUT: 25MHz Frequency Reference Push-Pull Output; Enabled or disabled by the state of CFG1 at power-up.<br><br>SCLK: SPI Clock. When configured as master, push-pull clock output. When configured as slave, clock input with internal 1MΩ pulldown to ground.<br><br>SD: $I^2S$ Serial-Data Input with internal 1MΩ Pulldown to Ground. Supports forward-path audio.<br><br>(HS: Horizontal Sync Push-Pull Output.)<br><br>GPIO0: Configurable General Purpose Input or Output. Default power-up, open-drain output, internal 40kΩ pullup to $V_{DDIO}$. |
| 2 | MFP1 | GPI*<br>MOSI<br>WS<br>(VS)<br>GPIO1 | GPI: General Purpose Input with internal 1MΩ pulldown to ground.<br><br>MOSI: SPI Master-Out Slave-In. When configured as master, push-pull output that drives data to external slave. When configured as slave, input with internal 1MΩ pulldown to ground that receives data from external master.<br><br>WS: $I^2S$ Word-Select Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio.<br><br>(VS: Vertical Sync Push-Pull Output.)<br><br>GPIO1: Configurable General-Purpose Input or Output. |

| PIN | NAME | FUNCTION MODE | FUNCTION |
|---|---|---|---|
| | | GMSL2 | |
| 3 | MFP2 | GPI*<br>MISO<br>SCK<br>PCLK<br>GPIO2 | GPI: General Purpose Input with internal 1MΩ pulldown to ground.<br><br>MISO: SPI Master In Slave Out. When configured as master, input with internal 1MΩ pulldown to ground that receives data from external slave. When configured as slave, push-pull output that drives data to an external master.<br><br>SCK: $I^2S$ Serial Clock Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio.<br><br>PCLK: Pixel Clock Push-Pull Output.<br><br>GPIO2: Configurable General-Purpose Input or Output. |
| 4 | MFP3/SDA_RX | SDA_RX*<br>GPIO3 | SDA: $I^2C$ Data Input/Open-Drain Output with Internal 40kΩ Pullup to $V_{DDIO}$ (SDA or RX selected by CFG0 at power-up). Provides access to internal GMSL device registers and peripheral registers.<br><br>RX: UART Input (SDA or RX selected by CFG0 at power-up). Provides access to internal GMSL device registers and peripheral registers.<br><br>GPIO3: Configurable General-Purpose Input or Output. |
| 10 | MFP4/LMN2 | GPI*<br>LMN2<br>BNE_SS1<br>SDA2_RX2<br>GPIO4 | GPI: General-Purpose Input with Internal 1MΩ Pulldown to Ground.<br><br>LMN2: Line Fault Monitor Input.<br><br>BNE: SPI Buffer Not Empty. When Configured as Slave, SPI Push-pull Output. BNE = high indicates SPI data is available.<br><br>SS1: SPI Slave Select. When configured as master, slave 1 select push-pull output.<br><br>SDA2: Pass-Through $I^2C$ Data Input/Open-Drain Output with Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>RX2: Pass-Through UART Input.<br><br>GPIO4: Configurable General-Purpose Input or Output. |

| PIN | NAME | FUNCTION MODE | FUNCTION |
|---|---|---|---|
| | | GMSL2 | |
| 11 | MFP5/LMN3 | GPI*<br>LMN3<br>RO_SS2<br>SCL2_TX2<br>GPIO5 | GPI: General-Purpose Input with Internal 1MΩ Pulldown to Ground.<br><br>LMN3: Line Fault Monitor Input.<br><br>RO: When Configured as Slave, SPI Mode-Select Input with Internal 1MΩ Pulldown to Ground. RO = high enables master read from MISO. RO = low enables master write to MOSI.<br><br>SS2: SPI Slave Select. When configured as master, slave 2 select push-pull output.<br><br>SCL2: Pass-Through $I^2C$ Clock Input/Open-Drain Output with Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>TX2: Pass-Through UART Output with Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>GPIO5: Configurable General-Purpose Input or Output. |
| 12 | MFP6/CFG0 | CFG0<br>HiZ*<br>GPO6 | CFG0: Configuration Pin 0. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between $V_{DDIO}$ and ground. See Table 4.<br><br>Hi-Z: Disabled. No Internal Pullup or Pulldown.<br><br>GPO6: General-Purpose Push-Pull Output. Disabled by default to accommodate CFG0 function. |
| 13 | MFP7/CFG1 | CFG1<br>Hi-Z*<br>GPO7 | CFG1: Configuration Pin 1. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between $V_{DDIO}$ and ground. See Table 5.<br><br>Hi-Z: Disabled. No Internal Pullup or Pulldown.<br><br>GPO7: General-Purpose Push-Pull Output. Disabled by default to accommodate CFG1 function. |
| 14 | MFP8/SCL_TX | SCL_TX*<br>GPIO8 | SCL: $I^2C$ Clock Input/Open-Drain Output with Internal 40kΩ Pullup to $V_{DDIO}$ (SCL or TX selected by CFG0 at power-up). Provides access to internal GMSL device registers and peripheral registers.<br><br>TX: UART Open-Drain Output with Internal 40kΩ Pullup to $V_{DDIO}$ (SCL or TX selected by CFG0 at power-up). Provides access to internal GMSL device registers and peripheral registers.<br><br>GPIO8: Configurable General Purpose Input or Output. Power-up configuration, push-pull output, output logic = High. |
| 17 | MFP9/ERRB | ERRB*<br>GPIO9 | ERRB: Open-Drain Error Indication Output with Internal 40kΩ Pullup to $V_{DDIO}$. ERRB = low indicates that a data error, line fault, or interrupt has been detected. ERRB is high when PWDNB is low.<br><br>GPIO9: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |

| PIN | NAME | FUNCTION MODE | FUNCTION |
|---|---|---|---|
| | | GMSL2 | |
| 24 | MFP10/CFG2 | CFG2<br>Hi-Z*<br>(DE)<br>GPO10 | CFG2: Configuration Pin 2. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between $V_{DDIO}$ and ground. See Table 6.<br><br>Hi-Z: Disabled. No Internal Pullup or Pulldown.<br><br>(DE: Data Enable. Nominally high during active video period.)<br><br>GPO10: General-Purpose Push-Pull Output. Disabled by default to accommodate CFG2 function. |
| 25 | MFP11/LMN0 | GPI*<br>LMN0<br>GPIO11 | GPI: General-Purpose Input.<br><br>LMN0: Line Fault Monitor Input<br><br>GPIO11: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |
| 26 | MFP12/LMN1 | GPI*<br>LMN1<br>GPIO12 | GPI: General-Purpose Input.<br><br>LMN1: Line Monitor Input.<br><br>GPIO12: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |
| 27 | MFP13 | GPI*<br>SDA1_RX1<br>BNE_SS1<br>GPIO13 | GPI: General-Purpose Input.<br><br>SDA1: Pass-Through $I^2C$ Data Input/Open-Drain Output with Internal 40kΩ Pullup to $V_{DDIO}$<br><br>RX1: Pass-Through UART Input.<br><br>BNE: SPI Buffer Not Empty. When configured as slave, SPI push-pull output. BNE = high indicates SPI data is available.<br><br>SS1: SPI Slave Select. When configured as master, slave 1 select push-pull output.<br><br>GPIO13: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |

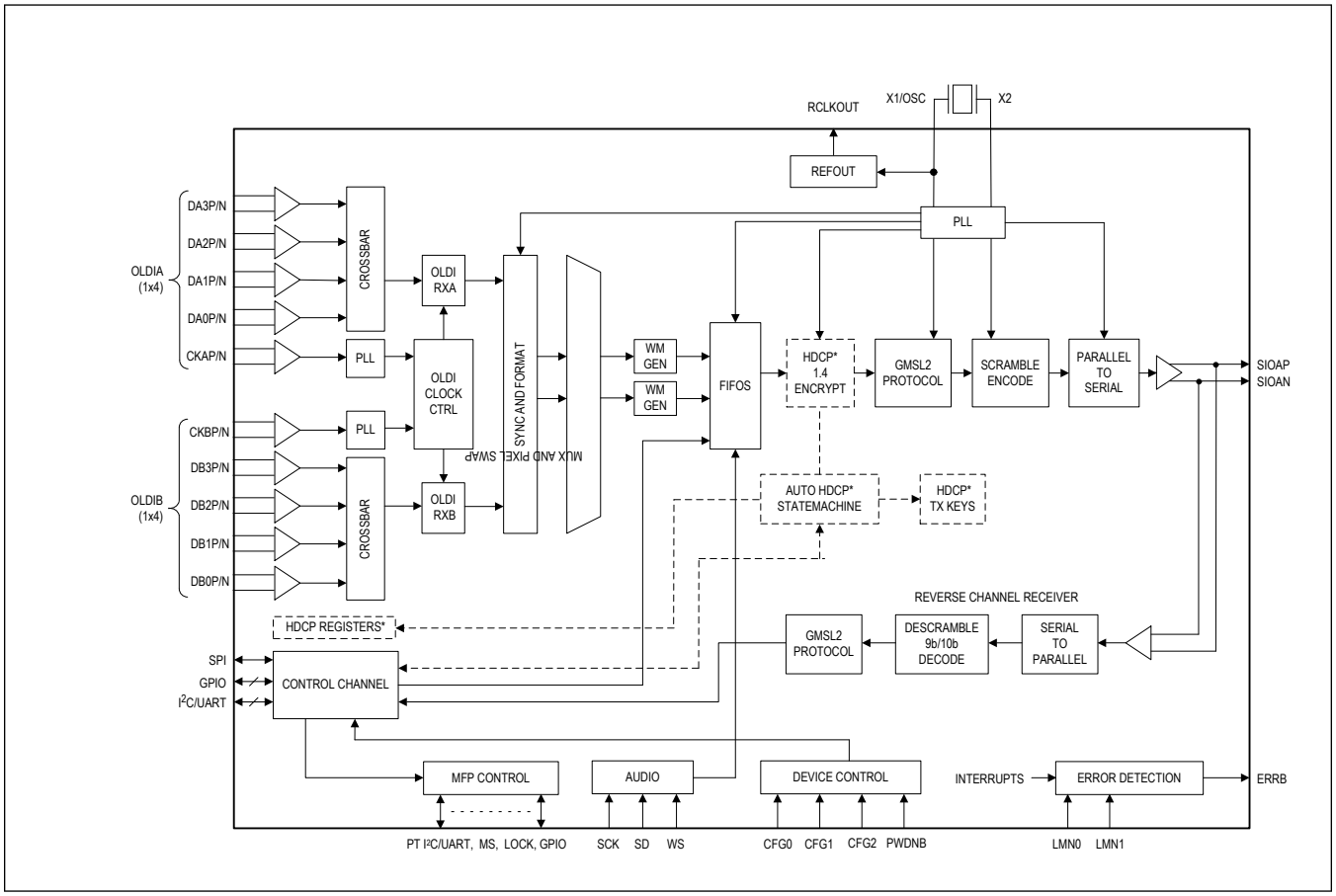
| PIN | NAME | FUNCTION MODE | FUNCTION |
|---|---|---|---|
| | | GMSL2 | |
| 29 | MFP14 | GPI*<br>SCL1_TX1<br>RO_SS2<br>GPIO14 | GPI: General-Purpose Input<br><br>SCL1: Pass-Through $I^2C$ Clock Input/Open-Drain Output with Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>TX1: Pass-Through UART Output with Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>RO: When Configured as Slave, SPI Mode-Select Input with Internal 1MΩ Pulldown to Ground. RO = high enables master read from MISO. RO = low enables master write to MOSI.<br><br>SS2: SPI Slave Select. When configured as master, slave 2 select push-pull output.<br><br>GPIO14: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |
| 30 | MFP15 | GPI*<br>SDA2_RX2<br>SCK<br>GPIO15 | GPI: General-Purpose Input.<br><br>SDA2: Pass-Through $I^2C$ Data Input/Open-drain Output with Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>RX2: Pass-Through UART Input.<br><br>SCK: $I^2S$ Serial Clock Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio.<br><br>GPIO15: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |
| 31 | MFP16 | GPI*<br>SCL2_TX2<br>WS<br>GPIO16 | GPI: General-Purpose Input.<br><br>SCL2: Pass-Through $I^2C$ Data Input/Open-drain Output with Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>TX2: Pass-Through UART Output with Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>WS: $I^2S$ Word-Select Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio.<br><br>GPIO16: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |

| PIN | NAME | FUNCTION MODE | FUNCTION |
|---|---|---|---|
| | | GMSL2 | |
| 54 | MFP17 | LOCK*<br>SD<br>MS<br>BNE_SS1<br>GPIO17 | LOCK: Open-Drain Lock Indication Output With Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>SD: $I^2S$ Serial-Data Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio.<br><br>MS: UART Mode Select with Internal 1MΩ Pulldown to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be temporarily overwritten by a register write.<br>BNE: SPI Buffer Not Empty. When Configured as Slave, SPI Push-pull Output. BNE = high indicates SPI data is available.<br><br>SS1: SPI Slave Select. When configured as master, slave 1 select push-pull output.<br><br>GPIO17: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |
| 55 | MFP18 | GPI/MS*<br>RCLKOUT<br>LOCK<br>RO_SS2<br>GPIO18 | Default is MS if UART mode is selected by CFG0, otherwise it is GPI.<br>● GPI: General-Purpose Input With Internal 1MΩ Pulldown to Ground.<br>● MS: UART Mode Select with Internal 1MΩ Pulldown to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be temporarily overwritten by a register write.<br>RCLKOUT: 25MHz Reference Clock Output. Enabled by CFG1 or a register write.<br><br>RO: When Configured as Slave, SPI Mode-Select Input with Internal 1MΩ Pulldown to Ground. RO = high enables master read from MISO. RO = low enables master write to MOSI.<br><br>SS2: SPI Slave Select. When configured as master, slave 2 select push-pull output.<br><br>LOCK: Open-Drain Lock Indication Output With Internal 40kΩ Pullup to $V_{DDIO}$.<br><br>GPIO18: Configurable General-Purpose Input or Output. Power-up default: CMOS in, GMSL2 GPIO tunnel disabled, local read enabled, 1MΩ pulldown. |
| **MISCELLANEOUS - See Table 2** | | | |
| 5 | PWDNB | PWDNB | Active-Low, Power-Down Input with Internal 1MΩ Pulldown to Ground. Apply logic low to place device in power-down mode. Connect to $V_{DDIO}$/logic high for normal operation. |
| 15 | X1/OSC | X1/OSC | X1/OSC: Crystal/Oscillator Input. Connect to either one terminal of a ±200ppm 25MHz crystal or a 25MHz external clock source. If crystal is used, connect a load capacitor from X1/OSC to ground (Load capacitor value depends on crystal used). |

| PIN | NAME | FUNCTION MODE | FUNCTION |
|---|---|---|---|
| | | GMSL2 | |
| 16 | X2 | X2 | X2: Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal. If crystal is used, connect a load capacitor from X2 to ground (Load capacitor value depends on crystal used). If external oscillator is connected to X1/OSC, leave X2 floating. |
| 18 | XRES | XRES | Output reference resistor. Connect a 402Ω 1% resistor between XRES and ground. |
| 7, 8, 9, 56 | RSVD | RSVD | Reserved. Make no electrical connection to this pin. |
| **POWER SUPPLIES — See Table 2** | | | |
| 6, 22 | CAP_VDD | CAP_VDD | Decoupling capacitor for 1V core supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible. |
| 23 | $V_{DD}$ | $V_{DD}$ | 1.0V Core Supply. This pin includes an optional on-chip LDO. Connect a 0.95V to 1.05V supply to bypass LDO. Connect a 1.14V to 1.26V supply to use the internal 1.0V regulator. In order to use the internal 1V regulator, first write REG_ENABLE = 1, and then write REG_MNL = 1. Place decoupling capacitor connected to PCB ground plane as close to pin as possible. |
| 19, 42 | $V_{DD18}$ | $V_{DD18}$ | 1.7V to 1.9V Analog Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible. |
| 28, 53 | $V_{DDIO}$ | $V_{DDIO}$ | 1.7V to 3.6V I/O Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible. |
| EP | - | EP | Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance. |

## Functional Diagrams

### Functional Block Diagram




* HDCP available only on MAX96737 variants supporting HDCP

## Recommended Operating Conditions

### Recommended Operating Conditions

### Table 1. Recommended Operating Conditions

| PARAMETER | PIN | NOMINAL VOLTAGE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply Range | $V_{DD18}$ | | 1.7 | 1.8 | 1.9 | V |
| | $V_{DD}$ | 1.0 | 0.95 | 1.0 | 1.05 | |
| | | 1.2 | 1.14 | 1.2 | 1.26 | |
| | $V_{DDIO}$ | 1.8 | 1.7 | 1.8 | 1.9 | |
| | | 3.3 | 3.0 | 3.3 | 3.6 | |
| Maximum Supply Noise | $V_{DD18}$ | | | 25 | | $mV_{P-P}$ |
| | $V_{DD}$ | 1.0V | | 50 | | |
| | | 1.2V | | 50 | | |
| | $V_{DDIO}$ | 1.8V | | 50 | | |
| | | 3.3V | | 100 | | |
| Operating Junction Temperature, $T_J$ | | | -40 | | +125 | ºC |

***Note:*** *Supply noise < 1MHz.*

### External Component Requirements

See Figure 14 and Figure 13

### Table 2. External Component Requirements

| COMPONENT | SYMBOL | CONDITION | VALUE | UNIT |
|---|---|---|---|---|
| XRES | $R_{XRES}$ | | 402 ±1%. Use a single resistor. | Ω |
| Line Fault Pulldown Resistor | $R_{PD}$ | | 49.9 ±1% | kΩ |
| Line Fault Series Resistor | $R_{EXT}$ | LMN0, LMN2 (STP Mode) | 42.2 ±1% | kΩ |
| | | LMN0, LMN2 (Coax Mode) | 48.7 ±1% | |
| | | LMN1, LMN3 (STP/Coax Mode) | 48.7 ±1% | |
| Link Isolation Capacitors | $C_{LINK}$ | Place close to the SIO_ pins (20 and 21) used in the application. | 0.1 | µF |
| Termination Resistors for Unused GMSL2 Output in Coax Mode | $R_{TERM}$ | Place close to the Link Isolation Capacitor for the unused SIO output in Coax Mode. See Figure [Typical GMSL2 Link Application Circuit for Coax Cable]. | 49.9 ±1% | Ω |
| Crystal | | Place as close as possible to pins 15 and 16. | 25MHz ±200ppm | |

## Table 2. External Component Requirements (continued)

| COMPONENT | SYMBOL | CONDITION | VALUE | UNIT |
|---|---|---|---|---|
| Crystal Load Capacitors | | Use crystal loading capacitor guidance from the crystal manufacturer. Select values that compensate for the X1/OSC and X2 input and PCB node capacitance's. Place the capacitors as close as possible to pins 15 (X1/OSC) and pin 16 (X2). | | |
| $V_{DDIO}$ Decoupling Capacitors | | Place 0.01µF capacitors as close as possible to pins 28 and 53. Include a minimum of 10µF bulk decoupling on the PCB. | | |
| $V_{DD18}$ Decoupling Capacitors | | Place 0.01µF capacitors as close as possible to pins 9, 19 and 42. Include a minimum of 10µF bulk decoupling on the PCB. | | |
| $V_{DD}$ Decoupling Capacitors | | Place a 0.01µF capacitor as close as possible to pin 23. Include a minimum of 47µF bulk decoupling on the PCB. | | |
| CAP_VDD Decoupling Capacitors | | Place a 0.1µF capacitor as close as possible to pin 22. Include a minimum of 10µF bulk decoupling near this pin. Connect pin 22 to pin 6 with a low impedance (<20mΩ) trace. | | |
| Open-Drain Pullup Resistors | | Application-specific. Quantity and values depend on multi-function GPIO pin configurations. | | |

### External Component Requirements

See Figure 14 and Figure 13

## Table 3. External Component Requirements

| COMPONENT | SYMBOL | CONDITION | VALUE | UNIT |
|---|---|---|---|---|
| XRES | $R_{XRES}$ | | 402 ±1%. Use a single resistor. | Ω |
| Line Fault Pulldown Resistor | $R_{PD}$ | | 49.9 ±1% | kΩ |
| Line Fault Series Resistor | $R_{EXT}$ | LMN0, LMN2 (STP Mode) | 42.2 ±1% | kΩ |
| | | LMN0, LMN2 (Coax Mode) | 48.7 ±1% | |
| | | LMN1, LMN3 (STP/Coax Mode) | 48.7 ±1% | |
| Link Isolation Capacitors | $C_{LINK}$ | Place close to the SIO_ pins (7, 8, 20, and 21) used in the application. | 0.1 | µF |
| Termination Resistors for Unused GMSL2 Outputs in Coax Mode | $R_{TERM}$ | Place close to the Link Isolation Capacitor(s) for the unused SIO output(s) in Coax Mode. See [Typical GMSL2 Link Application Circuit for Coax Cable]. | 49.9 ±1% | Ω |
| Crystal | | Place as close as possible to pins 15 and 16. | 25MHz ±200ppm | |
| Crystal Load Capacitors | | Use crystal loading capacitor guidance from the crystal manufacturer. Select values that compensate for the X1/OSC and X2 input and PCB node capacitance's. Place the capacitors as close as possible to pins 15 (X1/OSC) and pin 16 (X2). | | |

## Table 3. External Component Requirements (continued)

| COMPONENT | SYMBOL | CONDITION | VALUE | UNIT |
|---|---|---|---|---|
| $V_{DDIO}$ Decoupling Capacitors | | Place 0.01µF capacitors as close as possible to pins 28 and 53. Include a minimum of 10µF bulk decoupling on the PCB. | | |
| $V_{DD18}$ Decoupling Capacitors | | Place 0.01µF capacitors as close as possible to pins 9, 19 and 42. Include a minimum of 10µF bulk decoupling on the PCB. | | |
| $V_{DD}$ Decoupling Capacitors | | Place a 0.01µF capacitor as close as possible to pin 23. Include a minimum of 47µF bulk decoupling on the PCB. | | |
| CAP_VDD Decoupling Capacitors | | Place 0.1µF capacitors as close as possible to pins 6 and 22. Include a minimum of 10µF bulk decoupling near one of the pins. | | |
| Open-Drain Pullup Resistors | | Application-specific. Quantity and values depend on multi-function GPIO pin configurations. | | |

### Configuration Tables

## Table 4. CFG0 Mapped Configuration

| CFG0 INPUT VOLTAGE (PERCENTAGE OF $V_{DDIO}$) (Notes A, B) | | | SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note C) | | MAPPED CONFIGURATION (Note D) | | |
|---|---|---|---|---|---|---|---|
| MIN (%) | TYP (%) | MAX (%) | R1 (Ω) | R2 (Ω) | I2CSEL | DEVICE ADDRESS | **REMOTE ACCESS** |
| 0.0 | 0.0 | 11.7 | OPEN | 10,000 | $I^2C$ | 0x40 | DISABLED |
| 16.9 | 20.2 | 23.6 | 80,600 | 20,500 | | 0x44 | |
| 28.8 | 32.1 | 35.5 | 68,100 | 32,400 | | 0x40 | ENABLED |
| 40.7 | 44.0 | 47.4 | 56,200 | 44,200 | | 0x44 | |
| 52.6 | 56.0 | 59.3 | 44,200 | 56,200 | UART | 0x44 | ENABLED |
| 64.5 | 67.9 | 71.2 | 32,400 | 68,100 | | 0x40 | |
| 76.4 | 79.8 | 83.1 | 20,500 | 80,600 | | 0x44 | DISABLED |
| 88.3 | 100 | 100 | 10,000 | OPEN | | 0x40 | |

## Table 5. CFG1 Mapped Configuration

| CFG1 INPUT VOLTAGE (PERCENTAGE OF $V_{DDIO}$) (Notes A, B) | | | SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note C) | | MAPPED CONFIGURATION | | |
|---|---|---|---|---|---|---|---|
| MIN (%) | TYP (%) | MAX (%) | R1 (Ω) | R2 (Ω) | OLDI PORTS | RCLKOUT | **OPERATING MODE** |
| 0.0 | 0.0 | 11.7 | OPEN | 10,000 | A and B | Disabled | Ganged OLDI |
| 28.8 | 32.1 | 35.5 | 68,100 | 32,400 | A Only | | Single OLDI |
| 64.5 | 67.9 | 71.2 | 32,400 | 68,100 | A Only | Enabled | Single OLDI |
| 88.3 | 100 | 100 | 10,000 | OPEN | A and B | | Ganged OLDI |

## Table 6. CFG2 Mapped Configuration

| CFG2 INPUT VOLTAGE (PERCENTAGE OF $V_{DDIO}$) (Notes A, B) | | | SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note C) | | MAPPED CONFIGURATION (Note E) | |
|---|---|---|---|---|---|---|
| MIN (%) | TYP (%) | MAX (%) | R1 (Ω) | R2 (Ω) | **CXTP** | LINK RATE |
| 0.0 | 0.0 | 11.7 | OPEN | 10,000 | Coax | 6Gbps |
| 28.8 | 32.1 | 35.5 | 68,100 | 32,400 | | 3Gbps |

## Table 6. CFG2 Mapped Configuration (continued)

| CFG2 INPUT VOLTAGE (PERCENTAGE OF $V_{DDIO}$) (Notes A, B) | | | SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note C) | | MAPPED CONFIGURATION (Note E) | |
|---|---|---|---|---|---|---|
| 64.5 | 67.9 | 71.2 | 32,400 | 68,100 | STP | 6Gbps |
| 88.3 | 100 | 100 | 10,000 | OPEN | | 3Gbps |

Notes:

A) Voltage divider resistor tolerance, $V_{DDIO}$ supply ripple, and external loading must not cause the CFG_ input voltage to exceed the maximum or minimum limits.

B) Other than the voltage divider, any load on CFG_ must be ≥ 25 x (R1 + R2).

C) Each resistor in the voltage divider must be ≤ 100kΩ.

D) I2CSEL: $I^2C$ or UART interface for SDA_RX and SCL_TX.

DEVICE ADDRESS: device address.

E) CXTP: Serial link configured to use Coax (SIO_P) or shielded-twisted-pair (SIO_P, SIO_N).

# Functional Diagrams

### Serial Output Parameters

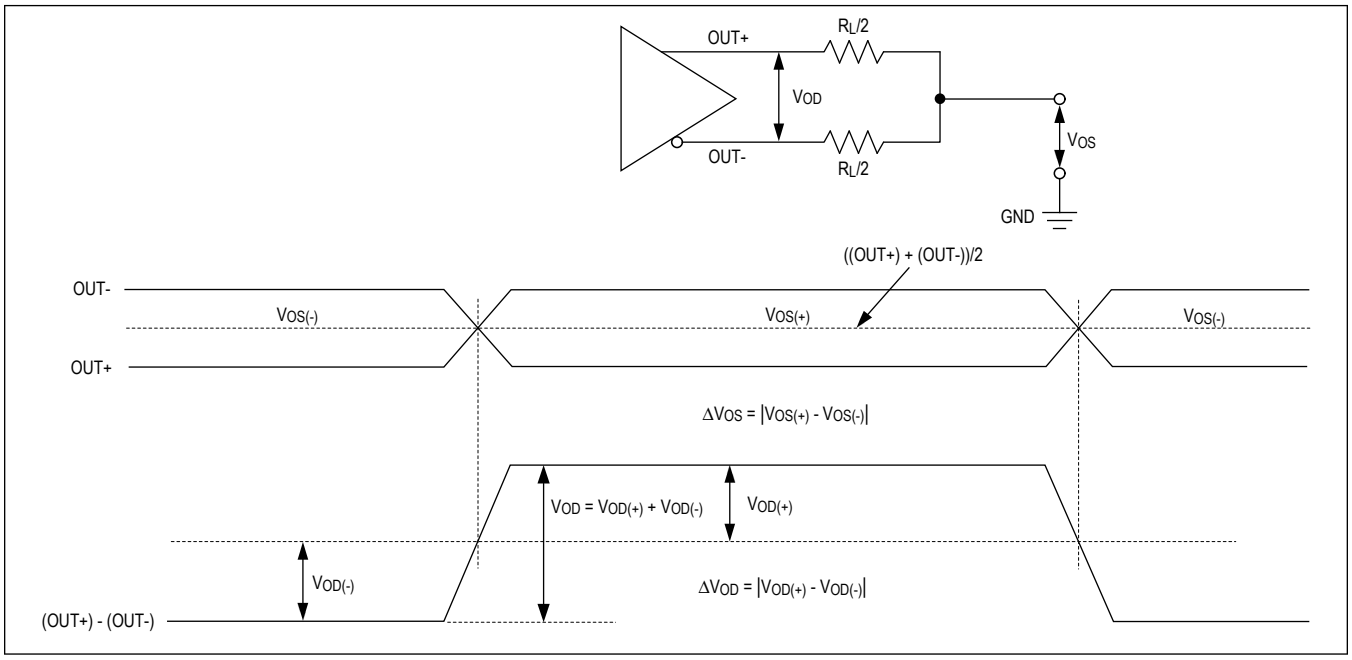



*Figure 1. Serial Output Parameters*

## GMSL2 Lock Time

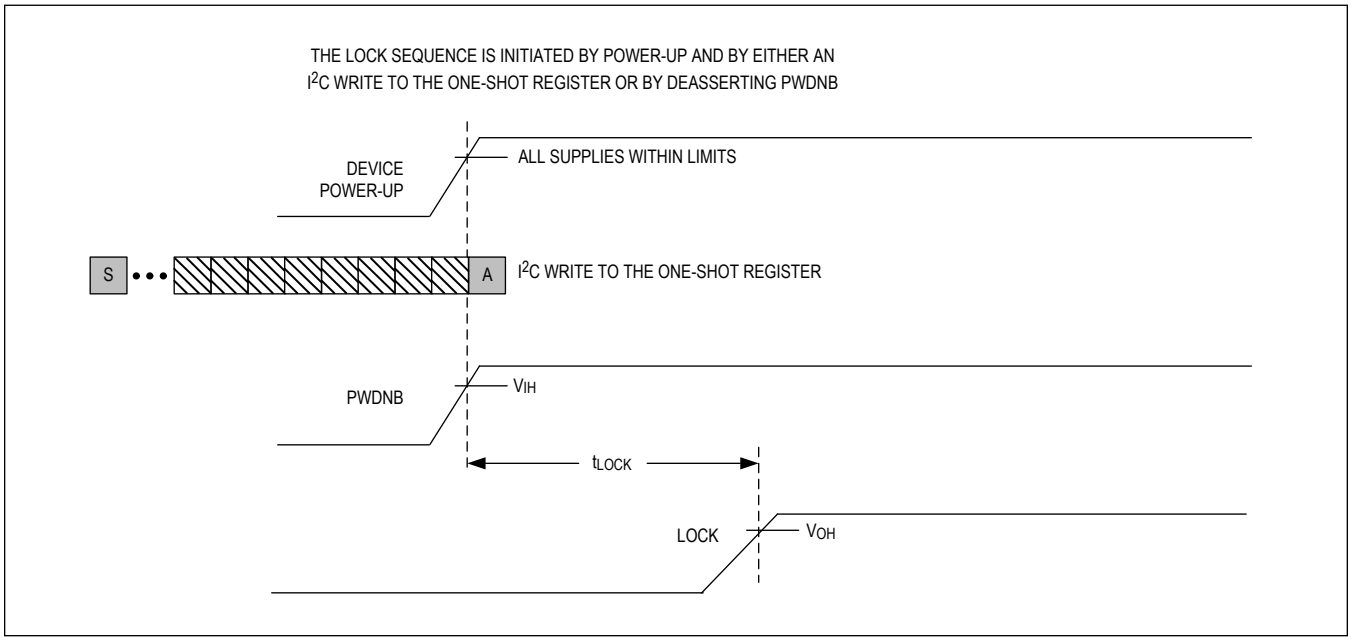



*Figure 2. GMSL2 Lock Time*

## GMSL2 Video Initialization Time

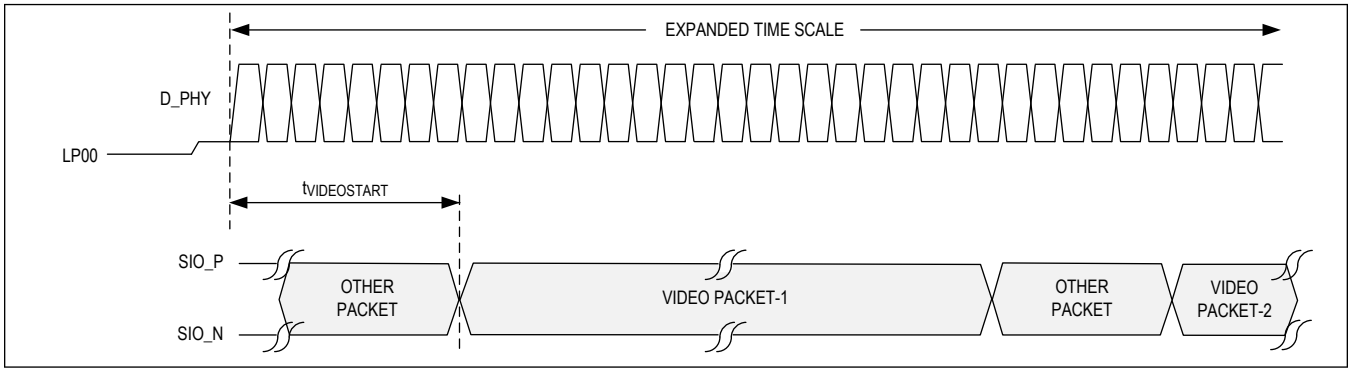



*Figure 3. GMSL2 Video Initialization Time*

## GMSL2 Video Latency

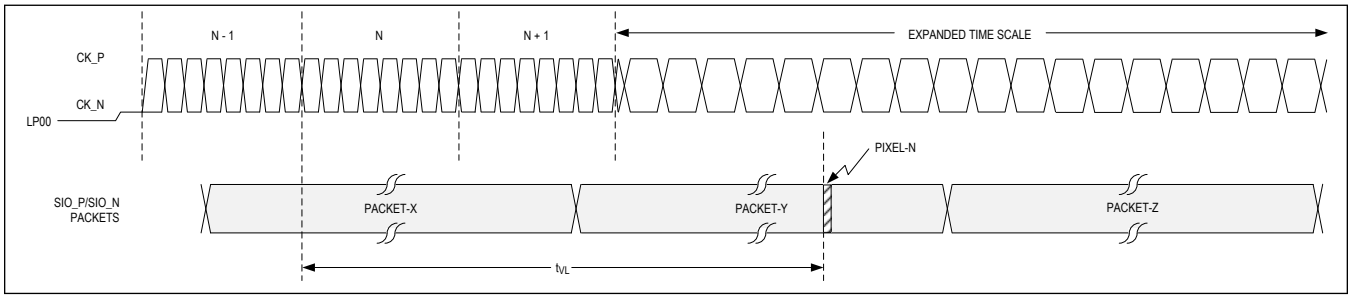



*Figure 4. GMSL2 Video Latency*

## LVDS Receiver Input Skew Margin

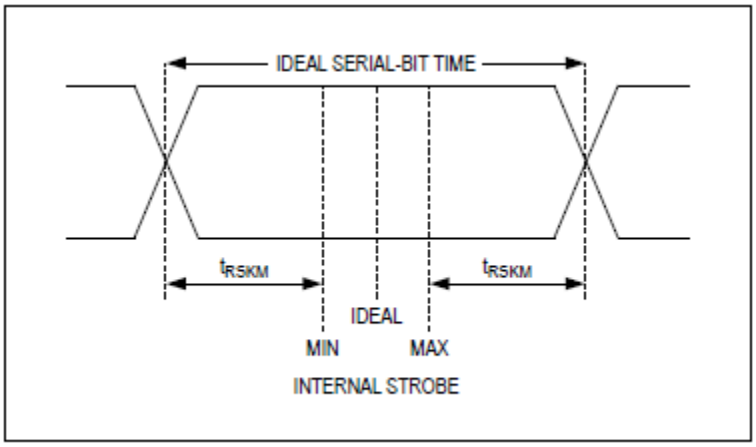



*Figure 9. LVDS Receiver Input Skew Margin*

Needs figure from MAX9277 and correct figure referencing in ECT

## LVDS Input Timing

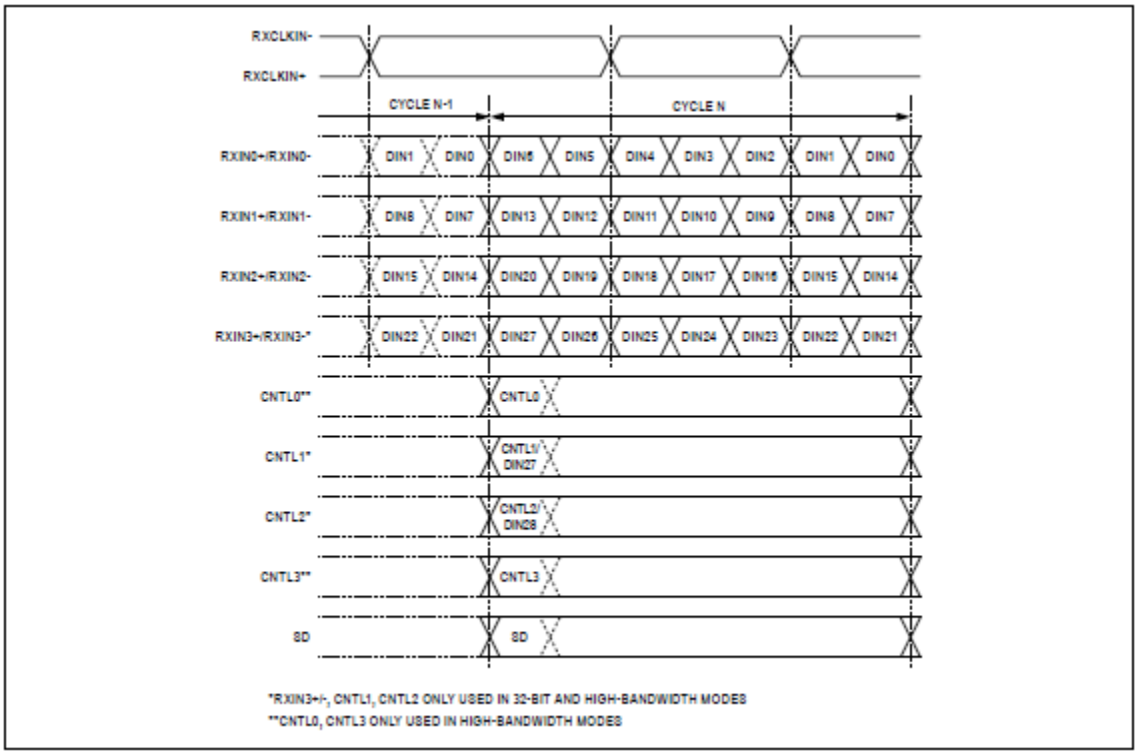



*Figure 15. LVDS Input Timing*

## LVDS Clock and Bit Assignment

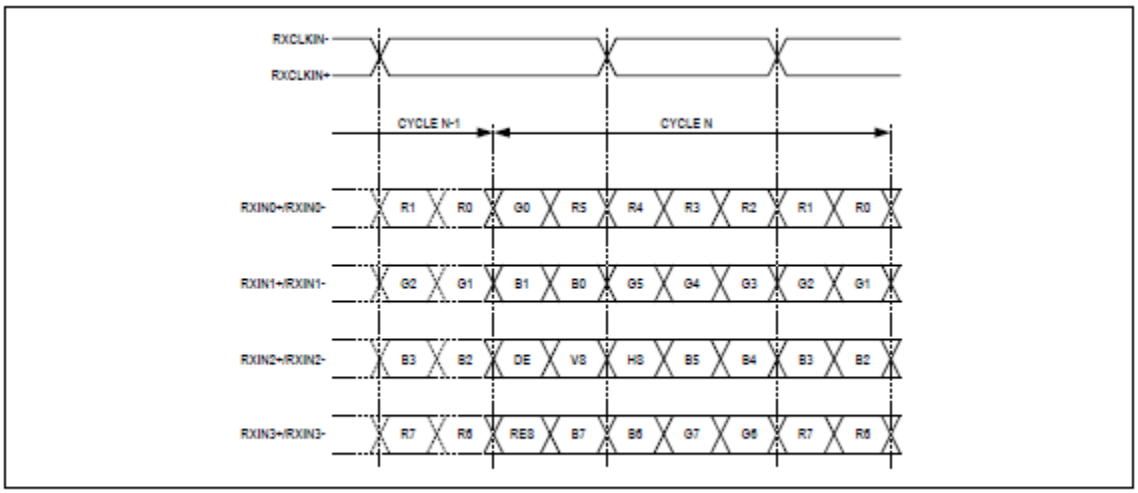



*Figure 16. LVDS Clock and Bit Assignment*

**VESA and oLDI define naming conventions with regards to MSB and LSB.*

## I²C Timing Parameters

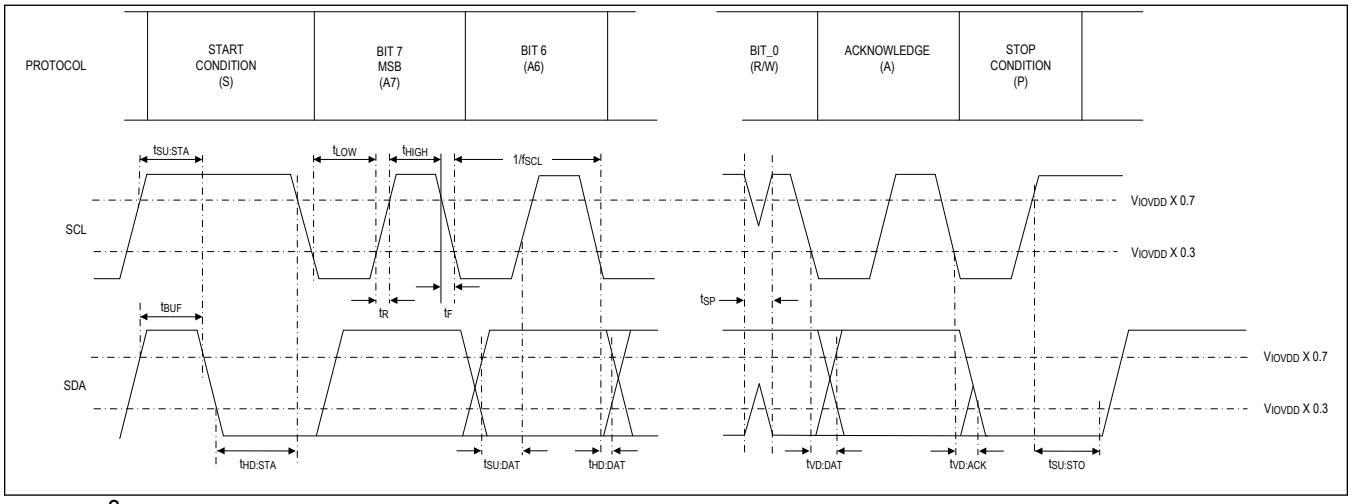



*Figure 5. I²C Timing Parameters*

## SPI Master Mode Timing Parameters

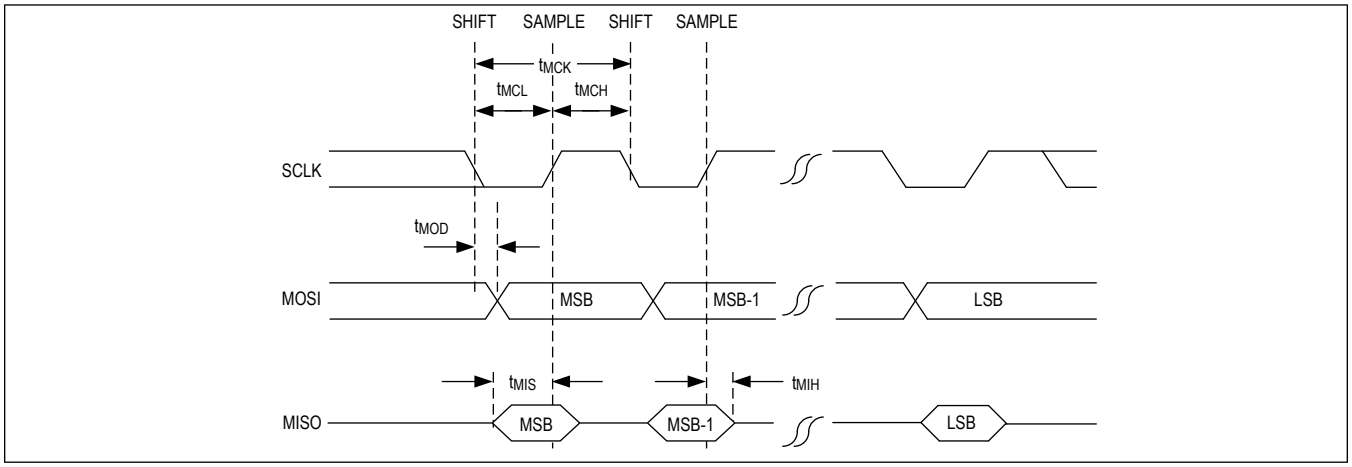



*Figure 6. SPI Master Mode Timing Parameters*

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### SPI Slave Mode Timing Parameters

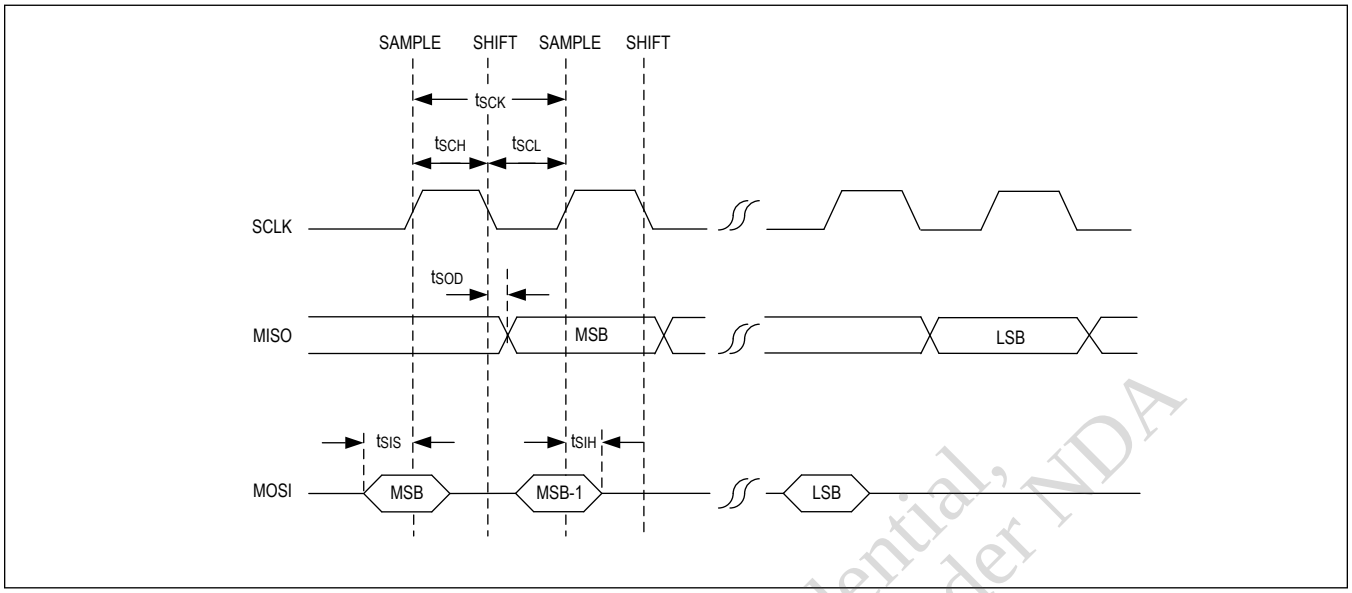



*Figure 7. SPI Slave Mode Timing Parameters*

### I²S Master Mode Timing Parameters

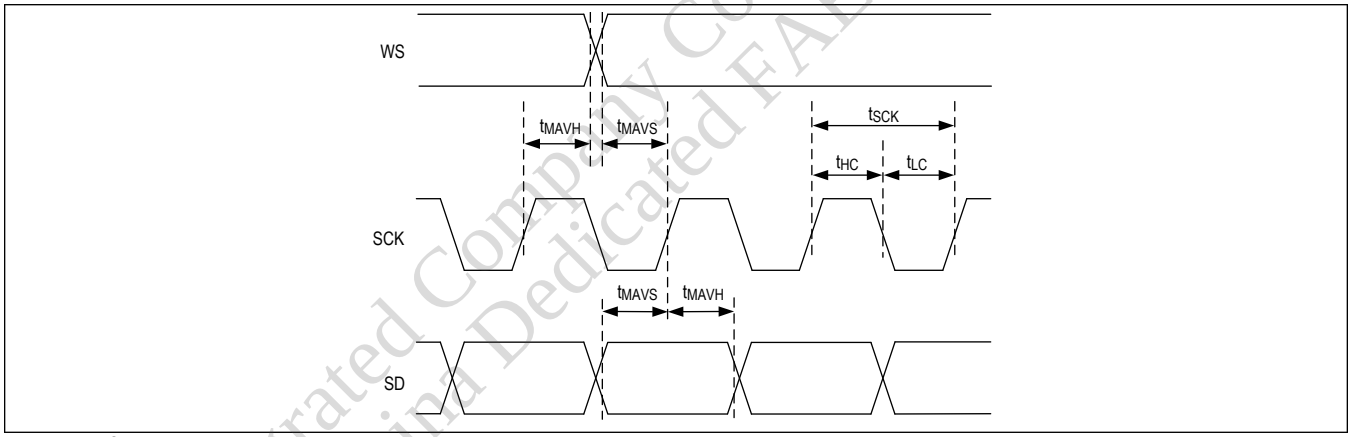



*Figure 8. I²S Master Mode Timing Parameters*

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### I²S Slave Mode Timing Parameters

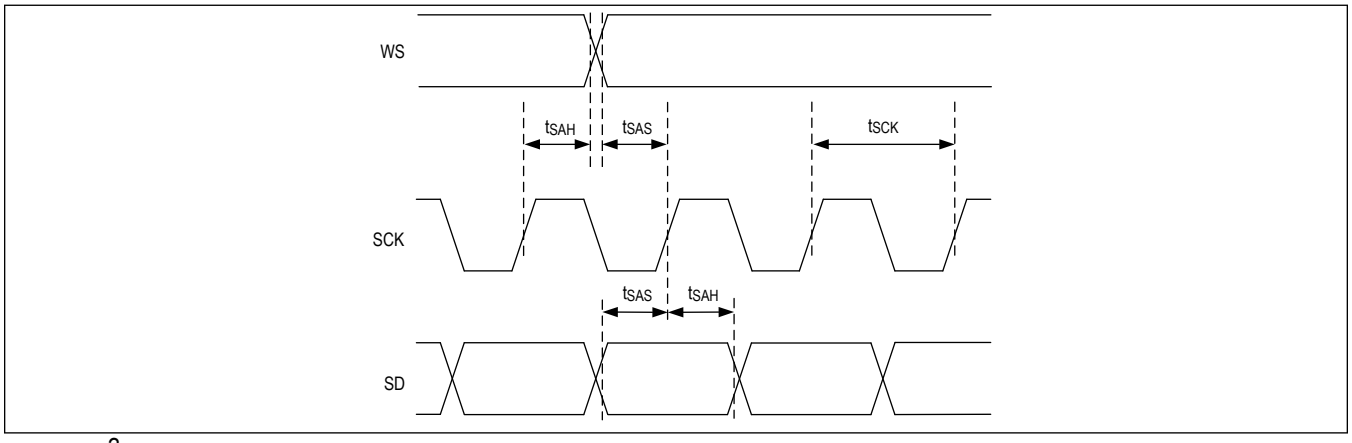



*Figure 9. $I^2S$ Slave Mode Timing Parameters*

## Detailed Description

### Introduction

Maxim's GMSL2 serializers and deserializers provide sophisticated link management of high-speed, low bit-error-rate, serial data transmissions. They support a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL2 provides up to 6Gbps forward and 187.5Mbps reverse packetized data transmission over each fixed-speed link. Devices with two GMSL2 links provide a total forward capacity of 12Gbps and 375Mbps reverse in specific configurations.

The following sections provide a brief overview of the devices' functions and features. Contact factory for additional information and details on the configuration of each function and feature.

### Product Overview

The MAX96737 serializers include 1 video pipe and convert single or dual 4-lane OLDI input ports to a single GMSL2 output. They support economical applications processors (APs) to drive a GMSL2 display from OLDI AP ports. The devices are specified to be located on the same PC board as the AP, using a common ground voltage. The MAX96737 pair with Maxim's GMSL2 OLDI and eDP deserializers, and support OLDI deserializer splitter mode (column/pixel interleave).

#### Ganged Dual-OLDI Input, Single GMSL2 Link

In this mode, the MAX96737 receive a single video stream from a dual-OLDI input and drive a single GMSL2 link. See Figure 10. A single master clock is preferred for timing the 2 OLDI inputs (1x8 mode). The default setting is 1x8 mode using Clock A. The 2 OLDI inputs can also be timed by individual port clocks from the AP (2x4 mode). In 2x4 mode, the clocks must be at the same frequency with skew that meets the data sheet timing specifications. Each OLDI clock period contains 2 pixels, 1 on each port. The MAX96737 aggregate the received pixels into a single video stream. The stream is output on GMSL2 PHY A. The transmitted pixel clock is equal to the OLDI clock x 2. The transmitted PCLK is limited to 104MHz, 160MHz, or by the maximum GMSL2 data rate of 6Gbps/s, depending on the device speed grade. PCLKs less than approximately 108MHz can be supported in GMSL2 3Gbps mode.

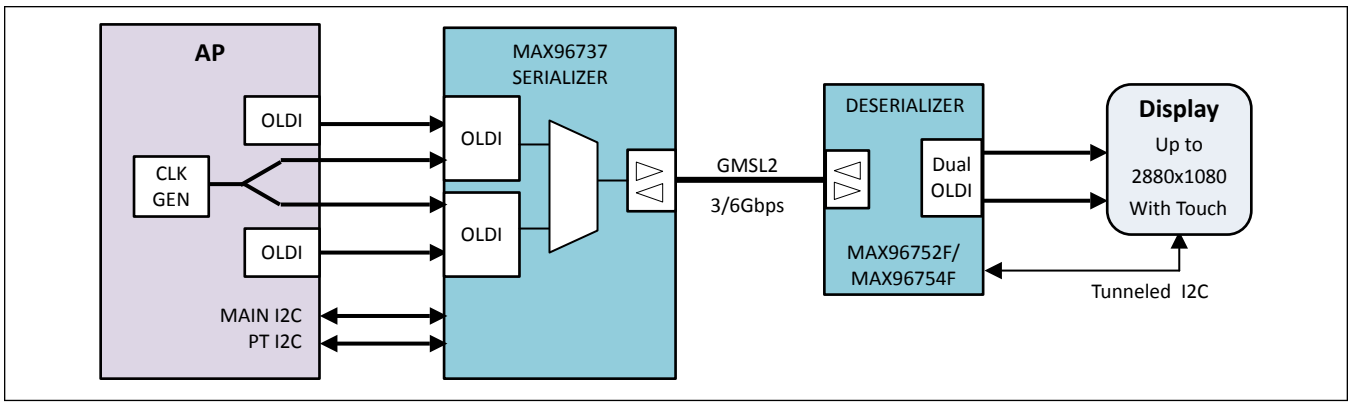



*Figure 10. Ganged OLDI Input With Single Link*

### Single OLDI Input, Single GMSL2 Link

This mode is similar to the Ganged Dual-OLDI Input, except that only a single OLDI port is used between the AP and serializer. Each OLDI clock period contains 1 pixel. Either OLDI port can be used. The single video stream is output on GMSL2 PHY A. The transmitted PCLK is limited to 104MHz or 160MHz, depending on the device speed grade. PCLKs less than approximately 108MHz can be supported in GMSL2 3Gbps mode.

### Configuration Guide

| BASE PART NUMBER | MAXIMUM PCLK/LINK | HDCP |
|---|---|---|
| MAX96737HD | 104MHz | No |
| MAX96737HQ | | Yes |
| MAX96737FD | 160MHz | No |
| MAX96737FQ | | Yes |
| MAX96737AD | 215MHz | No |
| MAX96737AQ | | Yes |

Note: GMSL2 6Gbps link bandwidth limits maximum "A" variant PCLK to approximately 215MHz.

### Other Functions

GMSL2 serializers and deserializers have a main $I^2C$/UART control channel interface that an ECU uses to access serializer and deserializer registers, as well as peripheral devices, from either end of the link. Each device also has two pass-through $I^2C$/UART channels available for local or remote peripheral control. The pass-through $I^2C$/UART channels do not have access to serializer and deserializer registers.

The MAX96737 additionally include an SPI master/slave interface, including two slave select pins, for peripheral control. The SPI interface enables a host SPI master on one side of the GMSL2 link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL2 devices (a GMSL2 device can be configured as a SPI master or slave).

A single forward-channel $I^2S$ audio input is available.

The MAX96737 provide up to 18 Multi-Function Pins (MFPs). MFPs (i.e. GPIOs) are typically used to tunnel low speed (< 100Kbps) signals over a GMSL2 link, although rates in excess of 1MHz can also be supported. A GPIO tunnel can be set up in the forward or reverse direction.

The devices include a video crossbar and watermark generation or detection. The crossbar can be used to reorder the color and sync signals. It can also be used for OLDI lane remapping and phase inversion if desired. The watermark generation and detection is used for verifying that the video image is not frozen.

GMSL2 devices incorporate numerous link margin optimization and monitoring functions to ensure high link margin.

Continuous (~1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor function for continuous link margin diagnosis with various threshold alarm levels is available for run-time alerts of link degradation. PRBS checking verifies correct link and video channel operation.

## Power Supplies

The MAX96737 provide flexible power-supply configurations.

The 1V core supply can be provided directly or supplied by an internal regulator. To minimize power dissipation, connect 1.0V ±5% to $V_{DD}$. If $V_{DD}$ < 1.1V and CAP_VDD < 1.05V, the regulator is automatically disabled at power-up and low-resistance switches connect $V_{DD}$ to the internal supply rails. For the internal regulator, connect 1.2V ±5% to $V_{DD}$. Following power-up, write REG_ENABLE = 1, then write REG_MNL = 1 as part of the device initialization to enable the internal LDO.

Connect CAP_VDD pins 22 and 6 with a low-impedance trace (<20mΩ). With a shortest-path trace under the package and 1oz. copper, the minimum trace width is 0.004" (0.15mm). For 0.5oz. copper, increase the trace width to 0.008"/0.3mm.

The $V_{DDIO}$ supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the part. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

$V_{DD18}$ is the primary analog supply. Connect 1.8V ±5%.

Properly bypassing all power supplies is essential to ensuring high frequency circuit stability. See Table 1 for power supply tolerances and noise requirements. Contact factory for guidance on sharing supplies and optimizing supply decoupling.

The MAX96737 provide extensive power supply diagnostics capabilities. Undervoltage detection is included for all power supplies. Moderate undervoltage conditions on the $V_{DD18}$ and $V_{DDIO}$ supply voltages can be indicated using either the ERRB pin or by reading the register field associated with the power supply undervoltage flag. An undervoltage condition on the $V_{DD}$ supply, which could corrupt the register configuration, is detected by the power manager and results in a reset. Similarly, a severe undervoltage condition on $V_{DD18}$ or $V_{DDIO}$ also results in a reset. When a reset occurs, device configuration reverts to the power-up default state when the supplies have recovered, and the host device must initiate the power-on initialization procedure to return the device to full operation.

Overvoltage detection is also provided, although only for the internal $V_{DD}$ supply voltage (CAP_VDD). As in the case of undervoltage events, an overvoltage situation can be reported by the ERRB pin in addition to a dedicated internal interrupt flag. No further action is taken by the power manager during an overvoltage situation, and the device will continue to operate normally, although it may sustain damage depending on the duration and magnitude of the overvoltage event.

When relying on the ERRB pin to convey the occurrence of an undervoltage event, connect an external 1MΩ resistor between the ERRB pin and ground because ERRB is not a power-up default MFP function. As a result, following a reset that is triggered by an undervoltage event, the ERRB MFP pin reverts to high impedance as opposed to ERRB. During an error state, the host device expects ERRB to drive logic low, and the presence of the aforementioned resistor enables the appropriate logic level to be maintained following the reset, alerting the host device that attention is required.

There is no specific power supply ramp sequence required.

## Thermal Management

Power consumption of GMSL2 devices varies based on their use case. Take care to provide sufficient heat dissipation with proper board and cooling design techniques. The package's exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below +125°C to meet electrical specifications and avoid impacting device reliability.

Refer to Tutorial 4083 (*www.maximintegrated.com/thermal-tutorial*) for further guidance.

## GMSL2 Protocol

GMSL2 is a fixed-rate transmission medium that is designed to carry multiple types of communication channels concurrently. The link bit rate is based on either a constant-frequency link clock generated from the 25MHz crystal oscillator or on an external reference frequency. The link clock is independent of the video pixel clock.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic. An inactive channel consumes no link bandwidth, which allows other active channels to share the full link bandwidth. Maximum packet size is limited, preventing a single channel from consuming link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement and idle packets are used to fill in the unused link bandwidth.

The same data protocol is used on forward and reverse channels.

### GMSL2 Bandwidth Sharing

GMSL2 forward bandwidth is shared between video, the $I^2C$/UART control channel, pass-through $I^2C$/UARTs, GPIOs, and $I^2S$/TDM audio and SPI (if supported), as well as various protocol specific data exchanges (i.e., info frames, sync, and acknowledgements). The reverse channel bandwidth is also shared with all the above, with the exception of video packets.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

A packet-based transmission format and dynamic bandwidth allocation allow link bandwidth to be shared flexibly among the various communication channels that request the link for packet transmissions. With dynamic bandwidth allocation, an inactive channel consumes no link bandwidth, leaving the full link bandwidth available to be shared by all active communication channels. The packet-based protocol limits the maximum packet size in order to prevent a single channel from monopolizing the link bandwidth at the expense of other channels.

The video and control-channel packets can be assigned a priority level of low, normal, high, or urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with maximum latency requirements can be assigned an increased priority.

### GMSL2 Bandwidth Calculations

GMSL2 forward links have a fixed data rate of 3Gbps or 6Gbps. The reverse link rate is also fixed at 187.5Mbps. The GMSL2 protocol overhead is roughly 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

Worst-case applications must not exceed the available throughput of the forward and reverse links. Maxim's evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that estimates initial bandwidth requirements. Maxim also offers other tools useful for calculating link bandwidth utilization. For high-bandwidth use cases, consult the factory to ensure error-free performance.

Table 7 provides rough estimates of the GMSL2 bandwidth utilization for each of the communication channels.

## Table 7. Forward and Reverse Link Bandwidth Utilization

| DATA | APPROXIMATE BANDWIDTH UTILIZATION |
|---|---|
| Display Video | H x V x fps x bpp x (1 + % blanking/100) x 1.14 (forward direction only) |
| $I^2C$ | 18 to 60 x I2C clock rate, depending on available link bandwidth |
| UART | 6 x UART bit rate, 5.5 x when parity bit enabled |
| SPI | 2.5 x SPI rate |
| $I^2S$/TDM | BW = ws_freq x roundup((bps x channelcnt + 27)/18) x 20 |
| GPIO | 60 x GPIO transition rate without delay compensation<br>80 x GPIO transition rate with delay compensation enabled |

Definitions:

H = Horizontal resolution

V = Vertical resolution

fps = Frames per second

bpp = Bits per pixel

ws_freq = Word select frequency

bps = Bits per sample, per audio channel

channelcnt = Number of audio channels

### Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. All GMSL2 devices support the following interfaces:

- Main $I^2C$/UART (internal access)
- Pass-through $I^2C$/UART
- SPI
- GPIO

All of the above interfaces can pass data through the GMSL2 link, but the GMSL2 device registers can be accessed and configured only through the main $I^2C$/UART interface.

The side channel, with its various interfaces, is accessed through multifunction GPIO pins (MFPs on some devices). Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit in the number of pins available on a given device, not all interfaces can be simultaneously supported.

See Table 12 and the Pin Description section for default and alternate multifunction pin functions, as well as available combinations of interfaces.

### Main and Pass-Through $I^2C$/UART

The MAX96737 support 3 SOC $I^2C$/UART channels, the main channel and 2 pass-through channels. Any of the 3 channels may be independently connected to the GMSL links to provide flexibility in interfacing to the deserializers and related peripherals.

The main control channel $I^2C$/UART is connected to the SDA_RX and SCL_TX pins of the MAX96737. It is the only port through which to program or read back the internal serializer registers. The main $I^2C$ (SDA, SCL) or UART (Tx, Rx) interface is selected by the CFG0 pin state at power-up. Unlike GMSL1 devices, there is no $I^2C$-to-UART conversion capability.

The main $I^2C$/UART channel is connected to the main $I^2C$/UART channels of the attached deserializers. This provides master access to deserializer registers and peripheral device registers from either end of the link.

The MAX96737 offer flexibility in control channel connections to the deserializers. Programming is controlled by register writes.

The deserializer registers are always accessed via the same $I^2C$/UART channel used to access the serializer registers. Additionally, either or both of the pass-through channels can be used to communicate with peripherals connected to the deserializers. This allows far-side peripherals to be interfaced using a different channel than the one connected to the deserializer registers.

This flexibility enables the serializer-side SOC to independently handle interrupts from remote peripherals.

All devices sharing a given channel must use the same channel mode ($I^2C$ or UART).

The master µC can reside on either end of the link (usually the serializer side for display applications. The MAX96737 support dual master µC controllers, provided that software arbitration (such as token passing) is used to prevent packet collisions. The control channel allows only one master µC to communicate at a time.

Disabling remote access via CFG0 at power up disables the deserializer from accessing the serializer control channel, and vice-versa. If there are microcontrollers on both ends of the link, this prevents control channel collisions and enables the microcontrollers on each side of the link to locally program their devices. No token passing or special software to

handle collisions are required.

I²C/UART outputs are open drain and require appropriately-sized external pullup resistors to VDDIO for proper operation.

For detailed main channel programming information, see the Control-Channel Programming section under Applications Information.

*** add description for configuration via CFG pins once this is set (Due to complexity, this will most likely be done via register control only)

*** add figure

### SPI

GMSL2 enables a host SPI master on one side of the GMSL2 link to control a peripheral SPI slave on the opposite side. Communication can be in either direction across the GMSL2 link.

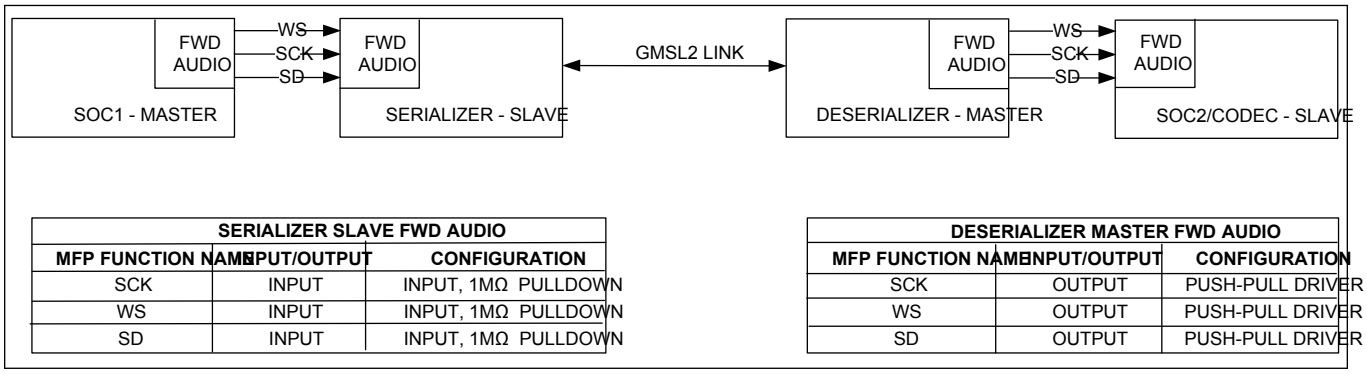
The SPI clock range is 600kHz to 50MHz. Take care to meet setup and hold time requirements when using at speeds higher than 20MHz.

## Table 8. SPI Latching Edge and Speed

| FREQUENCY (MHz) | $V_{DDIO}$ (V) | LATCHING EDGE | SPI_SPEED[1:0] |
|---|---|---|---|
| < 12.5 | 1.7–2.24 | Opposite | 01 |
| | 2.25–3.6 | | 10 |
| 12.5–25 | 1.7–2.24 | Opposite | 00 |
| | 2.25–3.6 | | 01 |
| 25–50 | 1.7–2.24 | Same | 00 |
| | 2.25–3.6 | | 01 |

### I²S/TDM Audio

The {max_num} support I²S stereo and up to 8 channels of audio in TDM mode. Sample rates of 8kHz to 192kHz and sample depths of 8- to 32-bits are supported. The maximum SCK frequency is 49.152MHz. Only forward-direction (serializer to deserializer) audio is supported, so the {max_num} is always the slave device.




| SERIALIZER SLAVE FWD AUDIO | | |
|---|---|---|
| MFP FUNCTION NAME | INPUT/OUTPUT | CONFIGURATION |
| SCK | INPUT | INPUT, 1MΩ PULLDOWN |
| WS | INPUT | INPUT, 1MΩ PULLDOWN |
| SD | INPUT | INPUT, 1MΩ PULLDOWN |

| DESERIALIZER MASTER FWD AUDIO | | |
|---|---|---|
| MFP FUNCTION NAME | INPUT/OUTPUT | CONFIGURATION |
| SCK | OUTPUT | PUSH-PULL DRIVER |
| WS | OUTPUT | PUSH-PULL DRIVER |
| SD | OUTPUT | PUSH-PULL DRIVER |

## Table 9. I2S_SPEED [1:0] Setting

| FREQUENCY (MHz) | $V_{DDIO}$ (V) | I2S_SPEED[1:0] |
|---|---|---|
| < 25 | 1.7–2.24 | 01 |
| | 2.25–3.6 | 10 |
| 25–50 | 1.7–2.24 | 00 |
| | 2.25–3.6 | 01 |

### Control Channel Latencies

## Table 10. Typical Control Channel Latencies

| FUNCTION | FORWARD (µs) | REVERSE (µs) | NOTES |
|---|---|---|---|
| $I^2C$ | < 10 | < 10 | |
| UART | < 10 | < 10 | |
| Audio | < 100 | NA | For typical use cases |
| SPI | < 10 | < 10 | Round trip |

### General-Purpose Inputs and Outputs (GPIO)

GPIOs are typically used to tunnel low speed (< 100kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based; a GPIO packet is created and transmitted on the GMSL2 link when a rising or falling edge transition is detected at a GPI pin. The transition is regenerated at a GPO on the other end of the link.

The multifunction pins GPIO can be programmed as GPI (input), GPO (push-pull output or open-drain output), or GPIO (bidirectional input/output). Each GPIO can also be programmed for 1MΩ or 40kΩ pullup or pulldown (or none). Although an internal pullup is provided, high-speed open-drain outputs require an appropriate value external pullup resistor to $V_{DDIO}$. Inputs cannot be left unconnected. Always ensure that every pin configured as an input has a pullup or pulldown programmed or is driven by another IC.

A GPI on one side of the serial link can be mapped to a single GPO or multiple GPOs on the other side of the link. Each GPI is assigned a pin ID with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0–GPIO0, GPIO1–GPIO1, GPIO2–GPIO2, etc. However, the GPIO mapping can be arbitrarily changed through register settings.

GPI transitions can be transmitted in two modes: delay-compensated and non-delay-compensated. When delay compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases, but jitter and skew decrease.

The state of each GPIO can be read or written by register, either locally or remotely, over the GMSL2 link by a µC using the control channel $I^2C$/UART interface.

In non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible based on priority and available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Non-delay-compensated mode should be used with signals tolerant to delay variation (i.e., µC interrupts).

MAX96737 register settings allow priorities to be assigned to GPI pins. If no priority is set, GPI transitions are transmitted in the order they occur. However, when priority is set transitions on GPI with higher priority are transmitted earlier.

Typical GMSL2-only GPIO delays for 6Gbps forward and 187Mbps reverse link rates are shown in Table 11.

## Table 11. Typical GPIO Delays for Forward and Reverse Link Transmission

| | DELAY COMPENSATION | DELAY |
|---|---|---|
| GPIO forwarding from serializer to deserializer (6Gbps forward channel) | 0 | 720ns |
| | 1 | 3.5µs |
| GPIO forwarding from deserializer to serializer (187Mbps reverse channel) | 0 | 6µs |
| | 1 | 15µs |

### Multifunction Pin Assignments

The MAX96737 provides a wide range of peripheral I/O functions. These functions are mapped through the register control to an array of multifunction pins (MFP). Each MFP has several possible functions, but only one can be used at a time.

In most cases, MFP pins can be used as a generic I/O pins, although there are some limitations with a limited number of

pins supporting only CMOS GPO functionality or open-drain output functions. The various peripheral interfaces and other special functions are distributed between different pins, enabling the user to utilize a variety of interfaces and special functions simultaneously.

Some functions require only a single MFP, but many are implemented across a group of MFPs. For example, LOCK is a single MFP, but SPI takes several MFPs. A user selects MFP functions to suit their use case by programming the appropriate registers.

The Pin Description section shows default and alternate functions for each MFP. The Table 12 provides guidance on how functions can be assigned to different pins to allow the desired combination of features to be used. Whenever a feature other than the default is enabled, other features must be disabled by register writes.

Each MFP has independent speed control. Table 12 list the default Transition Time Setting (TTS) for each MFP. Table 13 lists the typical rise and fall times for each of the 4 TTS settings. In general, use the slowest TTS possible for each function.

### MFP Pin Function Map

## Table 12. MFP Pin Function Map

| PIN | POWER UP USE | I²C/UART | SPI | AUDIO | OTHER FUNCTIONS | GPIO | DEFAULT SETTING | DEFAULT TTS |
|---|---|---|---|---|---|---|---|---|
| MFP0 | | | SCLK | SD | RCLKOUT, HS | GPIO0 | GPI (1MΩ pulldown) | 2 |
| MFP1 | | | MOSI | WS | VS | GPIO1 | GPI (1MΩ pulldown) | 2 |
| MFP2 | | | MISO | SCK | PCLK | GPIO2 | GPI (1MΩ pulldown) | 2 |
| MFP3 | | SDA_RX | | | | GPIO3 | SDA_RX (ODO, 40KΩ pullup or CMOS input) | I2C |
| MFP4 | | SDA2_RX2 | BNE_SS1 | | | GPIO4 | GPI (1MΩ pulldown) | 3 |
| MFP5 | | SCL2_TX2 | RO_SS2 | | | GPIO5 | GPI (1MΩ pulldown) | 3 |
| MFP6 | CFG0 | | | | | GPO6 | Disabled (Hi-Z) | 3 |
| MFP7 | CFG1 | | | | | GPO7 | Disabled (Hi-Z) | 3 |
| MFP8 | | SCL_TX | | | | GPIO8 | SCL_TX (CMOS input or ODO, 40KΩ pullup) | I2C |
| MFP9 | | | | | ERRB | GPIO9 | ERRB (ODO, 40KΩ pullup) | 3 |
| MFP10 | CFG2 | | | | DE | GPO10 | Disabled (Hi-Z) | 3 |
| MFP11 | | | | | LMN2 | GPIO11 | GPI (1MΩ pulldown) | 3 |
| MFP12 | | | | | LMN3 | GPIO12 | GPI (1MΩ pulldown) | 3 |
| MFP13 | | SDA1_RX1 | BNE_SS1 | | | GPIO13 | GPI (1MΩ pulldown) | 2 |
| MFP14 | | SCL1_TX1 | RO_SS2 | | | GPIO14 | GPI (1MΩ pulldown) | 2 |
| MFP15 | | SDA2_RX2 | | SCK | | GPIO15 | GPI (1MΩ pulldown) | 2 |
| MFP16 | | SCL2_TX2 | | WS | | GPIO16 | GPI (1MΩ pulldown) | 2 |
| MFP17 | | | BNE_SS1 | SD | LOCK, MS | GPIO17 | LOCK (ODO, 40KΩ pullup) | 2 |
| MFP18 | | | RO_SS2 | | MS, LOCK, RCLKOUT | GPIO18 | GPI in I²C Mode, MS in UART Mode (1MΩ pulldown in both modes) | 2 |

## Table 13. Control- and Side-Channel Typical Rise and Fall Times

| TRANSITION TIME SETTING (TTS) | RISE TIME (ns) (20% to 80%) | | FALL TIME (ns) (80% to 20%) | |
|---|---|---|---|---|
| | $V_{DDIO}$ = 1.8V | $V_{DDIO}$ = 3.3V | $V_{DDIO}$ = 1.8V | $V_{DDIO}$ = 3.3V |
| 00 | 1.0 | 0.6 | 0.8 | 0.5 |
| 01 | 2.1 | 1.1 | 2.0 | 1.1 |
| 10 | 4.0 | 2.3 | 4.3 | 2.3 |
| 11 | 8.8 | 5.0 | 10.1 | 5.1 |
| I2C | N/A | N/A | 40 | 30 |

### MFP I/O Properties

Table 14 defines the pin I/O properties for each of the MFP functions.

## Table 14. MFP Pin I/O Properties

| MFP FUNCTION | PIN I/O PROPERTIES |
|---|---|
| GPIOs | Programmable<br>Push-pull or push or pull or no_drive<br>Pullup, pulldown with selectable 1MΩ or 40kΩ<br>Input or output or input/output |
| SCLK, RO, MOSI, MISO, WS, SD, SCK, MS | CMOS in with 1MΩ pulldown, no drive |
| SCLK, BNE, SS1, SS2, MISO, MOSI, GPO, RCLKOUT | CMOS out push-pull driver, no pulldown or pullup |
| LOCK, ERRB | Open drain 40K pullup with strong drive to 0 |
| SDA_RX, SCL_TX, SDA1_RX1, SCL1_TX1, SDA2_RX2, SCL2_TX2, | Open drain I/O with 40K pullup. Strong output or input drive to 0. |

### MFP Pin Equivalent Circuits

In general, MFP pins can all be classified as either programmable high speed GPIO or programmable $I^2C$/ODO (Open Drain Output) GPIOs. Equivalent circuit representations are below.

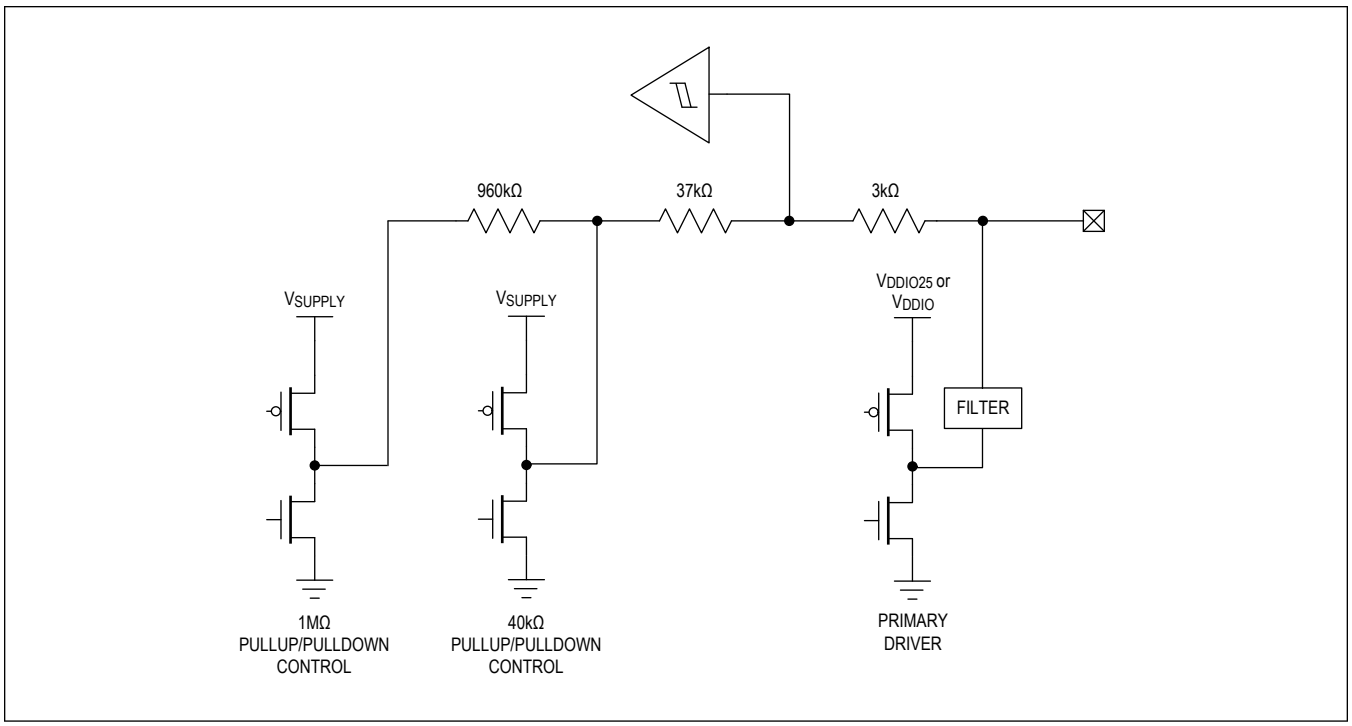



*Figure 11. Standard High Speed GPIO*

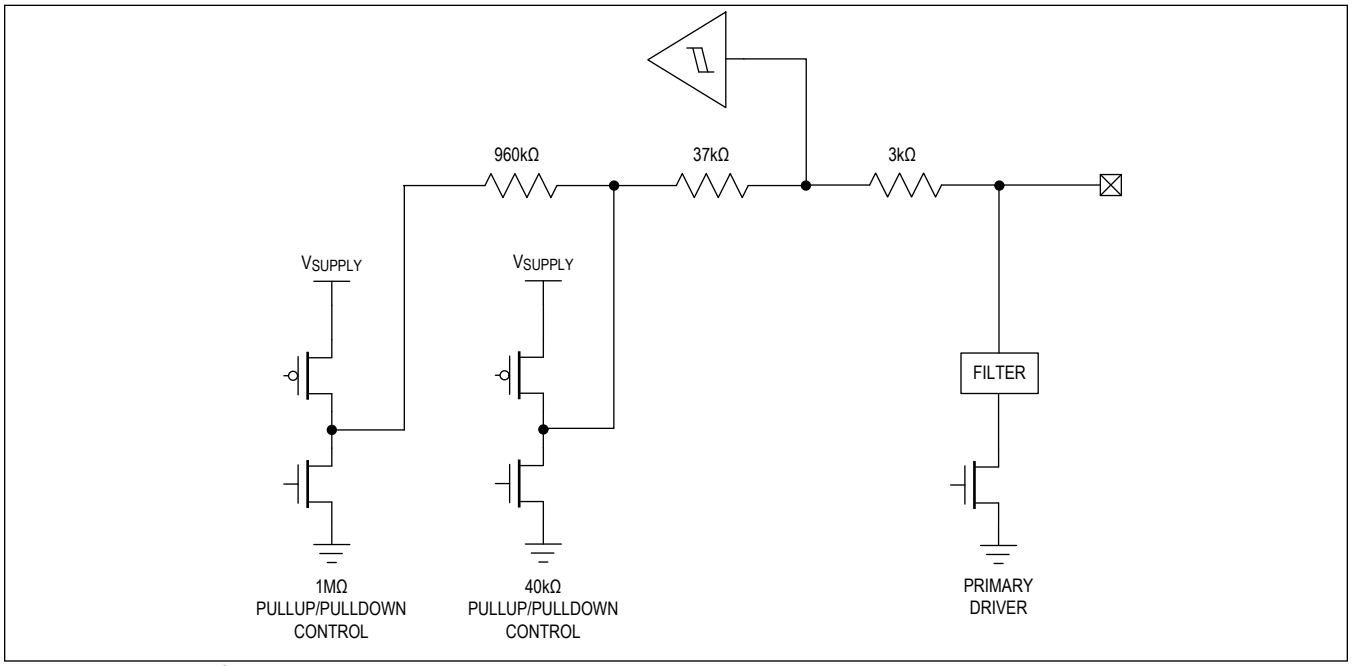



*Figure 12. Standard $I^2C$ GPIO*

## GMSL2 Physical Layer

Maxim's GMSL2 family of serial links have transmitter and receiver capability enabled simultaneously, allowing full-duplex operation on a single wire. A single cable between the serializer and deserializer delivers data transmitted from each end

of the link. Forward transmission is data sent from the serializer to the deserializer. Reverse transmission is data sent from the deserializer to the serializer.

Forward rate options are fixed at 3Gbps or 6Gbps, depending on CFG1 pin configuration at power-up. Reverse rate options are fixed at 187.5Mbps. Both forward and reverse rates are doubled in dual-link configuration, in which a serializer and paired deserializer are connected using two links. Dual-link mode is not available in all GMSL2 device configurations.

### Cabling Options

GMSL2 supports operation with either 50Ω coaxial or 100Ω shielded twisted pair (STP) cabling. Coax or STP configuration is determined by the level of CFG2 at power-up. See the Configuration Tables section. In coax mode, use only the noninverted SIO pin. In STP configurations, both the non-inverted and inverted SIO pins are enabled by default. Any unused SIO pins should be AC terminated with 50Ω to ground.

Cables must have sufficient return and insertion loss characteristics for best full duplex link performance. The available link rates and GMSL dynamic link optimization enable support of a wide range of cabling options. Contact the factory for insertion and return loss guidelines.

Following the GMSL2 design guidelines allows cables in excess of 15m length for coax or 7.5m for STP commonly used in the automotive industry. Longer cable lengths can potentially be used with careful system design and appropriate cable and connector specification. Achieving the greatest cable lengths makes some assumptions, including two in-line connectors in addition to the endpoint connectors, 25mm of PCB trace at each end, proper layout techniques, and high cable quality. Contact the factory for additional details regarding the GMSL2 channel specification.

A 100nF AC-coupling capacitor is used for GMSL2 links.

### Clocking

### GMSL Reference Clock

The GMSL2 devices require a reference clock source to generate the 6GHz line rate clock and associated internal clocks. Both the serializer and deserializer can be clocked with an external 25MHz crystal or an external clock source with a frequency accuracy of ±200ppm.

### Reference Clock Output

The MAX96737 can share a crystal by utilizing a reference clock output. RCLKOUT can be used as a reference clock by another serializer in close proximity. This arrangement eliminates the need for an additional external crystal or oscillator for the second serializer. The RCLKOUT has programmable division ratios of 1, 2, and 4.

### Spread-Spectrum Clocking

Maxim's GMSL2 links provide exceptional EMI performance. Optional spread-spectrum clocking (SSC) is available to mitigate electromagnetic interference emitted from devices and interconnections and to provide additional margin.

SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to 2500ppm peak-to-peak from the center frequency.

### AEQ (Adaptive Equalization)

GMSL2 devices automatically adapt receiver characteristics to compensate for the insertion and return loss characteristics of the channel, which consists of the cables, connectors, and PCBs. This optimizes performance on any channel that meets the GMSL2 channel specification. The equalizer architecture makes GMSL2 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock and then is invoked at a ~1Hz rate to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye opening by using the built in eye-opening monitor.

## Power-Up and Link Startup

GMSL2 ICs are in power-down mode when PWDNB pin is low or when any of the power supplies are disabled. When in power-down mode, device configuration is reset to the default power-up state.

The serializer and deserializer may power up in any order. After PWDNB is released and all power supplies have settled, each device starts its power-up sequence and performs the following operations:

1. CFG pin states are latched and internal registers are set accordingly. See Table 4, Table 5 and Table 6 for details.
2. The main control channel ($I^2C$ or UART) is functional on local side. The device registers are writable and readable.
3. The link is established based on the following settings:
    1. Single link auto selection mode (AUTO_LINK = 1 and LINK_CFG = 1 or 2): Automatically select which PHY to use to establish a GMSL2 link by periodically trying to handshake using PHY A and PHY B.
    2. Single link manual selection mode (AUTO_LINK = 0 and LINK_CFG = 1 or 2): If LINK_CFG = 1, establish a link using PHY A. If LINK_CFG = 2, establish a link using PHY B.
    3. Dual link mode (LINK_CFG = 0): Establish a link using both PHYs.
    4. Splitter (serializer)/aggregator (deserializer) mode (LINK_CFG = 3): Establish a link using both PHYs (for specific applications only).
4. Each enabled PHY performs link calibration, equalizer adaptation, and data channel locking. Both devices set their LOCK pins high.
5. The control channel is available from or to the remote side. If using the internal $V_{DD}$ regulator ($V_{DD}$ = 1.2V), enable the regulator function as described in the Power Supplies section.

The link-up process, from the time that the last part's PWDNB input is brought high, takes approximately 20ms nominally and 100ms maximum for any channels that meet the GMSL2 channel specification.

After the link is established, all devices can be configured. This can be done locally or remotely over the control channel by a microcontroller on either side of the link.

### CFG[2:0] Pins

The CFG[2:0] pins are used to set the initial register values and functional modes of the device at power-up. At power-up the voltage levels at the CFG[2:0] input pins are latched. The decoded levels set initial register values and functional modes that may not be easily programmed through $I^2C$ or UART after the IC powers up. The configuration tables provide the exact details on how to choose resistor values for the CFG[2:0] pins.

The CFG[2:0] pins are shared with MFP pins. Before the pin levels are latched, the chip does not drive the pin. The user should connect a proper valued precision resistor according to the required setting for each CFG pin. Use the MFP pins, which also function as CFG pins, only as outputs after power-up.

See Table 4, Table 5 and Table 6 for details.

### Link Lock

Link lock happens automatically on power-up and is an indication that the cable is plugged in and the system is up and running. Lock is obtained with no interaction or commands from the µC to the GMSL parts. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

Link lock indicates that the PLLs for the GMSL2 link are locked to each other and the data receive paths are locked (forward channel in the serializer, reverse channel in the deserializer). Video and control channel functions ($I^2C$/UART, SPI, GPIO, audio) can be used immediately after link lock is asserted.

In dual-link and splitter configurations, only one link locks automatically. The user must then program the serializer to the desired operating mode.

The GMSL2 link uses the crystal or external reference input as the reference clock for the GMSL2 link, so a valid video input (pixel clock) is not needed for the GMSL2 link to lock.

### Device Reset

There are three general reset options available through register writes:

1. RESET_ALL resets all blocks including all registers, digital blocks, and analog blocks. This process is similar to driving the PWDNB pin low and then high.
2. Setting RESET_LINK resets all GMSL PHY-related digital logic and all data pipeline. After this bit is set, all control registers are still accessible through local control channel. The link remains in RESET until RESET_LINK is cleared.

3. RESET_ONESHOT resets all GMSL PHY-related digital logic and all data pipeline and then automatically clears itself. This is similar to setting and clearing RESET_LINK.

Program registers that affect GMSL-2 link operation (i.e., TX_RATE, RX_RATE, CXTP_A/B, AUTO_LINK, LINK_CFG, GMSL2) first, followed by RESET_LINK or RESET_ONESHOT.

### Power Standby and Sleep Mode

A power manager block is present in all GMSL2 products. Its primary function is to monitor supply voltages and control power-down (standby) and sleep modes.

There are two ways to go into low power mode while all power supplies are active: assertion of the PWDNB pin or invocation of the sleep state. Both states offer very low-power supply currents.

Asserting the PWDNB pin (active-low) places the device in standby power mode and resets the digital registers and configurations to their default power-up condition. Any supply dropping below its internal threshold settings also places the device in power-down mode. In the event the power supply recovers, the device returns to the default power-up state with default register settings. The user must then reinitiate device startup and reprogram all registers.

The sleep state offers the preservation of all critical register settings and configurations. The device can be put into the sleep state through an $I^2C$/UART command. The resume state restores the device back to the presleep condition without the need for additional register writes. Resume is invoked by an $I^2C$ command or a low-frequency clock beacon transmitted from the master device over the GMSL2 link.

## Link Integrity Functions

### Line Fault

GMSL2 serializers include a novel line fault detection circuit. It detects and reports open-circuit, short-to-battery, short-to-ground, and line-to-line short. The line fault monitor requires external resistors $R_{EXT}$ and $R_{PD}$ connected to the LMN_ pins as shown in Figure 13 and Figure 14.

The line fault monitor is disabled by default, and configuration options are available through registers. Its status can be read by register. If unmasked, a line fault condition asserts ERRB. Line fault detection cannot be used in conjunction with power over coax (POC).

The line fault monitor pins offer flexible connection and programming. Either line fault pair (i.e. LMN0/1 or LMN2/3) can be used. In addition, the pins within each pair can be assigned to either polarity of the link.

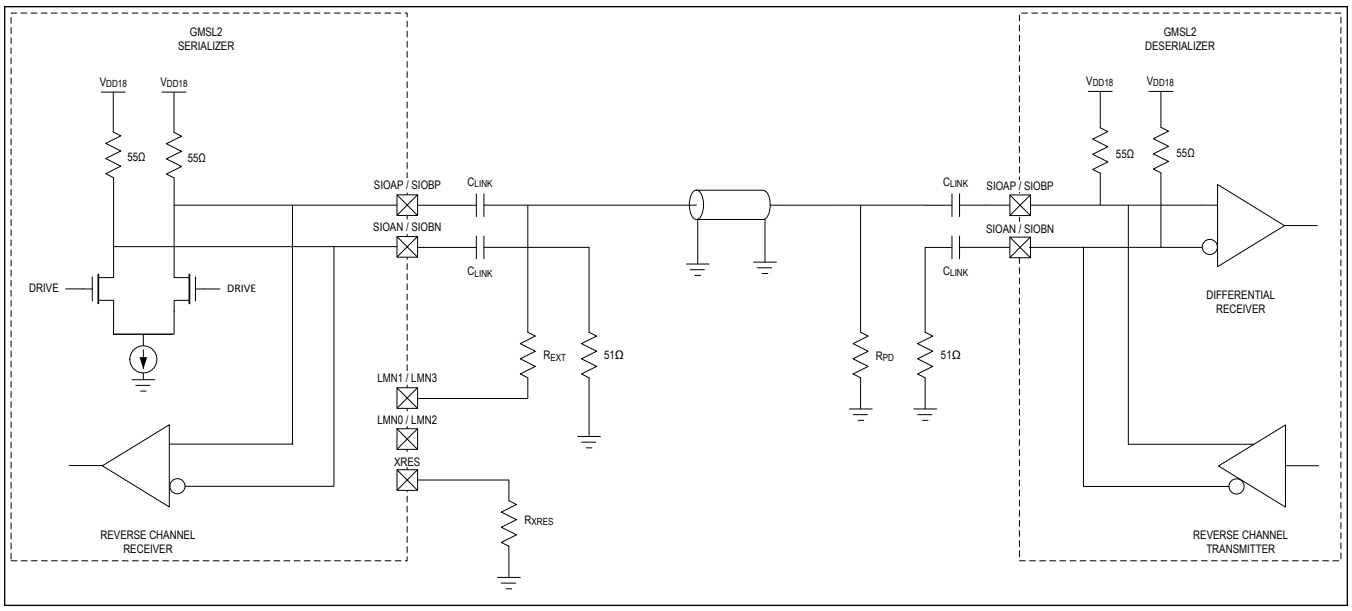



*Figure 13. Typical GMSL2 Link Application Circuit for Coax Cable*

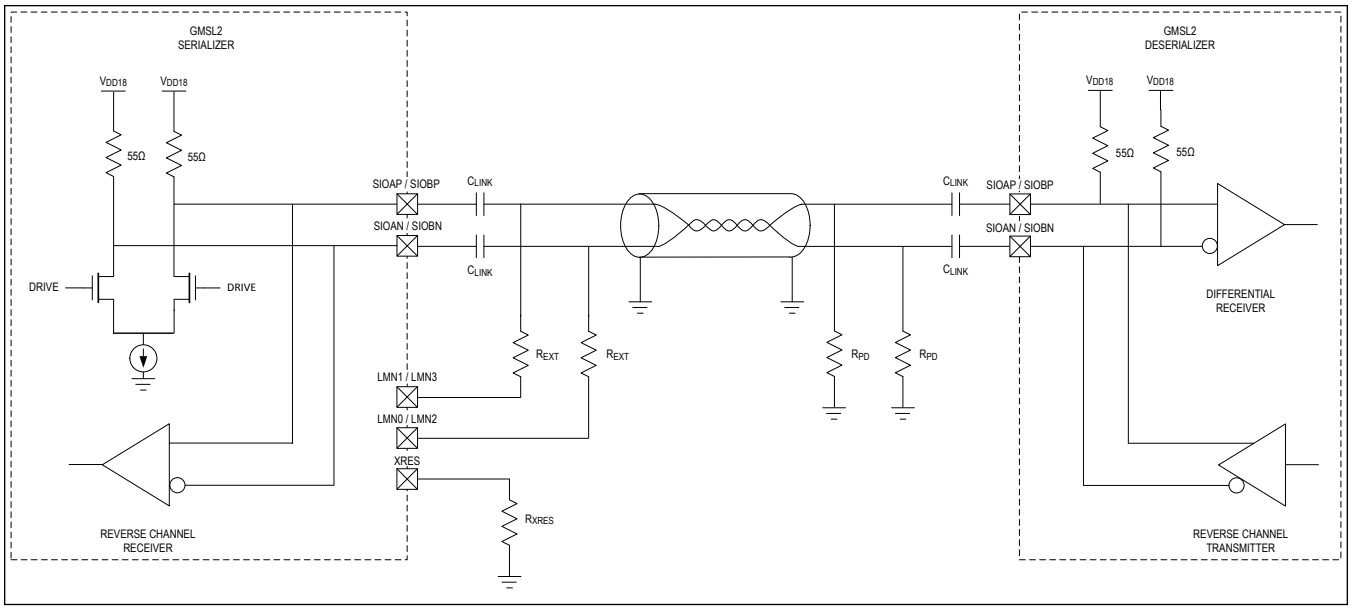



*Figure 14. Typical GMSL2 Link Application Circuit for Twisted Pair*

### Error and Fault Condition Monitoring

Both the serializer and deserializer have an open-drain, multipurpose error reporting and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a subblock of registers, so the reason for assertion of ERRB can be determined by reading the register status.

### Eye-Opening Monitor

The eye-opening monitor (EOM) enables GMSL2 parts to monitor the link margin on an active link and generate an

interrupt if it falls below an acceptable level. For example, if a cable is damaged the link can run error free, but have less link margin than desired. This allows the customer to proactively react to deteriorating cable performance before any link errors occur. GMSL2 devices can measure the horizontal or vertical eye opening of the equalizer's output. The measurement is activated automatically at a ~1Hz rate once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye opening is then reported, and the EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds.

#### Video Line CRC

A CRC32 polynomial is used to generate an optional 32-bit code at the end of each DE or HS pulse. This code is transferred to the receiver side using info frames. The CRC checker generates the same code on the receiver side and checks if the generated and received CRC codes are the same. If not, it asserts an error. The CRC check is done at every falling edge of DE on the receiver side even if the info frame is not received.

#### PRBS

#### Video PRBS

The video channel has a PRBS generator in the serializer and a PRBS checker in the deserializer for testing the video channel operation. The video PRBS generator can work with the PCLK recovered by the serializer from an HDMI, parallel, or MIPI input. Note that all link bandwidth is not used by the video channel alone in GMSL2 mode, so it is possible to have a bit error on the link that does not cause a video PRBS error.

#### Audio PRBS

The audio channel includes a PRBS generator on the transmitter side and a checker at the receiver side for testing the audio channel operation. The audio PRBS generator can operate using the incoming $I^2S$ SCK and WS signals or an internally generated reference clock. The detected audio channel bit errors are reported through a status register.

### Watermarking

The watermarking block allows users to detect a frozen frame failure in a frame-based processing system between the generator and detector. This feature is specifically targeted to detect frozen frames caused by SOCs in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector.

GMSL2 devices contain both a watermark generator and watermark detector. This allows both serializers and deserializers to insert a watermark or detect a watermark in a safety-relevant video stream. The watermark generator inserts a time-varying watermark that is highly redundant and robust to image processing and display stream compression. The watermark detector looks for this time-varying watermark, and if it fails to see all the generated watermarks, this indicates a frozen frame failure in a frame-based processing system between the generator and detector. Upon detection of this error condition, the watermark detector can generate an interrupt and/or blank the output video returning the display to a safe-state in less than 500ms.

### HDCP (High-Bandwidth Digital Content Protection)

#### Overview

High-bandwidth digital content protection (HDCP) is an encryption scheme to protect digital audio and digital video content in various protocols. The GMSL2 links support HDCP v1.4. For power savings, the HDCP circuits are powered down by default. Once the user enables HDCP, the function powers up and performs authentication, after which link integrity checks are periodically performed by hardware through a dedicated control channel over the GMSL2 link. HDCP interrupts can be generated and status registers provide status of authentication progress indicating success and a ready state to the upstream video source. Each HDCP device has a factory-programmed unique device ID called a key selection vector (KSV) and associated private keys. They are licensed from DCP LLC.

### Repeater Support

The MAX96737 variants supporting HDCP does not support HDCP repeater mode as there is no HDCP support at the DSI interface. It does support repeater mode for cascaded GMSL links.

### Auto HDCP Operation

GMSL2 has an auto HDCP (AHDCP) feature that fully automates the GMSL2 HDCP1.4 key exchange authentication without requiring external µC involvement. Authentication and link integrity checks are done by hardware through a dedicated control channel over the GMSL2 link.

GMSL2 AHDCP has an optional fast mode to perform a link integrity check on every frame. This reduces the video out of encryption synchronization duration down to as few as two frames.

## OLDI Input

### Port Configuration

The MAX96737 provides flexible interfacing to 1 or 2 OLDI ports. See the Detailed Description section.

### Jitter-filtering PLL

The clock PLLs include narrowband jitter filters that attenuate frequencies higher than 100kHz (typical).

### Spread-spectrum clocking

The MAX96737 accommodate spread-spectrum OLDI clocking to reduce radiated EMI. When using a spread clock, disable the jitter filter. Do not exceed +/-0.5% spread, and keep modulation less than 40kHz. Spread-spectrum programming of the GMSL2 link is independent of the OLDI input spread-spectrum.

### Clock and Data Integrity

The MAX96737 verifies that the clock frequency is within valid range and stable. It also checks that each of the data bits is toggling.

### Video Data Integrity

The MAX96737 provides 2 methods to verify video data integrity. Both require active involvement by the SOC.

The deserializer can perform a parity check of each pixel. The correct parity is transmitted by the SOC using the RES bit in 4-lane OLDI mode. If the deserializer parity calculation does not match the RES bit, an error is recorded in a register and can be programmed to assert ERRB.

The MAX96737 can also calculate a 32-bit frame CRC. The SOC and deserializer must use an identical CRC polynomial. The deserializer CRC result is read via the control channel by the SOC, which compares it to its result and handles the error processing. The MAX96737 CRC polynomial is programmable. The default is:

$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

## Applications Information

### Control Channel Programming

GMSL device registers can only be accessed and configured through the main I2C/UART interface. By default, the main I2C/UART channel is also sent to the remote-side device and any peripheral connections. In multi-master configurations, with microcontrollers connected to both the serializer and deserializer, disabling the remote control channel through register settings is recommended to prevent bus contention.

#### Device Address

Each device on the I2C/UART control channel must have a unique address. The GMSL2 device address is set to one of 2, 7-bit addresses according to the voltage level of the CFG0 pin at power-up. See the CFG[2:0] Pins section. Note that device address can be changed after power-up by writing to the DEV_ADDR register.

#### Host-to-Peripheral Main I2C and Pass-Through I2C Communication

When communicating between a host and peripheral, main and pass-through I2C operation is the same. An I2C tunnel across the GMSL2 link connects the host's I2C master to the remote I2C slave. This logically connects separated I2C buses, enabling I2C transactions across the serial link to occur (with some delay) as if performed on the same physical I2C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I2C master connects to a GMSL2 device I2C slave, and the peripheral I2C slave connects to a GMSL2 device I2C master.

For example, when the host I2C master transacts on one side of the link (local-side), data is forwarded to the other side (remote-side) by the I2C slave of the local-side GMSL2 device. Data is then received by the I2C master of the remote-side GMSL2 device, which in turn generates the same I2C transaction with the peripheral slave I2C. The remote-side GMSL2 device sends back any I2C data expected by the local-side.

The I2C interface uses clock stretching (holding SCL low) to account for timing differences between master and slave and to allow time for data to be forwarded and received across the serial link. The host I2C master and peripheral I2C slave must support clock stretching by the GMSL2 device.

SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

#### Main I2C Host-to-GMSL2 Device Communication

The host I2C master has access to GMSL2 serializer and deserializer registers. The host can program GMSL2 device registers to configure the pass-through I2C/UART interfaces as I2C or UART.

#### I2C Write Packet Format

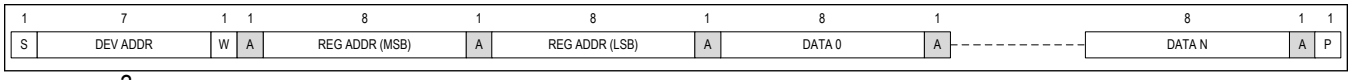



*Figure 15. I2C Write Packet Format*

#### I2C Read Packet Format

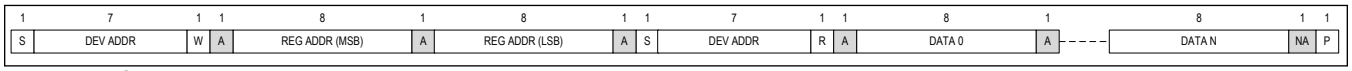



*Figure 16. I2C Read Packet Format*

### Main UART

When the main I2C/UART interface is configured as UART, there are two operating modes: base and bypass.

### UART Base Mode

Base mode is the communication means that allows a µC to access serializer/deserializer registers as well as registers on peripheral devices. Base mode is enabled by default at power-up. In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL2 UART packet protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings). The device addresses of the serializer and deserializer in this mode are programmable.

In base mode, serializer, deserializer and peripheral registers can be written and read using the half-duplex GMSL2 UART protocol.

Figure 17 shows the UART protocol for writing and reading in base mode.

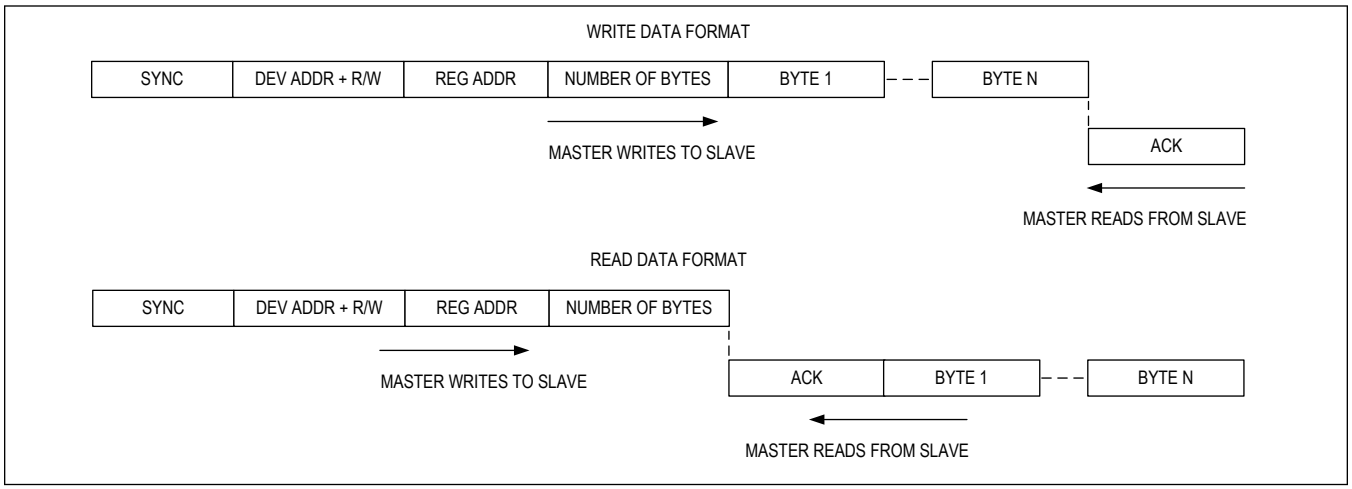



*Figure 17. GMSL2 UART Protocol for Base Mode*

### UART Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the µC, allowing the µC to communicate only with peripheral devices. The µC cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL link. Ignoring UART transactions prevents inadvertent misprogramming of serializer and deserializer registers. The device addresses of the serializer and deserializer in this mode are not programmable.

### Switching Between UART Base and Bypass Modes

There are two ways to switch between base mode and bypass mode: programming the register and using the Mode Select (MS) pin.

Two modes can be set by programming: temporary or permanent. In temporary mode, bypass mode is active only as long as there is UART activity. When there is no UART activity for a selected timeout, both devices exit bypass mode, and the register bit is automatically cleared. In permanent mode, the devices stay in bypass mode until the next power-down.

When set by the MS pin, a high pin level puts the device into bypass mode, and a low level puts the device in base mode. MS is set on the fly and is not latched on power-up.

### UART Frame Format

Regular UART frames with an even parity bit are used to carry 1 byte of data each. A frame consists of a low start bit

followed by eight data bits, a parity bit, and a high stop bit. The parity bit is high if the number of ones in the 8 bits of data is odd, otherwise, the parity bit is low. There must be at least one high stop bit. If the next frame is in the same packet, there can be at most four high bits from the end of the stop bit to the beginning of the next start bit. Note that in the case of a parity bit error, the packet, starting from the frame with the error, is discarded. The start of each frame is always a high-to-low transition (i.e., the stop bit is high and the start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer uses the synchronization frame (i.e. the first frame of a UART packet transmission) to calibrate the length of one UART bit in terms of the internal oscillator clock. In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions; the recipient of the data must perform error checking. The parity bit can optionally be disabled in bypass mode before entering bypass mode. Note that the bit rate in bypass mode must be the same bit rate last used in base mode.

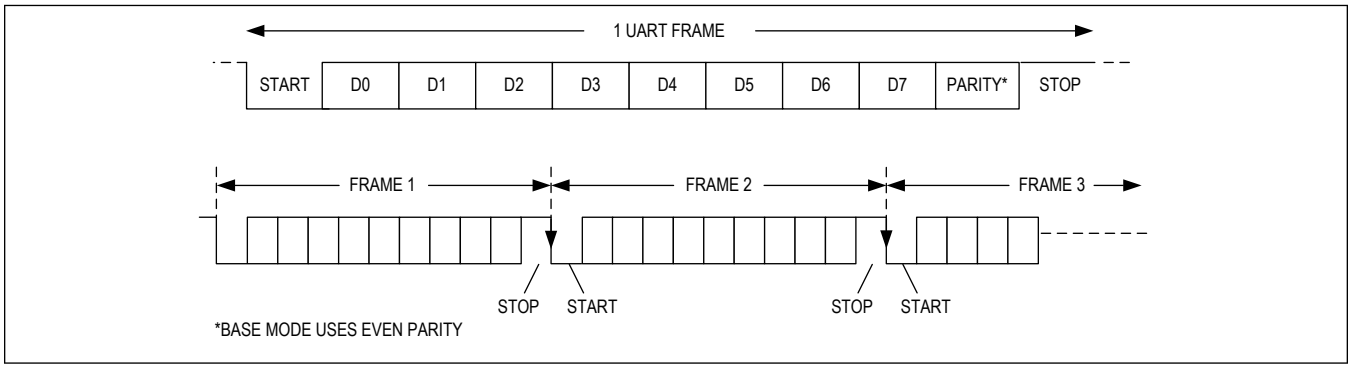



*Figure 18. UART Data Format for Base Mode*

### Synchronization Frame

The serializer/deserializer must calibrate internal bit length counters with the UART bit rate for proper recovery of UART frames. A sync frame (a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal 150MHz clock. Sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next sync frame.

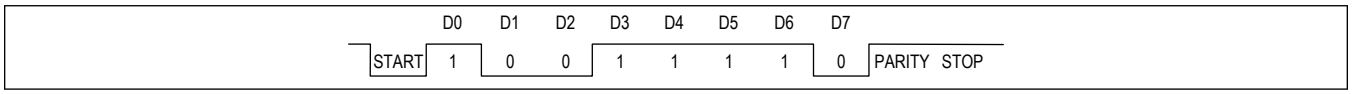



*Figure 19. UART Synchronization Frame*

### Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors were detected in the transmitted packet, and it was recognized as valid. This is sent after the last bit of a successfully recognized packet has been received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

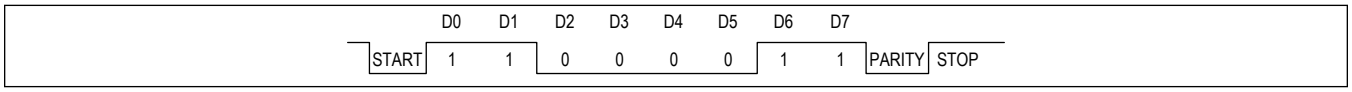



*Figure 20. UART Acknowledge Frame*

### Write Packet

Write packets consist of a five-byte packet header followed by one or more data bytes. A packet is recognized as a write packet when the LSB of the device address frame is 0. The addressed device responds with an acknowledge frame if no

errors were detected while receiving a valid write packet. Byte count indicates the number of data bytes to be written and this value cannot be 0.

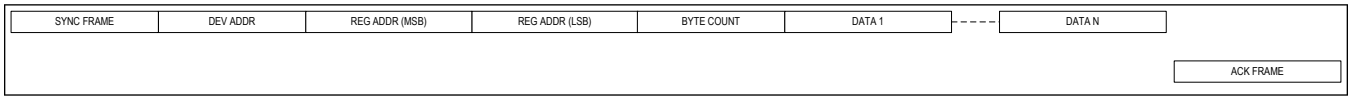



*Figure 21. UART Write Packet Format*

### Read Packet

Read packet consists of 5 bytes. The LSB of the device address frame is 1 for read packets. If no errors were detected while receiving a valid read packet, the addressed device responds with an acknowledge frame followed by 1 or more data bytes. Byte count indicates the number of data bytes to be read and this value cannot be 0.

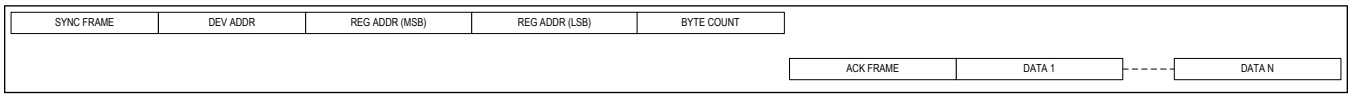



*Figure 22. UART Acknowledge Frame*

## Ordering Information

| PART NUMBER | MAX PCLK | HDCP | PIN-PACKAGE | TEMP RANGE |
|---|---|---|---|---|
| MAX96737HDGTN/V | 104MHZ | NO | 56-LEAD TQFN-EP | -40°C to +105°C |
| MAX96737HDGTN/VY* | 104MHZ | NO | 56-LEAD SW TQFN-EP | -40°C to +105°C |
| MAX96737HDGTN/V+T | 104MHZ | NO | 56-LEAD TQFN-EP | -40°C to +105°C |
| MAX96737HDGTN/VY+T* | 104MHZ | NO | 56-LEAD SW TQFN-EP | -40°C to +105°C |
| MAX96737HTGTN/V* | 104MHZ | YES** | 56-LEAD TQFN-EP | -40°C to +105°C |
| MAX96737HTGTN/VY* | 104MHZ | YES** | 56-LEAD SW TQFN-EP | -40°C to +105°C |
| MAX96737HTGTN/V+T* | 104MHZ | YES** | 56-LEAD TQFN-EP | -40°C to +105°C |
| MAX96737HTGTN/VY+T* | 104MHZ | YES** | 56-LEAD SW TQFN-EP | -40°C to +105°C |
| MAX96737ADGTN/V* | 215MHZ | NO | 56-LEAD TQFN-EP | -40°C to +105°C |
| MAX96737ADGTN/VY* | 215MHZ | NO | 56-LEAD SW TQFN-EP | -40°C to +105°C |
| MAX96737ADGTN/V+T* | 215MHZ | NO | 56-LEAD TQFN-EP | -40°C to +105°C |
| MAX96737ADGTN/VY+T* | 215MHZ | NO | 56-LEAD SW TQFN-EP | -40°C to +105°C |
| MAX96737ATGTN/V* | 215MHZ | YES** | 56-LEAD TQFN-EP | -40°C to +105°C |
| MAX96737ATGTN/VY* | 215MHZ | YES** | 56-LEAD SW TQFN-EP | -40°C to +105°C |
| MAX96737ATGTN/V+T* | 215MHZ | YES** | 56-LEAD TQFN-EP | -40°C to +105°C |
| MAX96737ATGTN/VY+T* | 215MHZ | YES** | 56-LEAD SW TQFN-EP | -40°C to +105°C |

*/V Denotes an automotive qualified part*

*+ Denotes a lead(Pb)-free/RoHS-compliant package*

*T Denotes tape and reel*

*Y Denotes Side-Wettable package*

*EP Denotes Exposed Pad*

***HDCP parts require registration with Digital Content Protection, LLC*

**Future product—contact factory for availability.*

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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