The documentation and process conversion measures necessary to comply with this document shall be completed by 30 June 2015.

INCH-POUND
MIL-PRF-19500/548J
30 March 2015
SUPERSEDING
MIL-PRF-19500/548H
1 May 2012

PERFORMANCE SPECIFICATION SHEET

COUPLER, OPTO ELECTRONIC, SEMICONDUCTOR DEVICE, SOLID STATE, THROUGH HOLE AND SURFACE MOUNT, TYPES 4N47, 4N48, AND 4N49, QUALITY LEVELS: JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for solid state optically coupled isolators in which a gallium aluminum arsenide diode light source is optically coupled to a silicon NPN phototransistor. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each type as specified in MIL-PRF-19500.

* 1.2 Package outlines and die topography. The device packages for the encapsulated device types are as follows: TO-78 in accordance with figure 1 (4N47, 4N47A, 4N48, 4N48A, 4N49, and 4N49A) and U and BU in accordance with figure 2 (4N47U, 4N48U, 4N49U, 4N47BU, 4N48BU, and 4N49BU).

1.3 Maximum ratings. Unless otherwise specified, maximum ratings apply to all case outlines, T_A = +25°C.

1.3.1 Infrared-emitting diode maximum rating.

V_R	I_F (1) (2)	I_P (3)
V dc	mA dc	A (pk)
2	40	1

(1) Derate linearly to 125°C at 0.67 mA/°C above +65°C.
(2) Minimum recommended operating I_F is 2 mA dc at +25°C.
(3) 1.0 μs pulse width, 300 pps.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

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1.3.2 Phototransistor maximum rating.

Type	V_{CEO}	V_{CBO}	V_{EBO}	P_T (1)	I_C
	V dc	V dc	V dc	mW	mA dc
4N47, 4N48, 4N49, 4N47A, 4N48A, 4N49A,4N47U, 4N48U, 4N49U	40	45	7	300	50
4N47BU, 4N48BU,4N49BU	60	60			

(1) Derate linearly to 125°C at 3 mW/°C above +25°C.

1.3.3 Total device ratings.

T_{OP}	T_{STG}	V_{IO}
°C	°C	Vdc
-55°C to 125°C	-65 to +125	1,000 V (max)

1.4 Primary electrical characteristics. Unless otherwise specified, electrical characteristics apply to all case outlines, T_A = +25°C.

1.4.1 LED (input) characteristics.

Limits	I_R V_R = 2 V dc	V_{F1} I_F = 10 mA dc
	µA dc	V dc
Minimum		0.8
Maximum	100	1.5

1.4.2 Phototransistor (output) characteristics.

Limits	$I_{C(OFF)}$	$V_{(BR)CEO}$	$V_{(BR)CBO}$	$V_{(BR)EBO}$	h_{FE}
	V_{CE} = 20 V dc	I_C = 1 mA dc	I_E = 100 µA dc	I_E = 100 µA dc	V_{CE} = 5 V dc I_C = 10 mA dc, I_F = 0
	nA	V dc	V dc	V dc	
4N47, 4N47A, 4N48, 4N48A, 4N49, 4N49A, 4N47U, 4N48U, 4N49U	100	40	45	7	100 minimum
4N47BU, 4N48BU,4N49BU		60	60		

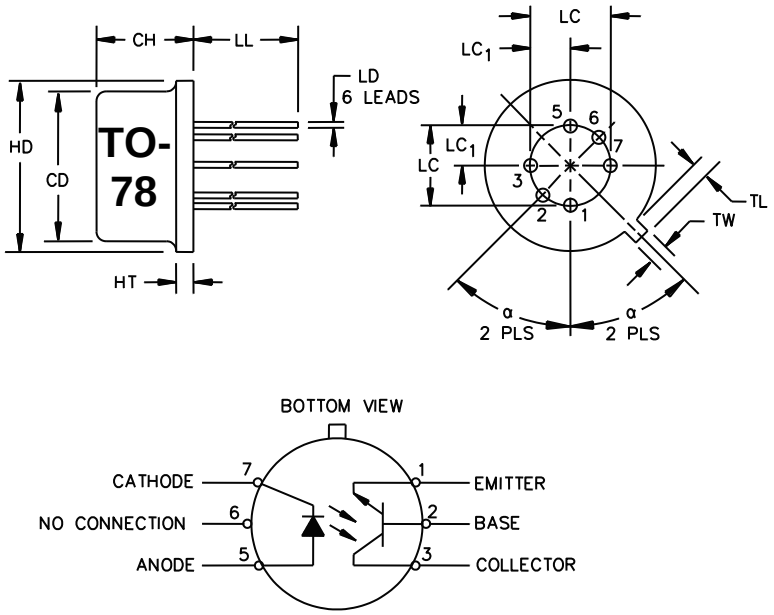
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1.4.3 Coupled (transfer) characteristics.

Limits	R_{IO} at 1,000 V (see 4.5.5)	C_{IO} V = 0, f = 1 MHz (see 4.5.5)	Phototransistor mode switching (see figure 3)						Photodiode mode switching (see figure 3)	
			t_r			t_f			t_r	t_f
			4N47 4N47A 4N47U 4N47BU	4N48 4N48A 4N48U 4N48BU	4N49 4N49A 4N49U 4N49BU	4N47 4N47A 4N47U 4N47BU	4N48 4N48A 4N48U 4N48BU	4N49 4N49A 4N49U 4N49BU		
	Ohms	pf	µs	µs	µs	µs	µs	µs	µs	µs
Minimum	10^{11}									
Maximum		5	20	20	20	20	20	20	3	3

Limits	$V_{CE(SAT)}$			$I_{C(ON)1}$			$I_{C(ON)2}$
	4N47 4N47A 4N47U 4N47BU	4N48 4N48A 4N48U 4N48BU	4N49 4N49A 4N49U 4N49BU	4N47 4N47A 4N47U 4N47BU	4N48 4N48A 4N48U 4N48BU	4N49 4N49A 4N49U 4N49BU	All
	I_F = 2 mA I_C = .5 mA	I_F = 2 mA I_C = 1 mA	I_F = 2 mA I_C = 2 mA	V_{CE} = 5 V I_F = 1 mA	V_{CE} = 5 V I_F = 1 mA	V_{CE} = 5 V I_F = 1 mA	V_{CE} = 5 V I_F = 10 mA
	V dc	V dc	V dc	mA dc	mA dc	mA dc	mA dc
Minimum				0.5	1.0	2.0	5.0
Maximum	0.3	0.3	0.3		5.0	10.0	

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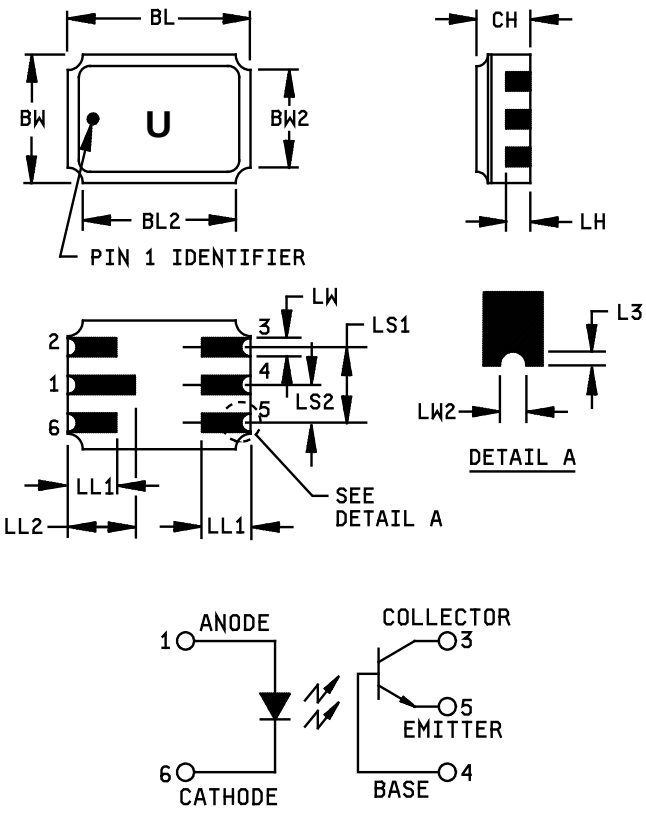
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.155	.185	3.94	4.70	
HD	.335	.370	8.51	9.40	
HT		.040		1.02	
LC	.200 T.P.		5.08 T.P.		3
LC1	.100 T.P.		2.54 T.P.		3
LD	.016	.019	0.41	0.48	
LL	.500	.600	12.70	15.24	
TL	.029	.045	0.74	1.14	
TW	.028	.034	0.71	0.86	
α	45° T.P.		45° T.P.		

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. T.P. designates true position. Leads having maximum diameter .019 inch (0.48 mm) measured in gauging plane .054 inch +.001, -.000 (1.37 mm +0.03, -0.00) below the seating plane of the device shall be within .007 inch (0.18 mm) of their true position relative to a maximum width tab.
4. Device types 4N47, 4N48, and 4N49 have the collector internally connected to the case.
5. Device types 4N47A, 4N48A, and 4N49A have the collector isolated from the case.
6. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

FIGURE 1. Physical dimensions (4N47, 4N47A, 4N48, 4N48A, 4N49, and 4N49A) (TO-78).

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Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.240	.250	6.10	6.35
BL2		.250		6.35
BW	.165	.175	4.19	4.44
BW2		.175		4.44
CH	.066	.080	1.68	2.03
LH	.036	.044	0.91	1.12
LL1	.060	.070	1.52	1.78
LL2	.082	.098	2.08	2.49
L3	.003		0.08	
LS1	.095	.105	2.41	2.67
LS2	.045	.055	1.14	1.39
LW	.022	.028	0.56	0.71
LW2	.006	.022	0.15	0.56



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Ceramic package. Due to the design of this case, the collector cannot be connected to the case.
4. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

* FIGURE 2. Physical dimensions (4N47U, 4N48U, 4N49U, 4N47BU, 4N48BU, AND 4N49BU).

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* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example, 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level. The JAN certification mark and quality level designator for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "4N".

* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "47", “48”, “49".

* 1.5.3 Suffix symbols. The following suffix letters are incorporated in the PIN in the order listed in the table as applicable:

	A blank first suffix symbol indicates an axial through-hole mount package (see figure 1).
A	Indicates an axial through-hole mount package (see figure 1).
U	Indicates a surface mount (see figure 2).
BU	Indicates a surface mount (see figure 2).

* 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-883 - Test Methods Standard Microcircuits.

* (Copies of these documents are available online at http://quicksearch.dla.mil).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

$I_{C(OFF)}$	Off-state collector current.
$I_{C(ON)}$	On-state collector current.
I_P	Peak forward pulse current.
R_{IO}	Input to output resistance.
V_{IO}	Input to output voltage.
V_{ISO}	Isolation voltage

* 3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1 (TO-78) and figure 2 (surface mount) herein. With the approval of the qualifying activity, the use of organic material is authorized.

* 3.4.1 Lead finish for 4N47, 4N47A, 4N48, 4N48A, 4N49, 4N49A. The lead finishes applicable to this specification sheet are listed on QML-19500. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

* 3.4.2 Lead finish for 4N47U, 4N48U, 4N49U, 4N47BU, 4N48BU, and 4N49BU. The lead finishes applicable to this specification sheet are listed on QML-19500. Terminal pad shall be tungsten co-fired to the ceramic package. Terminal pad finish shall be gold plated or solder dipped. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

* 3.4.3 Die shear. Die shear process control for die of less than 1.5×10^{-5} square inches of surface area shall be in accordance with the requirements for small area die in method 2019 of MIL-STD-883. Die shear is not required for the light emitting diode.

3.4.4 Moisture content. The internal moisture content of the device package shall not exceed 10,000 ppm at +100°C.

* 3.4.5 IGA Florocarbon Content. The devices are exempt from the 50 ppm limit on Florocarbon due to the internal organics.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I and II.

* 3.8 Workmanship. Optocouplers shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

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4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein shall be performed by the first inspection lot of this revision to maintain qualification. Group E qualification by extension may be granted for this specification if the qualifying activity determines it is structurally identical to other qualified devices.

* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV level
3a	See 4.3.1	See 4.3.1
3b and 3c	Not applicable	Not applicable
9	$I_{C(OFF)1}$ and h_{FE}; 100 percent read and record	$I_{C(OFF)1}$ and h_{FE}; 100 percent read and record
10	See 4.3.2	See 4.3.2
11	I_R, $I_{C(OFF)1}$, h_{FE}, and $I_{C(ON)2}$; $\Delta I_{C(OFF)1}$ = 100 percent of initial value or 25 nA dc (whichever is greater). $\Delta h_{FE} \leq \pm 20$ percent of initial reading	I_R, $I_{C(OFF)1}$, h_{FE}, and $I_{C(ON)2}$; $\Delta I_{C(OFF)1}$ = 100 percent of initial value or 25 nA dc (whichever is greater). $\Delta h_{FE} \leq \pm 20$ percent of initial reading
12	See 4.3.3	See 4.3.3
13	Subgroups 2 and 3 of table I herein; $\Delta I_{C(OFF)1} = \pm 100$ percent of initial value or 25 nA dc, (whichever is greater). $\Delta h_{FE} = \pm 20$ percent of initial reading; $\Delta I_{C(ON)2} = \pm 25$ percent of initial reading; $\Delta I_R = \pm 100$ percent of initial value or 25 μA dc, (whichever is greater)	Subgroup 2 of table I herein; $\Delta I_{C(OFF)1} = \pm 100$ percent of initial value or 25 nA dc (whichever is greater). $\Delta h_{FE} = \pm 20$ percent of initial reading; $\Delta I_{C(ON)2} = \pm 25$ percent of initial reading $\Delta I_R = \pm 100$ percent of initial value or 25 μA dc, (whichever is greater)

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4.3.1 Temperature cycling. All devices shall be subjected to temperature cycling in accordance with method 1051 of MIL-STD-750, test condition B, except $T_{(min)}$ = -55°C; 10 cycles, 15 minutes minimum dwell.

4.3.1.1 Monitored temperature cycling. One cycle of monitored temperature cycling shall be performed on 100 percent of the devices. This test shall be performed any time after the completion of the thermal shock test specified or it may be the last of the ten thermal cycles. The monitored temperature cycle is exempt from the ramp rate and time to temperature requirements in Method 1051 of MIL-STD-750 to allow for the increased thermal mass of the support circuitry. All junctions shall be monitored for electrical continuity. Any discontinuity shall be cause for rejection of the device(s) under test. If 10 percent or more of the number of devices subjected to monitored temperature cycling fail, the entire lot shall be rejected as any JAN quality level.

4.3.2 High temperature reverse bias (HTRB). All devices shall be subjected to high temperature reverse bias in accordance with method 1039 of MIL-STD-750, test condition A, T_A = +125°C, I_F = 0, V_{CB} = 36 V dc for 48 hours minimum.

4.3.3 Power burn-in conditions. Power burn-in conditions are as follows: See figure 4 for burn-in circuit. V_{CC} = 20 V dc, V_{CE} = 10 ±5 V dc, I_F = 40 mA dc, P_T = 275 ±25 mW at T_A = +25°C ±3°C. No heat sink or forced air cooling directly on the devices shall be permitted.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.1.1 Multiple device type processing and binning. The manufacturer may process structurally identical JAN JANTX or JANTXV devices from lots as a single intergral part number and segregate into specific part numbers at the conclusion of group A testing. When devices are processed using the MIL-PRF-19500 standard flow, each part number in the assembly lot must separately complete group A. When devices are processed using an alternate flow, the initial group A may be performed on a sample of randomly selected devices from each assembly lot that comprises the inspection lot through the use of a worst case or binning test. Each appropriate part number selected from the initial group A shall complete a final group testing (A_1, A_2, and B_1) by individual part number. Qualification by extension may be granted for this specification by the if the qualifying activity determines it is structurally identical to other qualified devices.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa (JANS) and table E-VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500, and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup II herein. Samples for group B testing of JAN, JANTX, or JANTXV devices processed through group A alternate flow shall be randomly selected from all appropriate part numbers represented in the inspection lot.

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4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

	Subgroup	Method	Condition
	B3	1056	Test condition B.
*	B3	1071	Fine leak: Condition G or H; Gross leak
	B3	2037	Bond strength: Test condition D. Sample used in decap internal visual design verification may be used in bond strength and die shear. Sample is in units.
	B4		High temperature isolation voltage test (see 4.5.2) and as follows: V_{ISO} = 150 V dc, T_A = +125°C, t = 24 hours minimum. n = 22, c = 0, small lot sample size n = 8, c = 0.
	B4	1037	V_{CE} = 10 V dc, I_F = 20 mA dc, P_T = 275 ±25 mW at T_A = +25°C ±3°C (see figure 4), t_{on} = t_{off} = 3 minutes minimum for 2,000 cycles. No heat sink or forced air cooling directly on the device shall be permitted.
	B5	1027	V_{CE} = 10 V dc, T_A = +100°C ±3°C for 96 hours, P_T = 275 ±25 mW, I_F = 20 mA dc (see figure 4). Marking legibility requirements shall not apply.
*	B5	2037	(Al-Au die interconnects only), test condition D.
	B6, B7		Not applicable.

4.4.2.2 Group B inspection, table E-VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

	Subgroup	Method	Condition
	B2	1056	Thermal shock: Test condition B (25 cycles). Total test time = 72 hours maximum.
*	B2	1071	Fine leak - condition G or H, gross leak.
	B3		High temperature isolation voltage test conditions: V_{ISO} = 150 V dc (see 4.5.2), T_A = +125°C, t = 24 hours minimum. n = 22, c = 0, small lot sample size = 8, c = 0.
	B3	1027	I_F = 20 mA dc, P_T = 275 ± 25 mW at T_A = +25°C ±3°C (see figure 4). No heat sink or forced air cooling directly on the device shall be permitted.
*	B4	2037	Test condition D.
	B5, B6		Not applicable.

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* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup II herein. Samples for group C testing of JAN, JANTX, and JANTXV devices processed through Group A alternate flow shall be randomly selected from all appropriate part numbers represented in the inspection lot.

	Subgroup	Method	Condition
	C2	1056	Thermal shock: Test condition A.
	C2	2036	Terminal strength, test condition E. Not applicable to surface mount devices.
*	C2	1071	Fine leak - condition G or H; gross leak.
	C3	2016	Non-operating; 1,500 G, t = 0.5 ms, 5 blows in each orientation: X_1, Y_1, Z_1
	C3	2056	50 G minimum. Non-operating.
	C3	2006	Non-operating, 30,000 G, X_1, Y_1, Z_1 orientations.
	C6	1026	I_F = 20 mA dc, P_T = 275 ±25 mW at T_A = +25°C ±3°C, T = 1,000 hours (see figure 4). No heat sink or forced air cooling directly on the device shall be permitted.
*	C7	1018	See 3.4.5.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with MIL-PRF-19500 and table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions of pulse measurements shall be as specified in MIL-STD-750.

4.5.2 High temperature isolation voltage lot verification. This test shall be performed by shorting both the anode and cathode terminals of the LED (light emitting diode) and shorting together the collector, emitter, and base terminals of the transistor. The sample shall be split into two approximately equal groups and the specified V_{ISO} applied between the LED terminals (positive) and transistor terminals (negative) of one group. The specified isolation voltage shall be repeated with the LED terminals (negative) and the transistor terminal (positive) for the remaining group. All voltages shall be applied at the specified ambient temperature.

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4.5.3 Input LED tests. These tests shall be performed with the output transistor terminals open.

4.5.4 Output transistor tests. These tests shall be performed with the input LED terminals open.

4.5.5 Isolation and coupling capacitance tests. These tests shall be performed in both polarities between both input terminals 5 and 7 shorted together and the output terminals 1, 2, and 3 shorted together (see figure 1) or input terminals 1 and 6 shorted together and output terminals 3, 4, and 5 shorted together (see figure 2).

4.5.6 On-State collector current, phototransistor mode. These tests shall be performed with the base open in the circuit, with the active area of the phototransistor tied to the base and LED biased on to emit light, to provide bias to the base.

4.6 Internal visual inspection (JANTXV and JANS only). Internal visual inspection shall be performed in accordance with methods 2072 and 2073 of MIL-STD-750, and as specified herein. Method 2072 shall be used for inspecting transistor die and completed assembly. Method 2073 shall be used for inspecting light emitting diode.

4.6.1 Gallium arsenide or gallium aluminum arsenide light emitting diode die inspection. The die shall be inspected under 100X magnification.

4.6.2 Silicon phototransistor visual inspection. The die shall be inspected under 100X magnification.

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TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2 2/						
LED characteristics:						
Reverse current leakage	4016	V_R = 2 V dc (see 4.5.3)	I_R		100	μA dc
Forward voltage	4011	I_F = 10 mA dc (see 4.5.3)	V_{F1}	0.8	1.5	V dc
Transistor characteristics:						
Collector to emitter breakdown voltage	3011					
4N47, 4N47A, 4N47U 4N48, 4N48A, 4N48U 4N49, 4N49A, 4N49U		I_C = 1 mA dc, I_B = 0, I_F = 0 (see 4.5.4)	$V_{(BR)CEO}$	40		V dc
4N47BU, 4N48BU,4N49BU				60		V dc
Collector to base breakdown voltage	3001					
4N47, 4N47A, 4N47U 4N48, 4N48A, 4N48U 4N49, 4N49A, 4N49U		I_C = 100 μA dc, I_F = 0, I_E = 0 (see 4.5.4)	$V_{(BR)CBO}$	45		V dc
4N47BU, 4N48BU,4N49BU				60		V dc
Emitter to base breakdown voltage	3026	I_E = 100 μA dc, I_C = 0, I_F = 0 (see 4.5.4)	$V_{(BR)EBO}$	7		V dc
Off-state collector current phototransistor mode:	3041	V_{CE} = 20 V dc, I_B = 0, I_F = 0, condition D (see 4.5.4)	$I_{C(OFF)1}$		100	nA dc
DC current gain	3076	V_{CE} = 5 V; I_C = 10 mA dc, I_F = 0 (see 4.5.4)	h_{FE}	100		

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 2/ - Continued						
Coupler characteristics:						
On-state collector current phototransistor mode:	3041	V_{CE} = 5 V dc, I_F = 1 mA dc	$I_{C(ON)1}$			
4N47, 4N47A, 4N47U, 4N47BU				0.5		mA dc
4N48, 4N48A, 4N48U, 4N48BU				1.0	5.0	mA dc
4N49, 4N49A, 4N49U, 4N49BU				2.0	10.0	mA dc
All types	3041	V_{CE} = 5 V dc, I_F = 10 mA dc	$I_{C(ON)2}$	5.0		mA dc
Collector to emitter saturation voltage			$V_{CE(SAT)}$			
4N47, 4N47A, 4N47U, 4N47BU		I_C = 0.5 mA dc, I_F = 2 mA dc			0.3	V dc
4N48, 4N48A, 4N48U, 4N48BU		I_C = 1 mA dc, I_F = 2 mA dc			0.3	V dc
4N49, 4N49A, 4N49U, 4N49BU		I_C = 2 mA dc, I_F = 2 mA dc			0.3	V dc
Subgroup 3 2/						
High temperature operation		T_A = +100°C				
Transistor characteristics:						
Off-state collector current phototransistor mode:	3041	V_{CE} = 20 V dc, I_F = 0, I_B = 0, condition D (see 4.5.4)	$I_{C(OFF)2}$		100	µAdc
Coupler characteristics:	3041					
On-state collector current phototransistor mode:		V_{CE} = 5 V dc, I_F = 2 mA dc	$I_{C(ON)3}$			
4N47, 4N47A, 4N47U, 4N47BU				0.5		mA dc
4N48, 4N48A, 4N48U, 4N48BU				1.0		mA dc
4N49, 4N49A, 4N49U, 4N49BU				2.0		mA dc
LED characteristics forward voltage	4011	I_F = 10 mA dc (see 4.5.3)	V_{F2}	0.7	1.3	V dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

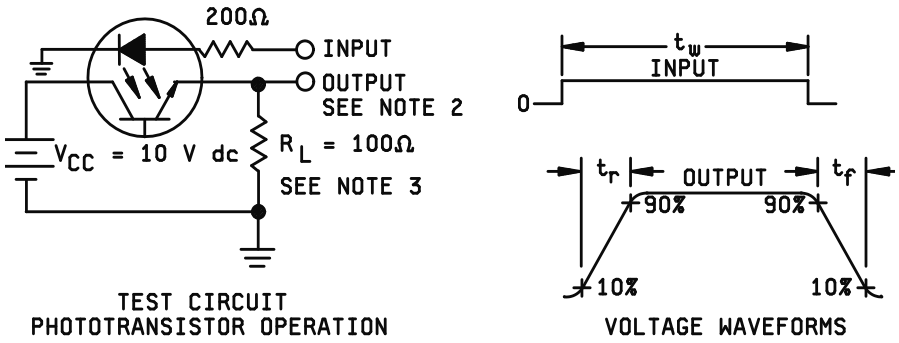
Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 3 2/ - Continued						
Low temperature operation Coupler characteristics:		T_A = -55°C				
On-state collector current phototransistor mode: 4N47, 4N47A, 4N47U, 4N47BU 4N48, 4N48A, 4N48U, 4N48BU 4N49, 4N49A, 4N49U, 4N49BU	3041	V_{CE} = 5 V dc, I_F = 2 mA dc	$I_{C(ON)4}$	 0.5 1.0 2.8		 mA dc mA dc mA dc
LED characteristics:						
Forward voltage	4011	I_F = 10 mA dc (see 4.5.3)	V_{F3}	1.0	1.7	V dc
Subgroup 4 2/						
Input to output capacitance		f = 1 MHz, (see 4.5.5), $\|V_{IN-OUT}\|$ = 0	C_{IO}		5	pF
Input to output internal resistance	1016	$\|V_{IN-OUT}\|$ = 1 kV dc (see 4.5.5)	R_{IO}	10^{11}		Ω
Rise time phototransistor mode:		V_{CC} = 10 V dc, I_F = 5 mA dc, R_L = 100 ohms (see figure 3)	t_r		20	µs
Fall time phototransistor mode:		V_{CC} = 10 V dc, I_F = 5 mA dc, R_L = 100 ohms (see figure 3)	t_r		20	µs
Rise time photodiode mode:		V_{CC} = 10 V dc, I_F = 5 mA dc, R_L = 100 ohms (see figure 3)	t_r		3	µs
Fall time photodiode mode:		V_{CC} = 10 V dc, I_F = 5 mA dc, R_L = 100 ohms (see figure 3)	t_r		3	µs
Subgroups 5 and 6						
Not applicable						
Subgroups 7						
Monitored thermal shock (temperature cycling)		See 4.3.1.1				

1/ For sampling plan, see MIL-PRF-19500.
2/ All devices required by the specified sampling plan are subjected to subgroups 2, 3, and 4 combined (JANS only).

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TABLE II. Group E inspections (all quality levels) for qualification only.

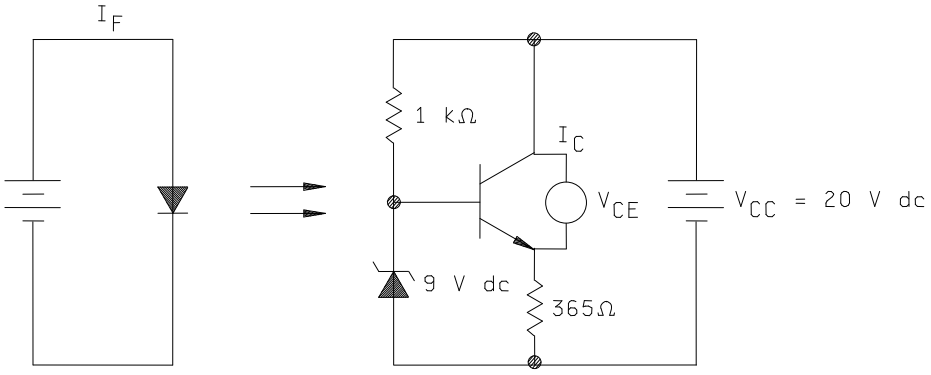
Inspections	MIL-STD-750		Quality conformance inspection sample size.
	Method	Conditions	
Subgroup 1			45 devices, c = 0
Temperature cycling	1051	Test condition B, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		Table I, subgroup II	
Subgroup 2			45 devices, c = 0
High temperature reverse bias	1039	For all devices with organic material.	
Electrical measurements		Table I, subgroup II	



NOTES:
1. The input waveform is supplied by a generator with the following characteristics: Z_{OUT} = 50 Ω, $t_r \leq$ 15 ns, duty cycle = 1 percent; t_W = 100 μs.
2. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, R_{in} = 1 MΩ, C_{in} = 20 pF.
3. Adjust amplitude of input for: I_F = 5mA dc.

FIGURE 3. Switching times.

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NOTES:
1. I_F = 20 mA dc for operation life tests.
2. I_F = 40 mA dc for burn-in of TX, TXV, and S.

FIGURE 4. Operation life test burn-in circuit.

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1 and 3.4.2).

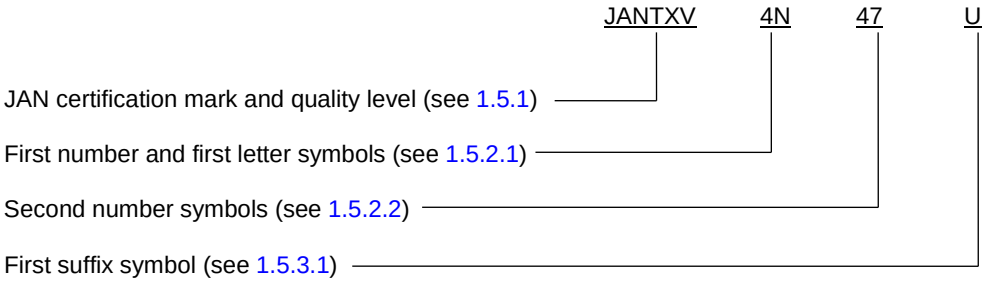
* d. The complete Part or Identifying Number (PIN), see title and section 1.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil . An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

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* 6.4 PIN construction example.

* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for types4N47, 4N48, 4N49			
JAN4N47	(1)	JANTXV4N47	(1)
JAN4N48	(1)	JANTXV4N48	(1)
JAN4N49	(1)	JANTXV4N49	(1)
JANTX4N7	(1)	JANS4N47	(1)
JANTX4N48	(1)	JANS4N48	(1)
JANTX4N49	(1)	JANS4N49	(1)

(1) This includes the A, U, and BU devices.

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* 6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
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Army - AR, MI, SM
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* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.

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