

## PROTECTION PRODUCTS

### Description

μClamp® series of TVS arrays are designed to protect sensitive electronics from damage or latch-up due to ESD. They feature large cross-sectional area junctions for conducting high transient currents. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

μClamp1211P is in a 2-pin SLP1006P2 package, measuring 1.0 x 0.6 x 0.5mm. Leads are spaced at a pitch of 0.65mm and are finished with lead-free NiPdAu. Each device will protect one bidirectional line operating at ±12 volts. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±30kV air, ±30kV contact discharge). The combination of small size and high ESD surge capability makes them ideal for use in applications such as cellular phones, industrial equipment, and portable instrumentation.

### Features

- High ESD withstand Voltage: +/-30kV (Contact) and +/-30kV (Air) per IEC 61000-4-2
- Ultra-small package(1.0 x 0.6 x 0.5mm)
- Protects one I/O or power line
- Low ESD clamping voltage
- Working voltage: +/-12V
- Low leakage current
- Solid-state silicon-avalanche technology

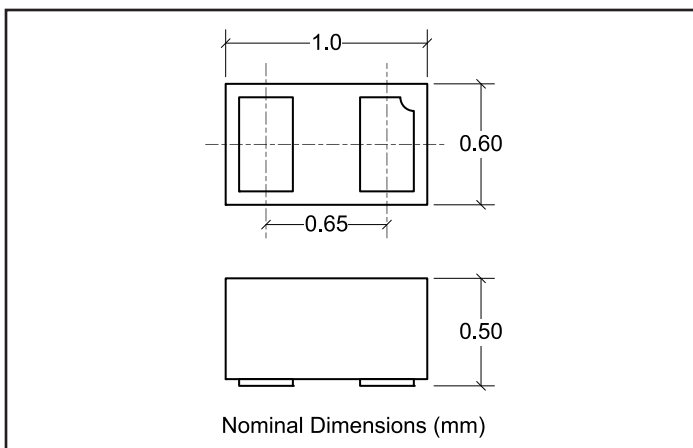
### Mechanical Characteristics

- SLP1006P2 package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Molding compound flammability rating: UL 94V-0
- Lead Finish: NiPdAu
- Marking: Marking code
- Packaging: Tape and Reel

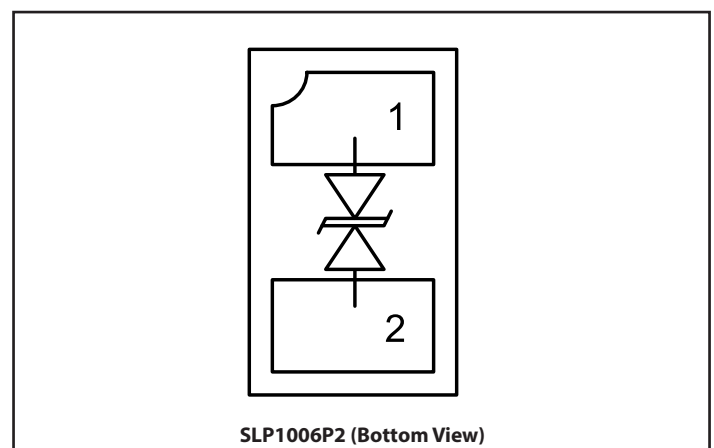
### Applications

- Cellular Handsets & Accessories
- Industrial Equipment
- Notebooks & Handhelds
- Portable Instrumentation
- RS-232 Interfaces
- Peripherals

### Package Dimension



### Schematic & Pin Configuration



## Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	$P_{PK}$	200	W
Peak Pulse Current ( $t_p = 8/20\mu s$ )	$I_{PP}$	7	A
ESD per IEC 61000-4-2 (Air) <sup>(1)</sup> ESD per IEC 61000-4-2 (Contact) <sup>(1)</sup>	$V_{ESD}$	$\pm 30$ $\pm 30$	kV
Operating Temperature	$T_J$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

## Electrical Characteristics (T=25°C unless otherwise specified)

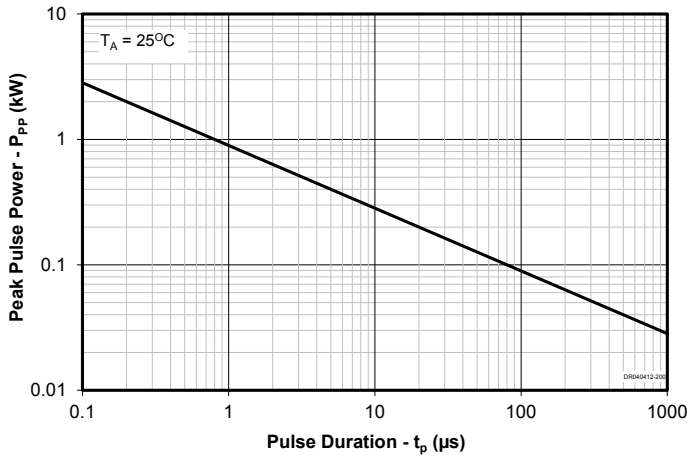
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	$V_{RWM}$				12	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	14.2	15.8	18	V
Reverse Leakage Current	$I_R$	$V_{RWM} = 12V$			1	$\mu A$
Clamping Voltage	$V_C$	$I_{PP}=1A, t_p = 8/20\mu s$			19	V
		$I_{PP}=7A, t_p = 8/20\mu s$			28.5	
Junction Capacitance	$C_J$	$V_R = 0V, f = 1MHz$			25	pF

### Notes

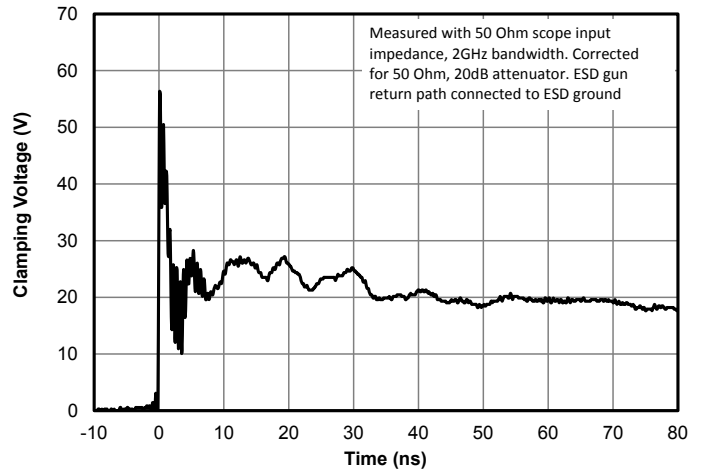
- 1) Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.
- 2) Transmission Line Pulse Test (TLP) Settings:  $t_p = 100ns$ ,  $t_r = 0.2ns$ ,  $I_{TLP}$  and  $V_{TLP}$  averaging window:  $t_1 = 70ns$  to  $t_2 = 90ns$ .
- 3) Dynamic resistance calculated from  $I_{TLP} = 4A$  to  $I_{TLP} = 16A$

# Typical Characteristics

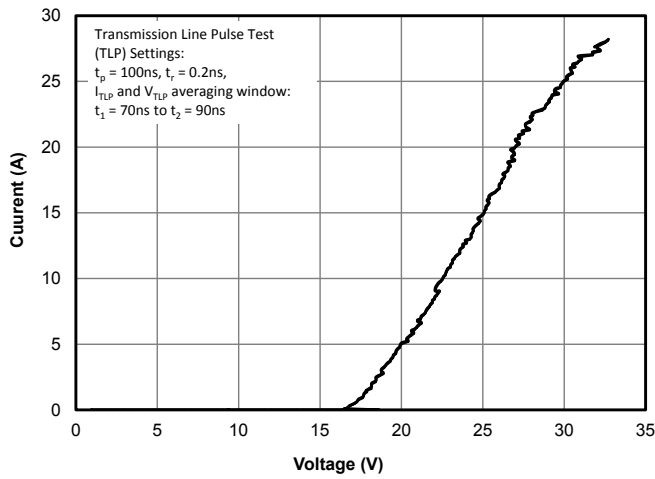
### Non-Repetitive Peak Pulse Power vs. Pulse Time



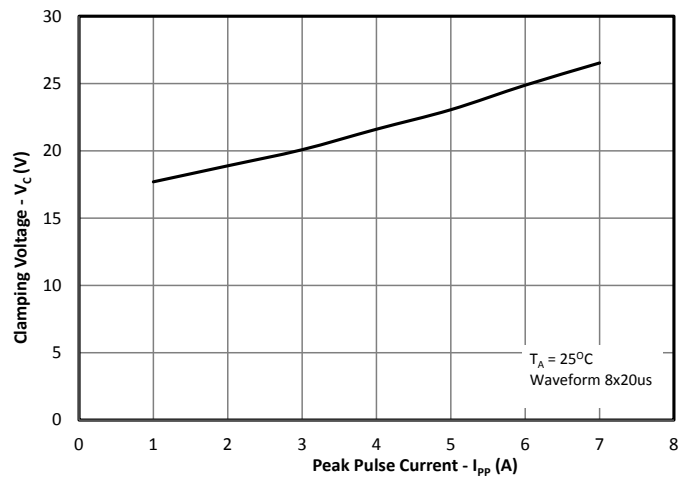
### ESD Clamping (-8kV Contact per IEC 61000-4-2)



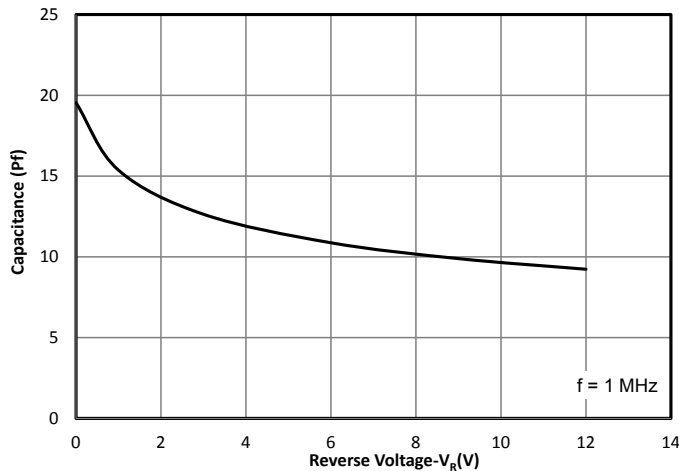
### TLP Characteristic (Positive Pulse)



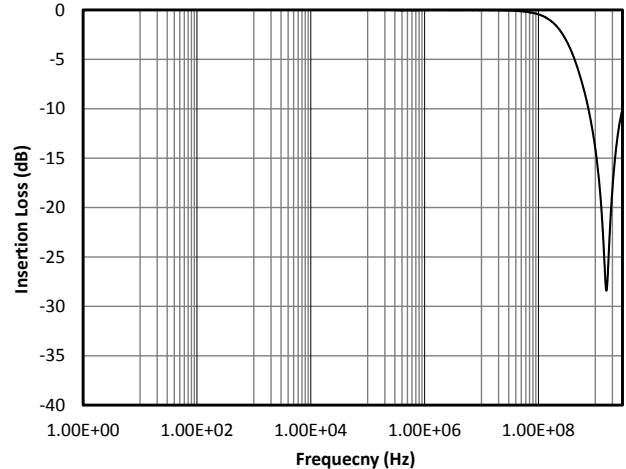
### Clamping Voltage vs. Peak Pulse Current ( $t_p = 8/20\mu$ s)



### Capacitance vs. Reverse Voltage



### Insertion Loss



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## Application Information

### Device Connection Options

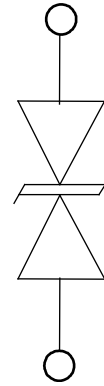
This TVS diode is designed to protect one data, I/O, or power supply line. The device is bidirectional and may be used on lines where the signal polarity can go above and below ground. The device is symmetrical, and therefore, the orientation of the device is not critical.

### Circuit Board Layout Recommendations for Suppression of ESD.

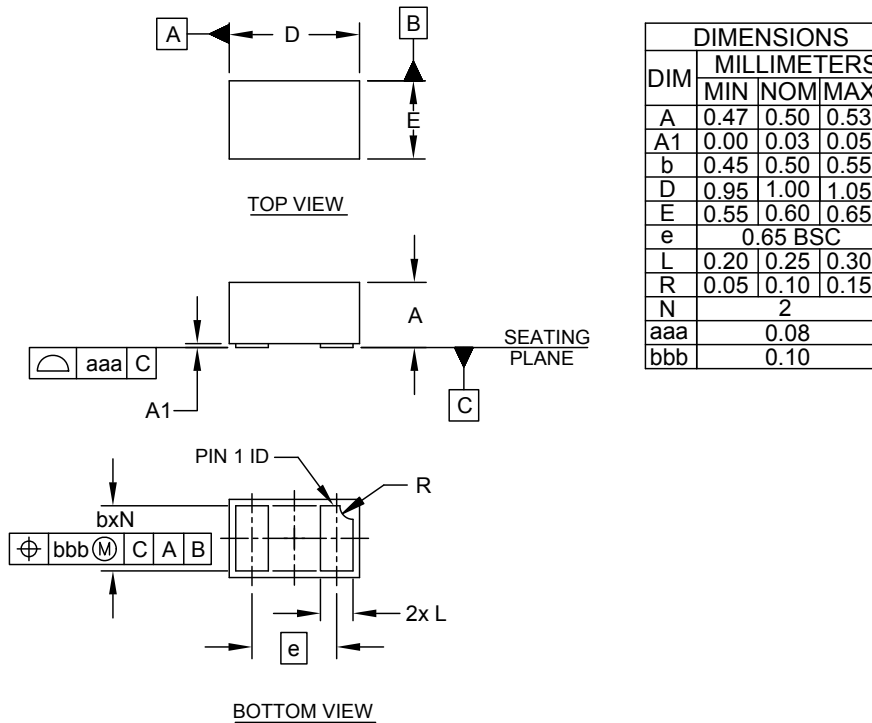
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

## Circuit Diagram



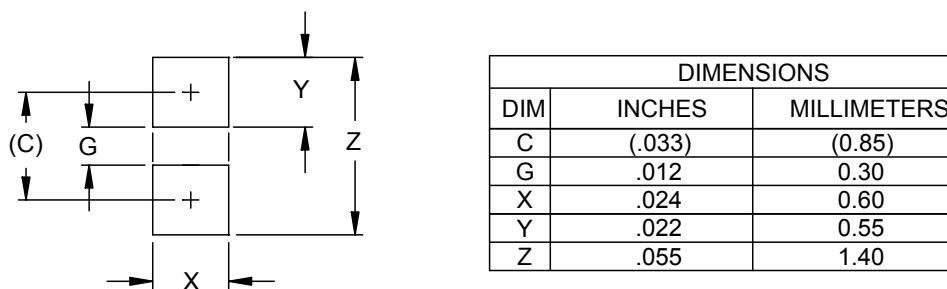
## Outline Drawing - SLP1006P2



**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

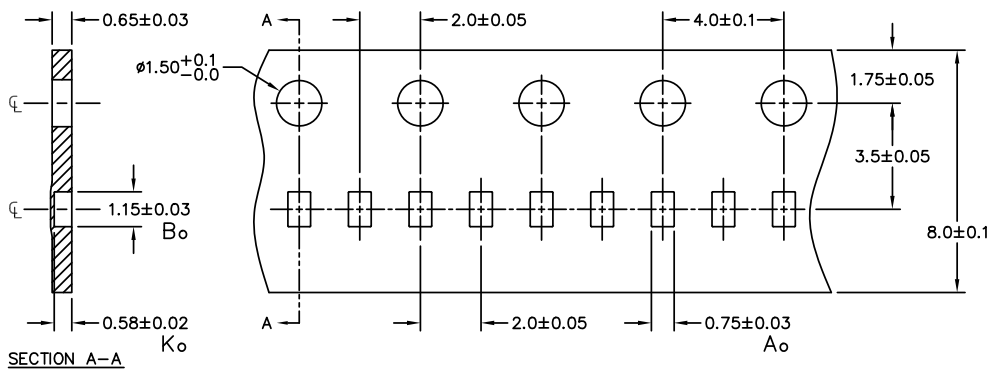
## Land Pattern - SLP1006P2



**NOTES:**

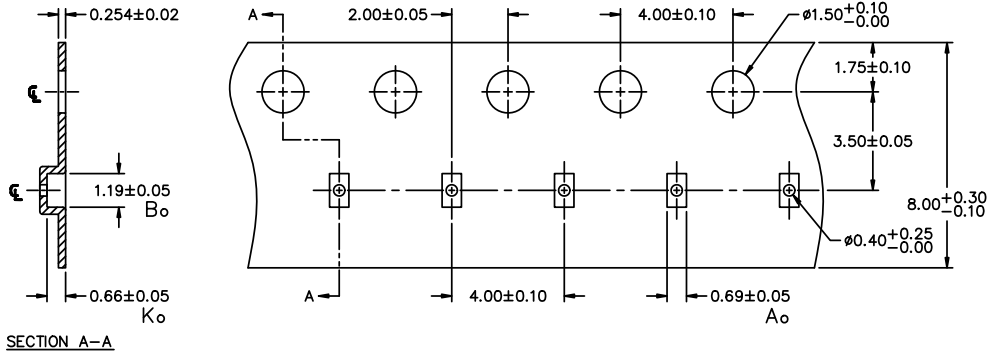
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.  
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

# Tape and Reel Specification



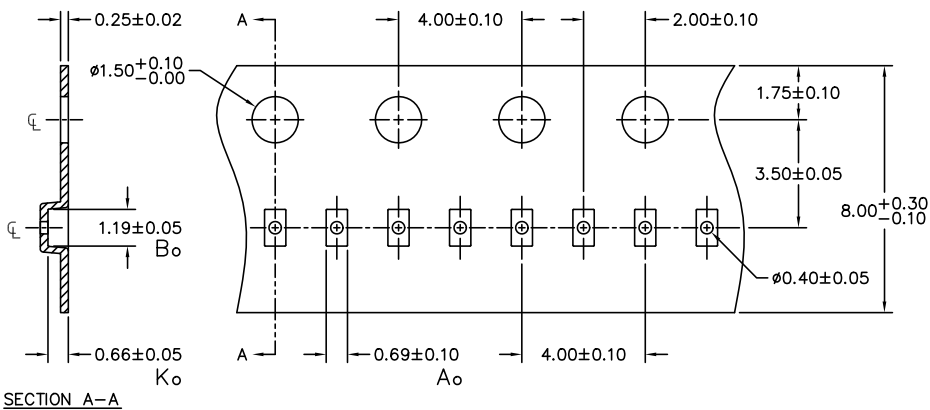
NOTES: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

Paper Carrier Tape, 2mm Pitch Option



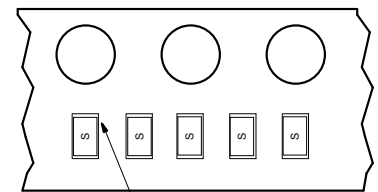
NOTES: 1.) ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

Plastic Carrier Tape, 4mm Pitch Option



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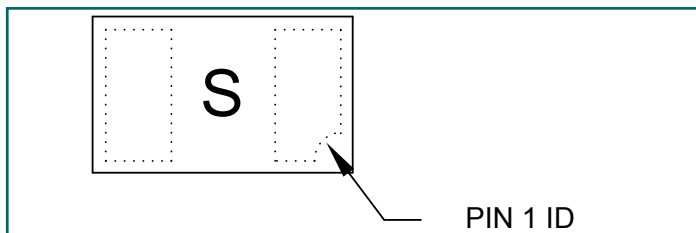
Plastic Carrier Tape, 2mm Pitch Option



Pin 1 Location  
(Towards Sprocket Holes)

Device Orientation in Tape

## Marking Code



## Ordering Information

Part Number	Qty per Reel	Pocket Pitch	Tape Material	Reel Size
$\mu$ Clamp1211P.TCT	3,000	4mm	Plastic	7"
$\mu$ Clamp1211P.TNT	10,000	2mm	Plastic	7"
$\mu$ Clamp1211P.TFT	15,000	2mm	Paper	7"



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