PT9528

2/1-Phase PWM Controller

with Embedded 5V MOSFET Driver for IMVP6

GENERAL DESCRIPTION

The PT9528 is a 2/1-phase synchronous rectified Buck controller specifically designed to deliver high quality output voltage for high-performance CPU. It integrates a 7-bit VID that supports Intel IMVP6 tables to set the output voltage between 0.3V and 1.5V.

The PT9528 combines true differential output voltage sense, differential inductor DCR current sense, input voltage sense and output voltage sense for notebook CPU. It adopts Constant On-time control topology to have fast transient response and smooth mode transition. This part has integrated bootstrap diode to minimize the external component count. The PT9528 features IMON function and output offset function to maximize the application flexibility. The PT9528 also provides complete fault protections such as over-voltage protection, under-voltage protection, channel current limit, over current protection and thermal shutdown. The PT9528 is available in a VQFN7x7-48L package.

FEATURES

- ❒ **Intel IMVP6 Compatible**
  - ■ **7-Bit VID Input**
  - ■ **Enable Control (VR_ON)**
  - ■ **Power State Indication (PSI#)**
  - ■ **DPRSLPVR/DPRSTP# Input and CLK_EN# Indication**
  - ■ **Thermal Sense with VR_TT# Indication**
  - ■ **Power Good Indication (PGOOD)**
- ❒ **2 Integrated 5V MOSFET Drivers**
  - ■ **Embedded Bootstrap Diode**
- ❒ **2/1 Phase Operation**
- ❒ **External Compensation**
- ❒ **Selectable Operation Frequency from 200kHz to 500kHz**
- ❒ **Differential Remote Voltage Sense**
- ❒ **Inductor DCR current sense**
- ❒ **OCP/OVP/UVP/Thermal Shutdown.**
- ❒ **RoHS Compliant and Halogen Free**

APPLICATIONS

- Notebook PC CPU Power Supplies

ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	MARKING
VQFN7x7-48L	-40℃ to 85℃	PT9528PQAK	PT9528 xxxxxX

TYPICAL APPLICATION CIRCUIT

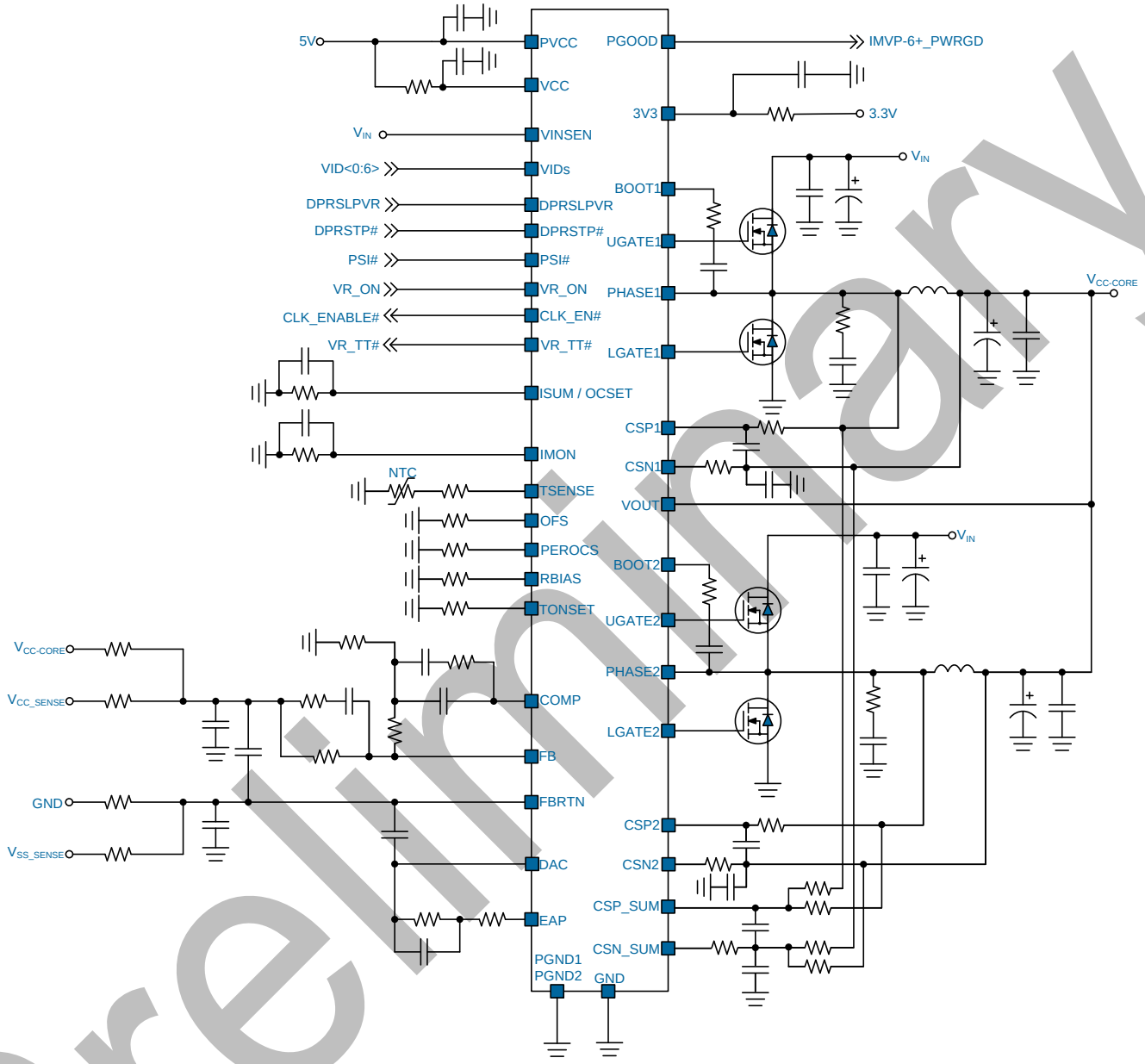


Figure1. Typical Application of PT9528

PIN ASSIGNMENT

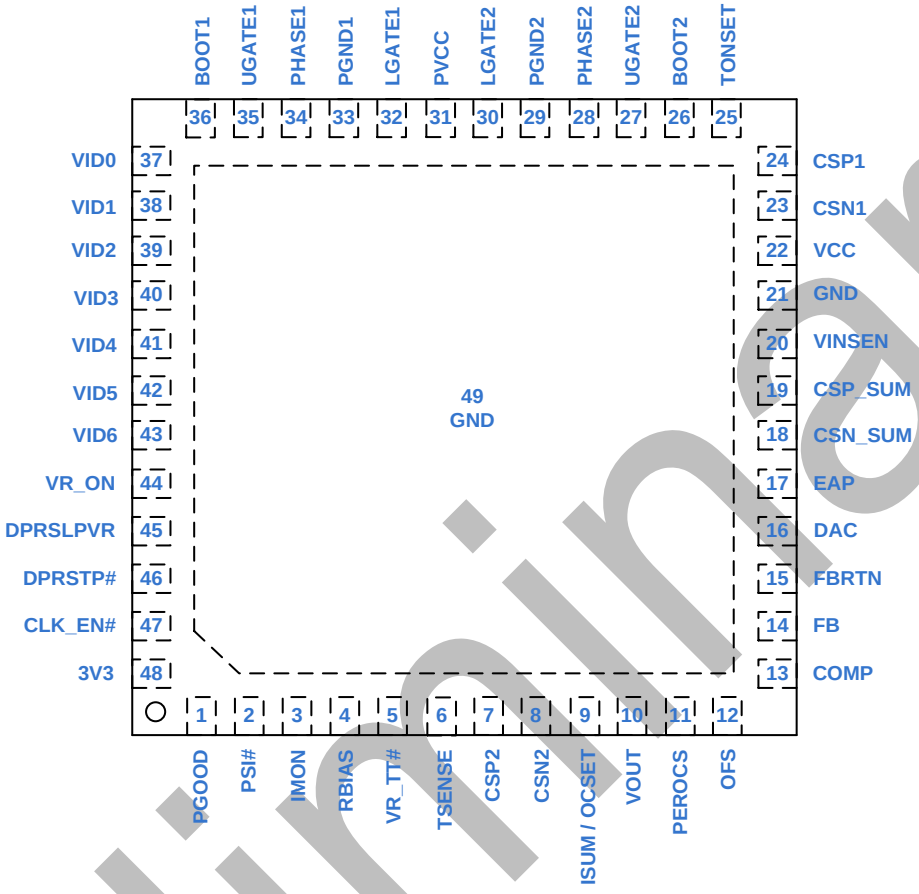


Figure 2. Pin Configuration of PT9528 (Top View)

PIN DESCRIPTIONS

NO.	Name	Pin Function
1	PGOOD	**Power Good Indication.** This pin is an open drain structure and it is active high. Pull up this pin through a proper resistor to a voltage source.
2	PSI#	**Power Status Indicator.** An input pin receives power saving control signal from CPU.
3	IMON	**Output Current Monitor.** The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMON voltage proportional to the total output current.
4	RBIAS	**Internal Current Reference.** Connect a 30kΩ resistor from this pin to GND and place this resistor close to the controller. Do NOT use other resistance value other than the value specified here.
5	VR_TT#	**Thermal Indicator.** This pin is an open drain structure and it is active low. The controller asserts VR_TT# to indicate the platform temperature is higher than the threshold.
6	TSENSE	**Thermal Monitoring Input.** Connect a specified negative temperature coefficient (NTC) thermistor network from this pin to GND for temperature sensing.
7	CSP2	**Positive Differential Current Sense Input for Phase2**. To disable the MOSFET driver of this phase (BOOT2, UGATE2, PHASE2, LGATE2), short this pin to GND.
8	CSN2	**Negative Differential Current Sense Input for Phase2**. To disable the MOSFET driver of this phase (BOOT2, UGATE2, PHASE2, LGATE2), pull high this pin to VCC through a 1kΩ resistor to disable this phase.
9	ISUM/OCSET	**Total Over Current Protection Setting and Sensing.** Connect a resistor from this pin to GND to set the over current protection threshold. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the ISUM voltage proportional to the total output current. This pin is used for total output current protection.
10	VOUT	**Output Voltage.** Connect this pin directly to output voltage plane.
11	PEROCS	**Per-Phase Over Current Protection Setting.** Connect a resistor from this pin to GND to set the per-phase current limit threshold.
12	OFS	**VOUT Offset.** Connect a resistor R_{OFS} from this pin to GND to set VOUT offset voltage. Connect R_{OFS} =300kΩ to disable this function.
13	COMP	**Compensation Output**. This pin is the output of the control loop error amplifier.
14	FB	**Feedback Pin**. This pin is the inverting input of the error amplifier.
15	FBRTN	**Output Voltage Feedback Return.** Inverting input to the differential voltage sense amplifier. FBRTN is the reference point in DAC output voltage measurement. Connect this pin directly to the processor output voltage feedback return sense point, namely VSS_SENSE.
16	DAC	**DAC Output.**The output voltage of this pin is the reference voltage**.** DAC voltage is measured with respect to FBRTN. Connect a capacitor recommend 22nF from this pin to FBRTN.

17	EAP	**Non-Inverting Input of the Error Amplifier**. Connect a resistor between this pin and DAC to set the droop (load line) function
18	CSN_SUM	**Inverting Input of the Total Current Sensing Amplifier.** Total load current sense inverting input. Connect a resistor between CSN_SUM and the VOUT side of all output inductors. The selected VOUT point should have equal resistance to the VOUT side of all inductors.
19	CSP_SUM	**Non-inverting Input of the Total Current Sensing Amplifier**. Resistors from each switch node to this pin average the inductor currents on the capacitor between CSP_SUM and VOUT.
20	VINSEN	**Power Stage Input Voltage Sense**. Directly connect this pin to the power stage input VIN. The controller senses the voltage on this pin for power stage input voltage VIN detection. The VINSEN voltage is also used for PWM on-time calculation.
21	GND	**Ground.**
22	VCC	**Supply Input for Logic Control Circuit.** Connect this pin to a 5V voltage source with a 2.2Ω and decouple using at least 1uF MLCC.
23	CSN1	**Negative Differential Current Sense Input for Phase 1.**
24	CSP1	**Positive Differential Current Sense Input for Phase 1.**
25	TONSET	**PWM On-time Setting**. Connect a resistor from this pin to GND to set the PWM on-time.
26	BOOT2	**BOOT for Phase 2**. Connect a capacitor from this pin to PHASE2 to form a bootstrap circuit for upper gate driver of the phase 2.
27	UGATE2	**Upper Gate Driver for Phase 2**. Connect this pin to the gate of phase 2 upper MOSFET.
28	PHASE2	**Phase Pin for Phase 2**. This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase 2.
29	PGND2	**The return path of the lower gate driver for phase 2.**
30	LGATE2	**Lower Gate Driver for Phase 2**. Connect this pin to the gate of phase 2 lower MOSFET
31	PVCC	**Supply Input for Embedded MOSFET Driver.** Connect this pin to a 5V voltage source, and bypass this pin to GND with at least 1.0uF MLCC placed very close to the PVCC pin. PVCC is the supply input for the embedded MOSFET drivers.
32	LGATE1	**Lower Gate Driver for Phase 1**. Connect this pin to the gate of phase 1 lower MOSFET.
33	PGND1	**The return path of the lower gate driver for phase 1.**
34	PHASE1	**Phase Pin for Phase 1**. This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
35	UGATE1	**Upper Gate Driver for Phase 1**. Connect this pin to the gate of phase 1 upper MOSFET

36	BOOT1	**BOOT for Phase 1**. Connect a capacitor from this pin to PHASE1 to form a bootstrap circuit for upper gate driver of the phase 1.
37	VID0	Bit 0 for VID Input.
38	VID1	Bit 1 for VID Input.
39	VID2	Bit 2 for VID Input.
40	VID3	Bit 3 for VID Input.
41	VID4	Bit 4 for VID Input.
42	VID5	Bit 5 for VID Input.
43	VID6	Bit 6 for VID Input.
44	VR_ON	**Voltage Regulator On.** Chip Enable Control Input.
45	DPRSLPVR	**Deeper Sleep Mode Enable Input Pin.** Deeper sleep enable signal. A logic high signal on this pin indicates the micro-processor is in deeper-sleep mode.
46	DPRSTP#	**Deeper Sleep Slow Wake Up Enable Input Pin.** A logic low signal on this pin indicates the micro-processor is in deeper-sleep mode.
47	CLK_EN#	**Start clock indicator.** This is a logic buffer output pin. This pin asserts low to indicate that the controller is ready to accept PVID command.
48	3V3	**3.3V supply Input for CLK_EN#.**
Exposed Pad		**Ground**. The exposed pad is the ground of logic control circuits, and it must be soldered to a large PCB and connected to GND.

ABSOLUTE MAXIMUM RATINGS (Note1)

Supply Input Voltage VCC to GND ---------- -0.3V to + 6V
Supply Input Voltage PVCC to GND ---------- -0.3V to + 6V
VINSEN ---------- -0.3V to + 30V
BOOTx to PHASEx ---------- -0.3V to + 6V
PHASEx to GND
DC ---------- -0.7V to +28V
< 100ns ---------- -8V to +36V
BOOTx to GND
DC ---------- -0.3V to + 34V
< 100ns ---------- -5V to + 42V
UGATEx to PHASEx
DC ---------- -0.3V to (BOOTx - PHASEx +0.3V)
<100ns ---------- -5V to (BOOTx - PHASEx+ 0.3V)
LGATEx to GND
DC ---------- -0.3V to (PVCC + 0.3V)
<100ns ---------- -5V to (PVCC + 0.3V)
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65℃to +150℃
Junction Temperature ---------- 150℃
Lead Temperature (Soldering, 10 sec) ---------- 260℃
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV

Thermal Information

Package Thermal Resistance (Note 3)
VQFN7x7 - 48L θ_{JA} ---------- 31℃/W
VQFN7x7 - 48L θ_{JC} ---------- 2℃/W
Power Dissipation, P_D @ T_A = 25℃
VQFN7x7 - 48L ---------- 3.23W

Recommended Operation Conditions

(Note 4)
Operating Junction Temperature Range ---------- -40℃ to +125℃
Operating Ambient Temperature Range ---------- -40℃ to +85℃
Supply Input Voltage VCC ---------- 4.5V to 5.5V
Supply Input Voltage PVCC ---------- 4.5V to 5.5V
Supply Input Voltage VIN ---------- 5V to 25V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at $T_A = 25^oC$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

SIMPLIFIED BLOCK DIAGRAM

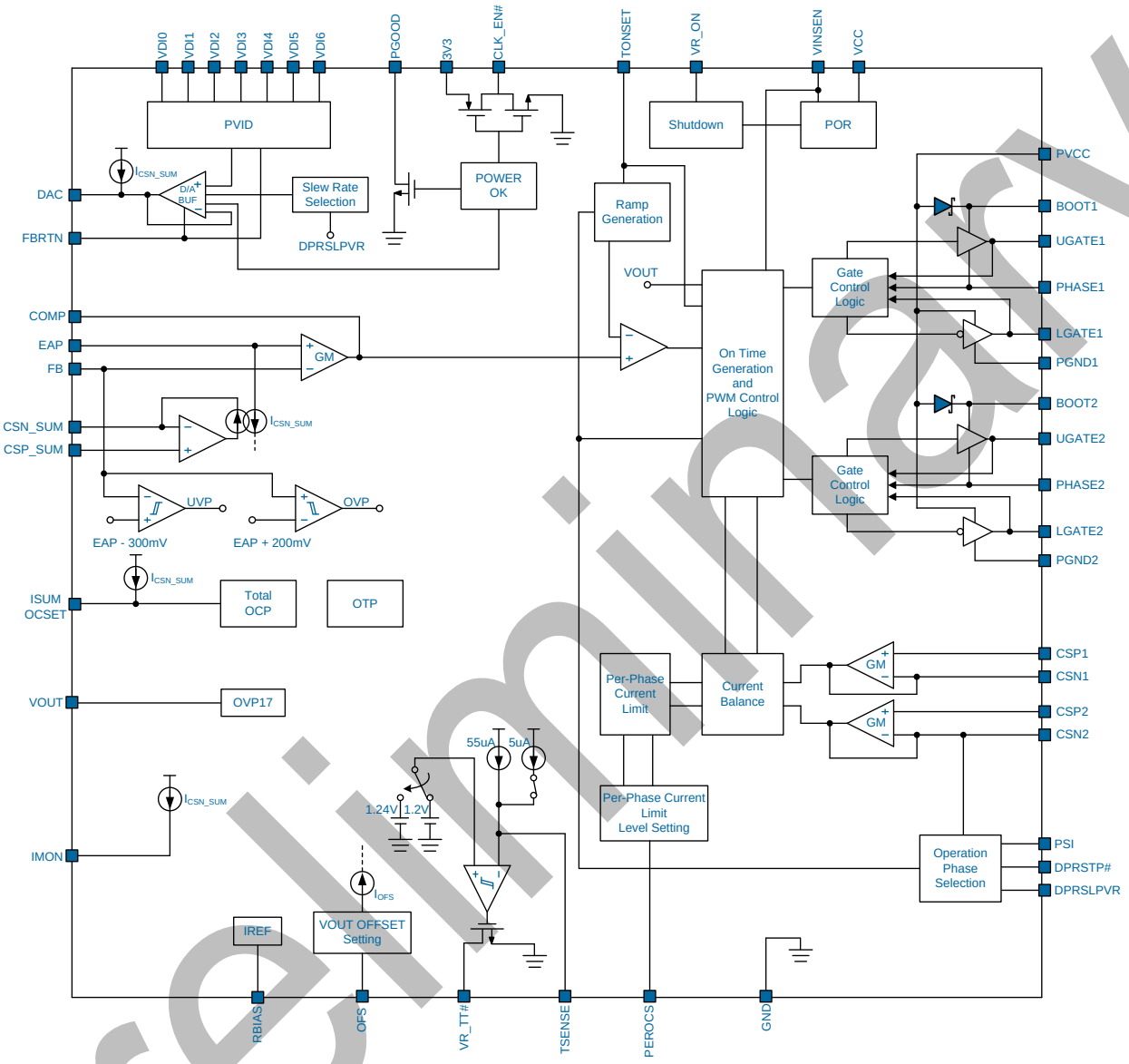


Figure 3. Simplified Block Diagram of PT9528

ELECTRICAL CHARACTERISTICS

(TA=25℃, VCC=5V，unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
5VCC POR Threshold	V_{VCCTH}	VCC Rising	--	4.25	--	V
5VCC POR Hysteresis	V_{VCCHYS}	VCC Rising - VCC Falling	--	0.25	--	V
5VCC Shutdown Current	I_{SHDN}	VR_ON = 0V	--	--	1	uA
5VCC Supply Current	I_{Q5}	VR_ON = 3.3V, No Switching 1-Phase DCM	--	3	--	mA
3.3VCC Supply Current	I_{Q33}	No Load on CLK_EN#	--	--	1	uA
VIN Sense						
VINSEN POR Rising Threshold	V_{VINSEN_PORH}	VINSEN Rising	--	4.5	--	V
VINSEN POR Falling Threshold	V_{VINSEN_PORL}	VINSEN Falling	--	3.75	--	V
VINSEN Supply Current	I_{VINSEN}	VR_ON = 0V, VIN=25V	--	--	1	uA
Logic Input						
VR_ON Input Low	V_{VRON_L}		--	--	1	V
VR_ON Input High	V_{VRON_H}		2.3	--	--	V
Internal Pull-Down Current	I_{VR_ON}	VR_ON = 3.3V	--	22	--	uA
DPRSLPVR Input LOW	V_{SLPVR_OL}		--	--	1	V
DPRSLPVR Input High	V_{SLPVR_OH}		2.3	--	--	V
PSI# Input Low	V_{PSI_OL}		--	--	0.3	V
PSI# Input High	V_{PSI_OH}		0.7	--	--	V
DPRSTP# Input Low	V_{STPB_OL}		--	--	0.3	V
DPRSTP# Input High	V_{STPB_OH}		0.7	--	--	V
VID0~6 Input Low	$V_{VID\ 0\sim6\_OL}$		--	--	0.3	V
VID0~6 Input High	$V_{VID\ 0\sim6\_OH}$		0.7	--	--	V
Soft Start						
Soft-Start Current	I_{SS}		--	40	--	uA
Fast Change VID Current	I_{SRFST}	VIDREF-DAC >100mV	--	±200	--	uA
Soft Deeper Sleep Entry Current	I_{SRSLW}	DPRSLPVR=3.3V	--	-40	--	uA
Soft Deeper Sleep Exit Current	I_{SRSLW_EXIT}	DPRSLPVR=3.3V	--	40	--	uA

Soft Deeper Sleep Exit Current	I_{SRFST_EXIT}	DPRSLPVR=0V	--	200	--	uA
Gate Drivers (UGATE1,UGATE2,LGATE1,LGATE2)						
Upper Gate Source	R_{UG_SRC}	Source Current =80mA, V_{BOOT} – V_{PHASE} = 5V	--	1	2	Ω
Upper Gate Sink	R_{UG_SNK}	Sink Current =80mA, V_{BOOT} – V_{PHASE} = 5V	--	1	2	Ω
Lower Gate Source	R_{LG_SRC}	Source Current =80mA	--	1	2	Ω
Lowe Gate Sink	R_{LG_SNK}	Sink Current = 80mA	--	0.5	1	Ω
Dead Time	T_{DT}		--	30	--	ns
Bootstrap Diode						
Forward Voltage of Bootstrap Diode	V_F	Forward Bias Current = 3.5mA	--	0.4	--	V
PGOOD						
Output Low Voltage of PGOOD	V_{PGD_OL}	Sink Current= 4mA	--	--	0.3	V
Output Leakage Current of PGOOD	I_{PGD_LEAK}	Pull up to 3.3V	--	--	0.1	uA
PGOOD Delay	T_{PGD_Delay}	CLK_EN# Low to PGOOD High	--	7.6	--	ms
CLK_EN#						
CLK_EN# High Output Voltage	$V_{CLKENBD\_OH}$	3V3=3.3V and source current = 4mA	2.9	3.1	--	V
CLK_EN# Low Output Voltage	$V_{CLKENBD\_OL}$	3V3=3.3V and sink current = 4mA	--	0.26	0.4	V
DAC Reference and DAC OTA Voltage						
DAC Voltage Accuracy1		VID=0.75 to 1.5V	-0.5	--	0.5	%
DAC Voltage Accuracy2		VID=0.7375 to 0.5V	-8	--	8	mV
DAC Voltage Accuracy3		VID=0.3 to 0.4875V	-15	--	15	mV
RBIAS PIN Voltage						
R_{BIAS} Voltage	V_{RBIAS}	R_{BIAS}=30kΩ	1.188	1.2	1.212	V
PWM On-Time						
On Time	T_{ON}	VINSEN = 12V, V_{OUT} = 1.2V, R_{TONSET} = 33.3kΩ	--	333	--	ns
Minimum Off Time	T_{OFF_MIN}	1-Phase Operation	--	370	--	ns
Minimum On Time	T_{On_MIN}		--	60	--	ns
Error Amplifier (COMP)						
Offset Voltage	V_{OFS}		-1	--	1	mV
Trans-Conductance	GM		--	2020	--	uA/V
EA Sourcing Current	$I_{SRC,COMP}$		--	320	--	uA

EA Sinking Current	$I_{SNK,COMP}$		--	320	--	uA
Current Sense Amplifier (DCR sensing)						
Offset Voltage	V_{OFS}		-1	--	1	mV
Maximum Sourcing Current	I_{SRC}		100	--	--	uA
Protection						
OVP Threshold	V_{OVP}	V_{FB}-V_{EAP}	--	200	--	mV
OVP Delay Time	T_{OVP_DELAY}		--	1.1	--	ms
UVP Threshold	V_{UVP}	V_{EAP}-V_{FB}	--	300	--	mV
UVP Delay Time	T_{UVP_DELAY}		--	1.1	--	ms
OVP 1.7V Threshold	V_{OVP17}	V_{OUT}>1.7V	--	1.7	--	V
OVP Delay Time	T_{OVP17_DELAY}		--	0.52	--	us
Thermal Shutdown Threshold	T_{OTP}		--	160	--	°C
Total Current OCP Threshold	V_{ISUMOC}	2-Phase Operation	--	2.4	--	V
		1-Phase Operation	--	1.6	--	V
Total Current OCP Delay	T_{ISUMOC_Delay}		--	0.52	--	uS
Per-Phase OC Limit Range	I_{OCLMT}	Measure I_{CSNx}	10	--	80	uA
Thermal Monitor						
TSENSE Source Current	I_{TSENSE}		53	60	67	uA
Over-Temperature Threshold	V_{TSE_VTH}		1.18	1.2	1.22	V
VRTT# low output resistors	R_{VRTTB}			6.5	9	Ω
Current Monitor for Protection						
Current Mirror Accuracy	I_{SUMOC}	R_{BIAS}=30kΩ, I_{SUMOC} to I_{CSN} ratio	95	100	105	%
Current Monitor for Droop						
Current Mirror Accuracy	I_{DROOP}	R_{BIAS}=30kΩ, I_{EAP} to I_{CSN} ratio	95	100	105	%
Current Mirror for Reporting						
Current Mirror Accuracy	I_{MON}	R_{BIAS}=30kΩ, I_{MON} to I_{CSN} ratio	95	100	105	%

OPERATION DESCRIPTION

The PT9528 is a 2/1-phase synchronous rectified Buck controller specifically designed to deliver high quality output voltage for high-performance CPU. It integrates a 7-bit VID that supports Intel IMVP6 tables to set the output voltage between 0.3V and 1.5V.

Power Input and Power On Reset

The PT9528 has three power inputs VCC, PVCC and 3V3. VCC is the 5V supply input for control logic circuit of the controller. RC filter to VCC is required for locally bypassing this supply input. PVCC is the supply power of two integrated 5V MOSFET gate drivers. 3V3 is the 3.3V supply input for CLK_EN# of the controller. VCC has power on reset (POR) function. VINSEN is the power stage input voltage sense pin, and it also has power on reset function. The controller monitors the VINSEN voltage for PWM on-time calculation. VR_ON is the chip enable input pin. Logic high to this pin enable the controller, and logic low to this pin disables the controller .The above three inputs (VCC, VINSEN and VR_ON,) are monitored to determine whether the controller is ready for operation.

Figure shows the power ready detection circuit. The VCC voltage is monitored for power on rest with typically 4.25V threshold at its rising edge. The VINSEN voltage is monitored for power on reset with typically 4.5V threshold at its rising edge. When VCC and VINSEN are all ready, the controller waits for VR_ON to start up. When VR_ON pin is driven above 2.3V, the controller begins its start up sequence. When VR_ON pin is driven below 1V, the controller will be turned off, and it will clear all fault state to prepare to next start up once the controller is re-enabled. Note that only VCC or VR_ON toggle will clear all fault state except for OVP17 (clear only by VCC), VINSEN toggle is not used for clearing fault state. Anytime any one of the three inputs falls below their power on reset level will shutdown the controller.

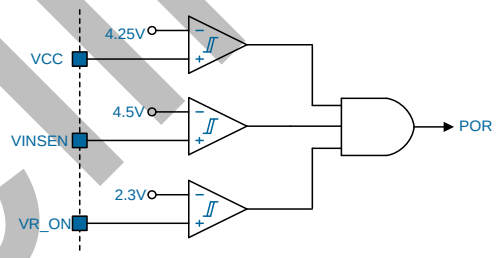


Figure 4. Circuit for Power Ready Detection

Soft Start Timing and Power up Sequence

When VINSEN and VCC inputs are all ready, the controller waits for VR_ON signal to initiate the power-on sequence. After VR_ON goes high, the controller waits for a delay time T_A (approximately 600us) then output voltage starts to ramp up to V_{BOOT}. At soft-start, the regulator always operates in a 2-phase CCM mode, regardless of control signal assertion levels. During this interval, the C_{DAC} where is connected between DAC pin and FBRTN pin is charged by 40μA current source to V_{DAC}. The soft-start ramp will be at 2mV/μs for a ramp up time of 600μs is determined by V_{BOOT} = 1.2V, C_{DAC} = 20nF, I_{DAC} =40uA.
Once output voltage V_{OUT} is settled 90% of the V_{BOOT} voltage for 60μs, then CLK_EN# goes low to indicate that the controller is ready for accepting PVID command. At the same time, the controller waits for a delay time T_B (approximately 8ms), then PGOOD goes high to indicate the start-up sequence is over. Figure shows the typical start up sequence.

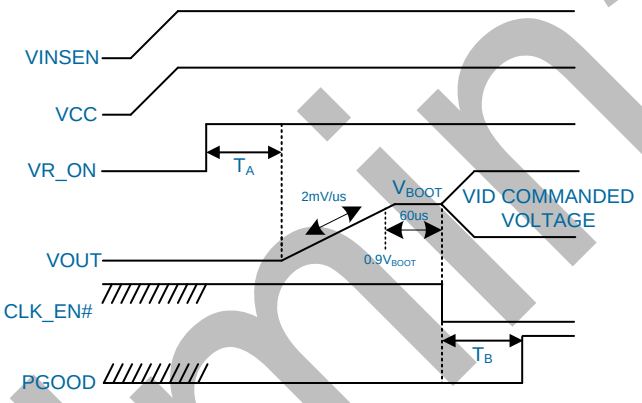


Figure 5. Typical Start up Sequence

PWM On Time Setting

The PWM on-time is set by an external resistor RTON connected between TONSET pin and GND. The controller senses VINSEN voltage to obtain input voltage information for PWM on-time calculation. The PWM on time can be calculated as below equation

$$T_{ON}(ns)=\left(\frac{V_{OUT}}{V_{IN}}\right)\times R_{TON}(k\Omega)\times 100$$

Table 1 lists the switching frequency and the recommended resistor R_{TON} value (with condition: VIN = 12V, VOUT = 1.2V). For example, given V_{IN} = 12V, V_{OUT} = 1.2V, R_{TON} = 33.3kΩ, TON is about 333ns by above equation. The PWM frequency is about 300kHz. Note that the resistance value of R_{TON} value must be greater than 15kΩ to ensure the PWM on-time calculation in normal operation.

Table 1. Switching Frequency and Resistor R_{TON}

Switch Frequency (kHz)	Recommended Resistor R_{TON}(KΩ)
200	49.9
300	33.3
400	24.9
500	20
Note: The Minimum of resistor R_{TON} value is 15kΩ	

Phase Number of Operation (Hardware Programming)

The PT9528 supports 2/1-phase operation. If CSN2 is pulled high to VCC through 1kΩ and CSP2 short to GND, the PT9528 operates at single-phase mode.

Power Saving Mode

The PT9528 has several operating modes to optimize efficiency. The controller's operational modes are designed to work in conjunction with the IMVP6 control signals to maintain the optimal system configuration for all IMVP6 conditions. These operating modes are established by the IMVP6 control signal inputs such as PSI#, DPRSLPVR, and DPRSTP# as shown in Table 2. At high current levels, the system will operate with both phases fully active, responding rapidly to transients and deliver the maximum power to the load. At reduced load-current levels, one of the phases may be idled. This configuration will minimize switching losses, while still maintaining transient response capability. At the lowest current levels, the controller automatically configures the system to operate in single-phase automatic-DCM mode, thus achieving the highest possible efficiency.

Table 2. **Operation Modes and Slew Rate**

DPRSLPVR	DPRSTP#	PSI#	Phase Number	MODE	Slew Rate (mV/us)	CPU MODE
0	1	1	2	CCM	10	Active
0	1	0	1	CCM	10	Active
1	0	1	1	DCM	2	Deeper sleep
1	0	0	1	DCM	2	Deeper sleep
0	0	1	2	CCM	10	Active
0	0	0	1	CCM	10	Active
1	1	1	2	CCM	2	Deeper sleep
1	1	0	1	CCM	2	Deeper sleep

VID Table

The PT9528 supports Intel IMVP6 VID table as shown in Table 3.

Table 3. IMVP6 VID table

VOUT (V)	VID0	VID1	VID2	VID3	VID4	VID5	VID6
1.5000	0	0	0	0	0	0	0
1.4875	1	0	0	0	0	0	0
1.4750	0	1	0	0	0	0	0
1.4625	1	1	0	0	0	0	0
1.4500	0	0	1	0	0	0	0
1.4375	1	0	1	0	0	0	0
1.4250	0	1	1	0	0	0	0
1.4125	1	1	1	0	0	0	0
1.4000	0	0	0	1	0	0	0
1.3875	1	0	0	1	0	0	0
1.3750	0	1	0	1	0	0	0
1.3625	1	1	0	1	0	0	0
1.3500	0	0	1	1	0	0	0

1.3375	1	0	1	1	0	0	0
1.3250	0	1	1	1	0	0	0
1.3125	1	1	1	1	0	0	0
1.3000	0	0	0	0	1	0	0
1.2875	1	0	0	0	1	0	0
1.2750	0	1	0	0	1	0	0
1.2625	1	1	0	0	1	0	0
1.2500	0	0	1	0	1	0	0
1.2375	1	0	1	0	1	0	0
1.2250	0	1	1	0	1	0	0
1.2125	1	1	1	0	1	0	0
1.2000	0	0	0	1	1	0	0
1.1875	1	0	0	1	1	0	0
1.1750	0	1	0	1	1	0	0
1.1625	1	1	0	1	1	0	0
1.1500	0	0	1	1	1	0	0
1.1375	1	0	1	1	1	0	0
1.1250	0	1	1	1	1	0	0
1.1125	1	1	1	1	1	0	0
1.1000	0	0	0	0	0	1	0
1.0875	1	0	0	0	0	1	0
1.0750	0	1	0	0	0	1	0
1.0625	1	1	0	0	0	1	0
1.0500	0	0	1	0	0	1	0
1.0375	1	0	1	0	0	1	0
1.0250	0	1	1	0	0	1	0
1.0125	1	1	1	0	0	1	0
1.0000	0	0	0	1	0	1	0
0.9875	1	0	0	1	0	1	0
0.9750	0	1	0	1	0	1	0
0.9625	1	1	0	1	0	1	0
0.9500	0	0	1	1	0	1	0
0.9375	1	0	1	1	0	1	0
0.9250	0	1	1	1	0	1	0
0.9125	1	1	1	1	0	1	0
0.9000	0	0	0	0	1	1	0
0.8875	1	0	0	0	1	1	0
0.8750	0	1	0	0	1	1	0
0.8625	1	1	0	0	1	1	0

0.8500	0	0	1	0	1	1	0
0.8375	1	0	1	0	1	1	0
0.8250	0	1	1	0	1	1	0
0.8125	1	1	1	0	1	1	0
0.8000	0	0	0	1	1	1	0
0.7875	1	0	0	1	1	1	0
0.7750	0	1	0	1	1	1	0
0.7625	1	1	0	1	1	1	0
0.7500	0	0	1	1	1	1	0
0.7375	1	0	1	1	1	1	0
0.7250	0	1	1	1	1	1	0
0.7125	1	1	1	1	1	1	0
0.7000	0	0	0	0	0	0	1
0.6875	1	0	0	0	0	0	1
0.6750	0	1	0	0	0	0	1
0.6625	1	1	0	0	0	0	1
0.6500	0	0	1	0	0	0	1
0.6375	1	0	1	0	0	0	1
0.6250	0	1	1	0	0	0	1
0.6125	1	1	1	0	0	0	1
0.6000	0	0	0	1	0	0	1
0.5875	1	0	0	1	0	0	1
0.5750	0	1	0	1	0	0	1
0.5625	1	1	0	1	0	0	1
0.5500	0	0	1	1	0	0	1
0.5375	1	0	1	1	0	0	1
0.5250	0	1	1	1	0	0	1
0.5125	1	1	1	1	0	0	1
0.5000	0	0	0	0	1	0	1
0.4875	1	0	0	0	1	0	1
0.4750	0	1	0	0	1	0	1
0.4625	1	1	0	0	1	0	1
0.4500	0	0	1	0	1	0	1
0.4375	1	0	1	0	1	0	1
0.4250	0	1	1	0	1	0	1
0.4125	1	1	1	0	1	0	1
0.4000	0	0	0	1	1	0	1
0.3875	1	0	0	1	1	0	1
0.3750	0	1	0	1	1	0	1

0.3625	1	1	0	1	1	0	1
0.3500	0	0	1	1	1	0	1
0.3375	1	0	1	1	1	0	1
0.3250	0	1	1	1	1	0	1
0.3125	1	1	1	1	1	0	1
0.3000	0	0	0	0	0	1	1
OFF	1	1	1	1	1	1	1

Dynamic VID

The PT9528 can accept VID input changing while the controller is running. This allows the output voltage VOUT to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF may occur under either light or heavy load condition. This change can be positive or negative. During VID OTF, V_{DAC} slew rate can be set by DPRSLPVR pin.

VOUT Offset Voltage

Connect a resistor R_{OFS} from OFS pin to GND to set VOUT offset voltage that is added to the VID setting for voltage margining. Table 4 lists the offset voltage and the recommended resistor R_{OFS} value.

Table 4. Offset Voltage and R_{OFS}

R_{FB}=10kΩ	
R_{OFS} (Ω)	Offset Voltage (mV)
30K	400
37.5K	320
50K	240
75K	160
150K	80
300K	Disable

Output Voltage Differential Sense

The PT9528 uses differential sense by a high-gain low offset error amplifier for output voltage differential sense as show in Figure . The CPU voltage is sensed by the FB pin and FBRTN pins. FB pin is connected to the positive remote sense pin VCC_SENSE of the CPU via the resister R_{FB}, FBRTN pin is connected to the negative remote sense pin VSS_SENSE of CPU directly. The error amplifier compares the V_{FB} with V_{EAP} (= V_{DAC} - I_{CSN_SUM} x R_{DRP}) to regulate the output voltage.

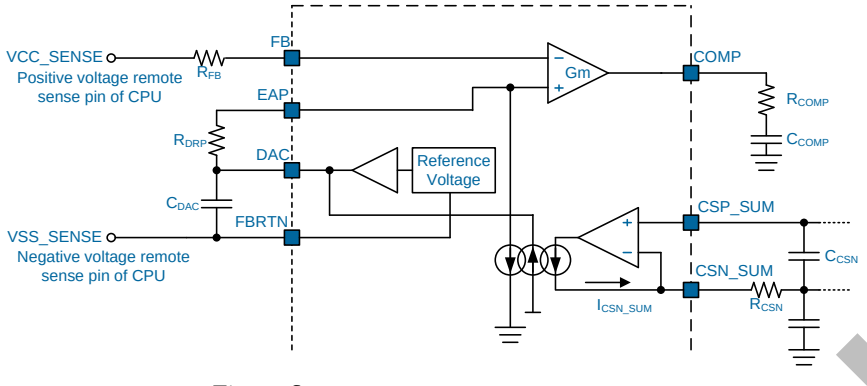


Figure 6. Output Voltage Differential Sense

Total Load Current Sensing

The PT9528 uses a low input offset current sense amplifier (CSA) to sense the total load current flowing through inductors for droop function by CSP_SUM and CSN_SUM as shown in Figure .

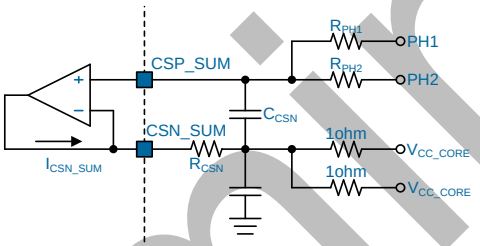


Figure 7. Total Load Current Sense

The voltage across C_{CSN} is proportional to the total load current, and the output current of CSA (I_{CSN_SUM}) is also proportional to the total load current of the voltage regulator. The sensed current I_{CSN_SUM} represents the total output current of the regulator, and it is directly used for droop function, and further internally mirrored for total output over current protection. I_{CSN_SUM} is calculated as follows.

$$I_{CSN\_SUM} = \frac{I_{OUT} \times \frac{R_{DC}}{N}}{R_{CSN}}$$

In this inductor current sensing topology, R_{PH} and C_{CSN} must be selected according to the equation below:

$$k \times \frac{L}{R_{DC}} = \frac{R_{PH} \times C_{CSN}}{N}$$

Where R_{DC} is the DCR of the output inductor L, N is the operation phase number. Theoretically, k should be equal to 1 to sense the instantaneous total load current. But in real application, k is usually between 1.2 to 1.8 for better load transient response. Note that the resistance value of R_{CSN} must be less than 2kΩ to ensure the current sensing circuit in normal operation.

Droop (Load Line) Setting

As shown in Figure , the current I_{CSN_SUM} denotes the sensed total load current, which is mirrored to the EAP pin. When load current increases, I_{CSN_SUM} also increases and creates a voltage drop across R_{DRP}, and makes V_{EAP} lower than the V_{DAC} as follows.

$$V_{EAP} = V_{DAC} - I_{CSN\_SUM} \times R_{DRP} = V_{DAC} - \left(\frac{I_{OUT} \times R_{DC}}{R_{CSN} \times N} \right) \times R_{DRP}$$

Where R_{DC} is the DCR of output inductor, N is the operation phase number, and I_{OUT} denotes the total load current. In steady state, the output voltage is regulated to V_{EAP}. As the total load current I_{OUT} increases, I_{CSN_SUM} increases proportionally, making V_{EAP} decreases linearly as the total output current increases, which is also known as active voltage positioning (AVP). The slope of output voltage decrease over the slope of total load current increase is refereed to as load line. The load line is defined as follows

$$\text{Load Line} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{DC} \times R_{DRP}}{R_{CSN} \times N}$$

Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds V_{EAP} + 200mV sustained 1.1ms, OVP is triggered and latched. The PT9528 will turn off both high/low side MOSFETs. The OVP is latch-off type protection, and it can be reset by VCC or VR_ON toggling.

Absolute Over Voltage Protection (OVP17)

The absolute over voltage protection OVP17 monitors the output voltage via the V_{OUT} pin. The OVP17 is triggered if V_{OUT} > 1.7V sustained 0.52us, OVP17 is triggered and latched. The PT9528 will turn on low side MOSFET and turn off high side MOSFET to protect CPU. The OVP17 is latch-off type protection, and it can only be reset by VCC toggling.

Under Voltage Protection (UVP)

The under voltage protection monitors the output voltage via the FB pin. Once V_{FB} is below V_{EAP} - 300mV sustained 1.1ms,, UVP is triggered and latched. The PT9528 will turn off both high/low side MOSFETs. The UVP is latch-off type protection, and it can be reset by VCC or VR_ON toggling.

Total output over current protection (TOCP)

The PT9528 provides total output over current protection. Connect a resistor (R_{ISUM}) from ISUM pin to GND to set the over current protection threshold. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of ISUM pin, and a resistor from this pin to GND makes the ISUM voltage (V_{ISUM}) proportional to the total output current protection. Please follow Table 5 for the total output over current protection setting.

Table 5. Total Output Over Current Protection Settings

2 Phase (I_{CSN_SUM})	1 Phase (I_{CSN_SUM})	R_{ISUM}
120uA	80uA	20kΩ
100uA	66uA	24kΩ
80uA	53uA	30kΩ
60uA	40uA	40kΩ
40uA	26uA	60kΩ

Over Temperature Protection (OTP)

The PT9528 monitors the temperature of itself. If the temperature exceeds typical 160℃, the PT9528 is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by VCC or VR_ON toggling.

Per-Phase Over Current Limit

In addition to total output OCP, the controller provides channel over current limit to protect the voltage regulator. The current uses DCR current sensing technique to sense the inductor current in each phase for per-phase over current limit. Connect a resistor (R_{PEROCS}) from PEROCS pin to GND to set the per-phase over current limit threshold. Table 6 shows the recommended R_{PEROCS} resistance for per-phase over current limit setting.

Table 6. Per-Phase Over Current Limit Settings

Per-Phase Over current limit (I_{CSNX})	R_{PEROCS}
60uA	50kΩ
50uA	60kΩ
40uA	75kΩ
30uA	100kΩ
20uA	150kΩ

Thermal Monitoring and VR_TT# (Thermal Throttling)

The TSENSE pin is used for voltage regulator thermal monitoring. Connect a negative temperature coefficient (NTC) thermistor network from TSENSE pin to GND to implement this function as shown in Figure . The NTC thermistor is placed close to the hottest point of the regulator, normally close to the inductor and low-side MOSFET of phase 1.

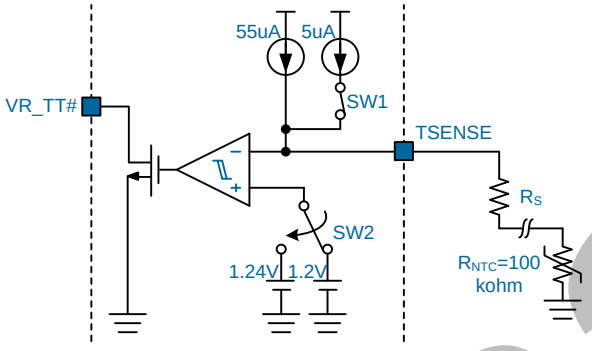


Figure 8. Regulator Temperature Sense

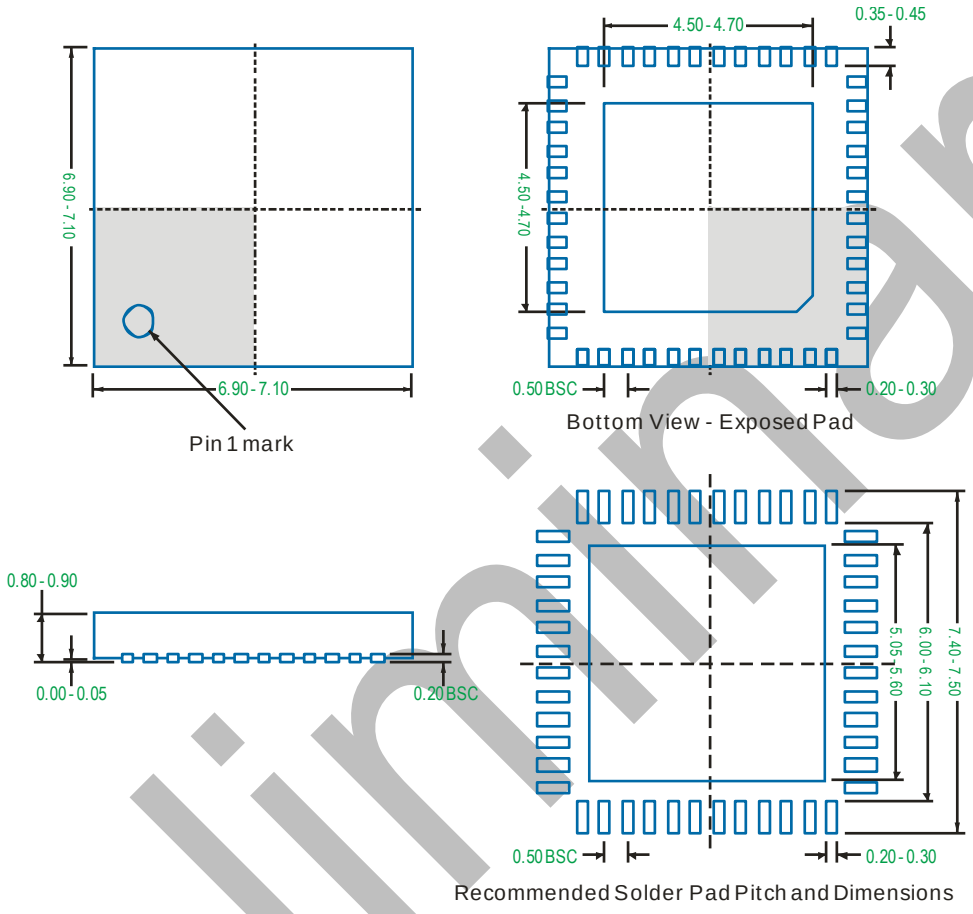
Figure illustrates the implementation of thermal throttling feature with hysteresis. At low temperature, SW1 is on and SW2 connects to the 1.2V side. A precision 60uA current source flows out of the TSENSE pin through the temperature sense network to create a voltage drop V_{TSENSE} on this pin. The V_{TSENSE} is higher than threshold voltage of 1.2V and the comparator output is low. VR_TT# is pulling up high by the external resistor. As regulator temperature rises, the V_{TSENSE} decreases to a level lower than 1.2V. The comparator output change pull low VR_TT# and turns SW1 off and connects SW2 to 1.24V. In this state, 5uA current reduction on TSENSE pin and 40mV voltage increase on threshold voltage of the comparator contribute to the hysteresis.

TYPICAL PERFORMANCE CHARACTERISTICS

T B D ...

PACKAGE INFORMATION

VQFN7x7 - 48L Package



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP. Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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