

MC74VHCT244A

Octal Bus Buffer/Line Driver with 3-State Outputs

The MC74VHCT244A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT244A is a noninverting 3-state buffer, and has two active-low output enables. This device is designed to be used with 3-state memory address drivers, etc.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT244A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage-input/output voltage mismatch, battery backup, hot insertion, etc.

Features

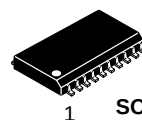
- High Speed: $t_{PD} = 5.6$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 4.0$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 1.1$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- Chip Complexity: 112 FETs or 28 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant



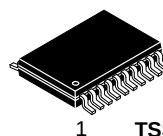
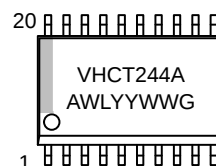
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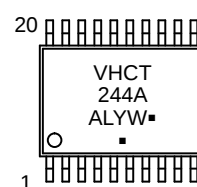
MARKING DIAGRAMS



SOIC-20WB
SUFFIX DW
CASE 751D



TSSOP-20
SUFFIX DT
CASE 948E



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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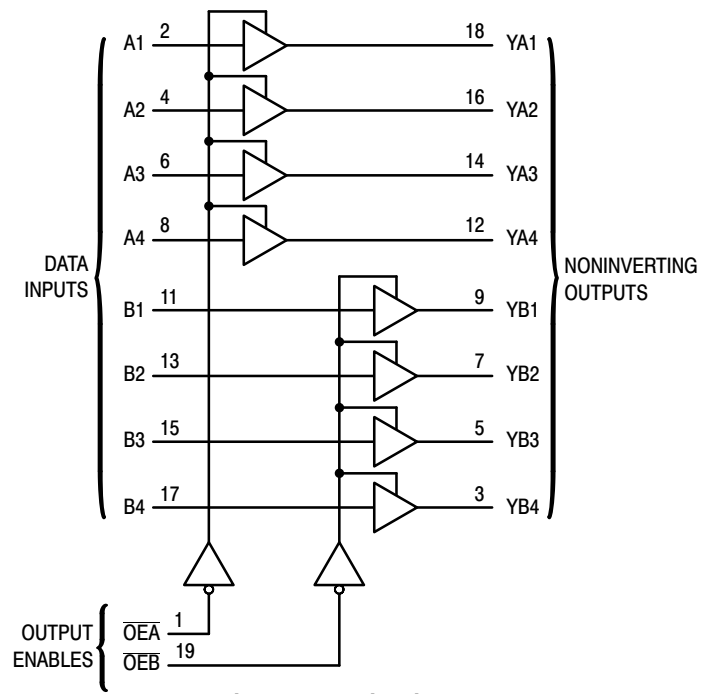


Figure 1. Logic Diagram

$\overline{OEA}$	1 •	20	V_{CC}
A1	2	19	$\overline{OEB}$
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Outputs
$\overline{OEA}, \overline{OEB}$	A, B	YA, YB
L	L L	L L
L	H H	H H
H	X Z	Z Z

Figure 2. Pin Assignment

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	−0.5 to +7.0	V
V _{in}	DC Input Voltage	−0.5 to +7.0	V
V _{out}	DC Output Voltage Output in 3-State High or Low State	−0.5 to +7.0 −0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	−20	mA
I _{OK}	Output Diode Current (V _{OUT} < GND; V _{OUT} > V _{CC})	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	−65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating – SOIC Packages: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	4.5	5.5	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage Output in 3-State High or Low State	0 0	5.5 V _{CC}	V
T _A	Operating Temperature	−40	+125	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 5.0 V ± 0.5 V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = − 40 to 85°C		T _A = 85 to 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{in} = V _{IH} or V _{IL}	I _{OH} = −50 μA	4.5	4.4	4.5		4.4		4.4		V
		I _{OH} = −8 mA	4.5	3.94			3.80		3.66		
V _{OL}	Maximum Low-Level Output Voltage V _{in} = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5		0.0	0.1		0.1		0.1	V
		I _{OL} = 8 mA	4.5			0.36		0.44		0.52	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{OZ}	Maximum 3-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5			±0.25		±2.5		2.5	μA
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			4.0		40.0		40.0	μA
I _{CCT}	Quiescent Supply Current	Per Input: V _{IN} = 3.4 V Other Input: V _{CC} or GND	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0			0.5		5.0		10	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40$ to 85°C		$T_A = 85$ to 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Maximum Propagation Delay A to YA or B to YB	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		5.4 5.9	7.4 8.4	1.0 1.0	8.5 9.5	11.0 1.0	9.5 10.5	ns
t_{PZL} , t_{PZH}	Output Enable Time $\overline{OE}A$ to YA or $\overline{OE}B$ to YB	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $R_L = 1$ k Ω $C_L = 50$ pF		7.7 8.2	10.4 11.4	1.0 1.0	12.0 13.0	1.0 1.0	13.5 14.5	ns
t_{PLZ} , t_{PHZ}	Output Disable Time $\overline{OE}A$ to YA or $\overline{OE}B$ to YB	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF $R_L = 1$ k Ω		8.8	11.4	1.0	13.0	1.0	14.5	ns
t_{OSLH} , t_{OSHL}	Output to Output Skew	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF (Note 1)			1.0		1.0		1.0	ns

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Typical @ 25°C , $V_{CC} = 5.0$ V			Unit
		Min	Typ	Max	
C_{PD}	Power Dissipation Capacitance (Note 2)		18		pF
C_{in}	Maximum Input Capacitance		4	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)		9		pF

- Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
- C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.1	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.9	-1.1	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74VHCT244ADWRG	SOIC-20WB (Pb-Free)	1000 / Tape & Reel
MC74VHCT244ADTG	TSSOP-20 (Pb-Free)	75 Units / Rail
MC74VHCT244ADTRG		2500 / Tape & Reel
NLV74VHCT244ADTRG*		2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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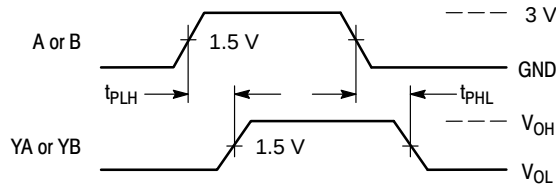


Figure 3. Switching Waveform

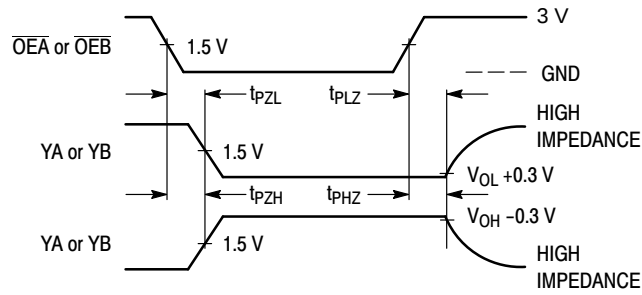
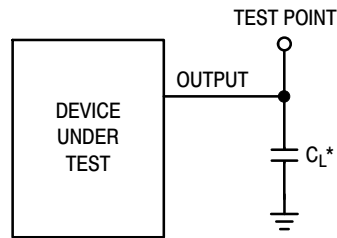
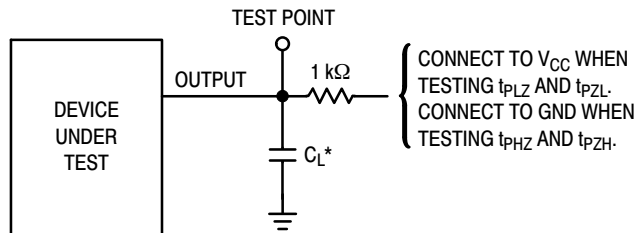


Figure 4. Switching Waveform



*Includes all probe and jig capacitance

Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

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