

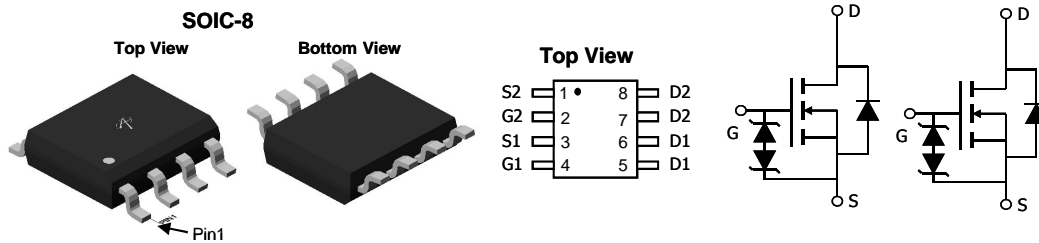
General Description

The AO4822A uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	8A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	<19m Ω
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 26m Ω

ESD Protected
 100% UIS Tested
 100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A=25^\circ C$	8
		$T_A=70^\circ C$	6.5
Pulsed Drain Current ^C	I_{DM}	48	A
Avalanche Current ^C	I_{AS}, I_{AR}	19	A
Avalanche energy $L=0.1mH$ ^C	E_{AS}, E_{AR}	18	mJ
Power Dissipation ^B	P_D	$T_A=25^\circ C$	2
		$T_A=70^\circ C$	1.3
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^{A D}		Steady-State	74	90
Maximum Junction-to-Lead	$R_{\theta JL}$	32	40	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.8	2.4	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	48			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =8A T _J =125°C		15.5 21	19 25	mΩ
		V _{GS} =4.5V, I _D =6A		18.5	26	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =8A		30		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	600	740	888	pF
C _{oss}	Output Capacitance		77	110	145	pF
C _{riss}	Reverse Transfer Capacitance		50	82	115	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.5	1.1	1.7	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =8A	12	15	18	nC
Q _{g(4.5V)}	Total Gate Charge		6	7.5	9	nC
Q _{gs}	Gate Source Charge		2	2.5	3	nC
Q _{gd}	Gate Drain Charge		2	3	5	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.8Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			3.5		ns
t _{D(off)}	Turn-Off DelayTime			19		ns
t _f	Turn-Off Fall Time			3.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =8A, di/dt=500A/μs	6	8	10	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =8A, di/dt=500A/μs	14	18	22	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

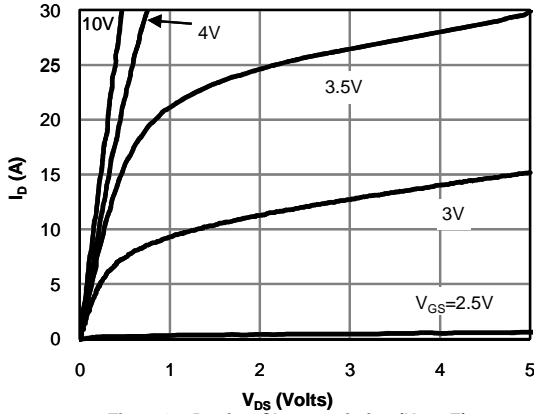


Figure 1: On-Region Characteristics (Note E)

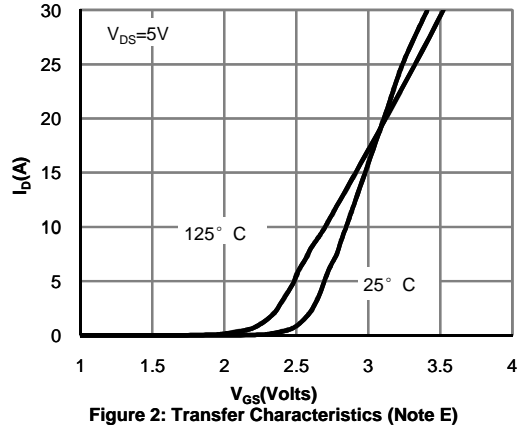


Figure 2: Transfer Characteristics (Note E)

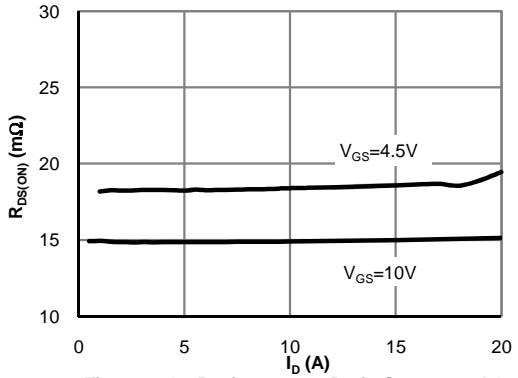


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

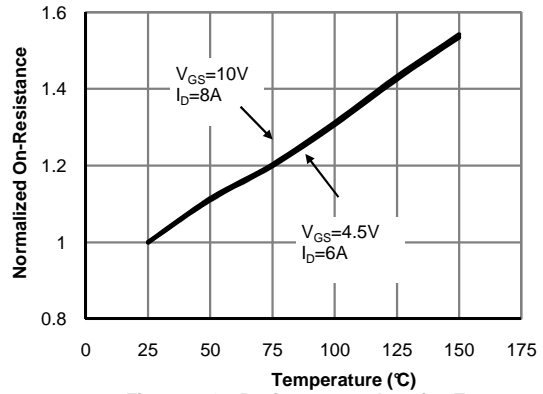


Figure 4: On-Resistance vs. Junction Temperature (Note E)

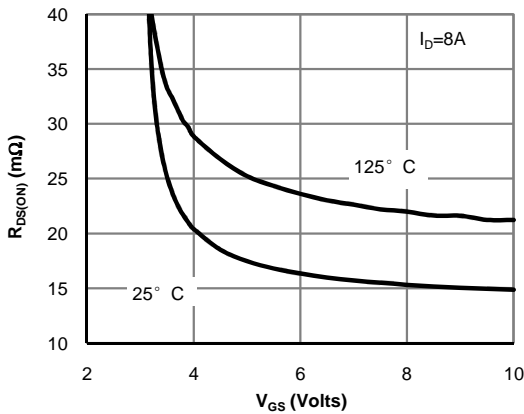


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

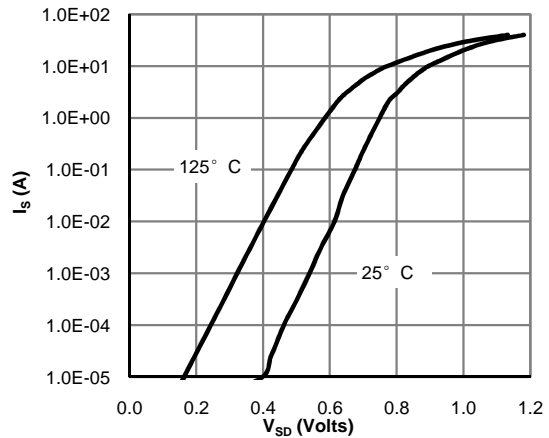


Figure 6: Body-Diode Characteristics (Note E)

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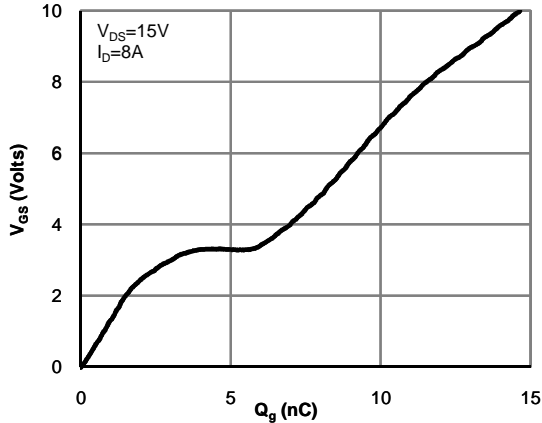


Figure 7: Gate-Charge Characteristics

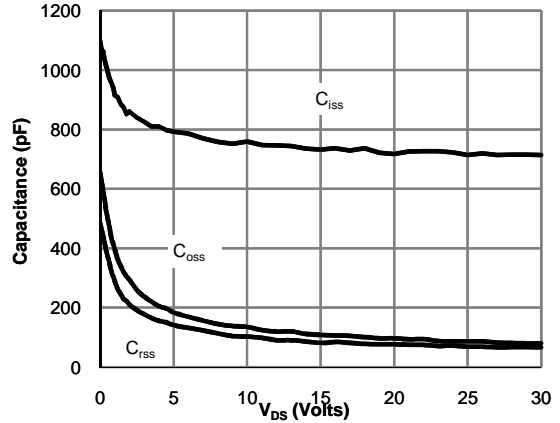


Figure 8: Capacitance Characteristics

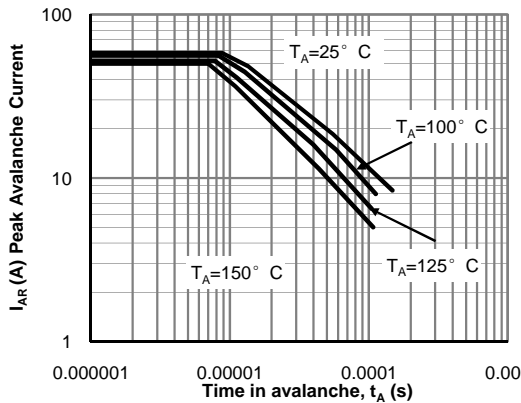


Figure 9: Single Pulse Avalanche capability (Note C)

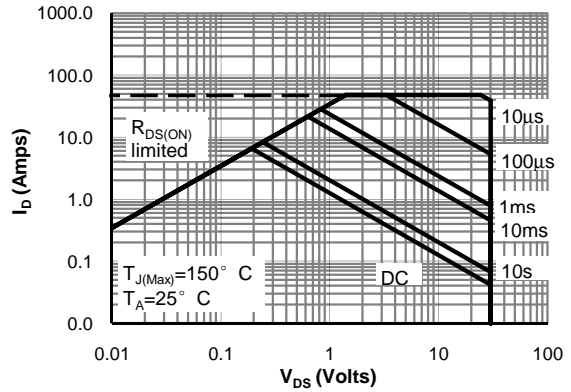


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

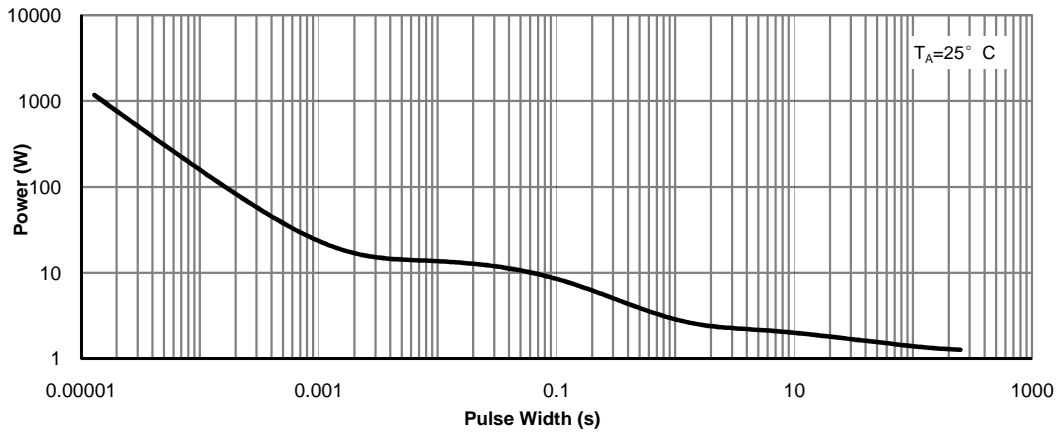


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

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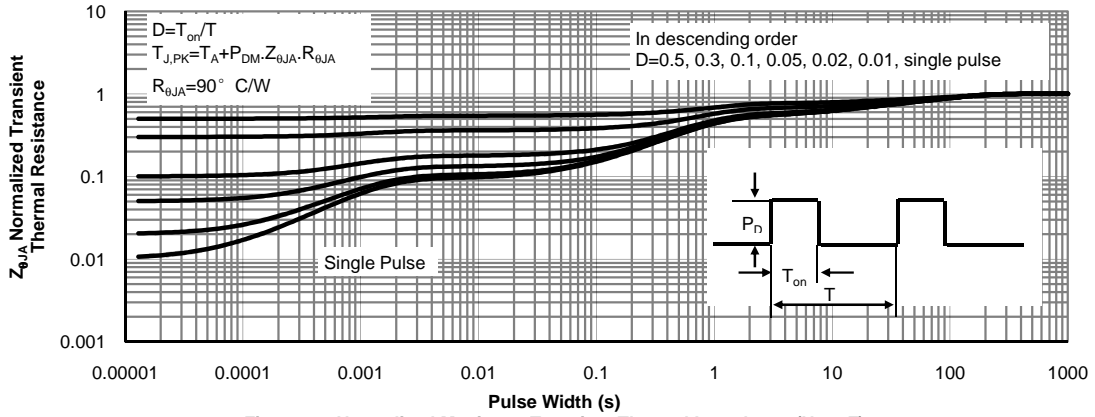
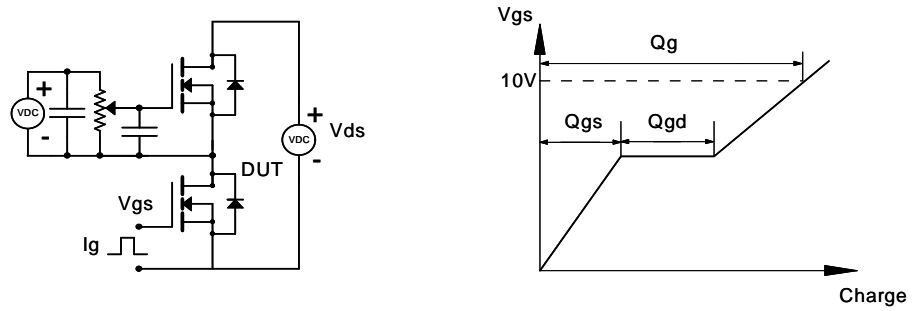
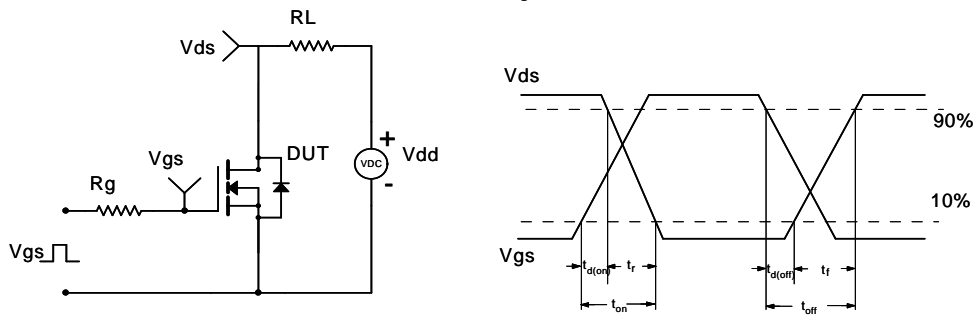


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

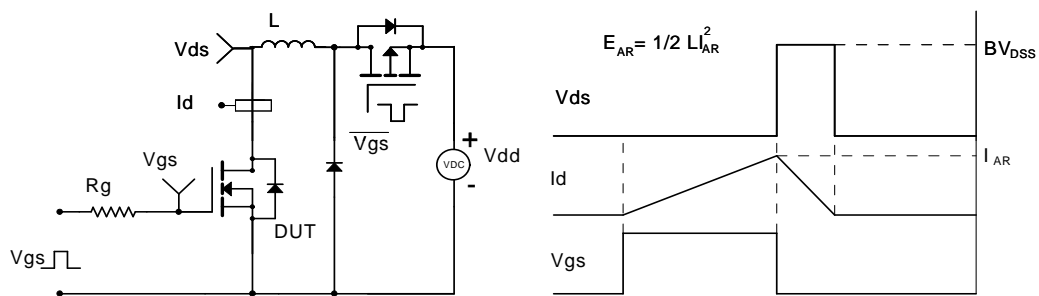
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

