

N-channel 650 V, 0.335 Ω typ., 10 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data

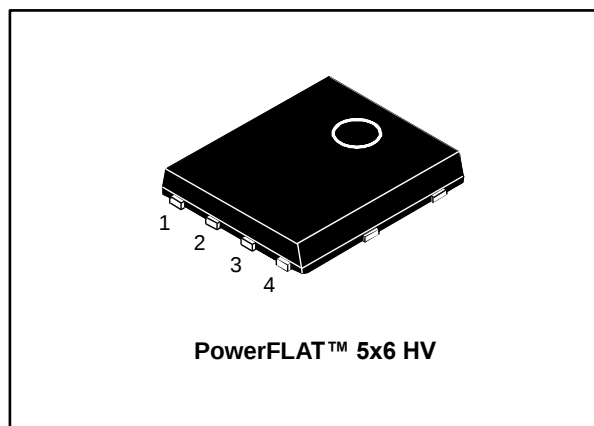
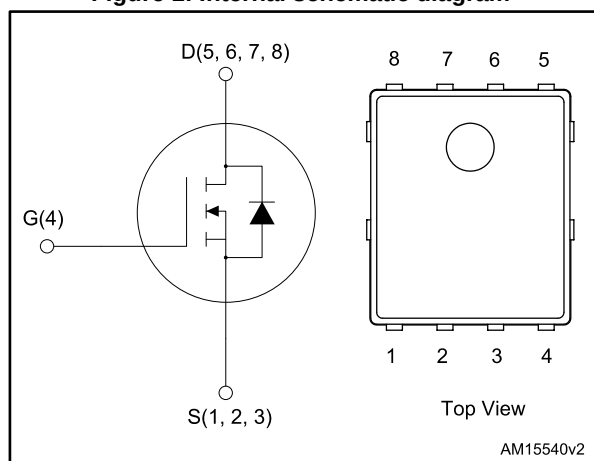


Figure 1: Internal schematic diagram



Features

Order code	$V_{DS} @ T_J \text{ max.}$	$R_{DS(on)} \text{ max}$	I_D
STL15N65M5	710 V	0.375 Ω	10 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL15N65M5	15N65M5	PowerFLAT™ 5x6 HV	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	10	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	52	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	160	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} \leq 10\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} \leq V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case	2.4	$^{\circ}\text{C}/\text{W}$
$R_{thj\text{-pcb}}^{(1)}$	Thermal resistance junction-pcb	59	$^{\circ}\text{C}/\text{W}$

Notes:

⁽¹⁾When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	650			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 650 V			1	μA
		V _{DS} = 650 V, T _C = 125 °C ⁽¹⁾ , V _{GS} = 0 V			100	μA
I _{GSS}	Gate-body leakage current	V _{GS} = ± 25 V, V _{DS} = 0			± 100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 5 A		0.335	0.375	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	816	-	pF
C _{oss}	Output capacitance		-	23	-	pF
C _{rss}	Reverse transfer capacitance		-	2.6	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 520 V, V _{GS} = 0 V	-	70	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	21	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	5	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 5.5 A, V _{GS} = 10 V (see Figure 16: "Test circuit for gate charge behavior")	-	22	-	nC
Q _{gs}	Gate-source charge		-	5.5	-	nC
Q _{gd}	Gate-drain charge		-	11	-	nC

Notes:

⁽¹⁾C_{oss} eq. time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80 % V_{DSS}.

⁽²⁾C_{oss} eq. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80 % V_{DSS}.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 7\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times" and Figure 20: "Switching time waveform")	-	30	-	ns
$t_{r(V)}$	Voltage rise time		-	8	-	ns
$t_{f(I)}$	Current fall time		-	11	-	ns
$t_{c(off)}$	Crossing time		-	12.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 10\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	244		ns
Q_{rr}	Reverse recovery charge		-	2.35		μC
I_{RRM}	Reverse recovery current		-	19.2		A
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	308		ns
Q_{rr}	Reverse recovery charge		-	2.93		μC
I_{RRM}	Reverse recovery current		-	19		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

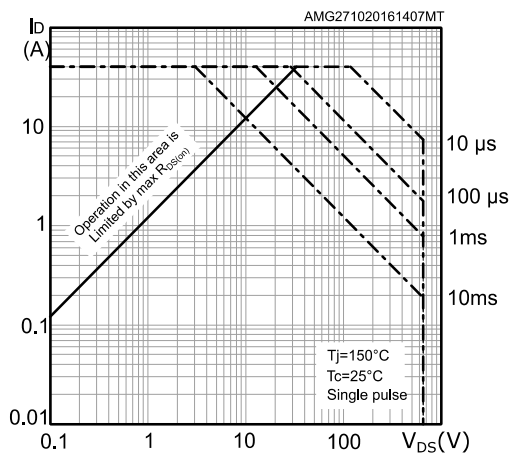


Figure 3: Thermal impedance

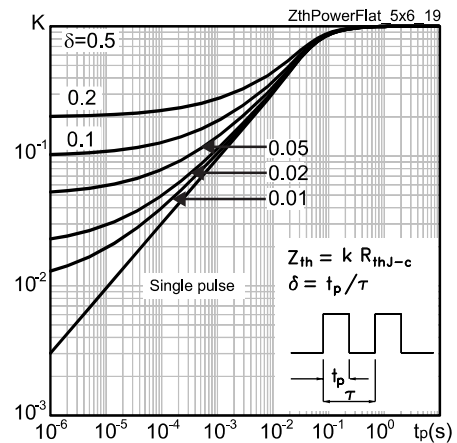


Figure 4: Output characteristics

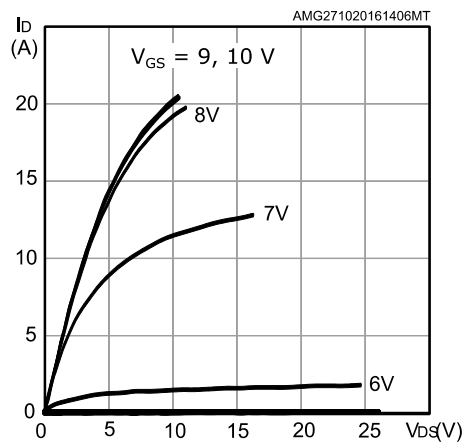


Figure 5: Transfer characteristics

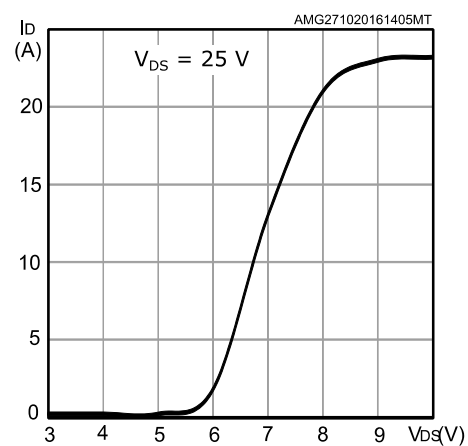


Figure 6: Static drain-source on-resistance

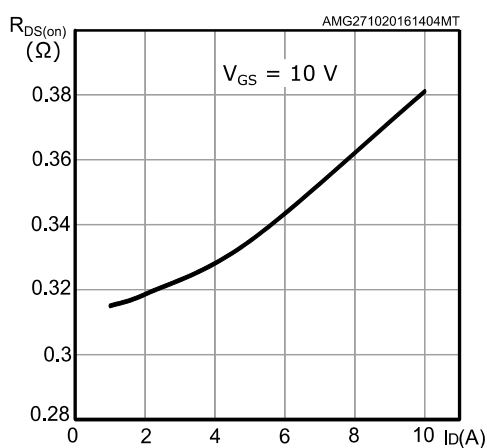


Figure 7: Gate charge vs gate-source voltage

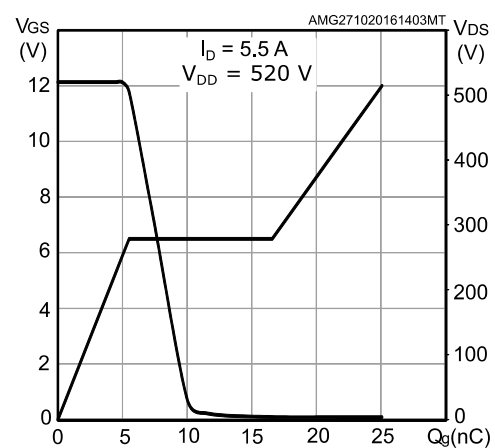


Figure 8: Capacitance variations

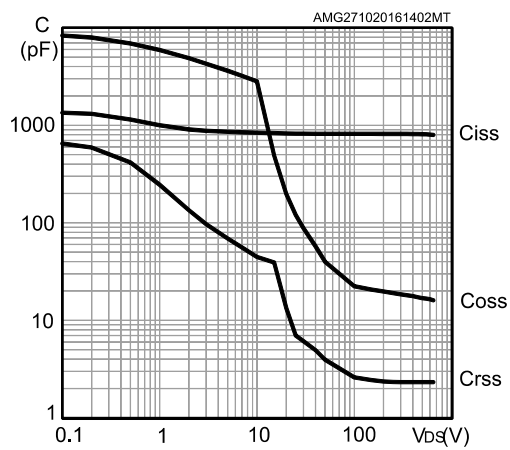


Figure 9: Output capacitance stored energy

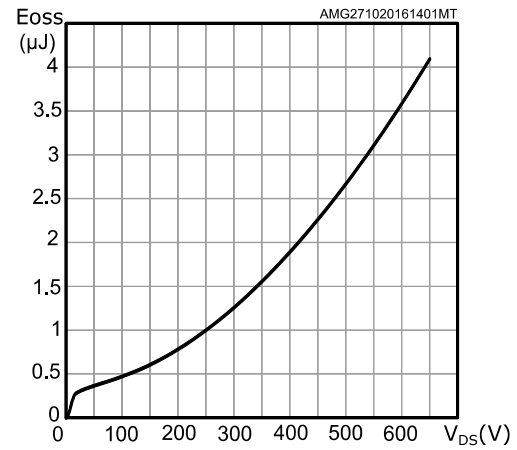


Figure 10: Normalized gate threshold voltage vs temperature

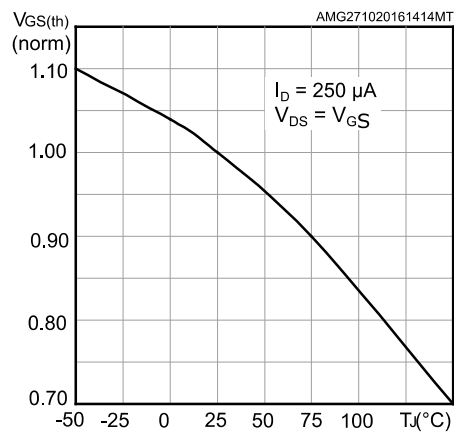


Figure 11: Normalized on-resistance vs temperature

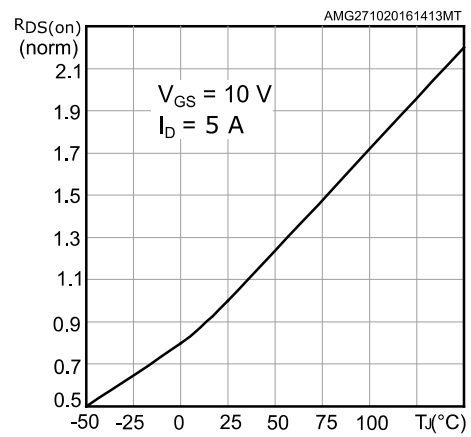


Figure 12: Source-drain diode forward characteristics

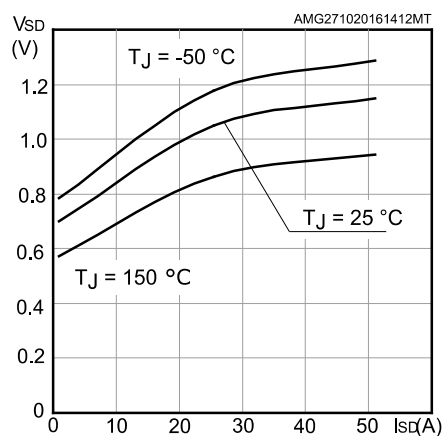
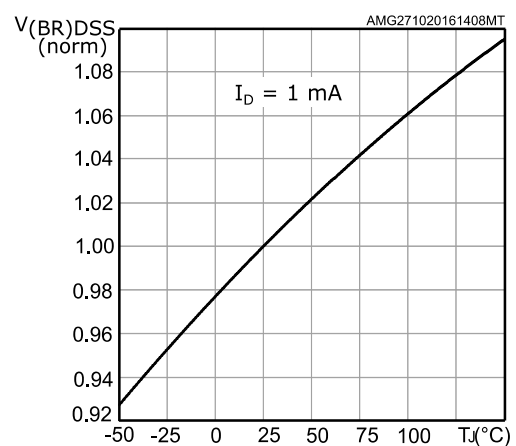
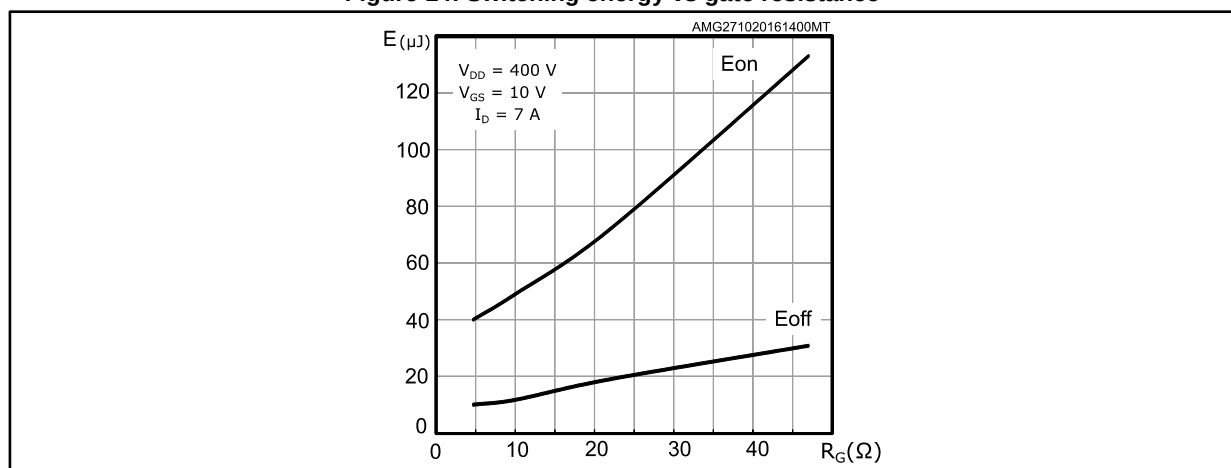
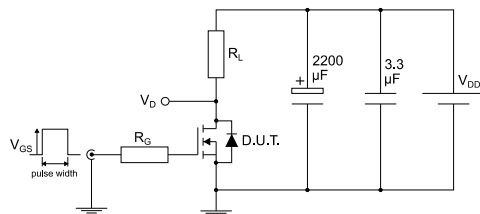
Figure 13: Normalized $V_{(BR)DSS}$ vs temperature

Figure 14: Switching energy vs gate resistance⁽¹⁾**Notes:**

⁽¹⁾ E_{on} including reverse recovery of a SiC diode.

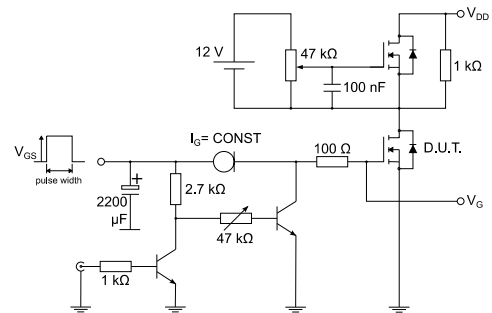
3 Test circuits

Figure 15: Test circuit for resistive load switching times



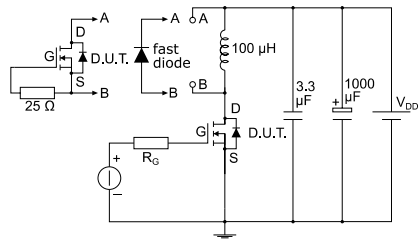
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Figure 16: Test circuit for gate charge behavior



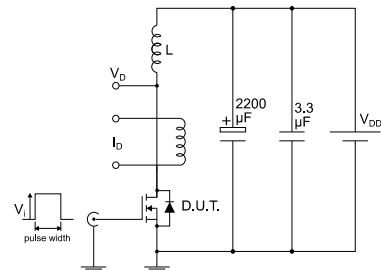
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Figure 17: Test circuit for inductive load switching and diode recovery times



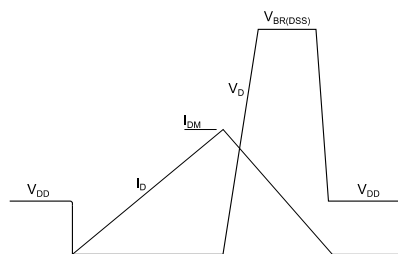
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Figure 18: Unclamped inductive load test circuit



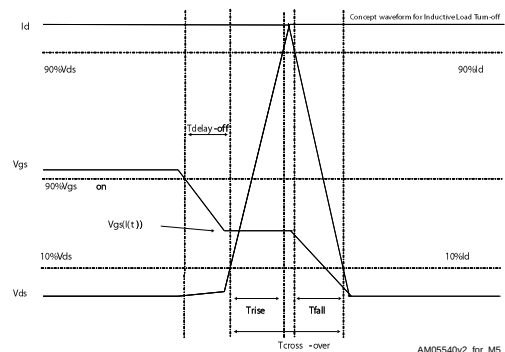
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Figure 19: Unclamped inductive waveform



AM01472v1

Figure 20: Switching time waveform



AM05540v2_for_M5

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 Power Flat™ 5x6 HV package information

Figure 21: PowerFLAT™ 5x6 HV package outline

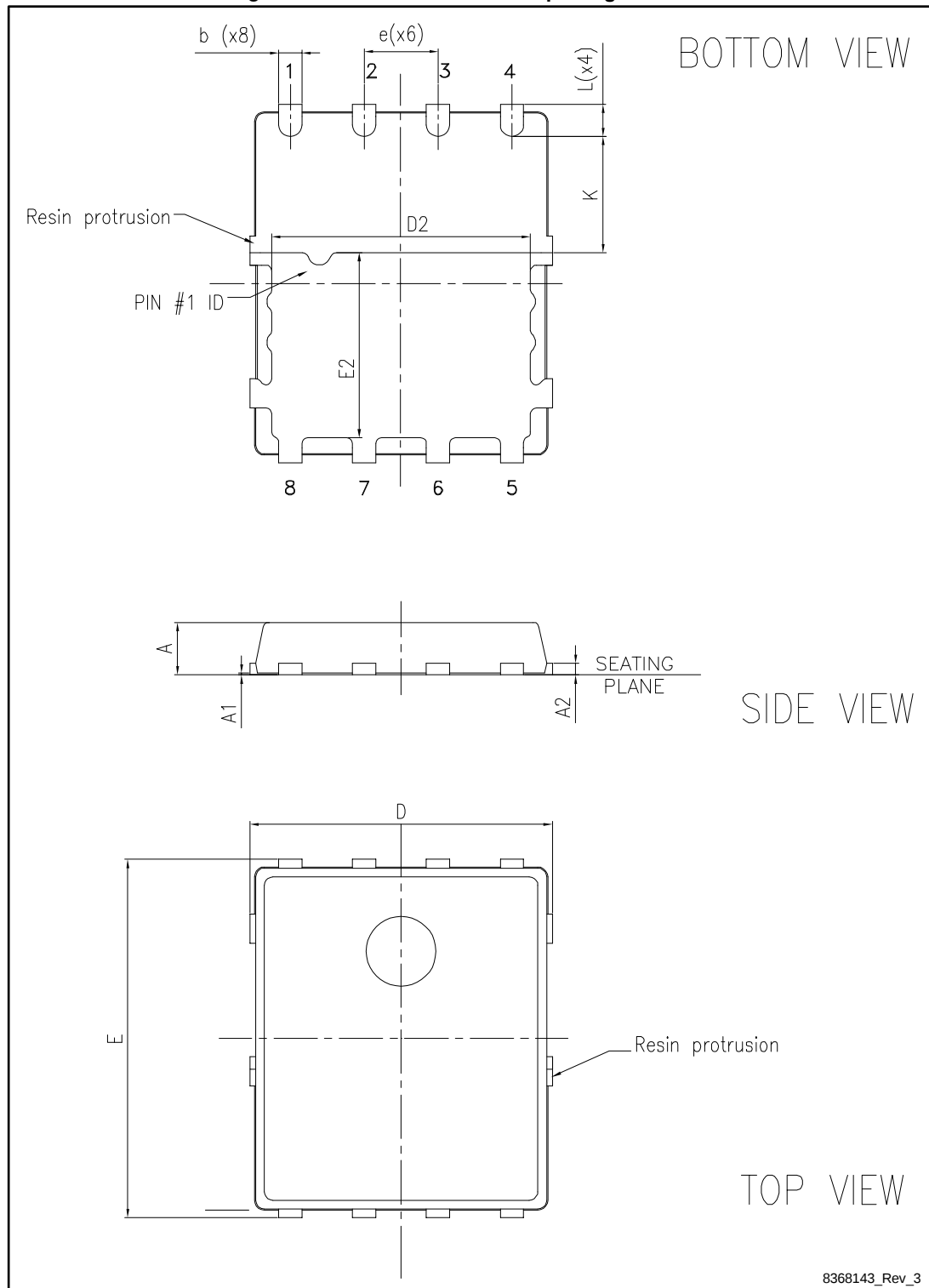
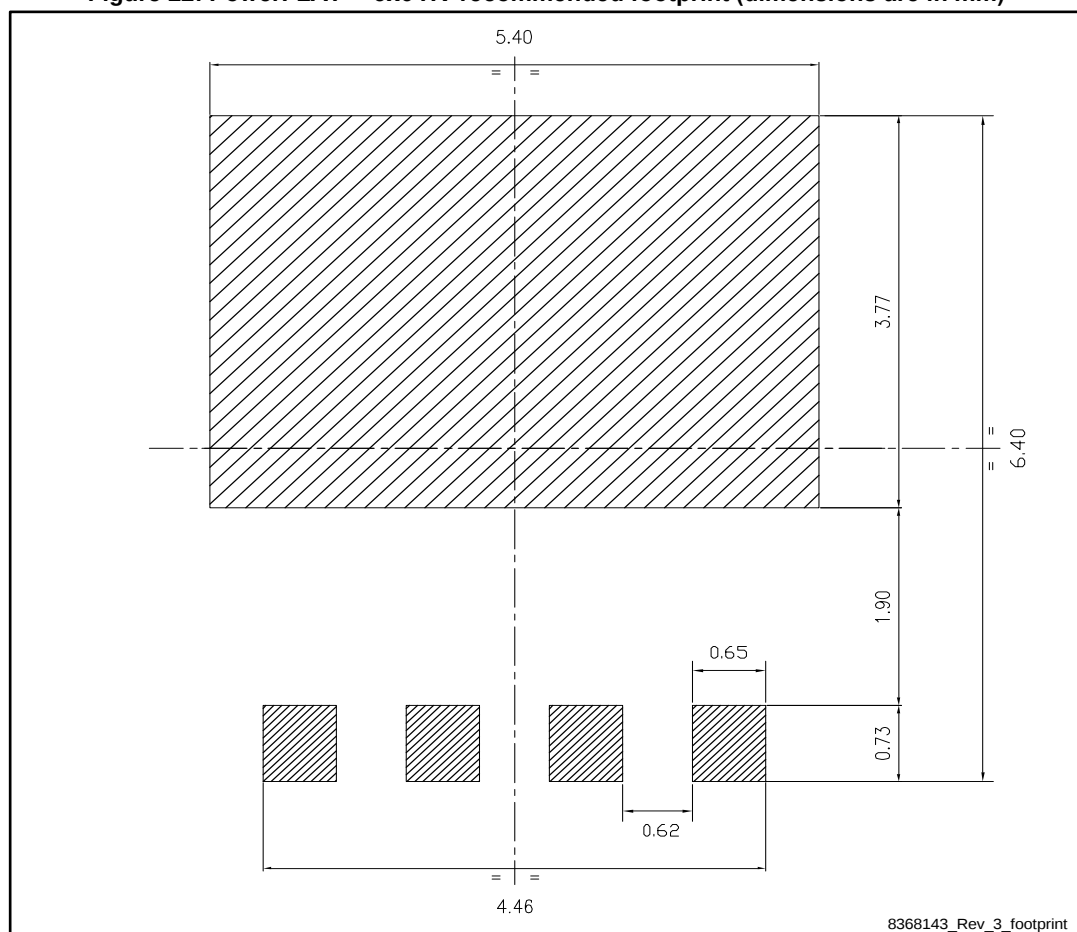


Table 8: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 22: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 Power Flat™ 5x6 HV packing information

Figure 23: PowerFLAT™ 5x6 tape (dimensions are in mm)

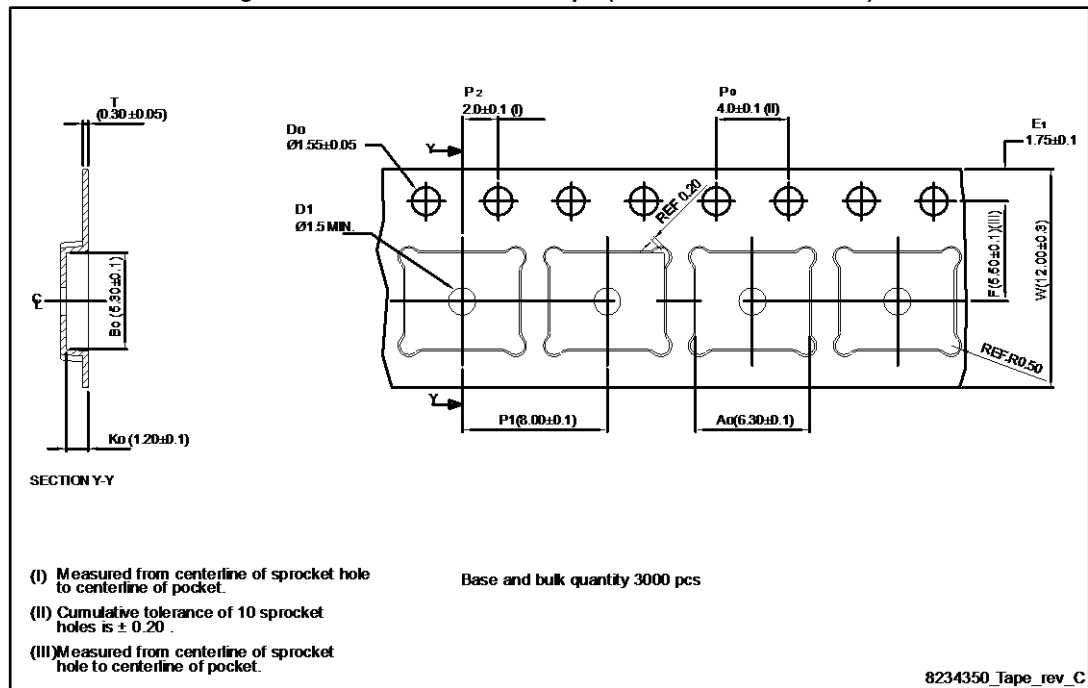


Figure 24: PowerFLAT™ 5x6 package orientation in carrier tape

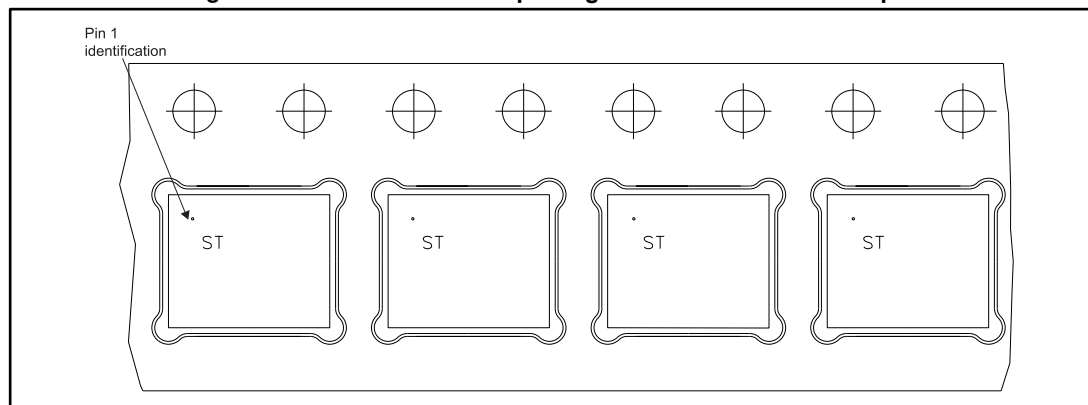
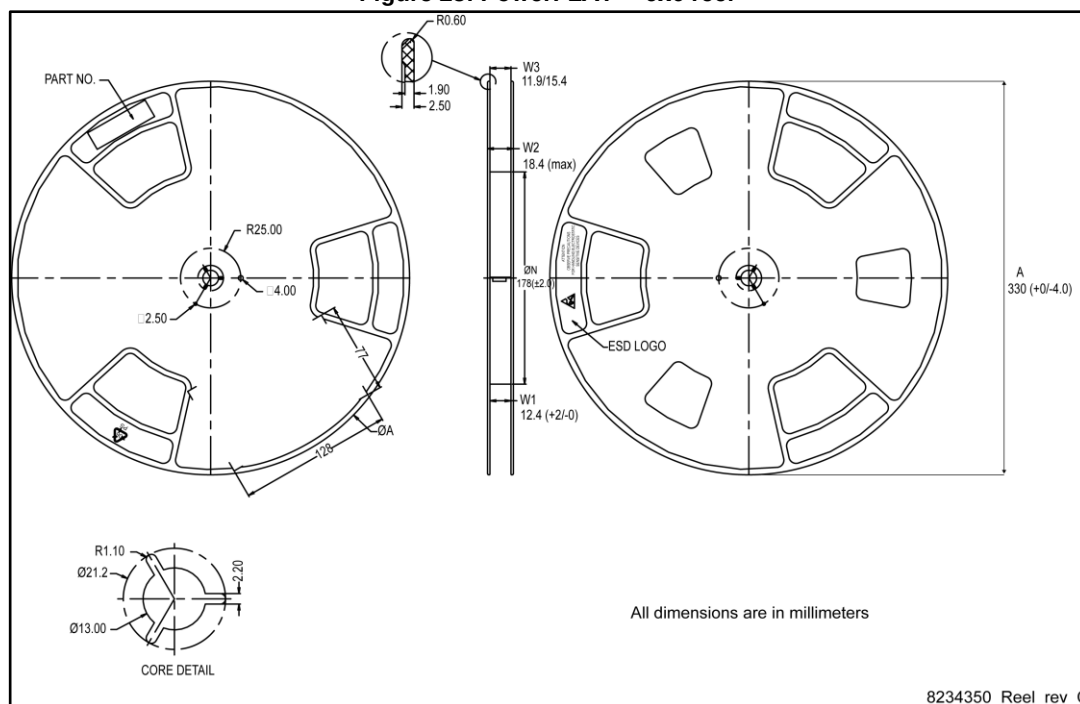


Figure 25: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Jun-2013	1	First release
05-Dec-2016	2	Updated title, features and description in cover page. Updated Figure 1: "Internal schematic diagram" , Table 2: "Absolute maximum ratings" and Section 4: "Package information" . Minor text changes.

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