

FEATURES

Pin to pin compatible with popular High-Speed optocouplers
 High data rates 10Mbps
 High common-mode transient immunity: 50kV/μs typical
 High robustness to radiated and conducted noise
 Diode emulator input
 4.5V-26.4V open collector output
 Propagation delay 65ns

3750Vrms/5000Vrms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

DIN V VDE V 0884-11:2017-01

$V_{ORM} = 1200V$ peak

Wide temperature range: -40°C to 125°C

RoHS-compliant, DIP-8/NB SOIC-8 package

APPLICATIONS

General-purpose isolation
 Industrial field bus isolation
 Motor controls and drives
 EV traction inverters

FUNCTIONAL BLOCK DIAGRAMS

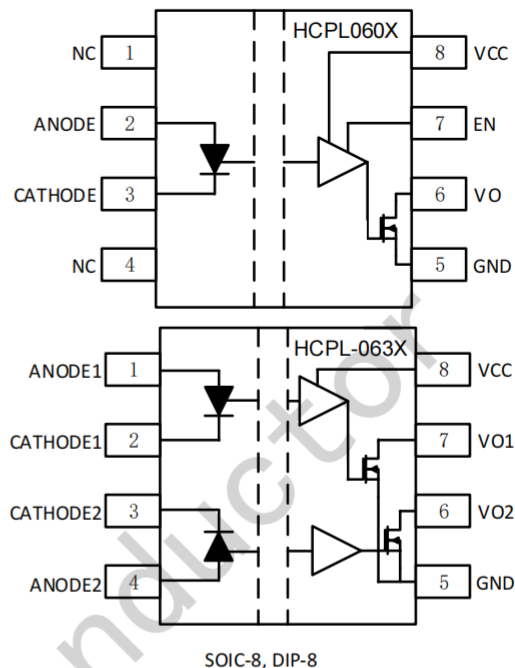


Figure1. HCPL060X/HCPL-063XXX
 functional Block Diagram

SELECTION GUIDE

Table 1. Selection guide

Model Name ¹	Temperature Range	No. of channels	Data rate (Mbps)	Isolation Rating (kV rms)	Package
HCPL0602R2	-40~125°C	1	1	3750	NB SOIC-8
HCPL0601R2	-40~125°C	1	10	3750	NB SOIC-8
HCPL-0630-400E	-40~125°C	2	1	3750	NB SOIC-8
HCPL-0630-500E	-40~125°C	2	10	3750	NB SOIC-8
HCPL0602R3	-40~125°C	1	1	5000	DIP-8
HCPL0601R3	-40~125°C	1	10	5000	DIP-8
HCPL-0630-400C	-40~125°C	2	1	5000	DIP-8
HCPL-0630-500C	-40~125°C	2	10	5000	DIP-8

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2. Absolute Maximum Ratings

Parameter	Rating
INPUT	
Average forward current (I_F)	20mA
Reverse input voltage (V_R)	5 V (min)
Enable input voltage (V_E)	VDD+ 0.5 V
Input Power Dissipation (P_I)	90mW
OUTPUT	
Supply voltage (VDD)	27V
Output sink current (I_{SINK})	50mA
Output voltage (V_O)	27V
Output power dissipation (P_{diss})	50mW
ISOLATOR	
Total Power Dissipation (P_T)	140mW
HBM Rating ESD	$\pm 4\text{KV}$
Maximum Isolation Voltage DIP-8	5000V _{RMS}
Maximum Isolation Voltage SO-8	3750V _{RMS}
Storage Temperature (T_{STG})	-65°C to +150°C
Operating Temperature (T_A)	-40°C to +125°C
Junction Temperature (T_J)	+150°C

RECOMMENDED OPERATING CONDITIONS

Table 3. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5		26.4	V
Input Current, low level each channel	$I_{F(OFF)}$	0		250	μA
Input Current, high level each channel	$I_{F(ON)}$	3		15	mA
Enable Voltage, Low Level	V_{EL}	0		0.8	V
Enable Voltage, High Level	V_{EH}	2		V_{DD}	V
Output Pull-up Resistor	RL	330		4k	Ω

Ambient Operating Temperature	T _A	-40	125	°C
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Truth Tables

Table 4. HCPL060X/HCP-063XXXX Truth Table ¹

Input	V _{DD}	EN	VO ²
OFF	> UVLO	H	HIGH
OFF	> UVLO	L	HIGH
OFF	< UVLO	H	HIGH
OFF	< UVLO	L	HIGH
ON	> UVLO	H	LOW
ON	> UVLO	L	HIGH
ON	< UVLO	H	HIGH
ON	< UVLO	L	HIGH

Notes:

¹ The output voltage level is determined by the external pull-up supply.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 5. DC Specifications

V_{CC} = 5 V; GND = 0 V; T_A = -40 to +125 °C; typical specs at 25°C; unless otherwise noted.

Parameter	Symbol	Device	Min	Typ	Max	Unit	Test Conditions/Comments
Supply Voltage	V _{CC}		4.5		26.4	V	
Supply Current	I _{CC}	Single		0.7	2	mA	
		Dual		1.4	4		
Input Current Threshold	I _{F(TH)}			2.0	3	mA	
Input Forward Voltage (OFF)	V _{F(OFF)}			1.5	1.7	V	
Input Forward Voltage (ON)	V _{F(ON)}		1.8	2	2.2	V	
Logic Low Output Voltage	V _{OL}			0.25	0.6	V	V _{CC} = 5.5 V, I _F = 5 mA, I _{OL} (Sinking) = 13 mA
Logic High Output Current	I _{OH}				0.5	μA	
Peak Output Current	I _{OPK}			50		mA	
Enable High Min	V _{EH}	Single	2		V _{CC}	V	
Enable Low Max	V _{EL}	Single			0.8	V	
Enable High Current Draw	I _{EH}	Single		10		μA	
Enable Low Current Draw	I _{EL}	single		-100		μA	

Table 6. Switching Specifications

V_{DC} = 5 V; GND = 0 V; R_L = 350 Ω ; C_L = 30 pF; T_A = -40 to +125 °C; typical specs at 25 °C; T_J = -40 to +125 °C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Maximum Data Rate	HCPL06XX/500X F _{DATA}			10	Mbps	Within pulse width distortion (PWD) limit
	HCPL06XX/400X F _{DATA}			1	Mbps	Within pulse width distortion (PWD) limit
Minimum Pulse Width	MPW	50			ns	Within PWD limit
Propagation Delay (Low-to-High)	t _{PLH}		40	60	ns	The different time between 50% input signal to 50% output signal 50% @ 5V _{DC} supply
Propagation Delay (High-to-Low)	t _{PHL}		40	60	ns	@ 5V _{DC} supply
Pulse Width Distortion	PWD		8	30	ns	The max different time between t _{PHL} and t _{PLH} @ 5V _{DC} supply. And The value is t _{PHL} - t _{PLH}
Propagation Delay Skew	t _{PSK(p-p)}			45	ns	@ 5V _{DC} supply
Rise Time	t _R		25	40	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V _{DC} supply
Fall Time	t _F		5	10	ns	@ 5V _{DC} supply
Device Startup Time	t _{START}		13	25	μ s	The max amount propagation delay time differs between any two output channels in the single device @ 5V _{DC} supply.
Propagation Delay Time of Enable from VEH to VEL	t _{ELH}		9	30	ns	VDD = 5 V, R _L = 350 Ω , C _L = 30 pF
Propagation Delay Time of Enable from VEL to VEH	t _{EHL}		13	30	ns	VDD = 5 V, R _L = 350 Ω , C _L = 30 pF
Common Mode Transient Immunity	CMTI	50			kV/ μ s	@ 5V _{DC} supply

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 7. Insulation Specifications

Parameter	Symbol	DIP-8	NB SOIC-8	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	3750	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	≥ 7.1	≥ 4	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	≥ 7.4	≥ 4	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		≥ 21	≥ 21	μ m min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II	II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 8. Package Characteristics

Parameter	Symbol	Typical Value		Unit	Test Conditions/Comments
		DIP-8	NB SOIC-8		
Resistance (Input to Output) ¹	R _{I-O}	10 ¹¹	10 ¹¹	Ω	
Capacitance (Input to Output) ¹	C _{I-O}	0.6	0.6	pF	@1MHz
Input Capacitance ²	C _I	3	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ _{JA}	100	45	°C/W	Thermocouple located at center of package underside

Notes:

¹The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4 (DIP-8 Pin 1-Pin4) are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8 (DIP-8 Pin 5-Pin8) are shorted together as the other terminal.

²Testing from the input signal pin to ground.

REGULATORY INFORMATION

See Table 9 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 9. Regulatory

Regulatory	DIP-8	NB SOIC-8
UL	Recognized under UL 1577	Recognized under UL 1577
	Component Recognition Program ¹	Component Recognition Program ¹
	Single Protection, 5000 V rms Isolation Voltage	Single Protection, 3750V rms Isolation Voltage
	File (pending)	File (pending)
VDE	DIN V VDE V 0884-11 (VDE V 0884-11):2017-01 ²	DIN V VDE V 0884-11 (VDE V 0884-11):2017-01 ²
	Basic insulation, V _{IORM} = 1200 V peak, V _{IOSM} = 6250 V peak	Basic insulation, V _{IORM} = 1200 V peak, V _{IOSM} = 6250 V peak
	File (pending)	File (pending)
CQC	Certified under	Certified under
	CQC11-471543-2012	CQC11-471543-2012
	GB4943.1-2011	GB4943.1-2011
	Basic insulation at 845 V rms (1200 V peak) working voltage	Basic insulation at 845 V rms (1200 V peak) working voltage
	Reinforced insulation at 422 V rms (600 V peak)	Reinforced insulation at 422 V rms (600 V peak)
	File (pending)	File (pending)

Notes:

¹In accordance with UL 1577, SOP-8 is tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec; DIP-8 is tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec

²In accordance with DIN V VDE V 0884-10, SOP-8 is tested by applying an insulation test voltage ≥ 1800V peak for 1 sec (partial discharge detection limit = 5 pC); DIP-8 is tested by ≥ 1800V peak for 1 sec.

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 10. VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic		Unit
			DIP-8	NB SOIC-8	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150 V rms			I to IV	I to IV	

For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to III I to III	I to III I to III	
Climatic Classification			40/105/21	40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum Working Insulation Voltage		V_{IORM}	1200	1200	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1800	1800	V peak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.3 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1560	1560	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1440	1440	V peak
Highest Allowable Overvoltage		V_{IOTM}	7071	5300	V peak
Surge Isolation Voltage	Basic insulation, 1.2 μ s rise time, 50 μ s, 50% fall time $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification) ¹	V_{IOSM}	5000	5000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure				
Maximum Junction Temperature		T_s	150	150	°C
Total Power Dissipation at 25°C		P_s	0.14	0.14	W
Insulation Resistance at T_s	$V_{IO} = 500$ V	R_s	$>10^9$	$>10^9$	Ω

Notes:

¹In accordance with DIN V VDE V 0884-11, HCPL060X/HCP-063XXXX is proof tested by applying a surge isolation voltage 6500 V.

TYPICAL CHARACTERISTIC

VCC=5V, 0.1 μ F capacitor from VCC to GND, $T_A = -40^\circ\text{C}$ to 125°C (Unless otherwise noted).

Figure 2: Typical High Level Output Current vs. Temperature

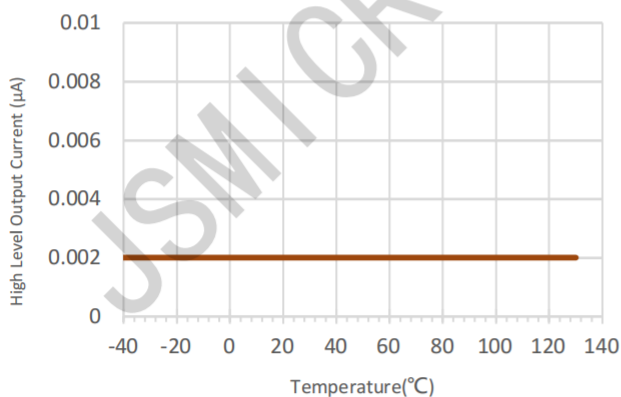


Figure 3: Typical Input Threshold Current vs. Temperature

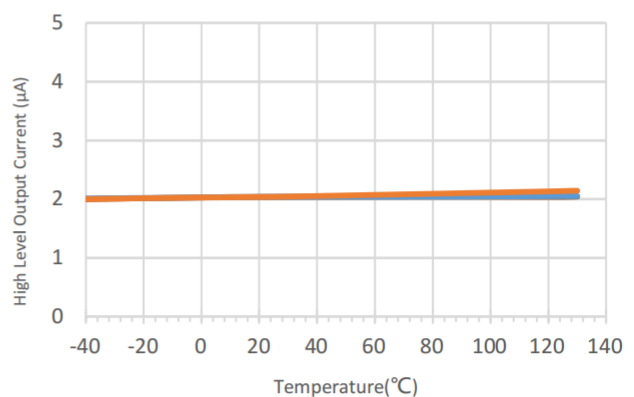


Figure 4: Typical Low Level Output Voltage vs. Temperature

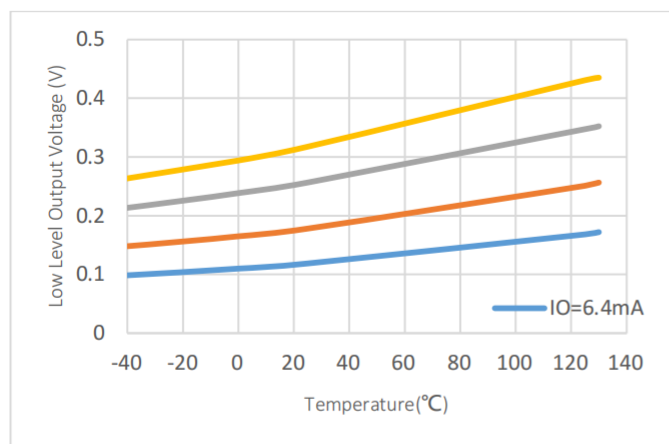


Figure 5: Typical Low Level Output Current vs. Temperature

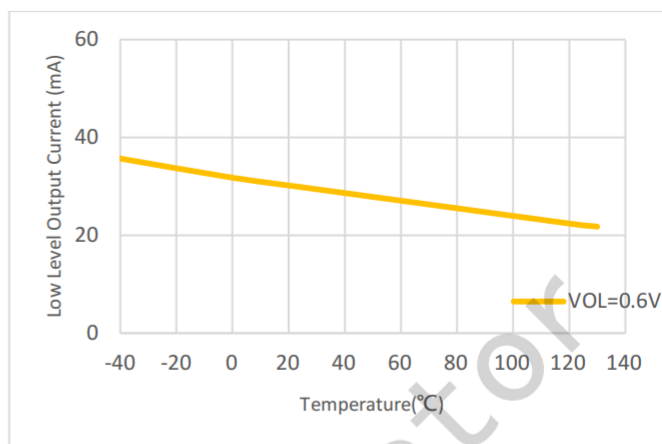


Figure 6: Typical Propagation Delay T_{PHL} vs. Temperature

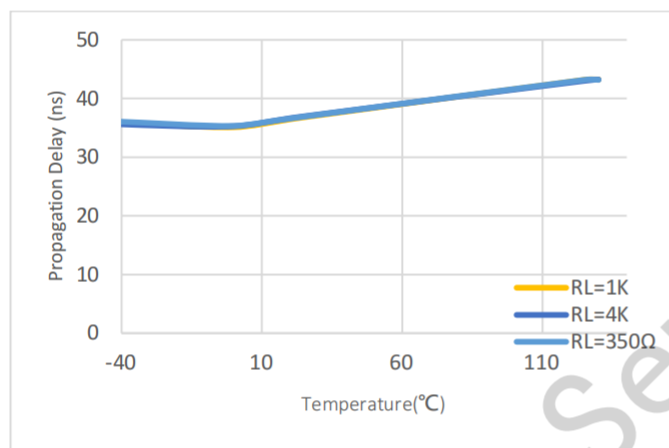


Figure 7: Typical Propagation Delay T_{PLH} vs. Temperature

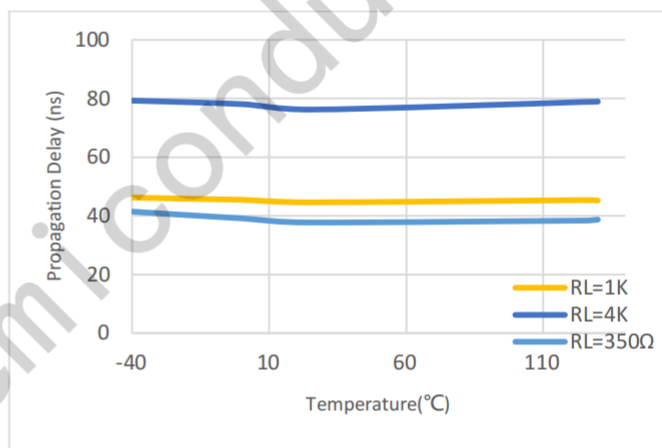


Figure 8: Typical Rise Time vs. Temperature

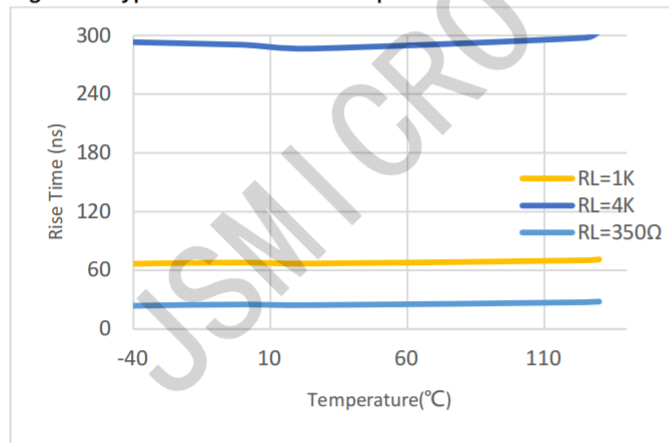


Figure 9: Typical Fall Time vs. Temperature

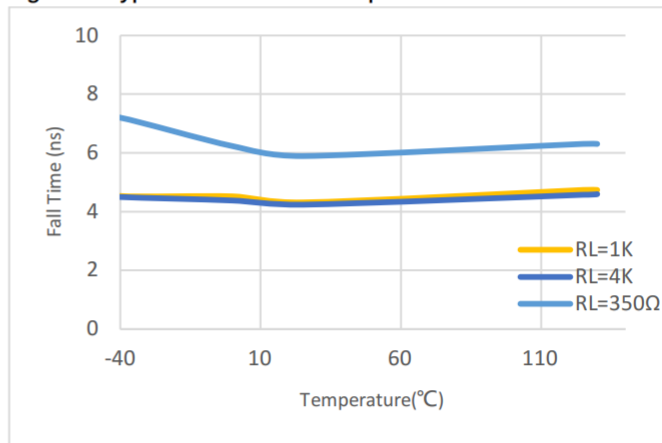


Figure 10: Enable Propagation Delay TEHL vs. Temperature

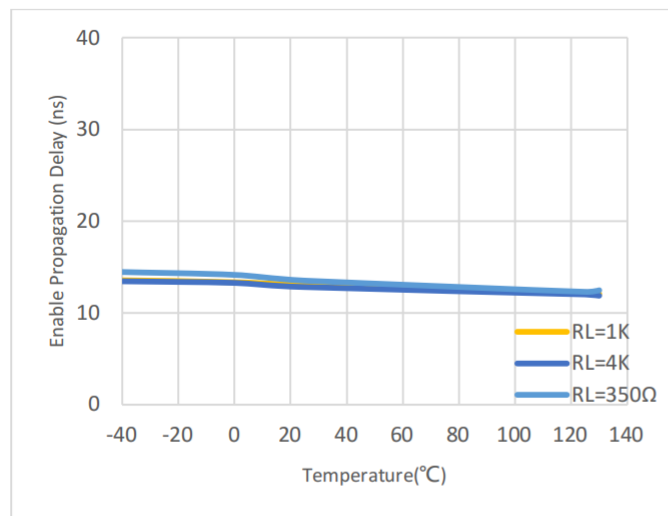


Figure 11: Enable Propagation Delay TELH vs. Temperature

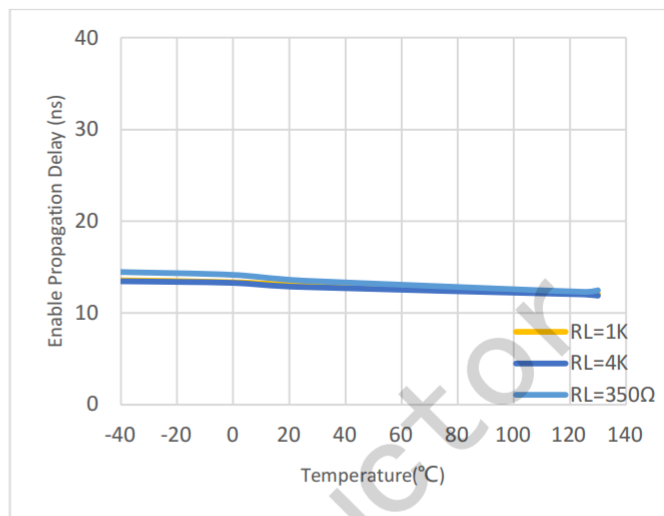


Figure 12: Typical Input Diode Forward Characteristic

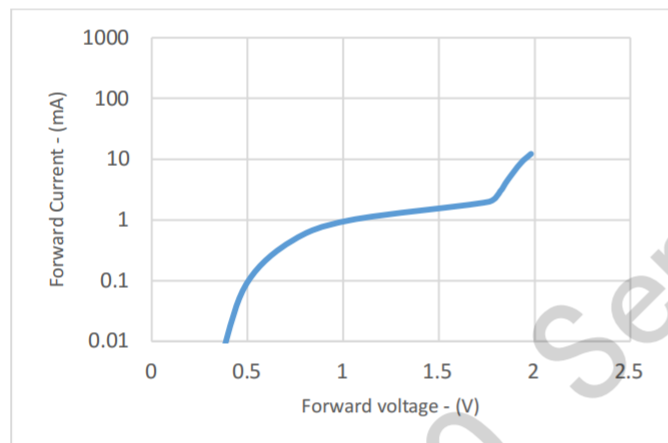


Fig. 13 Test circuit and waveforms for t_{PHL} , t_{PLH} , t_r , and t_f

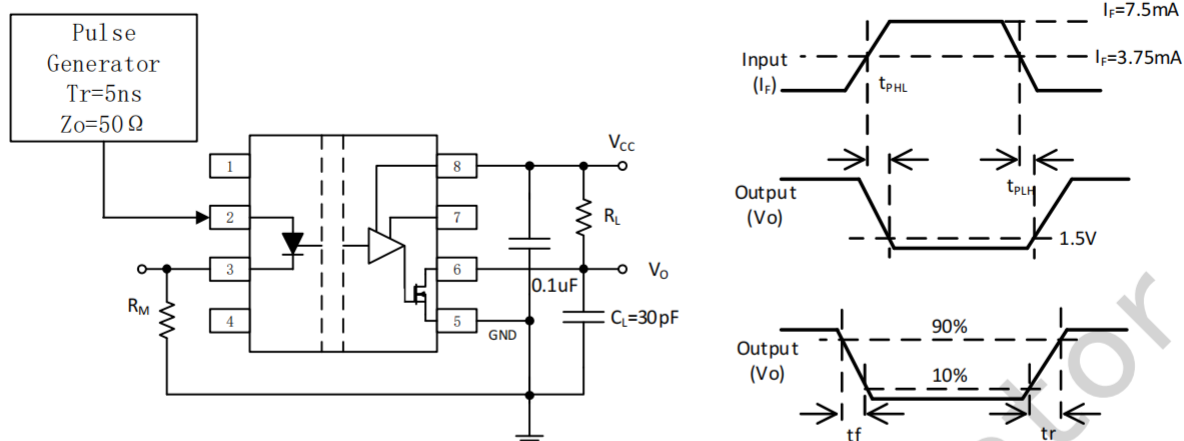


Fig. 14 Test circuit and waveform for t_{EHL} and t_{ELH}

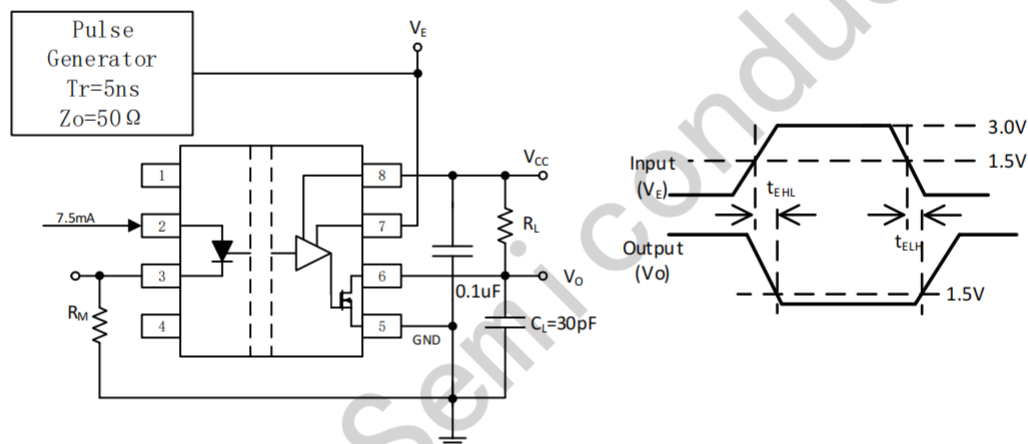
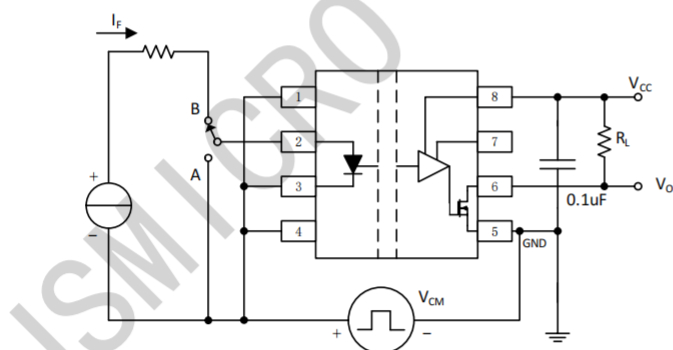
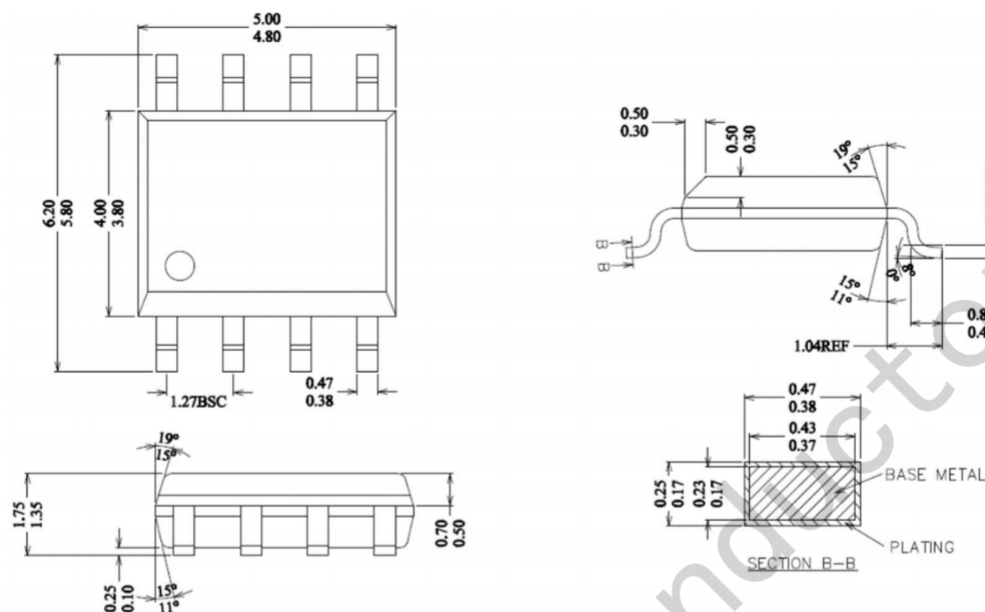


Fig. 15 Test circuit Common mode Transient Immunity

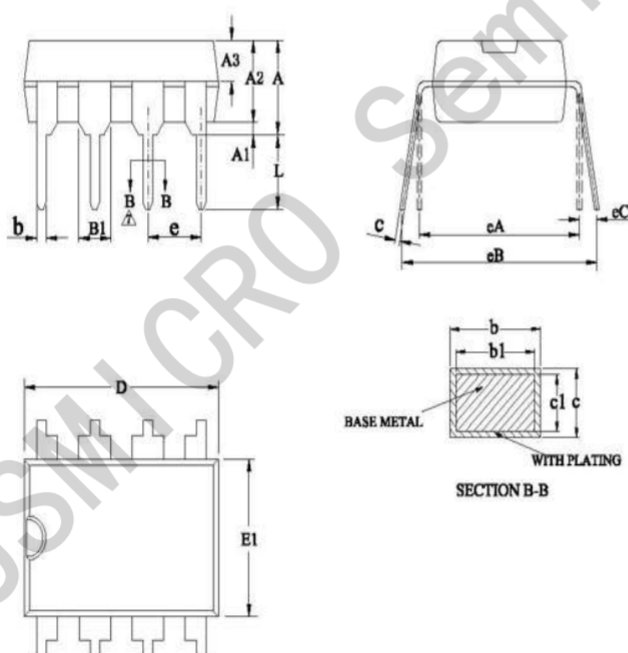


OUTLINE DIMENSIONS



NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure15. 8-Lead Standard Small Outline Package [NB SOIC-8]



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.20	3.30	3.40
A3	1.55	1.60	1.65
b	0.44	—	0.52
b1	0.43	0.46	0.49
B1	1.52REF		
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	9.15	9.25	9.35
E1	6.25	6.35	6.45
e	2.54BSC		
eA	7.62REF		
eB	7.62	—	9.30
eC	0	—	0.84
L	3.00	—	—

Figure16. 8-Lead DIP Outline Package [DIP-8]