20V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
20V	0.99Ω @ V_{GS} = 4.5V	760mA
	1.2Ω @ V_{GS} = 2.5V	700mA
	2.4Ω @ V_{GS} = 1.8V	500mA
	3.0Ω @ V_{GS} = 1.5V	350mA

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch

Features and Benefits

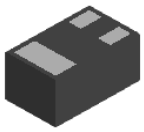
- Low On-Resistance
- Very Low Gate Threshold Voltage, 1.0V Max
- Low Input Capacitance
- Fast Switching Speed
- Ultra-Small Surface Mount Package 1mm x 0.6mm
- Low Package Profile, 0.5mm Maximum Package Height
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at https://www.diodes.com/products/automotive/automotive-products/.**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability. https://www.diodes.com/quality/product-definitions/**

Mechanical Data

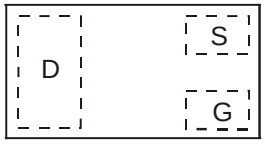
- Case: X1-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.001 grams (Approximate)

X1-DFN1006-3

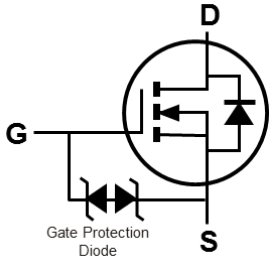




Bottom View



Top View
Pin Configuration



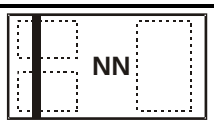
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Tape Pitch (mm)	Quantity per Reel
DMN21D2UFB-7	NN	7	8	4	3,000
DMN21D2UFB-7B	NN	7	8	2	10,000

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



NN = Product Type Marking Code

Top View
Bar Denotes Gate and Source Side

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 6) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	760 610	mA
	t<5s	T_A = +25°C T_A = +70°C	I_D	850 700	mA
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	0.8	A
Pulsed Drain Current (Note 7)			I_{DM}	1.0	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	0.38	W
	T_A = +70°C		0.25	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	325	°C/W
	t<5s		244	
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	0.9	W
	T_A = +70°C		0.57	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	141	°C/W
	t<5s		106	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current @T_c = +25°C	I_{DSS}	—	—	100	nA	V_{DS} = 20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±1	µA	V_{GS} = ±10V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.4	—	1.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	0.6	0.99	Ω	V_{GS} = 4.5V, I_D = 100mA
		—	0.7	1.2		V_{GS} = 2.5V, I_D = 50mA
		—	0.9	2.4		V_{GS} = 1.8V, I_D = 20mA
		—	1.2	3.0		V_{GS} = 1.5V, I_D = 10mA
Forward Transfer Admittance	$\|Y_{fs}\|$	180	—	—	ms	V_{DS} = 10V, I_D = 400mA
Diode Forward Voltage	V_{SD}	—	0.6	1.0	V	V_{GS} = 0V, I_S = 150mA
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	27.6	—	pF	V_{DS} = 16V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	4.0	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	2.8	—	pF	
Total Gate Charge, V_{GS} = 4.5V	Q_g	—	0.41	—	nC	V_{DS} = 10V, I_D = 250mA
Total Gate Charge, V_{GS} = 10V	Q_g	—	0.93	—	nC	
Gate-Source Charge	Q_{gs}	—	0.06	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.06	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.5	—	ns	V_{DD} = 10V, V_{GS} = 4.5V, R_L = 47Ω, R_g = 10Ω, I_D = 200mA
Turn-On Rise Time	t_r	—	4.2	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	19.6	—	ns	
Turn-Off Fall Time	t_f	—	9.8	—	ns	

Notes:
5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
7. Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

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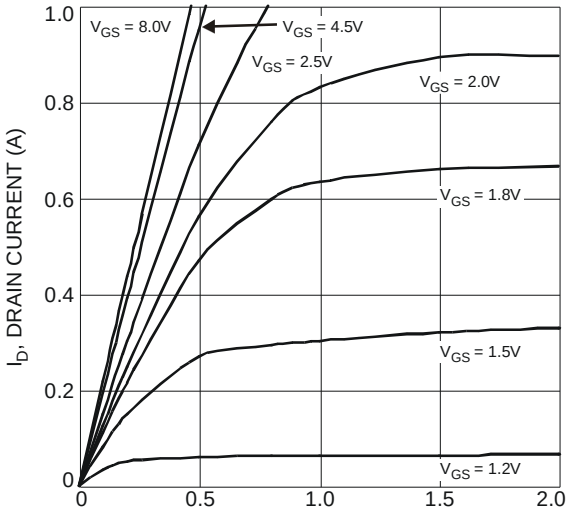


Fig. 1 Typical Output Characteristic

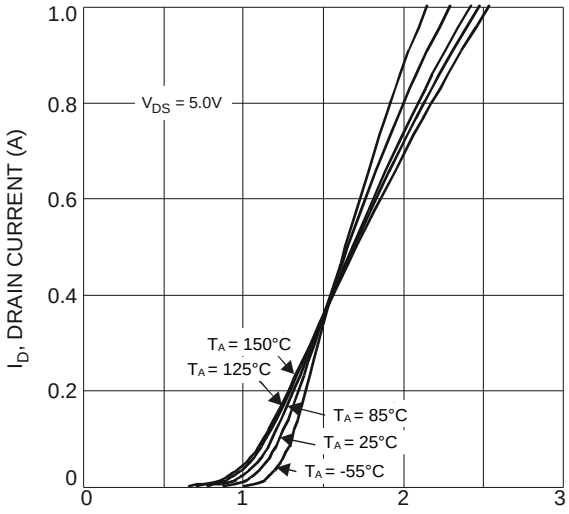


Fig. 2 Typical Transfer Characteristics

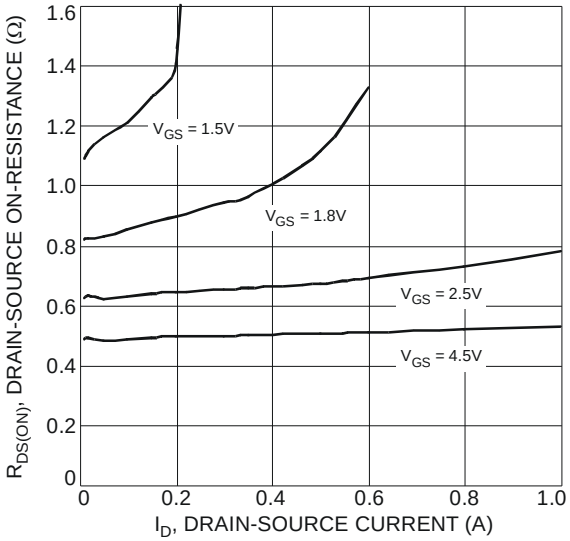


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

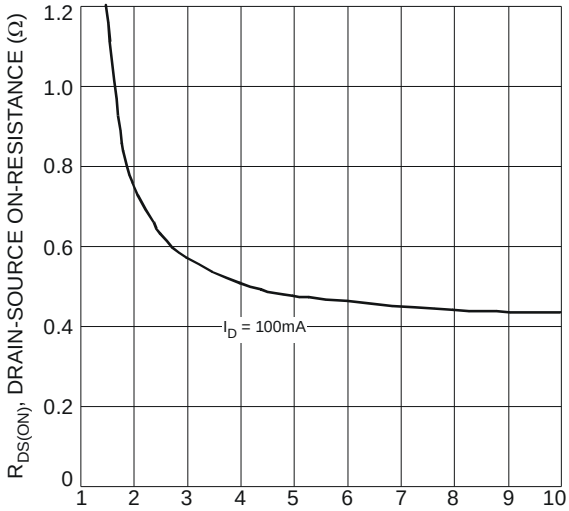


Fig. 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

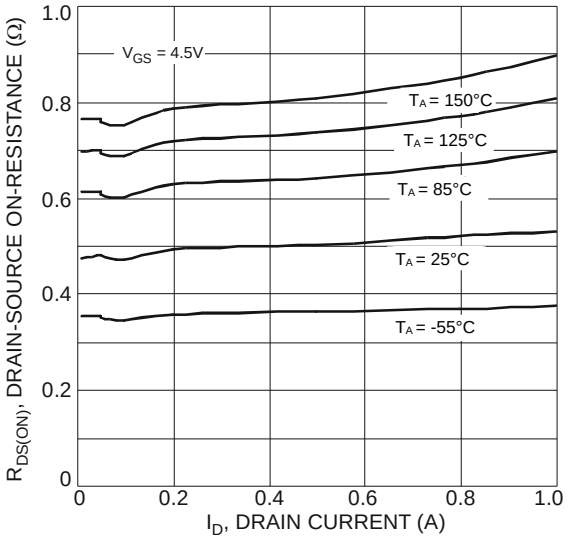


Fig. 5 Typical On-Resistance vs. Drain Current and Temperature

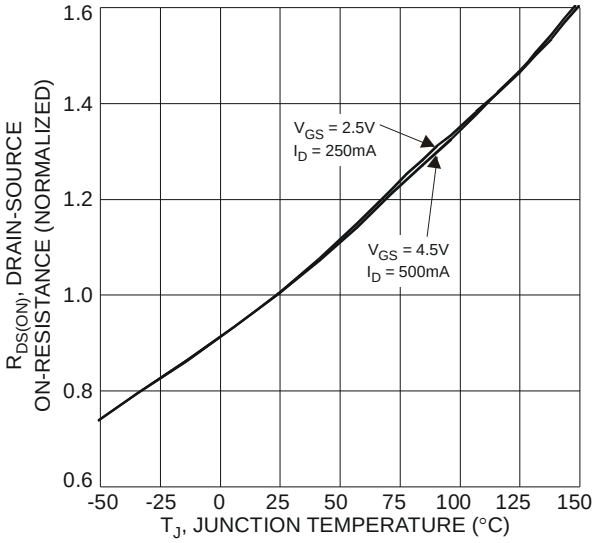


Fig. 6 On-Resistance Variation with Temperature

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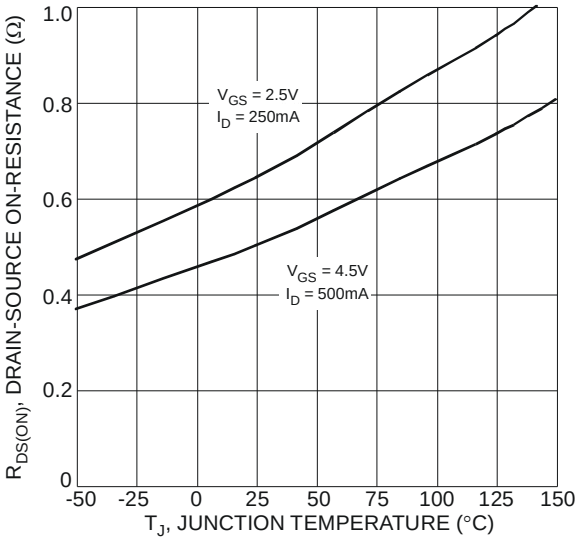


Fig. 7 On-Resistance Variation with Temperature

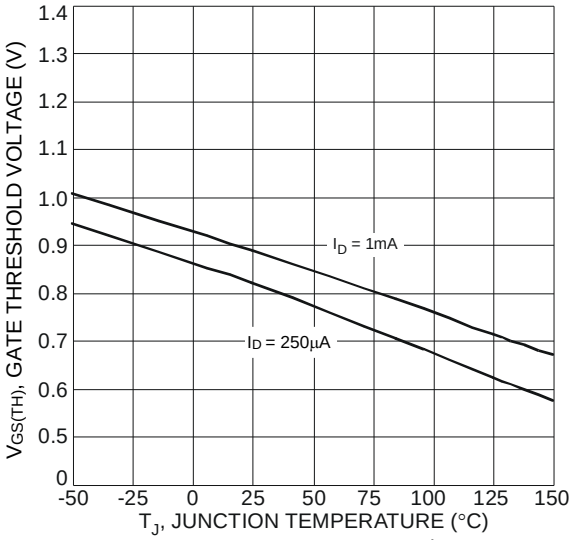


Fig. 8 Gate Threshold Variation vs. Junction Temperature

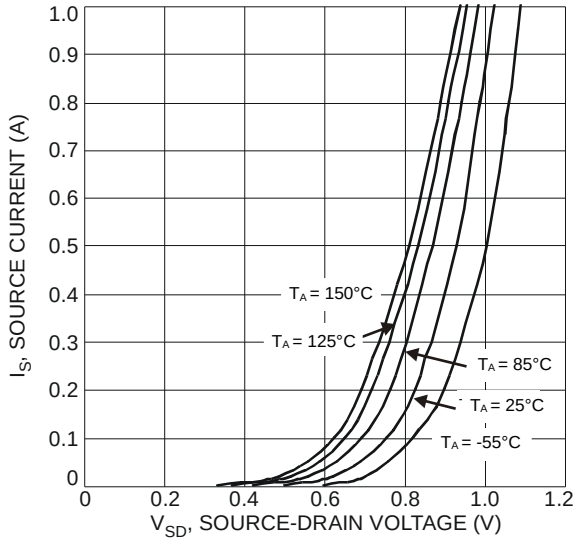


Fig. 9 Diode Forward Voltage vs. Current

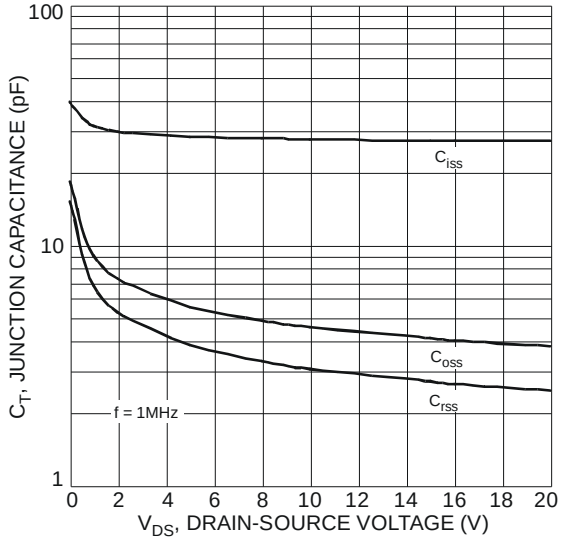


Fig. 10 Typical Junction Capacitance

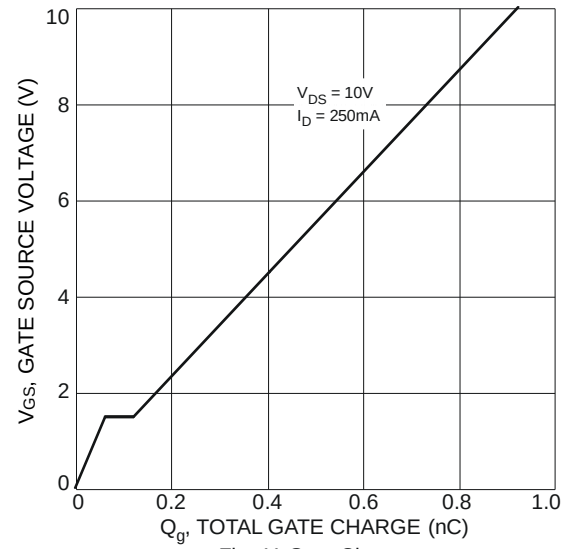


Fig. 11 Gate Charge

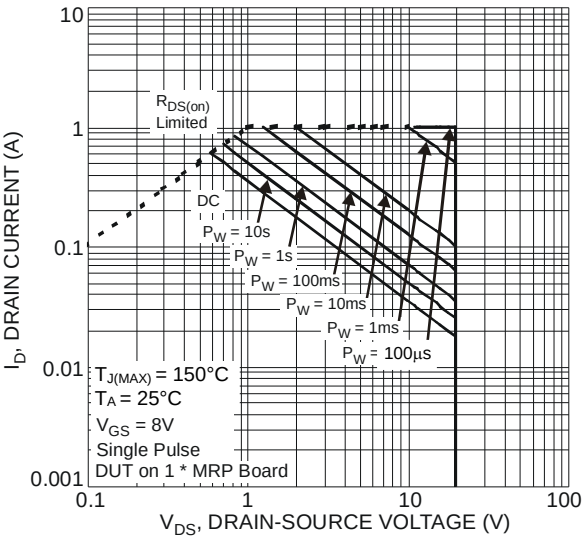


Fig. 12 SOA, Safe Operation Area

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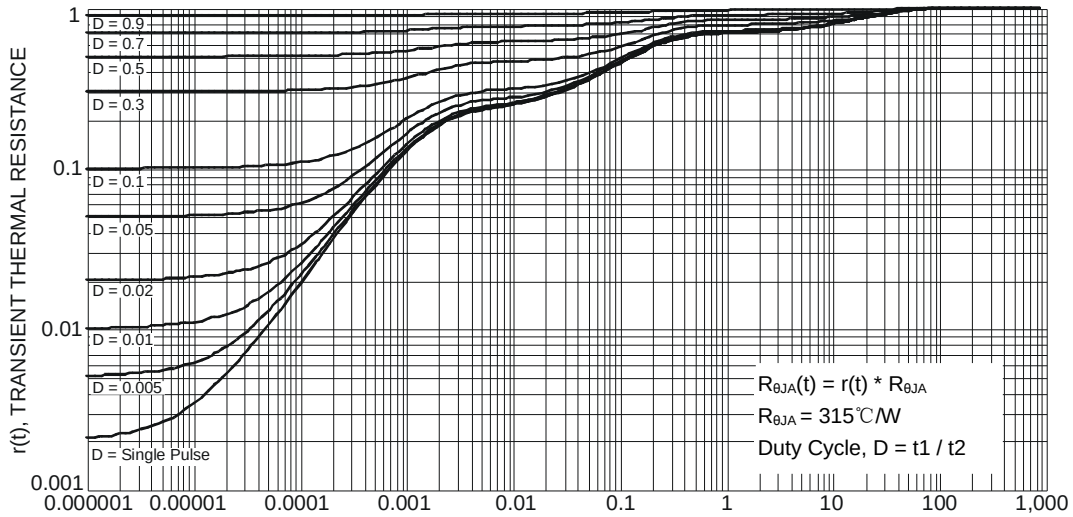
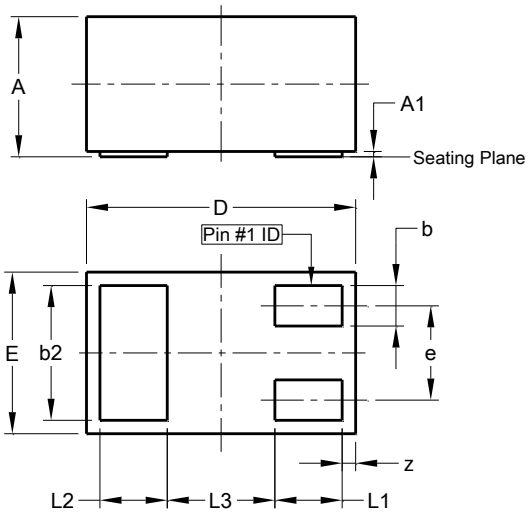


Fig. 13 Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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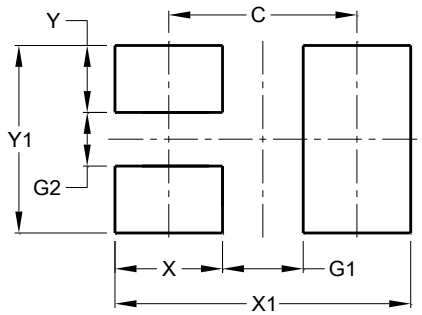


X1-DFN1006-3			
Dim	**Min**	**Max**	**Typ**
A	0.47	0.53	0.50
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.075	1.00
E	0.55	0.675	0.60
e	-	-	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	-	-	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-DFN1006-3



Dimensions	Value (in mm)
C	0.70
G1	0.30
G2	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70

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