FXLS6xxxx Dual Channel Inertial Sensor

FXLS6xxxx is a two channel DSI3, PSI5, SPI and I^2C compatible lateral (X-Axis or Y-Axis) or vertical (Z-Axis) inertial sensor.

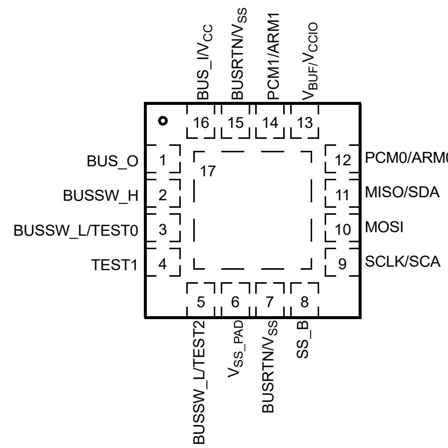
FXLS6xxxx

Revision 2.18, Dated: September 13, 2019

RoHS

DSI3, PSI5, SPI & IIC Dual Channel Inertial Sensor

QFN 4mm x 4mm x 1.45mm



Features

- Independent X-Axis, Y-Axis or Z-Axis Ranges for each Channel
  - Medium g ranges from ± 15.5 g to ± 150 g Nominal Full-Scale Range
  - High g ranges from ± 50 g to ± 500 g Nominal Full-Scale Range
- -40°C to 125°C Operating Temperature Range
- DSI3 Compatible
  - Discovery Mode for Physical Location Identification
  - High Side Bus Switch Output Driver
  - Command and Response Mode Support for Device Configuration
  - Periodic Data Collection Mode Support for Sensor Data Transfers.
  - Background Diagnostic Mode Support During Periodic Data Collection Mode
- PSI5 Version 2.1 Compatible
  - Compatible Modes:
    - P10P-500/3L
    - P10P-500/4H
    - A10P-228/1L
    - P10CRC-xxx/xx
    - P16CRC-xxx/xx
    - and many others
  - Programmable Time Slots with 1µs Resolution
  - Selectable Baud Rate: 125 kBaud or 189 kBaud
  - 10-Bit and 16-bit Data Options
  - Selectable Error Detection: Even Parity, or 3-bit CRC
  - Optional Daisy Chain with External Low Side Switch
  - Two-Wire Programming Mode
- 32-Bit SPI Compatible Serial Interface
  - 3.3V or 5V Single Supply Operation
  - Register Read and Write Commands
  - Sensor Data Transmission Commands
    - 12-Bit Data, Left Justified in a 16-Bit Data Field
    - Command Echo with 3-Bit Source Identification
    - 2-Bit Basic Status and 2-Bit Detailed Status Fields
    - 8-Bit CRC
- I^2C Compatible Serial Interface (UM 10204, Revision 5)
  - Slave Mode Operation
  - Standard Mode, Fast Mode and Fast Mode Plus Support
- Independent programmable arming functions for each channel
- DSP
  - Dual, independent signal chains from ADC to Communications Interface
  - Up to a 4^{th} order Low Pass Filter with Rolloff Frequency Options from 12.5Hz to 1500Hz
  - Optional Single Pole High Pass Filter with Fast Start Up & Output Rate Limiting
  - Optional Moving Average
  - Optional 16 to 1 output interpolation
- Pb-Free 16-Pin QFN 4mm x 4mm x 1.45mm Package

Referenced Documents

- DSI3 Standard Revision 1.0, Dated February 16, 2011
- PSI5 Technical Specification Version 2.1, Dated October 8, 2012
- AKLV27 V1.40
- NXP UM10204 I^2C Bus Specification and User Manual, Revision 5
- AECQ100, Revision H, AEC-Q006

Ordering Information (SPI, DSI3 and PSI5)

Part Number	Channel 0 Axis	Channel 0 Range	Channel 1 Axis	Channel 1 Range	Protocol	Design Type	Offset Cancellation Rate Limiting	Arming Function Threshold Resolution
FXLS60322	X	M	Y	M	SPI/DSI3		1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS60422	X	M	Z	M	SPI/DSI3	Z-Axis Bumper	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS60425	X	M	Z	M	SPI/DSI3	Z-Axis Geometric Stop	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS60333	X	H	Y	H	SPI/DSI3		1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS60433	X	H	Z	H	SPI/DSI3	Z-Axis Bumper	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS60436	X	H	Z	H	SPI/DSI3	Z-Axis Geometric Stop	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS63333	X	H	Y	H	PSI5		1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS63433	X	H	Z	H	PSI5	Z-Axis Bumper	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS63436	X	H	Z	H	PSI5	Z-Axis Geometric Stop	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS65322	X	M	Y	M	SPI/DSI3		1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS65422	X	M	Z	M	SPI/DSI3	Z-Axis Bumper	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS65425	X	M	Z	M	SPI/DSI3	Z-Axis Geometric Stop	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS65333	X	H	Y	H	SPI/DSI3		1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS65433	X	H	Z	H	SPI/DSI3	Z-Axis Bumper	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS65436	X	H	Z	H	SPI/DSI3	Z-Axis Geometric Stop	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS68333	X	H	Y	H	PSI5		1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS68433	X	H	Z	H	PSI5	Z-Axis Bumper	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS68436	X	H	Z	H	PSI5	Z-Axis Geometric Stop	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit

Ordering Information (I^2C)

Part Number	Channel 0 Axis	Channel 0 Range	Channel 1 Axis	Channel 1 Range	Protocol	Design Type	Offset Cancellation Rate Limiting	Arming Function Threshold Resolution
FXLS64322	X	M	Y	M	I^2C		1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS64422	X	M	Z	M	I^2C	Z-Axis Bumper	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS64425	X	M	Z	M	I^2C	Z-Axis Geometric Stop	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS64333	X	H	Y	H	I^2C		1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS64433	X	H	Z	H	I^2C	Z-Axis Bumper	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS64436	X	H	Z	H	I^2C	Z-Axis Geometric Stop	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
FXLS69322	X	M	Y	M	I^2C		1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS69422	X	M	Z	M	I^2C	Z-Axis Bumper	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS69425	X	M	Z	M	I^2C	Z-Axis Geometric Stop	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS69333	X	H	Y	H	I^2C		1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS69433	X	H	Z	H	I^2C	Z-Axis Bumper	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
FXLS69436	X	H	Z	H	I^2C	Z-Axis Geometric Stop	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit

SECTION 1 APPLICATION DIAGRAMS

1.1 DSI3 Application Diagrams

1.1.1 DSI3 Discovery Mode Application Diagram

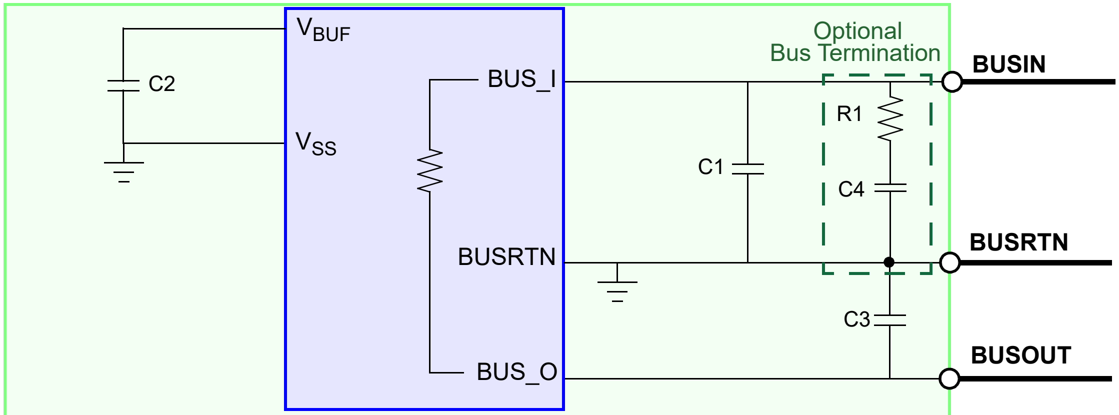


Figure 1-1 DSI3 Discovery Mode Application Diagram

External Component Recommendations				
Ref Des	**Type**	**Typical Value Description**	**Component Value Selection and Range**	**Comment**
R1	General Purpose	330 Ohm, 5%, 200PPM	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	Optional Bus termination for high inductance bus wire connections. For optimal EMC performance this component along with C4 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C1	Ceramic	220pF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing.	For optimal EMC performance this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	0.47µF, 10%, 10V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22µF. The maximum specified value including all tolerances is 2µF.	For optimal EMC performance this component is to be placed as close to the VBUF and BUSRTN pins as possible.
C3	Ceramic	100pF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	For optimal EMC performance this component is to be placed as close to the BUS_O and BUSRTN connector pins as possible.
C4	Ceramic	2.2nF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	Optional Bus termination for high inductance bus wire connections. For optimal EMC performance this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.

Notes: The total bus capacitance must not exceed the values specified in the DSI3 standard.
The external components are dependent on the bus master and bus impedance and may vary from application to application.

1.1.2 DSI3 Switch Connected Daisy Chain Mode Application Diagram

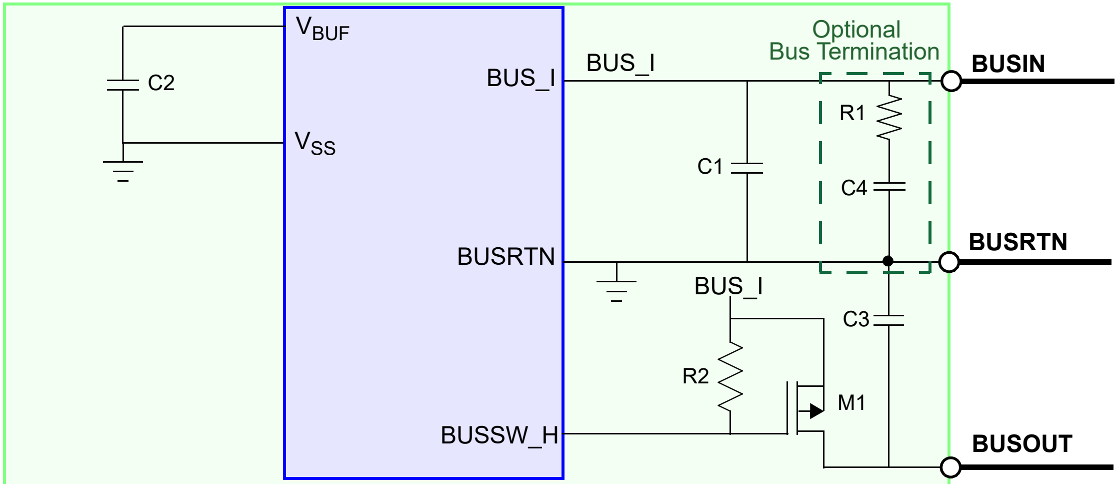


Figure 1-2 DSI3 Switch Connected Daisy Chain Application Diagram

External Component Recommendations				
Ref Des	**Type**	**Typical Value Description**	**Component Value Selection and Range**	**Comment**
R1	General Purpose	330 Ohm, 5%, 200PPM	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	Optional Bus termination for high inductance bus wire connections. For optimal EMC performance this component along with C4 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
R2	General Purpose	100 kOhm, 5%, 200PPM	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	Pullup Resistor for External High Side Daisy Chain FET
C1	Ceramic	220pF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing.	For optimal EMC performance this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	0.47µF, 10%, 10V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22µF. The maximum specified value including all tolerances is 2µF.	For optimal EMC performance this component is to be placed as close to the VBUF and BUSRTN pins as possible.
C3	Ceramic	100pF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	For optimal EMC performance this component is to be placed as close to the BUS_O and BUSRTN connector pins as possible.
C4	Ceramic	2.2nF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	Optional Bus termination for high inductance bus wire connections. For optimal EMC performance this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
M1	P-Channel MOSFET	NTR4502PT1G, or similar	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	High Side Daisy Chain Transistor

Notes: The total bus capacitance must not exceed the values specified in the DSI3 standard.
The external components are dependent on the bus master and bus impedance and may vary from application to application.

1.2 PSI5 Application Diagrams

1.2.1 PSI5 Parallel or Universal Mode Application Diagram

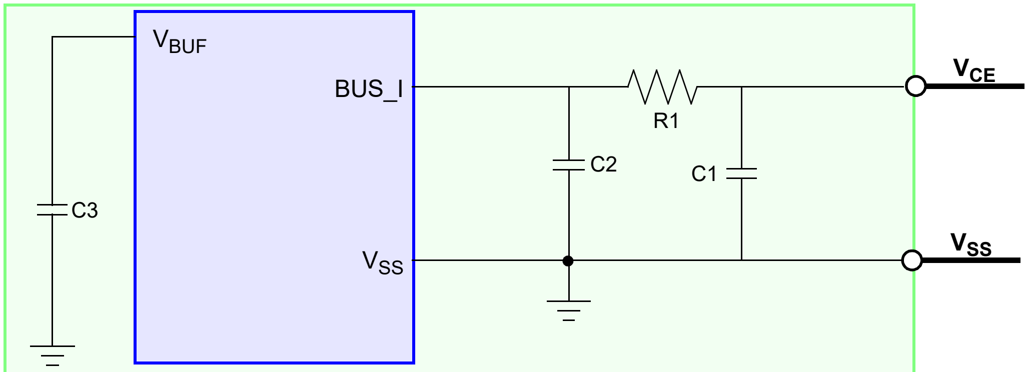


Figure 1-3 PSI5 Parallel or Universal Mode Application Diagram

External Component Recommendations				
Ref Des	**Type**	**Typical Value Description**	**Component Value Selection and Range**	**Comment**
R1	General Purpose	10 Ohm, 5%, 200PPM	The optimal value of this component should be determined by the system level communication, EMC and ESD testing. For proper device function the minimum value can be 0 Ohms. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 20.5 Ohms. If the low response current is used, the maximum resistance including all tolerances is 33.3 Ohms.	V_{CC} Filtering and Signal Damping
C1	Ceramic	2.2 nF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	V_{CC} Power Supply Decoupling and Signal Damping. For optimal EMC performance this component is to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	15 nF, 10%, 50V minimum, X7R		V_{CC} Power Supply Decoupling. For optimal EMC performance this component is to be placed as close to the BUS_I and BUSRTN pins as possible.
C3	Ceramic	0.47µF, 10%, 10V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22µF. The maximum specified value including all tolerances is 2µF.	For optimal EMC performance this component is to be placed as close to the VBUF and BUSRTN pins as possible.

Note: The total bus capacitance must not exceed the values specified in the PSI5 standard.

R1 must be sized to handle both the programming current at the maximum rated temperature for programming and the operating current at the maximum rated temperature for operation.

If the high baud rate is used, it is recommended to reduce the value of C2. The actual value will depend on the bus configuration and number of slaves.

1.2.2 PSI5 Daisy Chain Mode Application Diagram

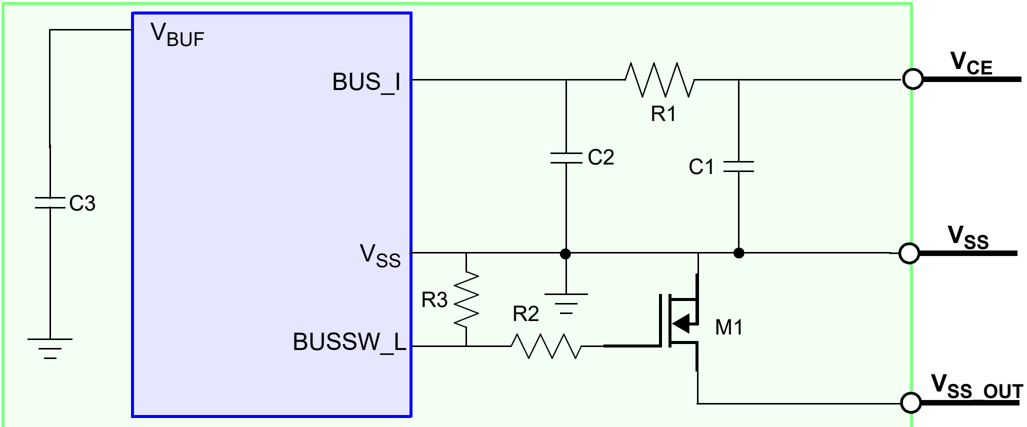


Figure 1-4 PSI5 Daisy Chain Mode Application Diagram

External Component Recommendations				
Ref Des	**Type**	**Typical Value Description**	**Component Value Selection and Range**	**Comment**
R1	General Purpose	10 Ohm, 5%, 200PPM	The optimal value of this component should be determined by the system level communication, EMC and ESD testing. For proper device function the minimum value can be 0 Ohms. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 20.5 Ohms. If the low response current is used, the maximum resistance including all tolerances is 33.3 Ohms.	V_{CC} Filtering and Signal Damping
R2	General Purpose	20 kOhm, 5%, 200PPM	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	Gate Resistor for External Low Side Daisy Chain FET
R3	General Purpose	100 kOhm, 5%, 200PPM	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	Gate Pulldown Resistor for External Low Side Daisy Chain FET
C1	Ceramic	2.2 nF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	V_{CC} Power Supply Decoupling and Signal Damping. For optimal EMC performance this component is to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	15 nF, 10%, 50V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	V_{CC} Power Supply Decoupling. For optimal EMC performance this component is to be placed as close to the BUS_I and BUSRTN pins as possible.
C3	Ceramic	0.47μF, 10%, 10V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22μF. The maximum specified value including all tolerances is 2μF.	For optimal EMC performance this component is to be placed as close to the VBUF and BUSRTN pins as possible.
M1	N-Channel MOSFET	NTR4501NT1G, or similar	The optimal value of this component should be determined by the system level communication, EMC and ESD testing	Low Side Daisy Chain Transistor

Note: The total bus capacitance must not exceed the values specified in the PSI5 standard.

R1 must be sized to handle both the programming current at the maximum rated temperature for programming and the operating current at the maximum rated temperature for operation.

If the high baud rate is used, it is recommended to reduce the value of C2. The actual value will depend on the bus configuration and number of slaves.

1.3 SPI Application Diagram

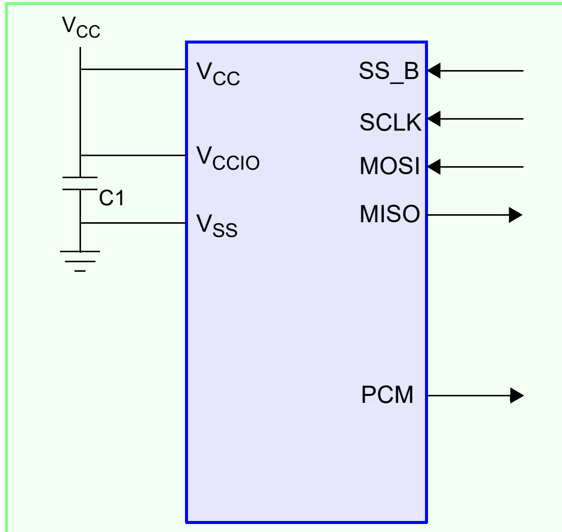


Figure 1-5 SPI Application Diagram

External Component Recommendations			
Ref Des	Type	Typical Value Description	Comment
C1	Ceramic	0.1 µF, 10%, 10V Minimum, X7R	V_{CC} Power Supply Decoupling. For optimal EMC performance this component is to be placed as close to the VCC and VSS pins as possible

1.4 I²C Application Diagram

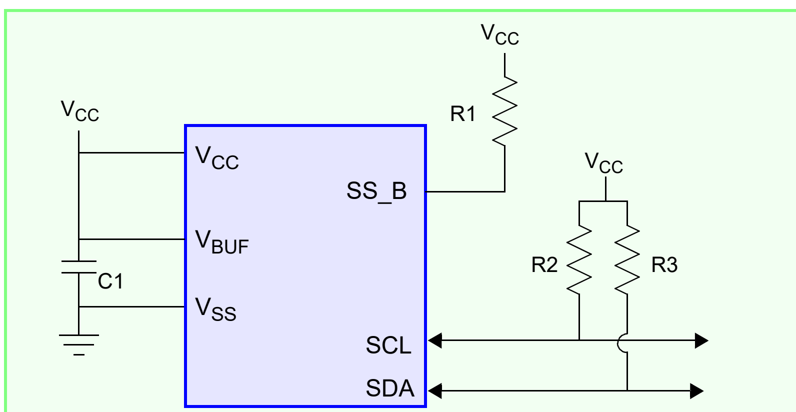


Figure 1-6 I²C Application Diagram

External Component Recommendations			
Ref Des	Type	Description	Purpose
R1	General Purpose	1000 Ohm, 5%, 200PPM	I2C Selection Pin Pull-up Resistor
R2	General Purpose	1000 Ohm, 5%, 200PPM	Serial Clock Pull-up Resistor
R3	General Purpose	1000 Ohm, 5%, 200PPM	Serial Data Pull-up Resistor
C1	Ceramic	0.1 µF, 10%, 10V Minimum, X7R	V_{CC} Power Supply Decoupling

SECTION 2 INTERNAL BLOCK DIAGRAM

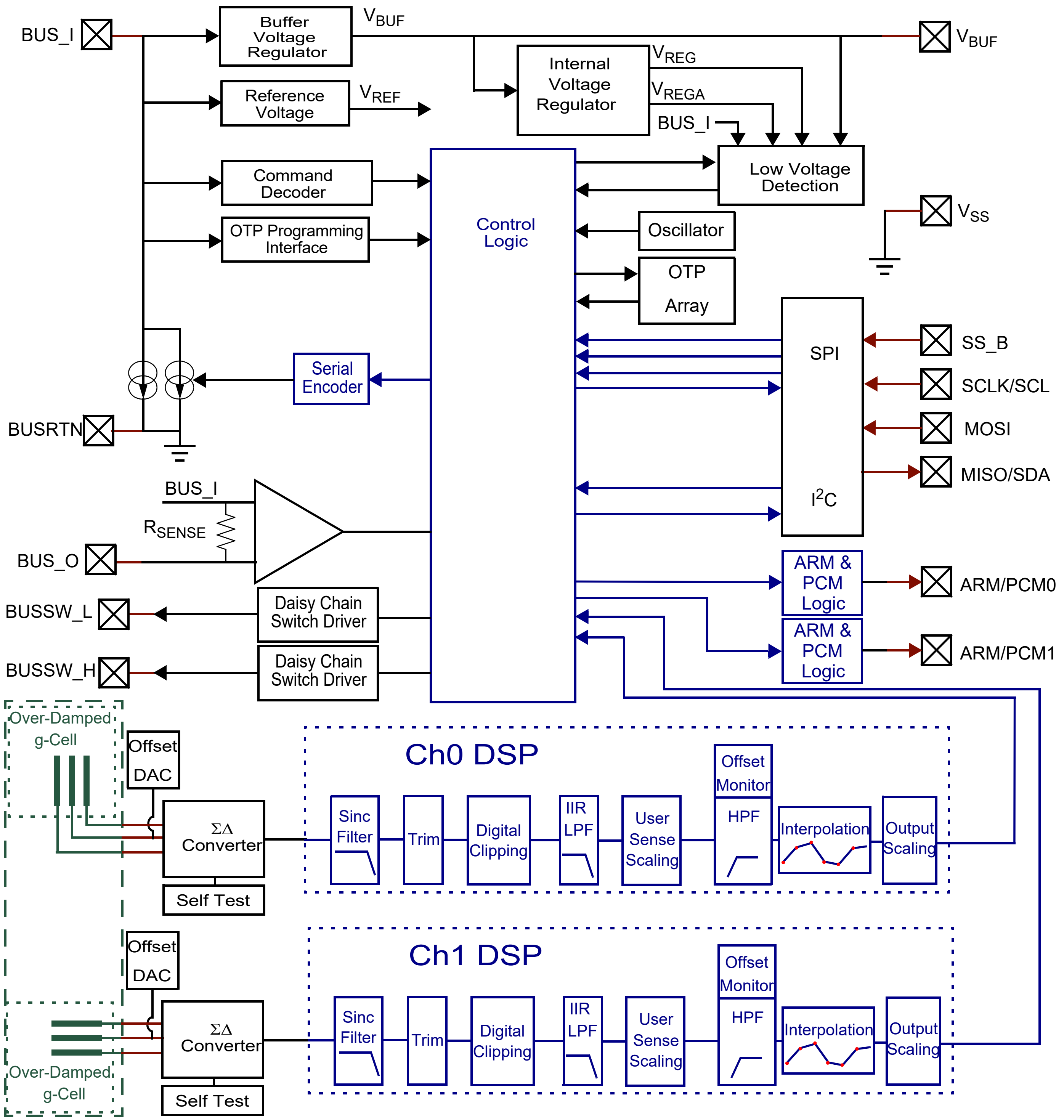
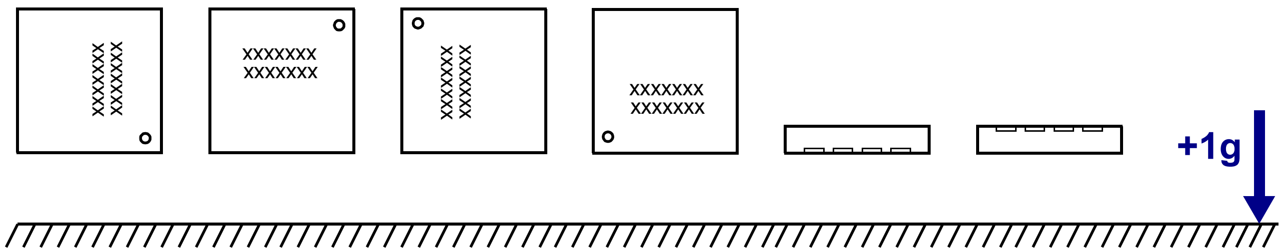


Figure 2-1 Dual Channel Internal Block Diagram

SECTION 3 DEVICE ORIENTATION DIAGRAMS



XY	Ch0: 0g	Ch0: +1g	Ch0: 0g	Ch0: -1g	Ch0: 0g	Ch0: 0g	
	Ch1: -1g	Ch1: 0g	Ch1: +1g	Ch1: 0g	Ch1: 0g	Ch1: 0g	
XZ	Ch0: 0g	Ch0: +1g	Ch0: 0g	Ch0: -1g	Ch0: 0g	Ch0: 0g	
	Ch1: 0g	Ch1: 0g	Ch1: 0g	Ch1: 0g	Ch1: +1g	Ch1: -1g	
YZ	Ch0: -1g	Ch0: 0g	Ch0: +1g	Ch0: 0g	Ch0: 0g	Ch0: 0g	
	Ch1: 0g	Ch1: 0g	Ch1: 0g	Ch1: 0g	Ch1: +1g	Ch1: -1g	

Part Marking

Data Code Legend:

WL: 2 alpha character representation of the wafer lot

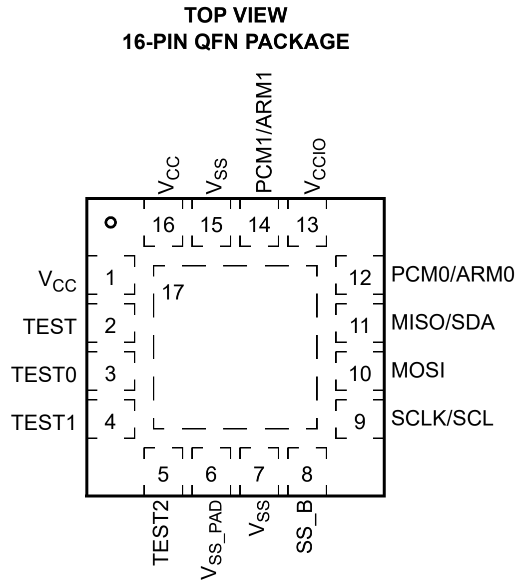
YW: 2 alpha character representation of the year and work week

Z: Assembly Split

Figure 3-1 Part Marking

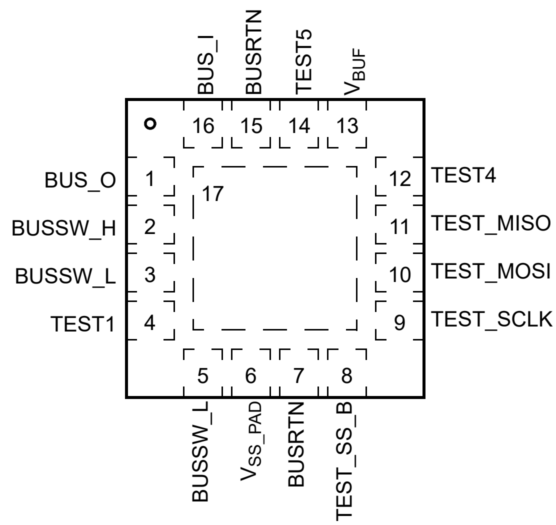
SECTION 4 PIN OUT

4.1 Device Pinout: SPI or I²C Mode



Pin	Pin Name	Definition	Description
1	V_{CC}	Supply	It is recommended that this pin be connected to V_{CC}. Optionally, this pin can be unterminated.
2,3,4,5	TEST	Test Pin	It is recommended that these pins be unterminated. Optionally, this pin can be tied to V_{SS}.
6	V_{SS_PAD}	Supply Return	This pin is internally connected to the die attach pad. It is recommended that this pin be unterminated or connected to V_{SS}.
7,15	V_{SS}	Supply Return	This pin is the supply return node.
8	SS_B	Slave Select	In SPI mode, this input pin provides the slave select for the SPI port. An internal pull-up device is connected to this pin. In I²C mode, this pin must be connected to V_{BUF} with an external pull-up resistor as shown in Figure 1-6.
9	SCLK/SCL	SPI Clock	In SPI mode, this input pin provides the serial clock. An internal pull-down device is connected to this pin. In I²C mode, this input pin provides the serial clock. This pin must be connected to V_{BUF} with an external pull-up resistor as shown in Figure 1-6.
10	MOSI	SPI Data In	In SPI mode, this pin functions as the serial data input to the SPI port. An internal pull-down device is connected to this pin. In I²C mode, it is recommended that this pin be unterminated. Optionally, this pin can be connected to V_{SS}.
11	MISO/SDA	SPI Data Out	In SPI mode, this pin functions as the serial data output. In I²C mode, this pin functions as the serial data input/output. This pin must be connected to V_{BUF} with an external pull-up resistor as shown in Figure 1-6.
12	PCM0 / ARM0	Channel 0 PCM Channel 0 Arm	This pin has multiplexed functions: – When the channel 0 arming output is selected, the pin can be configured as an open drain, active low output with a pull-up current; or an open drain, active high output with a pull-down current. – When PCM mode is selected, this pin can be configured as a digital output with PCM signal proportional to the channel 0 sensor data. If unused, or in I²C mode, it is recommended that this pin be unterminated.
13	V_{CCIO}	Supply	This pin must be connected directly to V_{CC}.
14	PCM1 / ARM1	Channel 1 PCM Channel 1 Arm	This pin has multiplexed functions: – When the channel 1 arming output is selected, the pin can be configured as an open drain, active low output with a pull-up current; or an open drain, active high output with a pull-down current. – When PCM mode is selected, this pin can be configured as a digital output with PCM signal proportional to the channel 1 sensor data. If unused, or in I²C mode, it is recommended that this pin be unterminated.
16	V_{CC}	Supply	This pin is connected to the supply for the device. An external capacitor must be connected between this pin and V_{SS} as shown in Section 1.3 and Section 1.4.
17	PAD	Die Attach Pad	This pin is the die attach flag, and must be connected to V_{SS}. Reference Section 11 for die attach pad connection details.

4.2 Device Pinout: DSI3 or PSI5 Mode



Pin	Pin Name	Definition	Description
1	BUS_O	Supply Out	This pin is connected to the BUS_I pin through an internal sense resistor and provides the supply connection to the next slave in a daisy chain configuration. In DSI3 mode, an external capacitor must be connected between this pin and V_{SS} as shown in Section 1.1. In PSI5 mode, it is recommended that this pin be unterminated. Optionally, this pin can be connected to BUS_I/V_{CC}.
2	BUSSW_H	High Side Bus Switch Driver	In DSI3 switch connected daisy chain mode, this pin is connected to the gate of a p-channel FET which connects BUS_I to the next slave in the daisy chain. An external pullup resistor is required on the gate of the p-channel FET as shown in Figure 1-2. If unused, or in PSI5 mode, it is recommended that this pin be unterminated. Optionally, this pin can be tied to V_{SS}.
3,5	BUSSW_L	Low Side Bus Switch Driver	In PSI5 daisy chain mode, these pins are connected to the gate of an n-channel FET which connects BUSRTN to the next slave in the daisy chain. An external pulldown resistor is required on the gate of the n-channel FET as shown in Figure 1-4. Note: both pins provide the identical function. It is necessary to connect only one pin is to the bus switch gate. If unused, or in DSI3 mode, it is recommended that this pin be unterminated. Optionally, this pin can be tied to V_{SS}.
4,12, 14	TEST	Test Pin	It is recommended that these pins be unterminated. Optionally, this pin can be tied to V_{SS}.
6	V_{SS_PAD}	Supply Return	This pin is internally connected to the die attach pad. It is recommended that this pin be unterminated or connected to V_{SS}.
7,15	BUSRTN/V_{SS}	Supply Return	This pin is the supply return node.
8	TEST_SS_B	Slave Select	It is recommended that this pin be unterminated. Optionally, this pin can be connected to V_{BUF}.
9	TEST_SCLK	SPI Clock	It is recommended that this pin be unterminated. Optionally, this pin can be connected to V_{SS}.
10	TEST_MOSI	SPI Data In	It is recommended that this pin be unterminated. Optionally, this pin can be connected to V_{SS}.
11	TEST_MISO	SPI Data Out	This pin must be left unconnected.
13	V_{BUF}	Power Supply	This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies the internal regulators to provide immunity from EMC and supply dropouts. An external capacitor must be connected between this pin and V_{SS} as shown in Section 1.1 and Section 1.2.
16	BUS_I	Supply and Communication	This pin is connected to the supply line and supplies power to the device. An external capacitor must be connected between this pin and BUSRTN as shown in Section 1.1 and Section 1.2. This pin also modulates the response current for DSI3 and PSI5 communication and provides the supply for OTP programming.
17	PAD	Die Attach Pad	This pin is the die attach flag, and must be connected to V_{SS}. Reference Section 11 for die attach pad connection details.

SECTION 5 ELECTRICAL CHARACTERISTICS

5.1 Maximum Ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

#	Rating	Symbol	Value	Unit	Test Notes
 3381 3383	Supply Voltage (BUS_I/V_{CC}, BUS_O, BUSSW_H) Reverse Current externally limited to ≤ 160mA, t ≤ 80ms Continuous	 BUS_I_{REV} BUS_I_{MAX}	 -0.7 +20.0	 V V	 6 6
3384	V_{BUF}	V_{BUFMAX}	-0.3 to +7.0	V	6
3385	SCLK, SS_B, MOSI, MISO (High Z), PCM0/ARM0, PCM1/ARM1	V_{IOMAX}	-0.3 to V_{BUF}+0.3	V	6
3386	BUS_I/V_{CC} and BUS_O Continuous Current	I_{SUPMAX}	200	mA	6
3387	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	±2000	g	5
3390	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	±2000	g	5
3389	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	±4000	g	9
3388	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	±4000	g	9
3391	Drop Shock (to concrete, tile or steel surface, 10 drops, any orientation)	h_{DROP}	1.2	m	5
3392	Electrostatic Discharge (per AEC-Q100), External Pins BUS_I/V_{CC}, BUS_O, BUSRTN, HBM (100pF, 1.5kΩ)	V_{ESD}	±4000	V	5
 3393 3395	Electrostatic Discharge (per AEC-Q100) HBM (100pF, 1.5kΩ) CDM (R = 0Ω)	 V_{ESD} V_{ESD}	 ±2000 ±750	 V V	 5 5
 3396 3397	Temperature Range Storage Junction	 T_{stg} T_J	 -40 to +125 -40 to +150	 °C °C	 5 7
3400	Thermal Resistance	θ_{JA}	47	°C/W	7,10

5.2 Operating Range - DSI / PSI5

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
3398 10468 10467 10466	DSI3 Supply Voltage (V_{HIGH}), Measured at BUS_I * DSI3 Supply Voltage (V_{LOW}) Measured at BUS_I * PSI5 Supply Voltage (Excluding Sync Pulse) * Supply Voltage (Undervoltage)	V_{HIGH} V_{LOW} V_{PSI5} $V_{BUS\_I\_UV}$	-- 4.0 4.2 $V_{BUS\_I\_UV\_F}$	-- -- --	20.0 -- 16.0 V_{LOW_min}	V V V V	5,6,7 1 1 3,6
10469	Programming Voltage (I_{PP} ≤ 5 mA, 10°C ≤ T_A ≤ 40°C) Applied to BUS_I	V_{PP}	9.0	10.0	11.0	V	3,6
10470	ESD Operating Voltage (No Device Reset, C_{BUS_IN} = 220pF) Maximum ±15kV Air Discharge, 330pF, 2.0kΩ	$V_{BUS\_I\_ESD}$	$V_{BUS\_I\_LOW\_min}$	--	10.0	V	7,9
 10471 10490	Operating Temperature Range Production Tested Operating Temperature Range Guaranteed Operating Temperature Range	 T_A T_A	T_L -40 -40	 -- --	T_H +105 +125	 °C °C	 1 5,6,7
10472	Supply Power On Ramp Rate	$V_{CC\_RAMP\_SAT}$	0.00001	--	10	V/µs	6

5.3 Operating Range - SPI / I²C

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
10501 10502 10502 10504	Supply Voltage (V_{CC}=V_{BUF}) Measured at V_{BUF} Supply Voltage (V_{CC}=V_{BUF}) Measured at V_{BUF} * Supply Voltage (V_{CC}=V_{BUF}) Measured at V_{BUF} Supply Voltage (Undervoltage)	V_{CC_BUF} V_{CC_BUF} V_{CC_Lo} $V_{BUF\_UV\_OP}$	-- 3.135 2.80 $V_{BUF\_UV\_F}$	-- -- --	5.25 -- -- $V_{CC\_BUF\_min}$	V V V V	5,6,7 1 6 3
 10507 10508	Operating Temperature Range Production Tested Operating Temperature Range Guaranteed Operating Temperature Range	 T_A T_A	T_L -40 -40	 -- --	T_H +105 +125	 °C °C	 1 5,6,7
10509	Supply Power On Ramp Rate	$V_{CC\_RAMP\_SPI}$	0.00001	--	10	V/µs	6

5.4 Electrical Characteristics - Supply and I/O

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
 39203 39204 39205	Quiescent Supply Current V_{BUS_I} = 4V, DSI, PSI5 * V_{BUS_I} = 20V, DSI / PSI5 * V_{BUS_I} = 3.135V, SPI, I^2C *	 $I_{q\_4\_2}$ $I_{q\_20\_2}$ $I_{q\_31\_2}$	 4.0 4.0 --	 -- -- --	 9.0 9.0 9.0	 mA mA mA	 1 1 3,6
 10515 10519 10518 10517	Response Current DSI Low * DSI High * PSI5 Normal * PSI5 Low *	 $I_{R\_DSI\_1}$ $I_{R\_DSI\_2}$ I_{R_PSI5} $I_{R\_PSI5\_Low}$	 I_q + 10.5 $I_{R\_DSI\_1}$ + 10.5 I_q + 22.0 I_q + 11.0	 I_q + 12.0 $I_{R\_DSI\_1}$ + 12.0 I_q + 26.0 I_q + 13.0	 I_q + 13.5 $I_{R\_DSI\_1}$ + 13.5 I_q + 30.0 I_q + 15.0	 mA mA mA mA	 1 1 1 3,6
10521	In-Rush Current: Maximum Time at Peak Current (C_{VBUF} = 1µF) In-Rush Current = 60mA In-Rush Current = 30mA (Limited by Master)	 t_{INRUSH_60} t_{INRUSH_30}	 -- --	 -- --	 75 200	 µs µs	 6 9
10522	Internally Regulated Voltage (V_{BUF}, V_{BUS_I} = 4V, V_{BUS_I} = 20V) *	V_{BUF}	2.85	3.00	3.15	V	1
 10523 10542	Low Voltage Detection Threshold BUS_I Falling * V_{BUF} Falling *	 $V_{BUS\_I\_UV\_F}$ $V_{BUF\_UV\_F}$	 3.85 2.64	 3.95 2.74	 4.00 2.84	 V V	 3,6 3,6
 10525 10543	V_{BUF} External Capacitor Capacitance ESR (including interconnect resistance)	 C_{VBUF} ESR	 100 0	 1000 --	 2000 200	 nF mΩ	 7,9 7,9
10526	DSI3 V_{LOW} Detection Threshold (Section 7.1.1) $V_{LOW\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{HIGH\_max}$ V_{LOW} Detection Threshold *	V_{DELTA_THRESH}	V_{HIGH}-1.25	V_{HIGH}-1.0	V_{HIGH}-0.75	V	3,6
 10527 10545	DSI3 Discovery Mode Current Sense (Section 7.2.3) Sense Resistor I_{RESP} Detection Threshold ($I_{BUS\_O\_q} \le$ 24mA)	 R_{SENSE} I_{RESP_Offset}	 1.0 6	 1.3 12	 3.0 18	 Ω mA	 6 3,6
10528	PSI5 Synchronization Pulse $V_{PSI5\_min} \le (V_{BUS\_I} - V_{SS}) \le BUS\_I_{MAX}$ DC Sync Pulse Detection Threshold *	ΔV_{SYNC}	V_{PSI5}+1.0	V_{PSI5}+1.5	V_{PSI5}+2.0	V	3,6
10529	PSI5 Sync Pulse Pulldown Current	I_{SYNC_PD}	--	I_{RESP_PSI5}	--	mA	7
10530	Bus Switch Output High Voltage (BUSSW_L, I_{Load} = -100 µA)	$V_{BUSSW\_L\_OH}$	V_{BUF} - 0.35	--	V_{BUF}	V	3,6
10546	Bus Switch Output Low Voltage (BUSSW_L, I_{Load} = 100 µA)	$V_{BUSSW\_L\_OL}$	--	--	0.1	V	3,6
10531	Bus Switch Open Drain Output Current (V_{BUSSW_H}=V_{BUS_I})	$I_{BUSSW\_H\_OL}$	--	--	10	µA	3,6
10533	Bus Switch Output Low Voltage (BUSSW_H, I_{Load} = 100 µA)	$V_{BUSSW\_H\_OL}$	--	--	0.1	V	3,6
10549	Open Drain Output Pulldown Current (ARM0, ARM1, V_{ARM} = 1.5V)	I_{ODPD}	10	20	100	µA	3,6
10536	Open Drain Output Pullup Current (ARM0, ARM1, V_{ARM} = 1.5V)	I_{ODPU}	-100	-20	-10	µA	3,6
 21205 10547	Output High Voltage (MISO/SDA, PCM0/ARM0, PCM1/ARM1 V_{BUF} = VCC, I_{Load} = -1 mA V_{BUF} internally regulated, I_{Load} = -1 mA	 V_{OH} V_{OH_SAT}	 V_{BUF} - 0.2 V_{BUF} - 0.2	 -- --	 V_{BUF} V_{BUF}	 V V	 3,6 3,6
10547	Output Low Voltage (MISO/SDA, PCM0/ARM0, PCM1/ARM1 I_{Load} = 2 mA	V_{OL}	--	--	0.4	V	3,6
10537	Input High Voltage SS_B, SCLK/SCL, MOSI	V_{IH}	2.0	--	--	V	3,7
10560	Input Low VoltageSS_B, SCLK/SCL, MOSI	V_{IL}	--	--	1.0	V	3,7
10561	Input Voltage Hysteresis SS_B, SCLK, MOSI	V_{I_HYST}	--	0.250	--	V	7
10562	Input Current High (at V_{IH})(SCLK/SCL, MOSI)	I_{IH}	10	20	70	µA	6
10565	Input Current Low (at V_{IL})(SS_B)	I_{IL}	-70	-20	-10	µA	6
10563	MISO Output Leakage	I_{MISO_Lkg}	-10	--	10	µA	6

5.5 Electrical Characteristics - Temperature Sensor Signal Chain

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
10520	Temperature Measurement Range	T_{RANGE}	-50	--	+160	°C	7,9
10559	Temperature Output at 25°C	T_{25}	83	93	103	LSB	6,7
10558	Range of Output (8-Bit) Unsigned Temperature	T_{RANGE}	0	--	255	LSB	7,8,9
10557	Temperature Output Sensitivity (8-Bit)	T_{SENSE}		1.00		LSB/°C	6,7
10556	Temperature Output Accuracy (8-Bit)	T_{ACC}	-10		+10	°C	6,7
10555	Temperature Output Noise RMS(8-Bit) Standard Deviation of 50 readings, f_{Samp} = 8kHz	T_{RMS}	—	—	+2	LSB	6,7

5.6 Electrical Characteristics - Inertial Sensor Signal Chain

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Sensitivity						
 10585 10584	Total Sensitivity Error Including Linearity (From Trim Target, Output @ 0Hz) Medium g, Lateral or Z-Axis, Verified with a 15g Range * High g, Lateral or Z-Axis, Verified with a 50g Range *	$SENS_{ERRM}$ $SENS_{ERRH}$	+5 +5	-- --	+5 +5	% %	10602 10612
10602	Medium g Standard Trim Range 12-Bit Sensitivity Target, Lateral or Z-Axis ± 62 g Range (± 2047 LSB, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00) *	$SENS_{062M}$	31.3650	33.0161	34.6670	LSB/g	1
10612	High g Standard Trim Range 12-Bit Sensitivity Target, Lateral or Z-Axis ± 187 g Range (± 2047 LSB, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00) *	$SENS_{187H}$	10.3990	10.9465	11.4940	LSB/g	1
	Offset						
 10627 10626	Digital Offset Before Offset Cancellation 12-Bit, Lateral or Z-Axis Medium g (25g Range, scales with user sensitivity scaling) * High g (100g Range, scales with user sensitivity scaling) *	OFF_{Med_1} OFF_{High_1}	-100 -100	-- --	+100 +100	LSB LSB	1 1
10583	Digital Offset After Offset Cancellation, Lateral or Z-Axis, All Ranges, 12-Bit	$OFFCANC_{12Bit}$	-1	0	+1	LSB	6,8,9
10619	Continuous Offset Monitor Limit (U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00) 12-Bit: Scales with user gain, Medium g = ~5g, High g = ~15g	OFF_{MON}	-164	--	+164	LSB	7,8,9
	Sensor						
 10635 10628 10636 10637	Range of Output (SPI, DSI3, Lateral or Z-Axis, All Ranges) Signed Sensor Data, 10-Bit Signed Sensor Data, 12-Bit Signed Error Code, 10-Bit Signed Error Code, 12-Bit	$RANGE_{Signed\_10}$ $RANGE_{Signed\_12}$ ERR_{Signed_10} ERR_{Signed_12}	-511 -2047 -- --	-- -- -512 -2048	+511 +2047 -- --	LSB LSB LSB LSB	7,8,9 7,8,9 7,8,9 7,8,9
 10638 10639 10640	Range of Output (SPI, DSI3, Lateral or Z-Axis, All Ranges) UnSigned Sensor Data, 10-Bit UnSigned Sensor Data, 12-Bit Unsigned Error Code, 10-Bit, 12-Bit	$RANGE_{Unsigned\_10}$ $RANGE_{Unsigned\_12}$ $ERR_{Unsigned}$	1 1 --	-- -- 0	1023 4095 --	LSB LSB LSB	7,8,9 7,8,9 7,8,9
10634	Range of Output (PSI5, Lateral or Z-Axis, All Ranges) Signed Sensor Data, 10-Bit	$RANGE_{Signed\_10}$	-480	--	+480	LSB	7,8,9
 10645 10647	Cross-Axis Sensitivity, Medium g or High g, Lateral or Z-Axis, All Ranges Z-axis to X-Axis, Y-axis to X-Axis, Z-axis to Y-Axis, X-axis to Y-Axis * X-axis to Z-Axis, Y-axis to Z-Axis *	V_{ZX}, V_{YX}, V_{ZY}, V_{XY} V_{XZ}, V_{YZ}	-5 -5	-- --	+5 +5	% %	6 6
 10669 10670	Non-Linearity (12-Bit, Lateral or Z-Axis, All Ranges) Differential Non-Linearity, (No Missing Codes) * Integral Non-Linearity, (Least Squares BFSL) *	DNL INL	-- --	-- --	+1.0 +20.0	LSB LSB	6 6
 10663 10682 10681 10680	Supply Coupling (C_{BUF} = 1µf, 12-Bit, DSI3, PSI5, Lateral or Z-Axis, All Ranges) 1kHz ≤ f_n ≤ 10kHz, BUS_I = 8.0V± 2.0V (Represents PSI5 Sync Pulse) 10kHz ≤ f_n ≤ 100kHz, BUS_I = 6.0V± 1.0V (Represents DSI3 BRC) 100kHz ≤ f_n ≤ 1MHz, BUS_I=6.0V± 0.5V (Represents DSI3/PSI5 Response) 1MHz ≤ f_n ≤ 20MHz, BUS_I = 6.0V± 0.1V(Represents Response Harmonics)	PSC_{PSI5} PSC_{DSI3C} PSC_{DSI3R} PSC_{SATH}	-- -- -- --	-- -- -- --	1 1 1 1	LSB LSB LSB LSB	6 6 6 6
 10675 10683	Supply Coupling (C_{BUF} = 0.1µf, 12-Bit, SPI, Lateral or Z-Axis, All Ranges) 1kHz ≤ f_n ≤ 20MHz, V_{BUF} = 5.0V± 0.1V 1kHz ≤ f_n ≤ 20MHz, V_{BUF} = 3.3V± 0.1V	PSC_{SPI5} PSC_{SPI3}	-- --	-- --	2 2	LSB LSB	6 6

The offset before offset cancellation scales with the user gain. The higher the gain (lower range), the higher the offset. The table below lists the adjusted offset specification limits for some SPI and DSI3 12-bit user gain settings.

User Range (g)	Offset (LSB, 12-Bit)
Medium g	
15.5	± 162
16	± 157
20	± 126
25	± 100
35	± 72
50	± 50
60	± 42
62	± 41
62.5	± 41
75	± 34
85.3	± 30
100	± 25
105	± 24
112.5	± 23
125	± 21
128	± 20
150	± 17
High g	
50	± 200
60	± 167
62	± 162
62.5	± 160
100	± 100
105	± 96
112.5	± 89
125	± 80
128	± 79
150	± 67
187	± 54
250	± 40
312.5	± 32
375	± 27
500	± 20

The table below lists the offset before offset cancellation limits for some PSI5 10-bit user gain settings.

User Range (g)	Offset (LSB, 10-Bit)
Medium g	
15, PSI5	± 40
20, PSI5	± 30
30, PSI5	± 20
60 PSI5	± 10
120 PSI5	± 5
High g	
60, PSI5	± 40
120, PSI5	± 20
240 PSI5	± 10
480 PSI5	± 5

5.7 Electrical Characteristics - Inertial Sensor Signal Chain

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Noise: Lateral Sensor						
	System Output Noise Peak (12-Bit) Medium g Range = 50g, High g Range = 125g, Lateral						
10653	Max. Deviation from Mean, Min. 2000 values, Min. f_{Samp} = 2kHz, LPF = 180Hz, 2-Pole *	n_{Peak_180}	-3	--	+3	LSB	6
10655	Max. Deviation from Mean, Min. 2000 values, Min. f_{Samp} = 2kHz, LPF = 400Hz, 4-Pole *	n_{Peak_400}	-4	--	+4	LSB	6
	System Output Noise Average (12-Bit) Medium g Range = 50g, High g Range = 125g, Lateral						
10654	Standard Deviation, Min. 2000 values, Min. f_{Samp} = 2kHz, LPF = 180Hz, 2-Pole *	n_{RMS_180}	--	--	+1.0	LSB	6
10656	Standard Deviation, Min. 2000 values, Min. f_{Samp} = 2kHz, LPF = 400Hz, 4-Pole *	n_{RMS_400}	--	--	+1.0	LSB	6
	Noise: Z-Axis Sensor						
	System Output Noise Peak (12-Bit) Medium g Range = 50g, High g Range = 125g, Z-Axis						
10659	Max. Deviation from Mean, Min. 2000 values, Min. f_{Samp} = 2kHz, LPF = 180Hz, 2-Pole *	n_{Peak_180}	-8	--	+6	LSB	6
10661	Max. Deviation from Mean, Min. 2000 values, Min. f_{Samp} = 2kHz, LPF = 400Hz, 4-Pole *	n_{Peak_400}	-8	--	+8	LSB	6
	System Output Noise Average (12-Bit) Medium g Range = 50g, High g Range = 125g, Z-Axis						
10660	Standard Deviation, Min. 2000 values, Min. f_{Samp} = 2kHz, LPF = 180Hz, 2-Pole *	n_{RMS_180}	--	--	+2.0	LSB	6
10662	Standard Deviation, Min. 2000 values, Min. f_{Samp} = 2kHz, LPF = 400Hz, 4-Pole *	n_{RMS_400}	--	--	+2.0	LSB	6

The signal noise scales with the user gain and with signal bandwidth. The higher the gain (lower range), the higher the noise. The wider the bandwidth, the higher the noise. The table below lists the adjusted specification limits for some SPI and DSI3 12-bit user gain settings and low pass filter selections.

User Range (g)	Lateral											
	LPF 400Hz, 4p		LPF 400Hz, 3p		LPF 180Hz, 2p		LPF 325Hz, 3p		LPF 1500Hz, 4p		LPF 800Hz, 4p	
	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit
	Medium g											
15.5	14	4	14	4	10	3	13	4	26	7	20	5
25	9	3	9	3	6	2	8	2	17	4	12	3
50	4	1	5	1	3	1	4	1	8	2	6	2
62.5	4	1	4	1	3	1	4	1	7	2	5	2
100	3	1	3	1	2	1	2	1	4	1	3	1
125	2	1	2	1	2	1	2	1	4	1	3	1
150	2	1	2	1	1	1	2	1	3	1	2	1
	High g											
50	11	3	11	3	8	2	10	3	21	5	15	4
62.5	9	3	9	3	6	2	8	2	17	4	12	3
100	5	2	6	2	4	1	5	2	11	3	8	2
125	4	1	4	1	3	1	4	1	8	2	6	2
187	3	1	3	1	2	1	3	1	6	2	4	1
250	3	1	3	1	2	1	2	1	4	1	3	1
312.5	2	1	2	1	2	1	2	1	4	1	3	1
375	2	1	2	1	1	1	2	1	3	1	2	1
500	2	1	2	1	1	1	1	1	2	1	2	1

User Range (g)	Z-Axis											
	LPF 400Hz, 4p		LPF 400Hz, 3p		LPF 180Hz, 2p		LPF 325Hz, 3p		LPF 1500Hz, 4p		LPF 800Hz, 4p	
	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit	Peak LSB 12-Bit	RMS LSB 12-Bit
	Medium g											
15.5	27	7	28	7	20	5	25	7	53	14	39	10
25	17	5	18	5	12	3	16	4	33	9	24	6
50	8	2	9	2	6	2	8	2	16	4	12	3
62.5	7	2	7	2	5	2	7	2	13	4	10	3
100	5	1	5	2	3	1	4	1	9	2	6	2
125	4	1	4	1	3	1	4	1	7	2	5	2
150	3	1	3	1	2	1	3	1	6	2	4	1
	High g											
50	21	6	22	6	15	4	20	5	41	11	30	8
62.5	17	5	18	5	12	3	16	4	33	9	24	6
100	11	3	11	3	8	2	10	3	21	6	15	4
125	8	2	9	2	6	2	8	2	16	4	12	3
187	6	2	6	2	4	1	6	2	11	3	8	2
250	5	1	5	2	3	1	4	1	9	2	6	2
312.5	4	1	3	1	3	1	3	1	7	2	5	2
375	3	1	3	1	2	1	2	1	6	2	4	1
500	3	1	3	1	2	1	2	1	5	1	3	1

The table below lists the adjusted specification limits for some PSI5 10-bit user gain settings and low pass filter selections.

User Range (g)	Lateral					
	LPF 400Hz, 4p		LPF 400Hz, 3p		LPF 800Hz, 4p	
	Peak LSB 10-Bit	RMS LSB 10-Bit	Peak LSB 10-Bit	RMS LSB 10-Bit	Peak LSB 10-Bit	RMS LSB 10-Bit
	Medium g					
30, PSI5	1.7	0.4	1.7	0.4	2.3	0.6
60, PSI5	0.8	0.2	0.9	0.2	1.2	0.3
120, PSI5	0.4	0.1	0.4	0.1	0.6	0.2
	High g					
60, PSI5	2.1	0.6	2.1	0.6	2.9	0.8
120, PSI5	1.1	0.3	1.1	0.3	1.5	0.4
240 PSI5	0.6	0.2	0.6	0.2	0.8	0.3
480 PSI5	0.6	0.2	0.6	0.2	0.8	0.2

User Range (g)	Z-Axis					
	LPF 400Hz, 4p		LPF 400Hz, 3p		LPF 800Hz, 4p	
	Peak LSB 10-Bit	RMS LSB 10-Bit	Peak LSB 10-Bit	RMS LSB 10-Bit	Peak LSB 10-Bit	RMS LSB 10-Bit
	Medium g					
30, PSI5	3.3	0.8	3.4	0.9	4.7	1.2
60, PSI5	1.7	0.4	1.7	0.4	2.3	0.6
120, PSI5	0.8	0.2	0.9	0.2	1.2	0.3
	High g					
60, PSI5	4.1	1.1	4.2	1.1	5.8	1.5
120, PSI5	2.1	0.6	2.1	1.0	2.9	0.8
240 PSI5	1.1	0.3	1.1	0.3	1.5	0.5
480 PSI5	0.6	0.2	0.6	0.2	0.8	0.3

5.8 Electrical Characteristics - Inertial Sensor Self Test

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic		Symbol	Min	Typ	Max	Units	Test Notes
	Med g Lateral Self Test, 62g, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00			ΔST_{MIN}	ΔST_{NOM}	ΔST_{MAX}		
	Hi Self Test, 44.50g, 10-Bit Signed Delta from Offset		$ST_{MH\_62X\_10}$	220	367	511	LSB	7
	Hi Self Test, 44.50g, 12-Bit Signed Delta from Offset		$ST_{MH\_62X\_12}$	881	1470	2047	LSB	7
	Hi Self Test, 44.50g, 16-Bit SPI/PSI5 Extended Signed Delta from Offset		$ST_{MH\_62X\_16}$	14080	23488	32767	LSB	7
10688	Hi Self Test, 44.50g, 16-Bit Signed SNSDATAx Register Delta from Offset	*	$ST_{MH\_62X\_13}$	1763	2939	4115	LSB	1
	Med g Z-Axis Self Test, 62g, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00			ΔST_{MIN}	ΔST_{NOM}	ΔST_{MAX}		
	Hi Self Test, 21.65g, 10-Bit Signed Delta from Offset		$ST_{MH\_62Z\_10}$	107	178	251	LSB	7
	Hi Self Test, 21.65g, 12-Bit Signed Delta from Offset		$ST_{MH\_62Z\_12}$	428	715	1001	LSB	7
	Hi Self Test, 21.65g, 16-Bit SPI/PSI5 Extended Signed Delta from Offset		$ST_{MH\_62Z\_16}$	6848	11392	16064	LSB	7
30135	Hi Self Test, 21.65g, 16-Bit Signed SNSDATAx Register Delta from Offset	*	$ST_{MH\_62Z\_13}$	857	1430	2002	LSB	1
	High g Lateral Self Test, 187g, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00			ΔST_{MIN}	ΔST_{NOM}	ΔST_{MAX}		
	Hi Self Test, 55.00g, 10-Bit Signed Delta from Offset		$ST_{HH\_187X\_10}$	90	150	212	LSB	7
	Hi Self Test, 55.00g, 12-Bit Signed Delta from Offset		$ST_{HH\_187X\_12}$	361	603	845	LSB	7
	Hi Self Test, 55.00g, 16-Bit SPI/PSI5 Extended Signed Delta from Offset		$ST_{HH\_187X\_16}$	5760	9600	13568	LSB	7
10686	Hi Self Test, 55.00g, 16-Bit Signed SNSDATAx Register Delta from Offset	*	$ST_{HH\_187X\_13}$	723	1206	1689	LSB	1
	High g Z-Axis Self Test, 187g, U_SNS_SHIFT = 0x2, U_SNS_MULT = 0x00			ΔST_{MIN}	ΔST_{NOM}	ΔST_{MAX}		
	Hi Self Test, 63.50g, 10-Bit Signed Delta from Offset		$ST_{HH\_187Z\_10}$	104	173	244	LSB	7
	Hi Self Test, 63.50g, 12-Bit Signed Delta from Offset		$ST_{HH\_187Z\_12}$	417	695	974	LSB	7
	Hi Self Test, 63.50g, 16-Bit SPI/PSI5 Extended Signed Delta from Offset		$ST_{HH\_187Z\_16}$	6656	11072	15616	LSB	7
30137	Hi Self Test, 63.50g, 16-Bit Signed SNSDATAx Register Delta from Offset	*	$ST_{HH\_187Z\_13}$	834	1390	1947	LSB	1
  10678 10690	Self Test Accuracy: Δ from Stored Value, including Sensitivity Error (12-Bit, Lateral or Z-Axis, All Ranges) 25 C, Post Pre-conditioning -40 C ≤ TA ≤ 125 C	 * *	 ΔSTACC_25P ΔSTACC_T	 -2 -10	 -- --	 +2 +10	 % %	 6 1
  10692 10692	Self Test Delta Offset: Δ Offset from Pre-Self Test to Post Self Test (12-Bit, Lateral or Z-Axis, All Ranges) 25 C -40 C ≤ TA ≤ 125 C		 ΔSTOFF_25 ΔSTOFF_T	 -2 -4	 -- --	 +2 +4	 LSB LSB	 1 1
 38350 38351	Self Test Cross Coupling (12-Bit, Lateral or Z-Axis, All Ranges) Channel 1 with Channel 0 Self-Test Active Channel 0 with Channel 1 Self-Test Active		 ΔSTCh0_1 ΔSTCh1_0	 -10 -10	 -- --	 +10 +10	 LSB LSB	 1 1
	Digital Self Test							
     44629 44630 44631 44632	Digital Self Test, U_SNS_SHIFT = 0x0, U_SNS_MULT = 0x00 Note: if OC is enabled, Digital Self test will not converge unless the OC fast startup has reached Phase 4 to allow for offset convergence to ±1 LSB Note: the digital self test scales with user gain. reference the latest application notes for detail on digital self test with different user gains Digital Self Test 0xC0, 16-Bit Signed SNSDATAx Register Value Digital Self Test 0xD0, 16-Bit Signed SNSDATAx Register Value Digital Self Test 0xE0, 16-Bit Signed SNSDATAx Register Value Digital Self Test 0xF0, 16-Bit Signed SNSDATAx Register Value		 DST_{C0} DST_{D0} DST_{E0} DST_{F0}	 E77F 0FA3 EFA2 07B7	 E780 0FA4 EFA3 07B8	 E781 0FA5 EFA4 07B9	 HEX HEX HEX HEX	 7 7 7 7

5.9 Electrical Characteristics - Lateral Inertial Sensor Overload

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

#	Characteristic		Symbol	Min	Typ	Max	Units	Test Notes
	Acceleration Range, Lateral Transducer							
10694	Medium g		$g_{g\text{-cell\_ClipMedX}}$	± 500	--	--	g	7
10693	High g		$g_{g\text{-cell\_ClipHiX}}$	± 2000	--	--	g	7
21074	Digital Clipping Limit (Medium g Lateral, must clip before transducer and ADC)		$g_{Dig\_ClipMedXHi}$	± 400	--	--	g	7
21082	Digital Clipping Limit (High g Lateral, must clip before transducer and ADC)		$g_{Dig\_ClipHiXHi}$	± 1500	--	--	g	7

5.10 Electrical Characteristics - Z-Axis Inertial Sensor Overload

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

#	Characteristic		Symbol	Min	Typ	Max	Units	Test Notes
	Acceleration Range, Z-Axis Transducer							
10698	Medium g		$g_{g\text{-cell\_ClipMedZ}}$	± 500	--	--	g	7
10699	High g		$g_{g\text{-cell\_ClipHiZ}}$	± 2000	--	--	g	7
21105	Digital Clipping Limit (Medium g Z-Axis, must clip before transducer and ADC)		$g_{Dig\_ClipMedZHi}$	± 400	--	--	g	7
21113	Digital Clipping Limit (High g Z-Axis, must clip before transducer and ADC)		$g_{Dig\_ClipHiZHi}$	± 1500	--	--	g	7

5.11 Dynamic Electrical Characteristics - DSI3

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Command Reception (General)						
10709	V_{HIGH} Low Pass Filter Time Constant (Section 7.1.1)	t_{VHIGH_RC}	60	120	180	µs	7,9
10722	V_{HIGH} Detection Analog Delay (Section 7.1.1)	t_{VHIGH_Delay}	--	--	600	ns	7,9
10721	Command Valid time (Section 7.1.1)	t_{Cmd_Valid}	--	2	--	µs	7,9
	Response Transmission (General, Slew Control Enabled, Section 7.3.3)						
10710	Response Slew Time: 2.0mA to 10.0mA, 10.0mA to 2.0mA	t_{SLEW1_RESP}	350	400	500	ns	1,7,9
10726	Response Slew Time: 4.0mA to 20.0mA, 20.0mA to 4.0mA	t_{SLEW2_RESP}	350	400	500	ns	1,7,9
10725	$t_{SLEW1\_RESP} - t_{SLEW2\_RESP}$	Δt_{SLEW}	-100	--	100	ns	7,9
10724	$t_{SLEW1\_RESP\_Rise} - t_{SLEW2\_RESP\_Fall}$	Δt_{SLEW_rf}	-250	--	250	ns	7,9
10723	Response Current Activation Time: Current Activated to 50%	t_{ACT_RESP}	200	--	400	ns	3,7,9
	Response Transmission (General, Slew Control Disabled, Section 7.3.3)						
10727	Response Slew Time: 2.0 mA to 10.0 mA, 10.0 to 2.0 mA	t_{nSLEW1_RESP}	--	--	300	ns	7,9
10728	Response Slew Time: 4.0 mA to 20.0 mA, 20.0mA to 4.0mA	t_{nSLEW2_RESP}	--	--	300	ns	7,9
10729	$t_{SLEW1\_RESP} - t_{SLEW2\_RESP}$	Δt_{nSLEW}	-300	--	300	ns	7,9
10730	$t_{SLEW1\_RESP\_Rise} - t_{SLEW2\_RESP\_Fall}$	Δt_{nSLEW_rf}	-300	--	300	ns	7,9
10731	Response Current Activation Time: Current Activated to 50%	t_{nACT_RESP}	--	--	300	ns	7,9
	Command Reception (Discovery Mode)						
10719	Command Start Time (Section 7.2)	t_{START_DISC}	t_{POR_DSI}	--	13.5	ms	7,8,9
10734	Command Bit Time (Section 7.2)	$t_{DISC\_BitTime}$	14	16	18	µs	7,8,9
10733	Command Transmission Period (Section 7.2)	t_{PER_DISC}	125	--	--	µs	7,8,9
10732	Command Blocking Time, Discovery Mode (Section 7.1.1)	$t_{CmdBlock\_DISC}$	--	96	--	µs	7,8,9
	Response Transmission (Discovery Mode)						
30078	Idle Current Sample Delay (Section 7.2)	t_{DISC_DLY}	--	48	--	µs	7,8,9
30079	Idle Current Sample Time (Section 7.2)	$t_{DISC\_ICCQ\_SAMP}$	--	15	--	µs	7,8,9
10718	Response Start Delay (Section 7.2)	$t_{START\_DISC\_RSP}$	--	64	--	µs	7,8,9
10738	Response Ramp Time (Section 7.2)	$t_{DISC\_Ramp\_RSP}$	--	16	--	µs	7,8,9
10737	Response Ramp Rate (Section 7.2)	I_{DISC_Ramp}	--	1.5	--	mA/µs	7,8,9
10736	Response Idle Time (Section 7.2)	$t_{DISC\_Idle\_RSP}$	--	16	--	µs	7,8,9
10735	Response Peak Current (Section 7.2)	I_{DISC_Peak}	--	$2*I_{RESP}$	--	mA	7,8,9
30081	Response Current Sample Delay (Section 7.2)	$t_{IDISC\_Samp\_Dly}$	--	65	--	µs	7,8,9
30080	Response Current Sample Time (Section 7.2)	t_{IDISC_Samp}	--	31	--	µs	7,8,9
	Command Reception (Command and Response Mode)						
10717	Command Bit Time (Section 7.3)	$t_{Cmd\_BitTime}$	--	8	--	µs	7,8,9
10741	Command Transmission Period (Section 7.3)	t_{PER_CRM}	475	--	--	µs	7,8,9
10740	Command Blocking Time, CRM (Section 7.1.1)	$t_{CmdBlock\_CRM}$	--	455	--	µs	7,8,9
10739	Command Blocking Start Time, CRM (Section 7.1.1)	$t_{CmdBlock\_ST\_CRM}$	--	290	--	µs	7,8,9
	Response Transmission (Command and Response Mode)						
10716	Response Chip Time	t_{CHIP_CRM}	--	5	--	µs	7,8,9
10742	Response Start Time (Section 7.3)	t_{START_CRM}	--	295	--	µs	7,8,9
	Command Reception (Periodic Data Collection Mode)						
10715	Command Bit Time (Section 7.4)	$t_{Cmd\_BitTime}$	--	8	--	µs	7,8,9
10743	Command Transmission Period (Section 7.4)	t_{PER_PDCM}	50	--	--	µs	7,8,9
	Response Transmission (Periodic Data Collection Mode)						
10714	Response Chip Time Typical (Section 6.2.14.2)	t_{CHIP_PDCM}	1.0	--	5.0	µs	7,8,9
10746	Min Programmed Start Time: PDCM_RSPSTx < 0x0015	$t_{START\_PDCM\_Min}$	--	20	--	µs	7,8,9
10745	Min Programmed Start Time: BDM Enabled	$t_{START\_PDCMBDMMin}$	--	51	--	µs	7,8,9
10744	Max Programmed Start Time: PDCM_RSPSTx = 0x1FFF	$t_{START\_PDCM\_Max}$	--	8191	--	µs	7,8,9
	Response Transmission (Background Diagnostic Mode)						
10713	Response Chip Time	t_{CHIP_CRM}	--	5	--	µs	7,8,9
10747	Response Start Time (Section 7.4)	t_{START_BDM}	--	20	--	µs	7,8,9
10712	DSI Data Latency	t_{LAT_DSI}	0	--	2.00	µs	7,8
	OTP Program Timing						
10711	Time to program an OTP User Region	$t_{OTP\_WRITE\_MAX}$	--	--	10	ms	7,8,9

5.12 Dynamic Electrical Characteristics - PSI5

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Initialization Timing						
10748	Phase 1	t_{PSI5_INIT1}	--	133	--	ms	7,8,9
10758	Phase 2 (Synchronous Mode, k = 4, t_{S-S} = 500µs)	$t_{PSI5\_INIT2\_10s}$	--	256 * t_{S-S}	--	s	7,8,9
10757	Phase 2 (Asynchronous Mode, k = 8)	$t_{PSI5\_INIT2\_10a}$	--	512 * t_{ASYNC}	--	s	7,8,9
10756	Phase 3 (Synchronous Mode, t_{S-S} = 500µs)	$t_{PSI5\_INIT3\_10s}$	--	2 * t_{S-S}	--	s	7,8,9
10755	Phase 3 (Asynchronous Mode)	$t_{PSI5\_INIT3\_10a}$	--	2 * t_{ASYNC}	--	s	7,8,9
10754	PSI5 Self Test Start Time	t_{PSI5ST_START}	--	133	--	ms	7,8
10753	PSI5 Self Test Time	t_{ST}	--	104	--	ms	7,8
10752	Self Test Repetitions	ST_RPT	0	--	4		7,8
41756	Programming Mode Entry Window	t_{PME}	--	75	--	ms	7,8,9
	Synchronization Pulse						
10759	Reset to first sync pulse (Program Mode Entry)	t_{RS_PM}	53	--	--	ms	7,8,9
10779	Reset to first sync pulse (Normal Mode)	t_{RS}	t_{PSI5_INIT1}	--	--	s	7,8,9
10778	Sync Pulse Period	t_{S-S}	175	--	--	µs	7,8,9
10777	Sync Pulse Width	t_{SYNC}	9	--	--	µs	7,8,9
10776	Sync Pulse Reference LPF time constant	t_{SYNC_LPF}	120	280	--	µs	7,9
10775	Sync Pulse Reference Discharge Start Time	$t_{SYNC\_LPF\_RST\_ST}$	--	9.0	--	µs	7,9
10774	Sync Pulse Reference Discharge Activation Time	$t_{SYNC\_LPF\_RST}$	--	154	--	µs	7,9
10773	Sync Pulse Detection Disable Time (PDCM_CMD_B = 0)	$t_{SYNC\_OFF\_500}$	--	450	--	µs	7,8,9
10772	Analog Delay of Sync Pulse Detection	$t_{A\_SYNC\_DLY}$	50	--	600	ns	7,9
10771	Sync Pulse Pulldown Function Delay Time	t_{PD_DLY}	--	9.0	--	µs	7,9
10770	Sync Pulse Pulldown Function Activate Time	t_{PD_ON}	--	16	--	µs	7,8
10769	Sync Pulse Detection Jitter	t_{SYNC_JIT}	0	--	0.5	µs	7,8
10768	Data Transmission Single Bit Time (PSI5 Standard Bit Rate)	$t_{BIT\_Standard}$	--	8.00	--	µs	7,8,9
10767	Data Transmission Single Bit Time (PSI5 High Bit Rate)	t_{BIT_HI}	--	5.30	--	µs	7,8,9
	Response Current Transmission (No external Components)						
10766	Response Slew Time: 20% to 80% of I_{R_PSI5}	t_{SLEW1_RESP}	350	400	500	ns	1,7,9
10765	Position of bit transition (All except 5.3us)	$t_{Bittrans\_LowBaud}$	49	50	51	%	8,9
10780	Position of bit transition (5.3us)	$t_{Bittrans\_HighBaud}$	49	—	51	%	8,9
10764	Asynchronous Response Time	t_{ASYNC}	--	228	--	µs	7,8,9
	Time Slots						
10763	Min Programmed Time Slot: PDCM_RSPSTx < 0x0014	$t_{TIMESLOTx\_MIN}$	--	20	--	µs	7,8,9
10790	Max Programmed Time Slot: PDCM_RSPSTx = 0x1FFF	$t_{TIMESLOTx\_MAX}$	--	8191	--	µs	7,8,9
10789	Default Time Slot (PDCM_RSPSTx = 0x0000)	$t_{TIMESLOT\_DFLT}$	--	20	--	µs	7,8,9
10788	Time Slot Resolution	$t_{TIMESLOTx\_RES}$	--	1.0	--	µs/LSB	7,8,9
10787	Sync pulse to Daisy Chain Default Time Slot 0	$t_{TIMESLOT\_DC0}$	--	46.5	--	µs	7,8,9
10786	Sync pulse to Daisy Chain Default Time Slot 1 (Low)	$t_{TIMESLOT\_DC1\_L}$	--	192	--	µs	7,8,9
10785	Sync pulse to Daisy Chain Default Time Slot 2 (Low)	$t_{TIMESLOT\_DC2\_L}$	--	350	--	µs	7,8,9
10784	Sync pulse to Daisy Chain Default Time Slot 1 (High)	$t_{TIMESLOT\_DC1\_H}$	--	150	--	µs	7,8,9
10783	Sync pulse to Daisy Chain Default Time Slot 2 (High)	$t_{TIMESLOT\_DC2\_H}$	--	260	--	µs	7,8,9
10782	Sync pulse to Daisy Chain Default Time Slot 3 (High)	$t_{TIMESLOT\_DC3\_H}$	--	380	--	µs	7,8,9
10781	Sync pulse to Daisy Chain Programming Time Slot	$t_{TIMESLOT\_DCP}$	--	46.5	--	µs	7,8,9
10762	PSI5 Data Latency	t_{LAT_PSI5}	0	--	1.00	µs	7,8
	Bus Switch Output Activation Time (C = 50pF)						
10761	From last bit of "SetAdr" Response to 80% of $V_{BUS\_SW\_OH}$	t_{BUS_SW}	—	—	300	µs	7
	PSI5 Programming Mode Sync Pulse Period						
10760	The user must provide a sync pulse period within this range to guarantee Programming Mode communications	t_{S-S_PM}	490	500	510	µs	7,8,9
	OTP Program Timing						
10793	Time to program one OTP User Region	$t_{OTP\_WRITE\_MAX}$	--	--	10	ms	7,8,9

5.13 Dynamic Electrical Characteristics - SPI

$V_{CC\_BUF\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{CC\_BUF\_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
10794	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) Clock (SCLK) period (10% of V_{CC} to 10% of V_{CC})	t_{SCLK}	88	--	--	ns	6
10801 10802	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) Clock (SCLK) high time (90% of V_{CC} to 90% of V_{CC}) Clock (SCLK) low time (10% of V_{CC} to 10% of V_{CC})	t_{SCLKH} t_{SCLKL}	30 30	-- --	-- --	ns ns	6 6
10800 10803	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) Clock (SCLK) rise time (10% of V_{CC} to 90% of V_{CC}) Clock (SCLK) fall time (90% of V_{CC} to 10% of V_{CC})	t_{SCLKR} t_{SCLKF}	-- --	10 10	25 25	ns ns	7 7
10799	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) SS_B asserted to SCLK high (SS_B = 10% of V_{CC} to SCLK = 10% of V_{CC})	t_{LEAD}	50	--	--	ns	6
10798	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) SS_B asserted to MISO valid (SS_B = 10% of V_{CC} to MISO = 10/90% of V_{CC})	t_{ACCESS}	--	--	50	ns	6
10797	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) Data setup time (MOSI = 10/90% of V_{CC} to SCLK = 10% of V_{CC})	t_{SETUP}	20	--	--	ns	6
10796 10804	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) MOSI Data hold time (SCLK = 90% of V_{CC} to MOSI = 10/90% of V_{CC}) MISO Data hold time (SCLK = 90% of V_{CC} to MISO = 10/90% of V_{CC})	t_{HOLD_IN} t_{HOLD_OUT}	10 0	-- --	-- --	ns ns	6 6
10795	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) SCLK low to data valid (SCLK = 10% of V_{CC} to MISO = 10/90% of V_{CC})	t_{VALID}	--	--	30	ns	6
10807	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) SCLK low to SS_B high (SCLK = 10% of V_{CC} to SS_B = 90% of V_{CC})	t_{LAG}	60	--	--	ns	6
10806	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) SS_B high to MISO disable (SS_B = 90% of V_{CC} to MISO = Hi Z)	$t_{DISABLE}$	--	--	60	ns	6
  10805 10813 10812	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) SS_B high to SS_B low (SS_B = 90% of V_{CC} to SS_B = 90% of V_{CC}) Following Sensor Data Request Commands Following Register Reads/Writes Registers Following Register Write to the UF_REGION_W Register	t_{SSN_SENSE} t_{SSN_R} t_{SSN_UF01}	500 500 50	-- -- --	-- -- --	ns ns µs	6 6 6
10810	Time Between Sensor Data Requests (Same Channel, SPI Only, Arm Enabled)	$t_{ACC\_REQ\_x}$	15	--	--	µs	6
 10809 10817 10816	Arming Output Activation Time (ARM0, ARM1, $I_{ARM} = 200\mu$A) Moving Average and Count Arming Modes Unfiltered Mode Activation Delay Unfiltered Mode Arm Assertion Time	t_{ARM} $t_{ARM\_UF\_DLY}$ $t_{ARM\_UF\_ASSERT}$	0 0 5.00	-- -- --	1.50 1.50 6.00	µs µs µs	6 6 6
10808	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) SCLK low to SS_B low (SCLK = 10% of V_{CC} to SS_B = 90% of V_{CC})	t_{CLKSS}	50	--	--	ns	6
10815	Serial Interface Timing (See Figure 9-4, $C_{MISO} \leq 80$pF, $R_{MISO} \geq 10$kΩ) SS_B high to SCLK high (SS_B = 90% of V_{CC} to SCLK = 90% of V_{CC})	t_{SSCLK}	50	--	--	ns	7
10818	SPI Data Latency	t_{LAT_SPI}	--	--	1	µs	7,8
	Pin Capacitance (MISO, MOSI, SCLK, SS_B to VSS)	C_{SPI_PIN}	--	--	10	pF	7

5.14 Dynamic Electrical Characteristics - I^2C

$V_{CC\_BUF\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{CC\_BUF\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Clock (SCL) Period (30% of V_{CC} to 30% of V_{CC})						
10819	100kHz Mode	t_{SCLK_100}	9.50	--	--	µs	6
10820	400kHz Mode	t_{SCLK_400}	2.37	--	--	µs	6
10821	1000kHz Mode	t_{SCLK_1000}	1.00	--	--	µs	6
	Clock (SCL) High Time (70% of V_{CC} to 70% of V_{CC})						
10823	100kHz Mode	t_{SCLH_100}	4.00	--	--	µs	6
10837	400kHz Mode	t_{SCLH_400}	0.60	--	--	µs	6
10836	1000kHz Mode (note: not compliant with UM10204 Revision 5)	t_{SCLH_1000}	0.50	--	--	µs	6
	Clock (SCL) Low Time (30% of V_{CC} to 30% of V_{CC})						
10835	100kHz Mode	t_{SCLL_100}	4.70	--	--	µs	6
10839	400kHz Mode	t_{SCLL_400}	1.30	--	--	µs	6
10838	1000kHz Mode	t_{SCLL_1000}	0.50	--	--	µs	6
	Clock (SCL) and Data (SDA) Rise Time (30% of V_{CC} to 70% of V_{CC})						
10834	100kHz Mode	t_{SRISE_100}	--	--	1000	ns	6
10841	400kHz Mode	t_{SRISE_400}	--	--	300	ns	6
10840	1000kHz Mode	t_{SRISE_1000}	--	--	120	ns	6
	Clock (SCL) and Data (SDA) Fall Time (70% of V_{CC} to 30% of V_{CC})						
10833	100kHz Mode	t_{SFALL_100}	--	--	300	ns	6
10844	400kHz Mode	t_{SFALL_400}	--	--	300	ns	6
10843	1000kHz Mode	t_{SFALL_1000}	--	--	120	ns	6
	Data Input Setup Time (SDA = 30/70% of V_{CC} to SCL = 30% of V_{CC})						
10832	100kHz Mode	t_{SETUP_100}	250	--	--	ns	6
10846	400kHz Mode	t_{SETUP_400}	100	--	--	ns	6
10845	1000kHz Mode	t_{SETUP_1000}	50	--	--	ns	6
	Data Input Hold Time (SCL = 70% of V_{CC} to SDA = 30/70% of V_{CC})						
10831	100kHz Mode	t_{HOLD_100}	0	--	900	ns	6
10848	400kHz Mode	t_{HOLD_400}	0	--	900	ns	6
10847	1000kHz Mode	t_{HOLD_1000}	0	--	300	ns	6
	Start Condition Setup Time (SDA = 30/70% of V_{CC} to SCL = 30% of V_{CC})						
10830	100kHz Mode	$t_{STARTSETUP\_100}$	4.70	--	--	µs	6
10851	400kHz Mode	$t_{STARTSETUP\_400}$	0.60	--	--	µs	6
10850	1000kHz Mode	$t_{STARTSETUP\_1000}$	0.26	--	--	µs	6
	Start Condition Hold Time (SCL = 70% of V_{CC} to SDA = 30/70% of V_{CC})						
10829	100kHz Mode	$t_{STARTHOLD\_100}$	4.00	--	--	µs	6
10853	400kHz Mode	$t_{STARTHOLD\_400}$	0.60	--	--	µs	6
10852	1000kHz Mode	$t_{STARTHOLD\_1000}$	0.26	--	--	µs	6
	Stop Condition Setup Time (SDA = 30/70% of V_{CC} to SCL = 30% of V_{CC})						
10828	100kHz Mode	$t_{STOPSETUP\_100}$	4.00	--	--	µs	6
10855	400kHz Mode	$t_{STOPSETUP\_400}$	0.60	--	--	µs	6
10854	1000kHz Mode	$t_{STOPSETUP\_1000}$	0.26	--	--	µs	6
	SCLK low to data valid (SCL = 30% of V_{CC} to SDA = 30/70% of V_{CC})						
10827	100kHz Mode	t_{VALID_100}	--	--	3.45	µs	6
10857	400kHz Mode	t_{VALID_400}	--	--	0.90	µs	6
10856	1000kHz Mode	t_{VALID_1000}	--	--	0.45	µs	6
	Bus Free Time (SDA = 70% of V_{CC} to SDA = 70% of V_{CC})						
10826	100kHz Mode	t_{FREE_100}	4.00	--	--	µs	6
10859	400kHz Mode	t_{FREE_400}	1.30	--	--	µs	6
10859	1000kHz Mode	t_{FREE_1000}	0.50	--	--	µs	6
10825	Bus Capacitive Load	C_{BUS}	--	--	400	pF	7,9

5.15 Dynamic Electrical Characteristics - Signal Chain, Low Pass Filter

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_min}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	DSP Low-Pass Filters Sample Times						
10872	SAMPLERATE = 00, 01 *	$t_{SigChain00}$, $t_{SigChain01}$	--	16	--	µs	7,8,9
10872	SAMPLERATE = 10 *	$t_{SigChain10}$	--	32	--	µs	7,8,9
10871	SAMPLERATE = 11 *	$t_{SigChain11}$	--	64	--	µs	7,8,9
	DSP Low-Pass Filters (Signal Chain Sample Time = 16µs)						
21379	Cutoff Frequency, Filter Option #0 and #2, 4-Pole *	f_{c0_16}, f_{c2_16}	--	400	--	Hz	7,8,9,11
21380	Cutoff Frequency, Filter Option #1 and #3, 3-Pole *	f_{c1_16}, f_{c3_16}	--	400	--	Hz	7,8,9,11
21381	Cutoff Frequency, Filter Option #4, 3-Pole *	f_{c4_16}	--	325	--	Hz	7,8,9,11
21382	Cutoff Frequency, Filter Option #5, 2-Pole *	f_{c5_16}	--	370	--	Hz	7,8,9,11
21383	Cutoff Frequency, Filter Option #6, 2-Pole *	f_{c6_16}	--	180	--	Hz	7,8,9,11
21384	Cutoff Frequency, Filter Option #7, 2-Pole *	f_{c7_16}	--	100	--	Hz	7,8,9,11
21385	Cutoff Frequency, Filter Option #8, 4-Pole *	f_{c8_16}	--	1500	--	Hz	7,8,9,11
26413	Cutoff Frequency, Filter Option #9, 3-Pole *	f_{c9_16}	--	500	--	Hz	7,8,9,11
10860	Cutoff Frequency, Filter Option #10, 4-Pole *	f_{c10_16}	--	800	--	Hz	7,8,9,11
10870	Cutoff Frequency, Filter Option #11, 4-Pole *	f_{c11_16}	--	1200	--	Hz	7,8,9,11
10869	Cutoff Frequency, Filter Option #12 and #13, 3-Pole *	f_{c12_16}, f_{c13_16}	--	120	--	Hz	7,8,9,11
10868	Cutoff Frequency, Filter Option #14, 2-Pole *	f_{c14_16}	--	120	--	Hz	7,8,9,11
38364	Cutoff Frequency, Filter Option #15, 2-Pole *	f_{c15_16}	--	50	--	Hz	7,8,9,11
	DSP Low-Pass Filters (Signal Chain Sample Time = 32µs)						
38378	Cutoff Frequency, Filter Option #0 and #2, 4-Pole *	f_{c0_32}, f_{c2_32}	--	200	--	Hz	7,8,9,11
38379	Cutoff Frequency, Filter Option #1 and #3, 3-Pole *	f_{c1_32}, f_{c3_32}	--	200	--	Hz	7,8,9,11
38380	Cutoff Frequency, Filter Option #4, 3-Pole *	f_{c4_32}	--	162.5	--	Hz	7,8,9,11
38381	Cutoff Frequency, Filter Option #5, 2-Pole *	f_{c5_32}	--	187.5	--	Hz	7,8,9,11
38382	Cutoff Frequency, Filter Option #6, 2-Pole *	f_{c6_32}	--	90	--	Hz	7,8,9,11
38383	Cutoff Frequency, Filter Option #7, 2-Pole *	f_{c7_32}	--	50	--	Hz	7,8,9,11
38384	Cutoff Frequency, Filter Option #8, 4-Pole *	f_{c8_32}	--	750	--	Hz	7,8,9,11
38385	Cutoff Frequency, Filter Option #9, 3-Pole *	f_{c9_32}	--	250	--	Hz	7,8,9,11
38386	Cutoff Frequency, Filter Option #10, 4-Pole *	f_{c10_32}	--	400	--	Hz	7,8,9,11
38387	Cutoff Frequency, Filter Option #11, 4-Pole *	f_{c11_32}	--	600	--	Hz	7,8,9,11
38388	Cutoff Frequency, Filter Option #12 and #13, 3-Pole *	f_{c12_32}, f_{c13_32}	--	60	--	Hz	7,8,9,11
38389	Cutoff Frequency, Filter Option #14, 2-Pole *	f_{c14_32}	--	60	--	Hz	7,8,9,11
38390	Cutoff Frequency, Filter Option #15, 2-Pole *	f_{c15_32}	--	25	--	Hz	7,8,9,11
	DSP Low-Pass Filters (Signal Chain Sample Time = 64µs)						
38365	Cutoff Frequency, Filter Option #0 and #2, 4-Pole *	f_{c0_64}, f_{c2_64}	--	100	--	Hz	7,8,9,11
38366	Cutoff Frequency, Filter Option #1 and #3, 3-Pole *	f_{c1_64}, f_{c3_64}	--	100	--	Hz	7,8,9,11
38367	Cutoff Frequency, Filter Option #4, 3-Pole *	f_{c4_64}	--	81.25	--	Hz	7,8,9,11
38368	Cutoff Frequency, Filter Option #5, 2-Pole *	f_{c5_64}	--	93.75	--	Hz	7,8,9,11
38369	Cutoff Frequency, Filter Option #6, 2-Pole *	f_{c6_64}	--	45	--	Hz	7,8,9,11
38370	Cutoff Frequency, Filter Option #7, 2-Pole *	f_{c7_64}	--	25	--	Hz	7,8,9,11
38371	Cutoff Frequency, Filter Option #8, 4-Pole *	f_{c8_64}	--	375	--	Hz	7,8,9,11
38372	Cutoff Frequency, Filter Option #9, 3-Pole *	f_{c9_64}	--	125	--	Hz	7,8,9,11
38373	Cutoff Frequency, Filter Option #10, 4-Pole *	f_{c10_64}	--	200	--	Hz	7,8,9,11
38374	Cutoff Frequency, Filter Option #11, 4-Pole *	f_{c11_64}	--	300	--	Hz	7,8,9,11
38375	Cutoff Frequency, Filter Option #12 and #13, 3-Pole *	f_{c12_64}, f_{c13_64}	--	30	--	Hz	7,8,9,11
38376	Cutoff Frequency, Filter Option #14, 2-Pole *	f_{c14_64}	--	30	--	Hz	7,8,9,11
38377	Cutoff Frequency, Filter Option #15, 2-Pole *	f_{c15_64}	--	12.5	--	Hz	7,8,9,11

5.16 Dynamic Electrical Characteristics - Signal Chain

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_min}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Offset Cancellation Low-Pass Filter						
10863	Sample Time, Phase 0	$t_{0CSAMP0}$	--	256	--	µs	7,8
10874	Cutoff Frequency, Phase 0, 1-Pole	f_{OC0}	--	163.8	--	Hz	7,8
10875	Time in Phase 0	t_{OC0}	--	4.096	--	ms	7,8
	Offset Cancellation Low-Pass Filter						
10888	Sample Time, Phase 1	$t_{0CSAMP1}$	--	256	--	µs	7,8
10889	Cutoff Frequency, Phase 1, 1-Pole	f_{OC1}	--	40.96	--	Hz	7,8
10890	Time in Phase 1	t_{OC1}	--	4.096	--	ms	7,8
	Offset Cancellation Low-Pass Filter						
10885	Sample Time, Phase 2	$t_{0CSAMP2}$	--	256	--	µs	7,8
10886	Cutoff Frequency, Phase 2, 1-Pole	f_{OC2}	--	10.24	--	Hz	7,8
10887	Time in Phase 2	t_{OC2}	--	16.388	--	ms	7,8
	Offset Cancellation Low-Pass Filter						
10900	Sample Time, Phase 3	$t_{0CSAMP3}$	--	256	--	µs	7,8
10901	Cutoff Frequency, Phase 3, 1-Pole	f_{OC3}	--	2.560	--	Hz	7,8
10902	Time in Phase 3	t_{OC3}	--	65.53	--	ms	7,8
	Offset Cancellation Low-Pass Filter						
10897	Sample Time, Phase 4	$t_{0CSAMP4}$	--	256	--	µs	7,8
10898	Cutoff Frequency, Phase 4, 1-Pole	f_{OC4}	--	0.6400	--	Hz	7,8
10899	Time in Phase 4	t_{OC4}	--	262.19	--	ms	7,8
	Offset Cancellation Low-Pass Filter						
10894	Sample Time, Phase 5	$t_{0CSAMP5}$	--	256	--	µs	7,8
10895	Cutoff Frequency, Phase 5, 1-Pole	f_{OC5}	--	0.1600	--	Hz	7,8
10896	Time in Phase 5	t_{OC5}	--	1049	--	ms	7,8
	Offset Cancellation Low-Pass Filter						
10891	Sample Time, Phase 6	$t_{0CSAMP6}$	--	256	--	µs	7,8
10892	Cutoff Frequency, Phase 6, 1-Pole *	f_{OC6}	--	0.0400	--	Hz	7,8
	Offset Cancellation Output Rate Limiting (PN = FXLS0 - FXLS4)						
10882	Rate Limiting Output Update Time	t_{RL_Rate}	--	2	--	s	7,8,9
10903	Rate Limiting Output Step Size (10-Bit: 1 LSB / 8s)	OFF_{Step}	--	0.25	--	LSB	7,8,9
	Offset Cancellation Output Rate Limiting (PN = FXLS5 - FXLS9)						
10882	Rate Limiting Output Update Time	t_{RL_Rate}	--	2	--	s	7,8,9
10903	Rate Limiting Output Step Size (10-Bit: 1 LSB / 4s)	OFF_{Step}	--	0.5	--	LSB	7,8,9
	Offset Monitor						
10883	Update Rate	$OFFMON_{OSC}$	--	0.5	--	ms	7,8
10905	Count Limit	$OFFMON_{CNTLIMIT}$	--	4096	--	1	7,8
10904	Counter Size	$OFFMON_{CNTSIZE}$	--	8192	--	1	7,8
10881	Signal Delay (Sinc Filter to Output Delay, excluding LPF)	$t_{SigDelay}$	--	--	128	µs	7,8
	Interpolation						
20923	$t_{SigChain} = t_{SigChain00}, t_{SigChain01}$	$t_{INTERP\_00, 01}$	--	1	--	µs	7,8
20922	$t_{SigChain} = t_{SigChain02}$	t_{INTERP_02}	--	2	--	µs	7,8
20921	$t_{SigChain} = t_{SigChain03}$	t_{INTERP_03}	--	4	--	µs	7,8
10877	Interpolation Latency	t_{LAT_INTERP}	--	$t_{SigChainxx}$	--	s	7,8

5.17 Dynamic Electrical Characteristics - Analog Self Test Response Time

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_min}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Medium g, Lateral						
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
10878	Medium g Lateral, LPF = 800Hz, 4-Pole	$t_{ST\_Resp\_MedX\_800\_4}$	750	795	1020	µs	7,8
44634	Medium g Lateral, LPF = 1500Hz, 4-Pole	$t_{ST\_Resp\_MedX\_1500\_4}$	395	415	725	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38147	Medium g Lateral, LPF = 400Hz, 4-Pole	$t_{ST\_Resp\_MedX\_400\_4}$	1510	1590	1810	µs	7,8
38151	Medium g Lateral, LPF = 400Hz, 3-Pole	$t_{ST\_Resp\_MedX\_400\_3}$	1420	1490	1710	µs	7,8
38150	Medium g Lateral, LPF = 180Hz, 2-Pole	$t_{ST\_Resp\_MedX\_180\_2}$	3030	3190	3470	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38149	Medium g Lateral, LPF = 300Hz, 4-Pole	$t_{ST\_Resp\_MedX\_300\_4}$	2010	2120	2360	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38148	Medium g Lateral, LPF = 188Hz, 4-Pole	$t_{ST\_Resp\_MedX\_188\_4}$	3210	3380	3680	µs	7,8
	High g, Lateral						
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38152	High g Lateral, LPF = 800Hz, 4-Pole	$t_{ST\_Resp\_HiX\_800\_4}$	750	795	892	µs	7,8
44636	High g Lateral, LPF = 1500Hz, 4-Pole	$t_{ST\_Resp\_HiX\_1500\_4}$	395	415	490	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38153	High g Lateral, LPF = 400Hz, 4-Pole	$t_{ST\_Resp\_HiX\_400\_4}$	1510	1590	1720	µs	7,8
38154	High g Lateral, LPF = 400Hz, 3-Pole	$t_{ST\_Resp\_HiX\_400\_3}$	1420	1490	1620	µs	7,8
38155	High g Lateral, LPF = 180Hz, 2-Pole	$t_{ST\_Resp\_HiX\_180\_2}$	3030	3190	3400	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38156	High g Lateral, LPF = 300Hz, 4-Pole	$t_{ST\_Resp\_HiX\_300\_4}$	2010	2120	2280	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38157	High g Lateral, LPF = 188Hz, 4-Pole	$t_{ST\_Resp\_HiX\_188\_4}$	3210	3380	3600	µs	7,8
	Medium g, Z-Axis						
	Self Test Response Time: Self Test Activation/Deactivation to 99% g_{ST}						
38158	Medium g Z-Axis, LPF = 800Hz, 4-Pole	$t_{ST\_Resp\_MedZ\_800\_4}$	750	795	1010	µs	7,8
44637	Medium g Z-Axis, LPF = 1500Hz, 4-Pole	$t_{ST\_Resp\_MedZ\_1500\_4}$	395	415	710	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38159	Medium g Z-Axis, LPF = 400Hz, 4-Pole	$t_{ST\_Resp\_MedZ\_400\_4}$	1510	1590	1810	µs	7,8
38160	Medium g Z-Axis, LPF = 400Hz, 3-Pole	$t_{ST\_Resp\_MedZ\_400\_3}$	1420	1490	1700	µs	7,8
38161	Medium g Z-Axis, LPF = 180Hz, 2-Pole	$t_{ST\_Resp\_MedZ\_180\_2}$	3030	3190	3470	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38162	Medium g Z-Axis, LPF = 300Hz, 4-Pole	$t_{ST\_Resp\_MedZ\_300\_4}$	2010	2120	2360	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38163	Medium g Z-Axis, LPF = 188Hz, 4-Pole	$t_{ST\_Resp\_MedZ\_188\_4}$	3210	3380	3680	µs	7,8
	High g, Z-Axis						
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38164	High g Z-Axis, LPF = 800Hz, 4-Pole	$t_{ST\_Resp\_HiZ\_800\_4}$	750	795	994	µs	7,8
44638	High g Z-Axis, LPF = 1500Hz, 4-Pole	$t_{ST\_Resp\_HiZ\_1500\_4}$	395	415	675	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38165	High g Z-Axis, LPF = 400Hz, 4-Pole	$t_{ST\_Resp\_HiZ\_400\_4}$	1510	1590	1800	µs	7,8
38166	High g Z-Axis, LPF = 400Hz, 3-Pole	$t_{ST\_Resp\_HiZ\_400\_3}$	1420	1490	1690	µs	7,8
38167	High g Z-Axis, LPF = 180Hz, 2-Pole	$t_{ST\_Resp\_HiZ\_180\_2}$	3030	3190	3470	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38168	High g Z-Axis, LPF = 300Hz, 4-Pole	$t_{ST\_Resp\_HiZ\_300\_4}$	2010	2120	2360	µs	7,8
	Self Test Response Time: Self Test Activation/Deactivation to 99%/0% g_{ST}						
38169	High g Z-Axis, LPF = 188Hz, 4-Pole	$t_{ST\_Resp\_HiZ\_188\_4}$	3210	3380	3680	µs	7,8

5.18 Dynamic Electrical Characteristics - Digital Self Test Response Time

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_min}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
44639	Self Test Response Time: Self Test Activation/Deactivation to Final Value LPF ≤ 60 Hz	$t_{DST\_Resp\_50}$	--	--	50	ms	7,8
44641	Self Test Response Time: Self Test Activation/Deactivation to Final Value 60 Hz ≤ LPF ≤ 200 Hz	$t_{DST\_Resp\_100}$	--	--	25	ms	7,8
44640	Self Test Response Time: Self Test Activation/Deactivation to Final Value 300 Hz ≤ LPF ≤ 1500 Hz	$t_{DST\_Resp\_400}$	--	--	12	ms	7,8
38176	Fixed Pattern Response Time: Self Test Activation/Deactivation	$t_{ST\_FP\_Resp}$	--	--	100	µs	7,8

5.19 Dynamic Electrical Characteristics - Transducer

$V_{BUS\_I\_L\_min} \leq (V_{BUS\_I} - V_{SS}) \leq V_{BUS\_I\_H\_min}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Lateral Transducer Rolloff Frequency (-3db)						
10917	Medium g	$f_{gcell\_3dB\_mid}$	1500	2500	4500	Hz	7
10915	High g	$f_{gcell\_3dB\_hi}$	4000	7000	13000	Hz	7
	Lateral Transducer Delay (@100Hz)						
10921	Medium g	$f_{gcell\_delay100\_mid}$	--	--	250	µs	7
10919	High g	$f_{gcell\_delay100\_hi}$	--	--	250	µs	7
	Z-Axis Transducer Rolloff Frequency (-3db)						
10923	Medium g	$f_{gcell\_3dB\_mid}$	1500	2500	4500	Hz	7
10925	High g	$f_{gcell\_3dB\_hi}$	1500	2500	7500	Hz	7
	Z-Axis Transducer Delay (@100Hz)						
10927	Medium g	$f_{gcell\_delay100\_mid}$	--	--	250	µs	7
10929	High g	$f_{gcell\_delay100\_hi}$	--	--	250	µs	7
10912	Package Resonance Frequency	$f_{Package}$	100	—	—	kHz	7

5.20 Dynamic Electrical Characteristics - Supply and Support Circuitry

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_min}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	Test Notes
	Reset Recovery (All Modes, excluding V_{BUS_I} voltage ramp time)						
10930	VCC = VCCMIN to POR Release	t_{VCC_POR}	--	--	1	ms	7,8,9
10939	POR to 1st DSI Command (Section 7.1)	t_{POR_DSI}	--	--	6	ms	7,8,9
10938	POR to PSI5 Initialization Phase 1 Start (Section 8.4)	t_{POR_PSI5}	--	--	6	ms	7,8
10937	POR to 1st SPI Command	t_{POR_SPI}	0.400	--	0.700	ms	7,8,9
10936	POR to Sensor Data Valid	$t_{POR\_DataValid}$	--	--	6	ms	7,8,9
10935	DSP Setting Change to Sensor Data Valid: DS3, SPI, I^2C	$t_{RANGE\_DataValid}$	--	--	6	ms	7,8,9
	Soft Reset Activation Time						
10934	SPI: SS_B high to Reset	$t_{SOFT\_RESET\_SPI}$	--	--	700	ns	7,8
30152	I^2C: Command Complete to Reset (No ACK follows)	$t_{SOFT\_RESET\_I2C}$	--	--	700	ns	7,8
30151	DSI3: Command/Response Complete to Reset	$t_{SOFT\_RESET\_DSI}$	--	--	11	µs	7,8
41495	PSI5: Command/Response Complete to Reset	$t_{SOFT\_RESET\_PSI}$	--	--	120	µs	7,8
	Internal Oscillator Period						
10933	Untrained *	f_{OSC}	9.500	10.000	10.500	MHz	1,7,8,9
10940	With Oscillator Training	f_{OSC_TRAIN}	9.900	10.000	10.100	MHz	7,8,9
	Oscillator Training (Section 6.5.1)						
10932	Oscillator Training Time	$t_{OscTrain}$	—	4	—	ms	7,8
10942	Oscillator Cycles in Training Time	$n_{OSC\_4ms\_TYP}$	—	40000	—	$1/f_{OSC}$	7,8
10944	Oscillator Training Window	$OscTrain_{WIN}$	38000	—	42000	$1/f_{OSC}$	7,8
10943	Oscillator Training Adjustment Threshold	$OscTrain_{ADJ}$	-400	—	400	$1/f_{OSC}$	7,8
10941	Oscillator Training Step Size	$OscTrain_{RES}$		250		$1/f_{OSC}$	7,8
10946	Quiescent Current Settling Time (Power Applied to Iq = I_{IDLE} +/- 2mA)	t_{SET}	—	—	4	ms	7,9
	BUS_I Micro-cut						
10931	Survival Time (BUS_I disconnect without Reset, C_{BUF}=1µF, Bus with 1 Slave)	$t_{BUS\_I\_MICROCUT}$	30	—	—	µs	7,9
10952	Reset Time (BUS_I disconnect time to Reset, C_{BUF}=1µF, Bus with 1 Slave)	$t_{BUS\_I\_RESET}$	—	—	1000	µs	7,9
10953	Survival Time (BUS_I disconnect without Reset, C_{BUF}=470nF, Bus with 1 Slave)	$t_{BUS\_I\_MICROCUT}$	15	—	—	µs	7,9
10954	Reset Time (BUS_I disconnect time to Reset, C_{BUF}=470nF, Bus with 1 Slave)	$t_{BUS\_I\_RESET}$	—	—	1000	µs	7,9
	BUS_I Undervoltage Detection Delay						
10947	BUS_I < $V_{BUS\_I\_UV\_F}$ to I_{RESP} Deactivation	$t_{BUS\_I\_POR}$	—	—	5	µs	7
	V_{BUF} Undervoltage Detection Delay						
10958	V_{BUF} < $V_{BUF\_UV\_F}$ to I_{RESP} Deactivation	t_{VBUF_POR}	—	—	5	µs	7
10957	Undervoltage/Overvoltage Recovery Delay	t_{UVOV_RCV}	—	100	—	µs	7
	V_{BUF} Capacitor Monitor						
36817	DSI Command Start to Capacitor Test	$t_{D\_CAPTEST}$	--	3.0	--	µs	7
36821	PSI5 Synchronous Command Start to Capacitor Test	$t_{P\_CAPTEST}$	--	9.2	--	µs	7
36823	PSI5 Asynchronous Response Start to Capacitor Test	$t_{A\_CAPTEST}$	--	179.2	--	µs	7
36822	Capacitor Test Disconnect Time	t_{CAPTST_TIME}	--	1	--	µs	7

Notes:

1. Parameter tested 100% at final test. Temperature = -40°C, 25°C and 105°C, V_{BUS_I} = 7V, Unless otherwise stated
2. Parameter tested 100% at final test during safe launch
3. Parameter verified by pass/fail testing at final test
4. Parameter verified by pass/fail testing at final test during safe launch
5. Parameter verified by qualification testing
6. Parameter verified by characterization
7. Functionality verified by modeling, simulation and/or design verification.
8. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
9. Parameter verified by functional evaluation
10. Thermal resistance provided with device mounted to a 2 layer, 1.6mm FR-4 PCB as documented in AN1902 with 1 signal layer and 1 ground layer.
11. Digital low pass filter characteristics are specified independently and do not include g-cell characteristics. Higher frequency filters will have lower system cut-off frequencies due to the g-cell damping.

* Indicates critical characteristic.

SECTION 6 FUNCTIONAL DESCRIPTION

6.1 User Accessible Data Array

A user accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block, an OTP user programmable block, and read only registers for data and device status. The OTP blocks incorporate independent data verification.

6.1.1 User Accessible Data - General Device Information

			Bit							
Type	**Address**	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	$00	COUNT	COUNT[7:0]							
R	$01	DEVSTAT	CH0_ERR	CH1_ERR	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
R	$02	DEVSTAT1	VBUFUV_ERR	BUSINUV_ERR	VBUFOV_ERR	RESERVED	INTREGA_ERR	INTREG_ERR	INTREGF_ERR	CONT_ERR
R	$03	DEVSTAT2	F_OTP_ERR	U_OTP_ERR	U_RW_ERR	U_W_ACTIVE	TEMP1_ERR	TEMP0_ERR	RESERVED	RESERVED
R	$04	DEVSTAT3	MISO_ERR	OSCTRAIN_ERR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R	$05	COMMREV	0	0	0	0	COMMREV[3:0]			
R	$06 - $0D	RESERVED	RESERVED							
R	$0E	TEMPERATURE	TEMP[7:0]							
R	$0F	RESERVED	RESERVED							

6.1.2 User Accessible Data - Communication Information

			Bit							
Type	**Address**	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	$10	DEVLOCK_WR	ENDINIT	RESERVED	RESERVED	RESERVED	SUP_ERR_DIS	RESERVED	RESET[1:0]	
R/W	$11	WRITE_OTP_EN	UOTP_WR_INIT	RESERVED	RESERVED	RESERVED	EX_COMMTYPE	EX_PADDR	UOTP_REGION[1:0]	
R/W	$12	BUSSW_CTRL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUSSW_CTRL[1:0]	
R/W	$13	PSI5_TEST	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PSI5_TEST
R/W	$14	UF_REGION_W	REGION_LOAD[3:0]				0	0	0	0
R	$15	UF_REGION_R	REGION_ACTIVE[3:0]				0	0	0	0
UF2	$16	COMMTYPE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	COMMTYPE[2:0]		
UF2	$17	RESERVED	RESERVED							
UF2	$18	PHYSADDR	0	0	0	0	PADDR[3:0]			
UF2	$19	RESERVED	RESERVED							
UF2	$1A	SOURCEID_0	SID0_EN	PDCMFORMAT[2:0]			SOURCEID_0[3:0]			
UF2	$1B	SOURCEID_1	SID1_EN	RESERVED	RESERVED	RESERVED	SOURCEID_1[3:0]			
UF2	$1C	SOURCEID_2	SID2_EN	RESERVED	RESERVED	RESERVED	SOURCEID_2[3:0]			
UF2	$1D	SOURCEID_3	SID3_EN	RESERVED	RESERVED	RESERVED	SOURCEID_3[3:0]			
UF2	$1E - $21	RESERVED	RESERVED							
UF2	$22	TIMING_CFG	PDCM_PER[2:0]			OSCTRAIN_SEL	CK_CAL_RST	CRM_PER[1:0]		CK_CAL_EN
UF2	$23	CHIPTIME	RESERVED	RESERVED	RESERVED	SS_EN	CHIPTIME[3:0]			
UF2	$24	BDM_CFG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BDM_FRAGSIZE	BDM_EN
UF2	$25	PSI5_CFG	SYNC_PD	DAISY_CHAIN	PSI5_ILOW	DUALTRANS	EMSG_EXT	P_CRC	INIT2_EXT	ASYNC
UF2	$26	PDCM_RSPST0_L	PDCM_RSPST0[7:0]							
UF2	$27	PDCM_RSPST0_H	BRC_RSP0[1:0]		RESERVED	PDCM_RSPST0[12:8]				
UF2	$28	PDCM_RSPST1_L	PDCM_RSPST1[7:0]							
UF2	$29	PDCM_RSPST1_H	BRC_RSP1[1:0]		RESERVED	PDCM_RSPST1[12:8]				
UF2	$2A	PDCM_RSPST2_L	PDCM_RSPST2[7:0]							
UF2	$2B	PDCM_RSPST2_H	BRC_RSP2[1:0]		RESERVED	PDCM_RSPST2[12:8]				
UF2	$2C	PDCM_RSPST3_L	PDCM_RSPST3[7:0]							
UF2	$2D	PDCM_RSPST3_H	BRC_RSP3[1:0]		RESERVED	PDCM_RSPST3[12:8]				
UF2	$2E - $37	RESERVED	RESERVED							
UF2	$38	PDCM_CMD_B_L	PDCM_CMD_B[7:0]							
UF2	$39	PDCM_CMD_B_H	RESERVED	RESERVED	RESERVED	PDCM_CMD_B[12:8]				
UF2	$3A - $3C	RESERVED	RESERVED							
UF2	$3D	SPI_CFG	RESERVED	DATASIZE	SPI_CRC_LEN[1:0]		SPICRCSEED[3:0]			
UF2	$3E	WHO_AM_I	WHO_AM_I[7:0]							
UF2	$3F	I2C_ADDRESS	I2C_ADDRESS[7:0]							

Memory Type Codes

R	Readable Register with No OTP
F	User Readable Register with OTP
UF0	One Time User Programmable OTP Location Region 0
UF1	One Time User Programmable OTP Location Region 1
UF2	One Time User Programmable OTP Location Region 2
R/W	User Writable Register

6.1.3 User Accessible Data - Sensor Specific Information

			Bit							
Type	Address	Register	7	6	5	4	3	2	1	0
UF2	$40	CH0_CFG_U1	LPF[3:0]				SAMPLERATE[1:0]		USER_SNS_SHIFT[1:0]	
UF2	$41	CH0_CFG_U2	U_SNS_MULT[7:0]							
UF2	$42	CH0_CFG_U3	UNSIGNEDDATA	DATATYPE0[1:0]		DATATYPE1[2:0]			MOVEAVG[1:0]	
UF2	$43	CH0_CFG_U4	RESERVED	INVERT	OC_FILT[1:0]		PCM	ARM_CFG[2:0]		
UF2	$44	CH0_CFG_U5	ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
UF2	$45	CH0_ARM_CFG	ARM_DS[1:0]		ARM_PS[1:0]		ARM_WS_N[1:0]		ARM_WS_P[1:0]	
UF2	$46	CH0_ARM_T_P	ARM_T_P[7:0]							
UF2	$47	CH0_ARM_T_N	ARM_T_N[7:0]							
UF2	$48	CH1_CFG_U1	LPF[3:0]				SAMPLERATE[1:0]		USER_SNS_SHIFT[1:0]	
UF2	$49	CH1_CFG_U2	U_SNS_MULT[7:0]							
UF2	$4A	CH1_CFG_U3	UNSIGNEDDATA	DATATYPE0[1:0]		DATATYPE1[2:0]			MOVEAVG[1:0]	
UF2	$4B	CH1_CFG_U4	RESERVED	INVERT	OC_FILT[1:0]		PCM	ARM_CFG[2:0]		
UF2	$4C	CH1_CFG_U5	ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
UF2	$4D	CH1_ARM_CFG	ARM_DS[1:0]		ARM_PS[1:0]		ARM_WS_N[1:0]		ARM_WS_P[1:0]	
UF2	$4E	CH1_ARM_T_P	ARM_T_P[7:0]							
UF2	$4F	CH1_ARM_T_N	ARM_T_N[7:0]							
UF2	$50-$5E	RESERVED	RESERVED							
F	$5F	CRC_UF2	LOCK_UF2	0	0	0	CRC_UF2[3:0]			
R	$60	CH0_STAT	SIGNALCLIP	OCPHASE[2:0]			ST_INCMPLT	ST_ACTIVE	OFFSET_ERR	ST_ERROR
R	$61	DEVSTAT_COPY	CH0_ERR	CH1_ERR	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
R	$62	CH0_SNSDATA0_L	CH0_SNSDATA0[7:0]							
R	$63	CH0_SNSDATA0_H	CH0_SNSDATA0[15:8]							
R	$64	CH0_SNSDATA1_L	CH0_SNSDATA1[7:0]							
R	$65	CH0_SNSDATA1_H	CH0_SNSDATA1[15:8]							
R	$66-$6F	RESERVED	RESERVED							
R	$70	CH1_STAT	SIGNALCLIP	OCPHASE[2:0]			ST_INCMPLT	ST_ACTIVE	OFFSET_ERR	ST_ERROR
R	$71	RESERVED	RESERVED							
R	$72	CH1_SNSDATA0_L	CH1_SNSDATA0[7:0]							
R	$73	CH1_SNSDATA0_H	CH1_SNSDATA0[15:8]							
R	$74	CH1_SNSDATA1_L	CH1_SNSDATA1[7:0]							
R	$75	CH1_SNSDATA1_H	CH1_SNSDATA1[15:8]							
R	$76-$9F	RESERVED	RESERVED							

6.1.4 User Accessible Data - Sensor Specific Information

			Bit							
Type	Address	Register	7	6	5	4	3	2	1	0
F	$A0	CH0_CFG_F	DEV_RANGE[3:0]				RESERVED	RESERVED	AXIS[1:0]	
F	$A1	RESERVED	RESERVED							
F	$A2	RESERVED	RESERVED							
F	$A3	RESERVED	RESERVED							
F	$A4	CH0_STH_P_L	CH0_STH_P[7:0]							
F	$A5	CH0_STH_P_H	CH0_STH_P[15:8]							
F	$A6	RESERVED	RESERVED							
F	$A7	RESERVED	RESERVED							
F	$A8	CH0_STH_N_L	CH0_STH_N[7:0]							
F	$A9	CH0_STH_N_H	CH0_STH_N[15:8]							
F	$AA-$AE	RESERVED	RESERVED							
F	$AF	CRC_F_A	LOCK_F_A	REGA_BLOCKID[2:0]			CRC_F_A[3:0]			
F	$B0	CH1_CFG_F	DEV_RANGE[3:0]				RESERVED	RESERVED	AXIS[1:0]	
F	$B1	RESERVED	RESERVED							
F	$B2	RESERVED	RESERVED							
F	$B3	RESERVED	RESERVED							
F	$B4	CH1_STH_P_L	CH1_STH_P[7:0]							
F	$B5	CH1_STH_P_H	CH1_STH_P[15:8]							
F	$B6	RESERVED	RESERVED							
F	$B7	RESERVED	RESERVED							
F	$B8	CH1_STH_N_L	CH1_STH_N[7:0]							
F	$B9	CH1_STH_N_H	CH1_STH_N[15:8]							
F	$BA-$BE	RESERVED	RESERVED							
F	$BF	CRC_F_B	LOCK_F_B	REGB_BLOCKID[2:0]			CRC_F_B[3:0]			

Memory Type Codes

R	Readable Register with No OTP
F	User Readable Register with OTP
UF0	One Time User Programmable OTP Location Region 0
UF1	One Time User Programmable OTP Location Region 1
UF2	One Time User Programmable OTP Location Region 2
R/W	User Writable Register

6.1.5 User Accessible Data - Traceability Information

			Bit							
Type	**Address**	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F	$C0	ICTYPEID	ICTYPEID[7:0]							
F	$C1	ICREVID	ICREVID[7:0]							
F	$C2	ICMFGID	ICMFGID[7:0]							
F	$C3	RESERVED	RESERVED							
F	$C4	PN0	PN0[7:0]							
F	$C5	PN1	PN1[7:0]							
F	$C6	SN0	SN[7:0]							
F	$C7	SN1	SN[15:8]							
F	$C8	SN2	SN[23:16]							
F	$C9	SN3	SN[31:24]							
F	$CA	SN4	SN[39:36] = DEVICE_REV[3:0]				SN[35:32]			
F	$CB	ASICWFR#	ASICWFR#[7:0]							
F	$CC	ASICWFR_X	ASICWFR_X[7:0]							
F	$CD	ASICWFR_Y	ASICWFR_Y[7:0]							
F	$CE	RESERVED	RESERVED							
F	$CF	CRC_F_C	LOCK_F_C	REGC_BLOCKID[2:0]			CRC_F_C[3:0]			
F	$D0	ASICWLOT_L	ASICWLOT[7:0]							
F	$D1	ASICWLOT_H	ASICWLOT[15:8]							
F	$D2	TRNS1WFR_X	TRNS1WFR_X[7:0]							
F	$D3	TRNS1WFR_Y	TRNS1WFR_Y[7:0]							
F	$D4	TRNS1LOT_L	TRNS1LOT[7:0]							
F	$D5	TRNS1LOT_H	TRNS1LOT[15:8]							
F	$D6-$D9	RESERVED	RESERVED							
F	$DA	TRNS1WFR#	TRNS_ASSY_REV[2:0]			TRNS1WFR#[4:0]				
F	$DB-$DE	RESERVED	RESERVED							
F	$DF	CRC_F_D	LOCK_F_D	REGD_BLOCKID[2:0]			CRC_F_D[3:0]			
UF0	$E0	USERDATA_0	USERDATA_0[7:0]							
UF0	$E1	USERDATA_1	USERDATA_1[7:0]							
UF0	$E2	USERDATA_2	USERDATA_2[7:0]							
UF0	$E3	USERDATA_3	USERDATA_3[7:0]							
UF0	$E4	USERDATA_4	USERDATA_4[7:0]							
UF0	$E5	USERDATA_5	USERDATA_5[7:0]							
UF0	$E6	USERDATA_6	USERDATA_6[7:0]							
UF0	$E7	USERDATA_7	USERDATA_7[7:0]							
UF0	$E8	USERDATA_8	USERDATA_8[7:0]							
UF0	$E9	USERDATA_9	USERDATA_9[7:0]							
UF0	$EA	USERDATA_A	USERDATA_A[7:0]							
UF0	$EB	USERDATA_B	USERDATA_B[7:0]							
UF0	$EC	USERDATA_C	USERDATA_C[7:0]							
UF0	$ED	USERDATA_D	USERDATA_D[7:0]							
UF0	$EE	USERDATA_E	USERDATA_E[7:0]							
F	$EF	CRC_UF0	LOCK_UF0	REGE_BLOCKID[2:0]			CRC_UF0[3:0]			
UF1	$F0	USERDATA_10	USERDATA_10[7:0]							
UF1	$F1	USERDATA_11	USERDATA_11[7:0]							
UF1	$F2	USERDATA_12	USERDATA_12[7:0]							
UF1	$F3	USERDATA_13	USERDATA_13[7:0]							
UF1	$F4	USERDATA_14	USERDATA_14[7:0]							
UF1	$F5	USERDATA_15	USERDATA_15[7:0]							
UF1	$F6	USERDATA_16	USERDATA_16[7:0]							
UF1	$F7	USERDATA_17	USERDATA_17[7:0]							
UF1	$F8	USERDATA_18	USERDATA_18[7:0]							
UF1	$F9	USERDATA_19	USERDATA_19[7:0]							
UF1	$FA	USERDATA_1A	USERDATA_1A[7:0]							
UF1	$FB	USERDATA_1B	USERDATA_1B[7:0]							
UF1	$FC	USERDATA_1C	USERDATA_1C[7:0]							
UF1	$FD	USERDATA_1D	USERDATA_1D[7:0]							
UF1	$FE	USERDATA_1E	USERDATA_1E[7:0]							
F	$FF	CRC_UF1	LOCK_UF1	REGF_BLOCKID[2:0]			CRC_UF1[3:0]			

Memory Type Codes

R	Readable Register with No OTP
F	User Readable Register with OTP
UF0	One Time User Programmable OTP Location Region 0
UF1	One Time User Programmable OTP Location Region 1
UF2	One Time User Programmable OTP Location Region 2
R/W	User Writable Register

6.2 Register Definitions

6.2.1 Rolling Counter Register (COUNT)

The count register is a read-only register which provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit pre-scaler divides the primary oscillator frequency by 1000. Thus, the value in the register increases by one count every 100μs and the counter rolls over every 25.6ms.

This register is readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$00	COUNT	COUNT[7:0]							
Reset Value		0	0	0	0	0	0	0	0

6.2.2 Device Status Registers (DEVSTATx)

The device status registers are read-only registers which contain device status information.

These registers are readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$01	DEVSTAT	CH0_ERR	CH1_ERR	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
Reset Value		1	1	0	0	x	0	1	1
$02	DEVSTAT1	VBUFUV_ERR	BUSINUV_ERR	VBUFOV_ERR	RESERVED	INTREGA_ERR	INTREG_ERR	INTREGF_ERR	CONT_ERR
Reset Value		x	x	x	x	x	x	x	0
$03	DEVSTAT2	F_OTP_ERR	U_OTP_ERR	U_RW_ERR	U_W_ACTIVE	TEMP1_ERR	TEMP0_ERR	RESERVED	RESERVED
Reset Value		0	0	0	0	0	0	x	x
$04	DEVSTAT3	MISO_ERR	OSCTRAIN_ERR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset Value		0	0	x	x	x	x	x	x

6.2.2.1 Channel 0 Error Flag (CH0_ERR)

The channel 0 error flag is set if a channel 0 specific error is present in the channel 0 DSP:

CH0_ERR = CH0_STAT[SIGNALCLIP] | CH0_STAT[ST_INCMPLT] | CH0_STAT[OFFSET_ERR] | CH0_STAT[ST_ERROR]

6.2.2.2 Channel 1 Error Flag (CH1_ERR)

The channel 1 error flag is set if a channel 1 specific error is present in the channel 1 DSP:

CH1_ERR = CH1_STAT[SIGNALCLIP] | CH1_STAT[ST_INCMPLT] |CH1_STAT[OFFSET_ERR] | CH1_STAT[ST_ERROR]

6.2.2.3 Communication Error Flag (COMM_ERR)

The communication error flag is set if any bit in DEVSTAT3 is set:

COMM_ERR = MISO_ERR | OSCTRAIN_ERR

6.2.2.4 Memory or Temperature Error Flag (MEMTEMP_ERR)

The memory error flag is set if any bit in DEVSTAT2 is set:

MEMTEMP_ERR = F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_W_ACTIVE | TEMP1_ERR | TEMP0_ERR

6.2.2.5 Supply Error Flag (SUPPLY_ERR)

The supply error flag is set if any bit in DEVSTAT1 is set:

SUPPLY_ERR = VBUFUV_ERR | BUSINUV_ERR | VBUFOV_ERR | INTREG_ERR | INTREGA_ERR | INTREGF_ER | CONT_ERR

A common timer is used for all error bits in the DEVSTAT1 register. If any bit in DEVSTAT1 is set, the timer is reset to t_{UVOV_RCV}. When no supply errors are present, the timer is decremented until it reaches zero. This error is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in the table below.

<table>
<tr><th>SUP_ERR_DIS</th><th>DSI3 and SPI Operating Modes
(COMMTYPE =0, 2, 3 and 4)</th><th>PSI5 Operating Mode
(COMMTYPE =1 and 5)</th><th>I²C Operating Modes
(COMMTYPE =6,7)</th></tr>
<tr><td>0</td><td>No Response until the supply monitor timer expires. The Sensor Data Field Error Code is transmitted for one response after the supply monitor timer expires.

All supply errors are cleared by a read of the DEVSTAT1 register through any communication interface or on a data transmission that includes the error in the status field if and only if the timer has reached zero.</td><td rowspan="2">No transmissions occur if the timer is non-zero. The error is cleared when the timer reaches zero and normal transmissions resume.</td><td rowspan="2">No response until the supply monitor timer expires.

All supply errors are cleared by a read of the DEVSTAT1 register.</td></tr>
<tr><td>1</td><td>No transmissions occur if the timer is non-zero. The error is cleared when the timer reaches zero and normal transmissions resume.</td></tr>
</table>

6.2.2.6 Test Mode (TESTMODE)

The test mode bit is set if the device is in test mode. The TESTMODE bit can be cleared by a test mode operation or by a power cycle.

TESTMODE	Operating Mode
0	Test Mode is not active
1	Test Mode is active

6.2.2.7 Device Reset (DEVRES)

The device reset bit is set following a device reset. This error is cleared by a read of the DEVSTAT register through any communication interface or on a data transmission that includes the error in the status field.

DEVRES	Error Condition
0	Normal operation
1	Device reset occurred

6.2.2.8 Device Initialization (DEVINIT)

The device initialization bit is set following either a device reset or a change to any of the following bits: CHx_CFG_U1[7:2] or CHx_CFG_U3[1:0]. The bit is cleared once sensor data is valid for read through one of the device communication interfaces ($t_{POR\_DataValid}$).

Note: Some LPF selections have a step response time longer than the $t_{POR\_DataValid}$ delay. If any of these filters are used, the filter may not have achieved the final value once DEVINIT is cleared.

DEVINIT	Condition
0	Normal operation
1	Device Initialization in Process

6.2.2.9 V_{BUF} Under-Voltage Error (VBUFUV_ERR)

The V_{BUF} under-voltage error bit is set if the VBUF voltage falls below the voltage specified in Section 5.4. Reference Section 6.4 for details on the V_{BUF} under-voltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 6.2.2.5.

VBUFUV_ERR	Error Condition
0	No error detected
1	VBUF Voltage Low

6.2.2.10 BUS IN Under-Voltage Error (BUSINUV_ERR)

The BUS IN under-voltage error bit is set if the BUS_IN voltage falls below the voltage specified in Section 5.4. Reference Section 6.4 for details on the BUS IN under-voltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 6.2.2.5.

BUSINUV_ERR	Error Condition
0	No error detected
1	BUS_IN Voltage Low

6.2.2.11 V_{BUF} Over-Voltage Error (VBUFOV_ERR)

The V_{BUF} over-voltage error bit is set if the VBUF voltage rises above the voltage specified in Section 5.4. Reference Section 6.4 for details on the V_{BUF} over-voltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 6.2.2.5.

VBUFUV_ERR	Error Condition
0	No error detected
1	VBUF Voltage High

6.2.2.12 Internal Analog Regulator Voltage Out of Range Error (INTREGA_ERR)

The internal analog regulator voltage out of range error bit is set if the internal analog regulator voltage falls outside of expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 6.2.2.5.

INTREGA_ERR	Error Condition
0	No error detected
1	Internal Analog Regulator Voltage Out of Range

6.2.2.13 Internal Digital Regulator Voltage Out of Range Error (INTREG_ERR)

The internal digital regulator voltage out of range error bit is set if the internal digital regulator voltage falls outside of expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 6.2.2.5.

INTREG_ERR	Error Condition
0	No error detected
1	Internal Digital Regulator Voltage Out of Range

6.2.2.14 Internal OTP Regulator Voltage Out of Range Error (INTREGF_ERR)

The internal OTP regulator voltage out of range error bit is set if the internal OTP regulator voltage falls outside of expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 6.2.2.5.

INTREGF_ERR	Error Condition
0	No error detected
1	Internal OTP Regulator Voltage Out of Range

6.2.2.15 Continuity Monitor Error (CONT_ERR)

The continuity monitor passes a low current through a connection around the perimeter of the device and monitors the continuity of the connection. The error bit is set if a discontinuity is detected in the connection. A common timer is used for all error bits in the DEVSTAT1 register. If the CONT_ERR bit is set, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 6.2.2.5.

CONT_ERR	Error Condition
0	No error detected
1	Error detected in the continuity of the monitor circuit

6.2.2.16 NXP OTP Array Error (F_OTP_ERR)

The factory OTP array error bit is set if a fault is detected in the factory OTP array. This error is cleared by a device reset.

F_OTP_ERR	Error Condition
0	No error detected
1	Error Detected in the Factory OTP Array

6.2.2.17 User OTP Array Error (U_OTP_ERR)

The user OTP array error bit is set if a fault is detected in the user OTP array. This error is cleared by a device reset.

U_OTP_ERR	Error Condition
0	No error detected
1	Error Detected in the User OTP Array

6.2.2.18 User Read/Write Array Error (U_RW_ERR)

When ENDINIT is set, an error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code. If a mismatch is detected in the error detection, the U_RW_ERR bit is set. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

U_RW_ERR	Error Condition
0	No error detected
1	Error Detected in the User Read/Write Array

6.2.2.19 User OTP Write In Process Status Bit (U_W_ACTIVE)

The user OTP write in process status bit is set if a user initiated write to OTP is currently in process. The U_W_ACTIVE bit is automatically cleared once the write to OTP is complete.

U_W_ACTIVE	Status Condition
0	No OTP Write in Process
1	OTP Write in Process

6.2.2.20 Channel 1 Temperature Sensor Error (TEMP1_ERR)

The channel 1 temperature error bit is set if an over or under temperature condition exists on channel 1. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

TEMP1_ERR	Error Condition
0	No error detected
1	Over- or Under-Temperature error condition detected

6.2.2.21 Channel 0 Temperature Sensor Error (TEMP0_ERR)

The channel 0 temperature error bit is set if an over or under temperature condition exists on channel 0. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

TEMP0_ERR	Error Condition
0	No error detected
1	Over- or Under-Temperature error condition detected

6.2.2.22 SPI MISO Data Mismatch Error Flag (MISO_ERROR)

In SPI mode, the MISO data mismatch flag is set when a MISO Data mismatch fault occurs as specified in Section 9.5.5. The MISO_ERROR bit is cleared by a read of the DEVSTAT3 register through any communication interface, or by a status transmission including the error status through the SPI.

MISO_ERROR	Error Condition
0	Normal operation
1	MISO Data Mismatch

6.2.2.23 Oscillator Training Error (OSCTRAIN_ERR)

The oscillator training error bit is set if an error detected in either the oscillator training settings, or the master communication timing. Reference Section 6.5.2. Once the error condition is corrected, the OSCTRAIN_ERR bit is cleared after a read of the OSCTRAIN_ERR bit through any communication interface, or by a status transmission including the error status through any communication interface.

OSCTRAIN_ERR	Error Condition
0	No error detected
1	Oscillator Training Error. Reference Section 6.5.2

6.2.3 Communication Protocol Revision Register (COMMREV)

The Communication Protocol Revision register is a read only register which contains the revision for the communication protocol used.

This register is readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$05	COMMREV	0	0	0	0	COMMREV[3:0]			
Reset Value for DSI3		0	0	0	0	0	0	0	1
Reset Value for PSI5		0	0	0	0	0	1	1	0
Reset Value for SPI		0	0	0	0	0	0	0	0
Reset Value for I^2C		0	0	0	0	0	1	0	1

Note: The response to a register write of the COMMREV register is a valid response with the register contents equal to 0x00.

6.2.4 Temperature Register (TEMPERATURE)

The temperature register is a read-only register which provides a temperature value from the channel 0 temperature sensor. The temperature value is specified in Section 5.5.

Note, the device is only guaranteed to operate within the temperature limits specified in Section 5. This includes the performance of the temperature register values.

This register is readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0E	TEMPERATURE	TEMP[7:0]							
Reset Value		0	0	0	0	0	0	0	0

6.2.5 Device Lock Register (DEVLOCK_WR)

The device lock register is a user programmed read/write register which contains the ENDINIT bit and reset control bits.

This register is readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$10	DEVLOCK_WR	ENDINIT	RESERVED	RESERVED	RESERVED	SUP_ERR_DIS	RESERVED	RESET[1:0]	
Reset Value		0	0	0	0	0	0	0	0

6.2.5.1 End Initialization Bit (ENDINIT)

The ENDINIT bit is a control bit used to indicate that the user has completed all device and system level initialization tests. Once the ENDINIT bit is set, writes to all writable register bits are inhibited except for the DEVLOCK_WR register. Once set, the ENDINIT bit can only be cleared by a device reset.

When ENDINIT is set, the following occurs:

- An error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code.
- The offset cancellation filter is forced to its final stage.
- Self test is disabled and inhibited.
- Register Writes are inhibited with the exception of the RESET[1:0] bits in the DEVLOCK_WR register.

In DSI3 mode, when the ENDINIT bit is set, the device is forced to PDCM according to the device settings and no longer responds to CRM commands.

In PSI5 mode, the ENDINIT bit is automatically set when the device exits Initialization Phase 3.

6.2.5.2 Supply Error Reporting Disable Bit (SUP_ERR_DIS)

The supply error disable bit allows the user to disable reporting of the supply errors in the DSI3 PDCM and SPI status fields. Reference Section 6.2.2.5.

6.2.5.3 Reset Control Bits (RESET[1:0])

In DSI3 mode, SPI mode, I^2C mode or PSI5 mode, a series of three consecutive register write operations to the reset control bits will result in a device reset. To reset the device, the following register write operations must be performed in consecutive commands and in the order shown below or the device will not be reset.

Register Write to DEVLOCK_WR	RES_1	RES_0	Effect
Register Write 1	0	0	No Effect
Register Write 2	1	1	No Effect
Register Write 3	0	1	Device RESET

The response to a register write returns the new register value, including the values written to the RESET[1:0] bits. After the 3rd Register Write command, the device initiates a reset and thus does not transmit a response to this command or an Acknowledge in I2C mode. The response to a register read returns ‘00’ for RESET[1:0] and terminates the reset sequence. The reset control bits are not included in the read/write array error detection.

6.2.6 Write OTP Enable Register

The write OTP enable register is a user programmed read/write register that allows the user to write the contents of the user programmed OTP array mirror registers to the OTP registers. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$11	WRITE_OTP_EN	UOTP_WR_INIT	RESERVED	RESERVED	RESERVED	EX_COMMTYPE	EX_PADDR	UOTP_REGION[1:0]	
Reset Value		0	0	0	0	0	0	0	0

Register writes executed by the user to the user programmed OTP array only update the mirror register contents for the OTP array, not the actual OTP registers. To copy the values to the actual OTP registers, a write must be executed to the WRITE_OTP_EN register with the UOTP_WR_INIT bit set. The state of the UOTP_REGION[1:0], the EX_COMMTYPE and the EX_PADDR bits in the command determine which region of OTP will be written as shown below.

EX_COMMTYPE	EX_PADDR	UOTP_REGION[1]	UOTP_REGION[0]	OTP Write Operation	Special Conditions
x	x	0	0	Write the current contents of the UF0 registers to OTP	
x	x	0	1	Write the current contents of the UF1 registers to OTP	
0	0	1	0	Write the current contents of the UF2 registers to OTP, including the COMMTYPE register and the PHYSADDR register	
0	1	1	0	Write the current contents of the UF2 registers to OTP, including COMMTYPE and excluding PHYSADDR.	PHYSADDR = 0x00 after OTP Write
1	0	1	0	Write the current contents of the UF2 registers to OTP, excluding COMMTYPE and including PHYSADDR.	User must not overwrite COMMTYPE
1	1	1	0	Write the current contents of the UF2 registers to OTP, excluding COMMTYPE and excluding PHYSADDR.	User must not overwrite COMMTYPE PHYSADDR = 0x00 after OTP Write
x	x	1	1	Reserved for Future Use	

The UF0 and UF1 user OTP regions as well as the NXP programmed F OTP regions share common mirror registers. For this reason, writes to the OTP for each region must be completed independently according to the procedure below.

Depending upon the operating mode used, the user will need to write the UF2 values to OTP either with or without the PHYSADDR register and the COMMTYPE register being written. If Discovery Mode or switch connected daisy chain mode will be used, the PHYSADDR register must remain un-programmed (0x0000). If a pre-programmed bus mode will be used, the PHYSADDR register must be programmed to a non-zero value. To support these two user modes, the EX_PADDR bit is used as described in the table above.

Once a region is written using the OTP Write sequence, the LOCK_Uxx bit in the appropriate CRC_xxx register is automatically set, locking the array from future writes. Once a region is locked, an error detection is activated to detect changes to the register values. Register values in the UF2 region can be over-written using register write commands, but no new values can be written to the OTP.

The procedure for writing to the user OTP array UF0 and UF1 regions is listed below:

1. Read the appropriate CRC_UFx register and confirm the LOCK_Uxx bit is not set.
2. Write the desired values to the user array registers for only the region to be written using the procedures in Section 6.2.9.
   – The user must take care to ensure the proper data is written to each region. If a register write is executed to a new region, the base address will change to the new region. The previous data written to the register block will remain in the shared registers and will be written to OTP if the Write OTP sequence is completed.
3. Execute a write to the WRITE_OTP_EN register with the appropriate bits set for the desired region to program.
   – Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit will remain set.
4. Delay $t_{OTP\_WRITE\_MAX}$ to allow the device to complete the writes to OTP.
5. Verify that the OTP write successfully completed by reading back all of the OTP registers using Register Read commands as defined in Section 6.2.9.
6. Repeat steps 1 through 4 for all regions to be programmed.

The procedure for writing to the user OTP array UF2 region is listed below:

1. Read the CRC_UF2 register and confirm the LOCK_UF2 bit is not set.
2. Write the desired values to the user array registers.
3. Execute a write to the WRITE_OTP_EN register with region 2 selected and the EX_COMMTYPE and EX_PADDR bit set as desired.
   – Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit will remain set.
4. Delay $t_{OTP\_WRITE\_MAX}$ to allow the device to complete the writes to OTP and an automatic read of the UF2 registers from OTP.
5. Verify that the OTP write successfully completed by reading back all of the OTP registers using Register Read commands.

6.2.7 Bus Switch Control Register (BUSSW_CTRL)

The bus switch control register is a user programmed read/write register which controls the state of the bus switch output driver. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$12	BUSSW_CTRL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUSSW_CTRL[1:0]	
Reset Value		0	0	0	0	0	0	0	0

The BUSSW_CTRL bit controls the state of the BUSSW_L and BUSSW_H pins.

BUSSW_CTRL[1]	BUSSW_CTRL[0]	BUSSW_L Pin State	BUSSW_H Pin State
0	0	High Impedance An external pullup or pulldown resistor is required if an external switch is connected	High Impedance An external pullup or pulldown resistor is required if an external switch is connected
0	1	High Impedance An external pullup or pulldown resistor is required if an external switch is connected	High Impedance An external pullup or pulldown resistor is required if an external switch is connected
1	0	Active Low	Active Low
1	1	Active High	High Impedance An external pullup or pulldown resistor is required if an external switch is connected

Note: In DSI3 and PSI5 DPM modes, the bus switch will be activated upon receipt of the register write command. The bus switch activation may impact the current on the bus and cause corruption of the register write response.

6.2.8 PSI5 Test Register (PSI5_TEST)

The PSI5 test register is a user read/write register that contains the PSI5 test control. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$13	PSI5_TEST	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PSI5_TEST
Reset Value		0	0	0	0	0	0	0	0

6.2.8.1 PSI5 Test Bit (PSI5_TEST)

If PSI5 mode is not enabled in the COMMTYPE, the PSI5 test bit enables a single PSI5 command receive and response transmission to allow for the PSI5 transceiver to be tested in other modes.

When the PSI5_TEST bit is set, the device and system proceed through following process.

- The device switches the BUS_I transceiver to PSI5 mode.
- The system must hold the BUS_I node constant for 2ms minimum to allow the BUS_I command receiver to capture the average voltage.
- The system must transmit a sync pulse meeting the specifications in Section 5.
- The device will transmit a response to the sync pulse with the following configuration:
  - The sync pulse will be pulled down as configured by the SYNC_PD bit in the PSI5_CFG register.
  - The response will start in the time slot selected in the PDCM_RSPST0 register.
  - The response bit time will be as configured in the CHIPTIME register.
  - The response current will be as configured by the PSI5_ILOW bit in the PSI5_CFG register.
  - Two start bits will be transmitted as specified in Section 8.3.2.
  - 10-bits of data equal to 0x2AA will be transmitted.
  - Error checking bits will be transmitted as configured by the P_CRC bit in the PSI5_CFG register.
- Once the transmission is complete, the PSI5_TEST bit is cleared and the device returns to the communication mode as defined in the COMMTYPE register.

If the bit is set from DSI3 mode, this process occurs once the device has replied to the write message, regardless of whether or not the reply attempted was successful.

If the bit is set from SPI mode, the process occurs once the PSI5_TEST bit is set with no SPI reply necessary.

If the bit is set from I^{2}C mode, the process occurs once the PSI5_TEST bit is set with no I^{2}C reply necessary.

If PSI5 mode is enabled in the COMMTYPE register, this bit has no impact on device operation or performance.

6.2.9 UF Region Selection Registers (UF_REGION_x)

The UF region load register is a user read/write register that contains the control bits for the UF0 and UF1 regions to be accessed. This register is included in the user read/write array error detection. The UF region active register is a read only register that contains the status bits for the UF0 and UF1 regions to be accessed.

The UF_REGION_W register is readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode. The UF_REGION_R register is readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$14	UF_REGION_W	REGION_LOAD[3:0]				0	0	0	0
$15	UF_REGION_R	REGION_ACTIVE[3:0]				0	0	0	0
Reset Value		1	1	1	0	0	0	0	0

The user OTP regions UF0, UF1 and F share a block of 16 registers. Prior to reading the registers via any communication interface, the user must ensure that the desired OTP registers are loaded into the readable registers. Below is the necessary procedure to ensure proper reading of the UF0, UF1 and F registers.

1. Write the desired address range to be read to the REGION_LOAD[3:0] bits in the UF_REGION_W register using one of the communication interfaces available via the COMMTYPE register.

REGION_LOAD[3:0]				OTP Register Addresses Loaded into the Readable Registers
0	0	0	0	Not Applicable
0	0	0	1	Not Applicable
0010 through 1001				RESERVED
1	0	1	0	Address Range $A0 through $AF
1	0	1	1	Address Range $B0 through $BF
1	1	0	0	Address Range $C0 through $CF
1	1	0	1	Address Range $D0 through $DF
1	1	1	0	Address Range $E0 through $EF
1	1	1	1	Address Range $F0 through $FF

2. Delay a minimum of t_{SSN_UF01}.
3. Optional: Execute a register read of the UF_REGION_R register and confirm the REGION_ACTIVE[3:0] bits match the values written to the REGION_LOAD[3:0] bits in the UF_REGION_W register.

REGION_ACTIVE[3:0]				OTP Register Addresses Loaded into the Readable Registers
0	0	0	0	Load of OTP registers is in process
0	0	0	1	The contents of the shared registers has been over-written by the user
0010 through 1001				Not Applicable
1	0	1	0	Address Range $A0 through $AF
1	0	1	1	Address Range $B0 through $BF
1	1	0	0	Address Range $C0 through $CF
1	1	0	1	Address Range $D0 through $DF
1	1	1	0	Address Range $E0 through $EF
1	1	1	1	Address Range $F0 through $FF

4. Execute a Register Read of the desired registers from the UF0, UF1 or F register section. Complete all desired Register Reads of the selected UF Region.
5. Repeat steps 1 through 4 for the next desired UF region to read.

Notes:

- The user must take care to ensure that the desired registers are addressed. For example, if the REGION_LOAD bits are set to 0xA and the user executes a read of address $C2, the contents of registers $A2 will be transmitted. No error detection is included other than a read of the REGION_ACTIVE bits.
- For COMMTYPE options with multiple protocol options (COMMTYPE = ‘000 or ‘001’), no error detection is included other than a read of the REGION_ACTIVE bits. The user must take care to ensure that the REGION_LOAD, bits are not inadvertently changed by an alternative protocol while executing register reads.
- In DSI3, BDM, writes to registers are inhibited. For this reason, reads of the UF0, UF1 and F registers will only be possible for the region selected by the REGION_ACTIVE bits at the time ENDINIT is set.
- In SPI and I^2C mode, once the ENDINIT bit is set, writes to registers other than the RESET[1:0] bits are inhibited. For this reason, reads of the UF0, UF1 and F registers will only be possible for the region selected by the REGION_ACTIVE bits at the time ENDINIT is set.

6.2.10 Communication Type Register (COMMTYPE)

The Communication Type register is a user programmed read/write register which contains user specific configuration information for communication type. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode and I^{2}C mode. In PSI5 Programming Mode, the value of this register must not be changed or a U_OTP Memory will occur.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$16	COMMTYPE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	COMMTYPE[2:0]		
Unprogrammed OTP Value: FXLS60xxx		0	0	0	0	0	0	0	0
Programmed OTP Value: FLXS63xxx		0	0	0	0	0	0	0	1

6.2.10.1 Communication Type (COMMTYPE[2:0])

The communication type bits select the available protocols for the device as shown in the table below.

COMMTYPE[2:0]			Available Communication Protocols				Arming Function Availability	BUS_I Undervoltage Detection
			DSI3 (Section 7)	PSI5 (Section 8)	32-Bit SPI (Section 9)	I2C (Section 10)		
0	0	0	X		X		Enabled based on ARM_CFG[2:0]	Disabled
0	0	1		X	X		Enabled based on ARM_CFG[2:0]	Disabled
0	1	0			X		Enabled based on ARM_CFG[2:0]	Disabled
0	1	1	X				Disabled	Enabled
1	0	0			X		Enabled based on ARM_CFG[2:0]	Disabled
1	0	1		X			Disabled	Enabled
1	1	0				X	Disabled	Disabled
1	1	1				X	Disabled	Disabled

When writing to this register, care must be taken to prevent from inadvertently disabling the desired communication mode. Communication mode register value changes which disable a protocol, including writes to OTP, will not take effect until a device reset to prevent from disabling a necessary communication method. The table below describes how communication mode register changes are handled.

Original COMMTYPE	New COMMTYPE	Device Effect
0 (DSI3 / SPI)	1 (PSI5 / SPI)	Protocol change will not occur until a device reset (assuming the OTP is programmed)
0 (DSI3 / SPI)	2,3,4,5 (SPI, DSI3 or PSI5)	Protocol change will not occur until a device reset (assuming the OTP is programmed)
0 (DSI3 / SPI)	6,7 (I^{2}C)	Protocol change will not occur until a device reset (assuming the OTP is programmed)
1 (PSI5 / SPI)	Any	No protocol change will occur
2,3,4,5 (SPI)	Any	No protocol change will occur
6,7 (I^{2}C)	Any	No protocol change will occur

Notes:

- In PSI5 / SPI mode (COMMTYPE = 1), SPI transactions are ignored by the device until PSI5 initialization 3 is complete. SPI Test Mode Entry is not restricted.
- In PSI5 / SPI mode (COMMTYPE = 1), only SPI read register transactions are available.
- In DSI3 / SPI mode (COMMTYPE = 0) and PSI5 / SPI mode (COMMTYPE = 1), registers accesses by protocol are completed in the order received. Care must be taken to prevent from incorrect addressing of the F, UF0 and UF1 registers.
- In SPI only mode and in I2C only mode, the BUS_I undervoltage detection is disabled to allow for 3.3V system operation. the V_{BUF} undervoltage detection replaces the BUS_I undervoltage detection.
- If the COMMTYPE register is pre-programmed in OTP to a specific communication type, the user must prevent writes to this register when writing the UF2 register to OTP. If a pre-programmed COMMTYPE register is over-written and then written to OTP, the UF2 CRC verification will fail.

6.2.11 Physical Address Register (PHYSADDR)

The physical address register is a user programmed OTP register which contains the physical address of the slave for use in DSI3. This register is included in the read/write array error detection.

If the physical address stored in the OTP array is zero, the address is assigned either during Discovery Mode or during Command and Response Mode.

If the physical address stored in the OTP array is non-zero, the device ignores Discovery Mode and uses the programmed physical address for Command and Response Mode. The physical address register value can be changed by a Command and Response Mode register write command. However, if the UF2 region is locked, the value will always be reset to the OTP array value after a reset.

In SPI mode, I^2C mode and PSI5 mode, the PHYSADDR register is readable and writable, but has no impact on device operation or performance.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$18	PHYSADDR	0	0	0	0	PADDR[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.12 Source Identification Registers (SOURCEID_x)

The source identification registers are user programmed read/write registers which contain the source identification information used for DSI3 PDCM, PSI5 mode and SPI Mode. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$1A	SOURCEID_0	SID0_EN	PDCMFORMAT[2:0]			SOURCEID_0[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0
$1B	SOURCEID_1	SID1_EN	RESERVED	RESERVED	RESERVED	SOURCEID_1[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0
$1C	SOURCEID_2	SID2_EN	RESERVED	RESERVED	RESERVED	SOURCEID_2[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0
$1D	SOURCEID_3	SID3_EN	RESERVED	RESERVED	RESERVED	SOURCEID_3[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.12.1 Data Source Enable Bits (SIDx_EN)

The SIDx_EN bits enable the data source for the associated source identification as described in Section 6.2.12.3.

6.2.12.2 PDCM Format Control Bits (PDCMFORMAT[2:0])

In DSI3 mode, the PDCM format control bits set the PDCM field sizes as shown below. Reference Section 7.4.2 for PDCM response format details.

PDCMFORMAT[2:0]			Source ID Field Size (Bits)	Keep Alive Counter Field Size (Bits)	Status Field Size (Bits)	Data Field Size (Bits)	Total including CRC (Bits)
0	0	0	0	2	4	10	24
0	0	1	4	2	4	10	28
0	1	0	0	0	4	12	24
0	1	1	4	0	4	12	28
1	0	0	0	2	0	10	20
1	0	1	0	0	0	16	24
1	1	0	0	0	4	16	28
1	1	1	4	0	4	16	32

In PSI5 mode, the PDCM format control bits set the PSI5 response format as shown below. Reference Section 8.3.2 for PSI5 response format details. Note: the data field size applies to all modes except Programming Mode which has a fixed size of 10 bits. The user must take care to prevent from combining incompatible data field sizes and transmission times.

PDCMFORMAT[2:0]			Data Field Size (Bits)
0	0	0	10
0	0	1	10
0	1	0	10
0	1	1	10
1	0	0	16
1	0	1	16
1	1	0	16
1	1	1	16

In SPI and I^2C mode, the PDCMFORMAT bits are readable and writable, but have no impact on device operation or performance.

6.2.12.3 Source Identification (SOURCEID_x)

In SPI mode, the SOURCEID field in the SPI command is compared against the values in the SOURCEID_x registers. If the SOURCEID field matches one of the values in the SOURCEID_x registers and the SIDx_EN bit is set for that register, the sensor data for that SOURCEID is transmitted as shown in the table below. If more than one enabled SOURCEID_x register value matches the SOURCEID field in the SPI command a SPI sensor data request error response is transmitted. If no enabled SOURCEID_X register value matches the SOURCEID field in the SPI command a SPI sensor data request error response is transmitted.

Source ID	Source ID Enable (SIDx_EN)	Transmitted Data
SOURCEID_0	0	SPI Error Response
	1	CH0_SNSDATA0
SOURCEID_1	0	SPI Error Response
	1	CH0_SNSDATA1
SOURCEID_2	0	SPI Error Response
	1	CH1_SNSDATA0
SOURCEID_3	0	SPI Error Response
	1	CH1_SNSDATA1

In DSI3 mode, if the SIDx_EN bit in the SOURCEID_x register is set, the associated SOURCEID value is transmitted in the SOURCEID field of PDCM mode using the associated transmission time shown in the table below.

Source ID	Source ID Enable (SIDx_EN)	Transmission Time Reference Section 6.2.17.1	Transmitted Data Reference Section 6.2.24.2 Reference Section 6.2.24.3
SOURCEID_0	0	NA	NA
	1	PDCM_RSPST0	CH0_SNSDATA0
SOURCEID_1	0	NA	NA
	1	PDCM_RSPST1	CH0_SNSDATA1
SOURCEID_2	0	NA	NA
	1	PDCM_RSPST2	CH1_SNSDATA0
SOURCEID_3	0	NA	NA
	1	PDCM_RSPST3	CH1_SNSDATA1

In PSI5 mode, the SOURCEID_x register SIDx_EN bit values control data transmissions as shown in the table below. The SOURCEID_x bits have no effect in PSI5 mode.

Source ID	Source ID Enable (SIDx_EN)	Asynchronous Mode		Synchronous Mode		Daisy Chain Mode		Dual Transmission Mode	
		Transmission Time	Transmission Data	Transmission Time Reference Section 6.2.17.1	Transmitted Data Reference Section 6.2.24.2 Reference Section 6.2.24.3	Transmission Time	Transmitted Data	Transmission Time	Transmitted Data
SOURCEID_0	0	t_{ASYNC}	CH0_SNSDATA0	NA	NA	Reference Section 8.7	CH0_SNSDATA0	PDCM_RSPST0	CH1_SNSDATA0, CH0_SNSDATA0 Reference Section 8.6
	1			PDCM_RSPST0	CH0_SNSDATA0				
SOURCEID_1	0	NA	NA	NA	NA	NA	NA	NA	NA
	1			PDCM_RSPST1	CH0_SNSDATA1				
SOURCEID_2	0	NA	NA	NA	NA	Reference Section 8.7	CH1_SNSDATA0	NA	NA
	1			PDCM_RSPST2	CH1_SNSDATA0				
SOURCEID_3	0	NA	NA	NA	NA	NA	NA	NA	NA
	1			PDCM_RSPST3	CH1_SNSDATA1				

In I^2C mode, the SOURCEID_x registers are readable and writable. Reference Section 10.6.3, for details regarding the effect of the SIDx_EN bits.

6.2.13 Communication Timing Register (TIMING_CFG)

The communication timing configuration register is a user programmed read/write register which contains user specific configuration information for protocol timing. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$22	TIMING_CFG	PDCM_PER[2:0]			OSCTRAIN_SEL	CK_CAL_RST	CRM_PER[1:0]		CK_CAL_EN
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.13.1 Periodic Data Collection Mode Period (PDCM_PER[3:0])

The Periodic Data Collection Mode period selection bits set the data collection mode period to be used by the DSI3, SPI, PSI5 or I^2C master as shown in the table below. This value is only necessary for oscillator training and is only used if the CK_CAL_EN bit is set in the TIMING_CFG register.

PDCM_PER[2]	PDCM_PER[1]	PDCM_PER[0]	Periodic Data Collection Mode Period
0	0	0	100 μs
0	0	1	125 μs
0	1	0	250 μs
0	1	1	333 μs
1	0	0	500 μs
1	0	1	800 μs
1	1	0	1000 μs
1	1	1	2000 μs

In DSI3 mode, PDCM and BDM commands are decoded and responded to regardless of the value of this register as long as the general PDCM timing parameters specified in Section 5.11 are met. Reference Section 6.5.1 for details regarding oscillator training.

In PSI5 synchronous mode, sync pulses are decoded and responded to regardless of the value of this register as long as the general timing parameters specified in Section 5.12 are met. Reference Section 6.5.1 for details regarding oscillator training.

In PSI5 asynchronous mode, oscillator training is not applicable.

In PSI5 Programming Mode, oscillator training is not applicable.

In PSI5 Daisy Chain command phase, oscillator training is not applicable.

In SPI mode, sensor data requests are decoded and responded to regardless of the value of this register as long as the general timing parameters specified in Section 5.13 are met. Reference Section 6.5.1 for details regarding oscillator training.

In I^2C mode, sensor data register reads are decoded and responded to regardless of the value of this register as long as the general timing parameters specified in Section 5.14 are met. Reference Section 6.5.1 for details regarding oscillator training.

6.2.13.2 Oscillator Training Protocol Selection Bit (OSCTRAIN_SEL)

The oscillator training selection bit selects the protocol to use for oscillator training for the COMMTYPE values that enable multiple protocols as shown in the table below:

COMMTYPE	OSCTRAIN_SEL	Protocol to use for Oscillator Training
0	0	DSI3
	1	SPI
1	0	PSI5
	1	SPI
2	x	SPI
3	x	DSI3
4	x	SPI
5	x	PSI5
6	x	I2C
7	x	I2C

6.2.13.3 Clock Calibration Value Reset (CK_CAL_RST)

The clock calibration reset bit controls the state of the oscillator training when the CK_CAL_EN bit is cleared as described in the table in Section 6.2.13.5. Reference Section 6.5.1 for details regarding oscillator training.

6.2.13.4 Command and Response Mode Period (CRM_PER[1:0])

In DSI3 mode, the Command and Response Mode period bits set the period for Command and Response Mode commands in increments of the Periodic Data Collection Mode period (PDCM_PER). This value is only necessary for DSI3 oscillator training and is only used if the CK_CAL_EN bit is set in the TIMING_CFG register. Command and Response Mode commands will be decoded and responded to regardless of the value of this register as long as the general Command and Response Mode timing parameters specified in Section 5.11 are met. Reference Section 6.5.1 for details regarding oscillator training.

In SPI and I^2C mode, the CRM_PER[1:0] bits are readable and writable, but have no impact on device operation or performance.

In PSI5 mode, the CRM_PER[1:0] bits are readable and writable, but have no impact on device operation or performance.

CRM_PER[1]	CRM_PER[0]	Command and Response Mode Period (Multiples of the Periodic Data Collection Mode Period)
0	0	1
0	1	2
1	0	4
1	1	8

6.2.13.5 Clock Calibration Enable (CK_CAL_EN)

The clock calibration enable bit enables oscillator training over the DSI3, PSI5, SPI or I^2C communication interface. Reference Section 6.5.1 for details regarding oscillator training.

CK_CAL_EN	CK_CAL_RST	Oscillator Training
0	0	The oscillator value is maintained at the last trained value prior to clearing the CK_CAL_RST bit.
0	1	The oscillator value is reset to the untrained value with a tolerance specified in Section 5.20.
1	x	Oscillator is trained as specified in Section 6.5.1

6.2.14 Chip Time and Bit Time Register (CHIPTIME)

The Chip Time and Bit Time register is a user programmed read/write register which contains user specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$23	CHIPTIME	RESERVED	RESERVED	RESERVED	SS_EN	CHIPTIME[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.14.1 Simultaneous Sampling Enable (SS_EN)

In DSI3 mode, the simultaneous sampling enable bit selects between one of two data latency methods. Reference Section 7.4.7 for details regarding sample timing.

SS_EN	Data Latency
0	Synchronous Sampling Mode: Latency relative to transmission start time (PDCM_RSPST)
1	Simultaneous Sampling Mode: Latency relative to the start of the Periodic Data Collection Mode command (falling edge)

In PSI5 mode, the simultaneous sampling enable bit selects between one of two data latency methods to accommodate synchronized sampling or simultaneous sampling.

SS_EN	Data Latency
0	Synchronous Sampling Mode (Latency relative to Time Slot)
1	Simultaneous Sampling Mode (Latency relative to sync pulse)

In SPI mode, the simultaneous sampling enable bit selects between one of two data latency methods.

SS_EN	Data Latency
0	Synchronous Sampling Mode: The data for all sources is latent relative to the falling edge of slave select for the response to the Sensor Data Request for the corresponding SOURCEID.
1	Simultaneous Sampling Mode: The data for all sources is latent relative to the falling edge of slave select for the response to the Sensor Data Request for SOURCEID_0. If SOURCEID_0 is disabled, then the data for all SOURCEIDs is latent relative to the falling edge of slave select for the response to the Sensor Data Request for lowest enabled SOURCEID register address. Note: If multiple SOURCEIDs are enabled, sensor data for the higher SOURCEID register addresses only changes on a sensor data request for the lowest enabled SOURCEID register address. If continuous sensor data requests occur without sensor data requests for the lowest SOURCEID register address, sensor data will not be updated. Care must be take by the user to ensure proper data transmissions.

In I^2C mode, the simultaneous sampling enable bit is readable and writable but has no impact on device operation or performance.

6.2.14.2 Chip Time (CHIPTIME)

In DSI3 mode, the CHIPTIME bits set the chip time for Periodic Data Collection Mode as described below. The chip time for Command and Response Mode and Background Diagnostic Mode is always set to 5μs with slew control enabled.

In PSI5 mode, the CHIPTIME bits set the bit time for the PSI5 response data as described below.

CHIPTIME[3]	CHIPTIME[2]	CHIPTIME[1]	CHIPTIME[0]	PSI5			DSI3		
				Period Time	Baud Rate	Slew Control	Chip Time	Chip Rate	Slew Control
0	0	0	0	5.3 μs	189 kHz	Enabled	1.0 μs	1000 kHz	Disabled
0	0	0	1	5.3 μs	189 kHz	Enabled	2.0 μs	500.0 kHz	Disabled
0	0	1	0	5.3 μs	189 kHz	Enabled	2.5 μs	400.0 kHz	Enabled
0	0	1	1	5.3 μs	189 kHz	Enabled	2.6 μs	384.6 kHz	Enabled
0	1	0	0	5.3 μs	189 kHz	Enabled	2.6 μs	384.6 kHz	Enabled
0	1	0	1	5.3 μs	189 kHz	Enabled	2.7 μs	370.3 kHz	Enabled
0	1	1	0	5.3 μs	189 kHz	Enabled	2.8 μs	357.1 kHz	Enabled
0	1	1	1	5.3 μs	189 kHz	Enabled	2.9 μs	344.8 kHz	Enabled
1	0	0	0	8.0 μs	125 kHz	Enabled	3.0 μs	333.3 kHz	Enabled
1	0	0	1	8.0 μs	125 kHz	Enabled	3.1 μs	322.6 kHz	Enabled
1	0	1	0	8.0 μs	125 kHz	Enabled	3.2 μs	312.5 kHz	Enabled
1	0	1	1	8.0 μs	125 kHz	Enabled	3.3 μs	303.0 kHz	Enabled
1	1	0	0	8.0 μs	125 kHz	Enabled	3.5 μs	294.1 kHz	Enabled
1	1	0	1	8.0 μs	125 kHz	Enabled	4.0 μs	250.0 kHz	Enabled
1	1	1	0	8.0 μs	125 kHz	Enabled	4.5 μs	222.2 kHz	Enabled
1	1	1	1	8.0 μs	125 kHz	Enabled	5.0 μs	200.0 kHz	Enabled

In SPI and I^2C mode, the CHIPTIME bits are readable and writable but have no impact on device operation or performance.

6.2.15 DSI3 Background Diagnostic Mode Configuration Register (BDM_CFG)

The DSI3 Background Diagnostic Mode configuration register is a user programmed read/write register which contains user specific configuration information for DSI3 Background Diagnostic Mode. This register is included in the read/write array error detection. Reference Section 7.4 for details regarding Background Diagnostic Mode.

This register is readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$24	BDM_CFG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BDM_FRAGSIZE	BDM_EN
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.15.1 Background Diagnostic Mode Fragment Size (BDM_FRAGSIZE)

The Background Diagnostic Mode fragment size bit sets the number of background diagnostic command bits and response chips to be sent per Periodic Data Collection Mode sampling period.

BDM_FRAGSIZE	BDM Command Fragment Size (Bits)	BDM Response Fragment Size (Chips)
0	2	3
1	4	6

In SPI and I^2C mode, the BDM_FRAGSIZE bit is readable and writable, but has no impact on device operation or performance.

In PSI5 mode, the BDM_FRAGSIZE bit is readable and writable, but has no impact on device operation or performance.

6.2.15.2 Background Diagnostic Mode Enable (BDM_EN)

The Background Diagnostic Mode enable bit enables background diagnostic mode as described in the table below. Reference Section 7.4 for details regarding Background Diagnostic Mode.

BDM_EN	Background Diagnostic Mode
0	Disabled
1	Enabled

In SPI and I^2C mode, the BDM_EN bit is readable and writable, but has no impact on device operation or performance.

In PSI5 mode, the BDM_EN bit is readable and writable, but has no impact on device operation or performance.

6.2.16 PSI5 Configuration Register (PSI5_CFG)

The PSI5 configuration register is a user programmable OTP register that contains PSI5 specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$25	PSI5_CFG	SYNC_PD	DAISY_CHAIN	PSI5_ILOW	DUALTRANS	EMSG_EXT	P_CRC	INIT2_EXT	ASYNC
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.16.1 Sync Pulse Pull-Down Enable Bit (SYNC_PD)

In PSI5 mode, the sync pulse pull-down enable bit selects if the Sync pulse pull-down is enabled once a sync pulse is detected. Reference Section 6.2.17.1 for more information regarding the sync pulse pulldown.

SYNC_PD	Sync Pulse Pull-Down
0	Disabled
1	Enabled for all PSI5 operating modes

In DSI3 mode, the SYNC_PD bit is readable and writable, but has no impact on device operation or performance.

in SPI and I^2C mode, the SYNC_PD bit is readable and writable, but has no impact on device operation or performance.

6.2.16.2 PSI5 Daisy Chain Selection Bit (DAISY_CHAIN)

In PSI5 mode, the transmission mode selection bits select the PSI5 transmission mode as shown below.

DAISY_CHAIN	Operating Mode	Response (PDCM_RSTST0)	Reference
0	Normal Mode (Asynchronous or Parallel, Synchronous)	SNSDATA0	Section 8.5
1	Daisy Chain Mode	SNSDATA0	Section 8.7

In DSI3 mode, the DAISY_CHAIN bit is readable and writable, but has no impact on device operation or performance.

In SPI and I^2C mode, the DAISY_CHAIN bit is readable and writable, but has no impact on device operation or performance.

6.2.16.3 PSI5 Low Response Current Selection Bit (PSI5_ILOW)

In PSI5 mode, the PSI5 low response current selection bit selects the low PSI5 response current specified in Section 5.4 as shown below.

PSI5_ILOW	PSI5 Response Current
0	Normal Response Current
1	Low Response Current

In DSI3 mode, the PSI5_ILOW bit is readable and writable, but has no impact on device operation or performance.

In SPI and I^2C mode, the PSI5_ILOW bit is readable and writable, but has no impact on device operation or performance.

6.2.16.4 Dual Transmission Mode (DUALTRANS)

In PSI5 mode, the dual transmission mode bit enables dual data transmission as described in Section 8.6 only if the DAISY_CHAIN bit is not set and the ASYNC bit is not set.

DUALTRANS	Operating Mode	Response (PDCM_RSTST0)	Reference
0	Normal Mode (Asynchronous or Parallel, Synchronous, Daisy Chain)	SNSDATA0	Section 8.5, Section 8.7
1	Dual Data Transmission Mode	SNSDATA0 and SNSDATA1	Section 8.6

In DSI3 mode, the DUALTRANS mode is readable and writable, but has no impact on device operation or performance.

In SPI and I^2C mode, the DUALTRANS bits are readable and writable, but has no impact on device operation or performance.

6.2.16.5 Error Message Information Extension Bit (EMSG_EXT)

In PSI5 mode, the error message information extension bit enables or disables additional PSI5 error message information as shown below.

EMSG_EXT	Description
0	All internal Errors map to 0x1F4 (Reference Section 8.3.4)
1	Additional PSI5 reserved codes are used for internal error distinction (Reference Section 8.3.4)

In DSI3 mode, the EMSG_EXT bit is readable and writable, but has no impact on device operation or performance.

In SPI and I^2C mode, the EMSG_EXT bit is readable and writable, but has no impact on device operation or performance.

6.2.16.6 PSI5 Response Message Error Detection Selection Bit (P_CRC)

In PSI5 Mode, the response message error detection selection bit selects either even parity, or a 3-Bit CRC for error detection of the PSI5 response message. Reference Section 6.2.17.1 for details regarding response message error detection.

P_CRC	Parity or CRC
0	Parity
1	CRC

In DSI3 mode, the P_CRC bit is readable and writable, but has no impact on device operation or performance.

in SPI and I^2C mode, the P_CRC bit is readable and writable, but has no impact on device operation or performance.

6.2.16.7 Initialization Phase 2 Data Extension Bit (INIT2_EXT)

In PSI5 mode, the initialization phase 2 data extension bit enables or disables data transmission in data fields D33 through D48 of PSI5 Initialization Phase 2 as shown below.

INIT2_EXT	Description
0	D33 through D48 are not transmitted
1	D33 through D48 are transmitted as defined in Section 8.4.2.1

In DSI3 mode, the INIT2_EXT bit is readable and writable, but has no impact on device operation or performance.

in SPI and I^2C mode, the INIT2_EXT bit is readable and writable, but has no impact on device operation or performance.

6.2.16.8 Asynchronous Mode Bit (ASYNC)

In PSI5 mode, the asynchronous mode bit enables asynchronous data transmission as described in Section 6.2.17.1 only if the DAISY_CHAIN bit is not set.

In DSI3 mode, the ASYNC bit is readable and writable, but has no impact on device operation or performance.

in SPI and I^2C mode, the ASYNC bit is readable and writable, but has no impact on device operation or performance.

6.2.17 DSI3 and PSI5 Start Time Registers (PDCM_RSPSTx_x)

The DSI3 and PSI5 start time registers are user programmed read/write registers which contain user specific configuration information for DSI3 Periodic Data Collection Mode and PSI5 Synchronous Mode. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$26	PDCM_RSPST0_L	PDCM_RSPST0[7:0]							
$27	PDCM_RSPST0_H	BRC_RSP0[1:0]		RESERVED	PDCM_RSPST0[12:8]				
$28	PDCM_RSPST1_L	PDCM_RSPST1[7:0]							
$29	PDCM_RSPST1_H	BRC_RSP1[1:0]		RESERVED	PDCM_RSPST1[12:8]				
$2A	PDCM_RSPST2_L	PDCM_RSPST2[7:0]							
$2B	PDCM_RSPST2_H	BRC_RSP2[1:0]		RESERVED	PDCM_RSPST2[12:8]				
$2C	PDCM_RSPST3_L	PDCM_RSPST3[7:0]							
$2D	PDCM_RSPST3_H	BRC_RSP3[1:0]		RESERVED	PDCM_RSPST3[12:8]				
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.17.1 Periodic Data Collection Mode Response Start Time (PDCM_RSPSTx[12:0])

The Periodic Data Collection Mode response start time registers set the DSI3 Periodic Data Collection Mode or PSI5 Synchronous mode response start time for the associated data and SOURCEID. The value is stored in 1.0μs increments.

PDCM_RSPSTx[12:0]	Periodic Data Collection Mode Response Start Time
0	See Table Below
0 < PDCM_RSPSTx[12:0] < 20	20.0μs
20 < PDCM_RSPSTx[12:0]	PDCM response start = PDCM_RSPST x 1.0μs

The table below shows the relationship of the SOURCEID, the transmitted data, the response start times and the default states for each set of registers in DSI3 Periodic Data Collection Mode. Care must be taken to prevent from programming response start times which cause data contention in the system.

SOURCEID REGISTER	Transmitted Data	Start Time Registers	Default Start (PDCM_RSPSTx[12:0] = 0x00)
SOURCEID_0	CH0_SNSDATA0	PDCM_RSPST0[12:0]	Transmit Data with a start time of 20μs
SOURCEID_1	CH0_SNSDATA1	PDCM_RSPST1[12:0]	Transmit Data with a start time of 20μs
SOURCEID_2	CH1_SNSDATA0	PDCM_RSPST2[12:0]	Transmit Data with a start time of 20μs
SOURCEID_3	CH1_SNSDATA1	PDCM_RSPST3[12:0]	Transmit Data with a start time of 20μs

The table below shows the PSI5 data transmission start times based on the values in the PDCM_RSPSTx registers and the value of the ASYNC bit. Care must be taken to prevent from programming time slots which violate the PSI5 Version 1.3 specification, or time slots which will cause data contention.

ASYNC Bit	SOURCEID REGISTER	Transmitted Data	Time Slot Start Time	Default Start (PDCM_RSPSTx[12:0] = 0x00)
1	SOURCEID_0	CH0_SNSDATA0	Asynchronous Mode	t_{ASYNC}
0	SOURCEID_0	CH0_SNSDATA0	PDCM_RSPST0[12:0]	Transmit Data with a start time of 20μs
	SOURCEID_1	CH0_SNSDATA1	PDCM_RSPST1[12:0]	Transmit Data with a start time of 20μs
	SOURCEID_2	CH1_SNSDATA0	PDCM_RSPST2[12:0]	Transmit Data with a start time of 20μs
	SOURCEID_3	CH1_SNSDATA1	PDCM_RSPST3[12:0]	Transmit Data with a start time of 20μs

In SPI and I^{2}C mode, the PDCM_RSPSTx registers are readable and writable, but have no impact on device operation or performance.

6.2.17.2 Broadcast Read Command Type Selection Bits (BRC_RSP[1:0])

The broadcast read command type selection bits select the Broadcast Read Command types that the device responds to for each Source ID as shown in the table below:

BRC_RSP[1]	BRC_RSP[0]	Response
0	0	Respond to all Broadcast Read Commands
0	1	Respond to Broadcast Read Command 0 only
1	0	Respond to Broadcast Read Command 1 only
1	1	Respond to all Broadcast Read Commands

If a device is programmed to respond only to BRC0 or BRC1 commands, it will synchronize to alternate responses when BDM commands are received.

- If the last command prior to a BDM command is a BRC0, a device programmed to respond only to BRC0 commands will not respond to the first BDM command and will then respond to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC0, a device programmed to respond only to BRC1 commands will respond to the first BDM command, and will then response to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC1, a device programmed to respond only to BRC0 commands will respond to the first BDM command, and will then response to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC1, a device programmed to respond only to BRC1 commands will not respond to the first BDM command and will then respond to every other BDM command until the next BRC command is received.

In PSI5 mode, the BRC_RSP[1:0] bits are readable and writable, but have no impact on device operation or performance.

In SPI and I^2C mode, the BRC_RSP[1:0] bits are readable and writable, but have no impact on device operation or performance.

6.2.18 DSI3 and PSI5 Command Blocking Time Registers (PDCM_CMD_B_x)

The DSI3 and PSI5 Command Blocking registers are user programmed read/write registers which contain user specific configuration information for DSI3 mode and PSI5 mode. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$38	PDCM_CMD_B_L	PDCM_CMD_B[7:0]							
$39	PDCM_CMD_B_H	RESERVED	RESERVED	RESERVED	PDCM_CMD_B[12:8]				
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

In DSI3 mode, the DSI3 Periodic Data Collection Mode command blocking time bits set the Periodic Data Collection Mode command blocking time in 1.0µs increments, with zero as the default value of 450µs. For proper communication, the command blocking time must exceed the completion of the last source response transmission. Reference Section 7.1.1 for details regarding the command receiver and command blocking.

Care must be taken to prevent from programming command blocking times which prevent proper command decoding in the system and to ensure proper sampling of the VHIGH voltage. As shown in Section 7.1.1, Section 7-2, The VHIGH voltage is initially captured at the end of the command blocking time and then filtered. The user must ensure that the command blocking end time is set for a time when no command or response transmissions are occurring to provide the most stable BUS_I voltage.

PDCM_CMD_B[12:0]	Sync Pulse Blocking Time
0	450µs
Non-Zero	Sync Pulse Blocking Time = PDCM_CMD_B x 1µs

In PSI5 mode, the command blocking time bits set the PSI5 sync pulse blocking time in 1.0µs increments, with zero as the default value of 450µs. Reference Section 8.2.1 for details regarding the PSI5 sync pulse receiver and command blocking.

Care must be taken to prevent from programming command blocking times which prevent proper sync pulse decoding in the system and to ensure proper sampling of the PSI5 voltage.

PDCM_CMD_B[12:0]	Sync Pulse Blocking Time
0,1, 2, 3, 4, 5, 6, 7, 8, 9	450µs
10 - 8191	Sync Pulse Blocking Time = PDCM_CMD_B x1µs

in SPI and I^2C mode, the PDCM_CMD_B bits are readable and writable, but have no impact on device operation or performance.

6.2.19 SPI Configuration Control Register

In SPI mode, the SPI configuration control register is a user programmed read/write register which contains the SPI protocol configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$3D	SPI_CFG	RESERVED	DATASIZE	SPI_CRC_LEN[1:0]		SPICRCSEED[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.19.1 SPI Data Field Size Bit (DATASIZE)

The SPI data field size bit controls the size of the SPI data field as shown below. Reference Section 6.6.4.9.

DATASIZE	SPI Data Field Size
0	12-Bits
1	16-Bits

In DSI3 mode, the DATASIZE bit is readable and writable, but has no impact on device operation or performance.

in PSI5 mode, the DATASIZE bit is readable and writable, but has no impact on device operation or performance.

in I^2C mode, the DATASIZE bit is readable and writable, but has no impact on device operation or performance.

6.2.19.2 SPI CRC Length and Seed Bits (SPI_CRC_LEN[1:0], SPICRCSEED[3:0])

The SPI_CRC_LEN[1:0] bits select the CRC length for SPI Mode as shown in the table below. The SPI CRC seed bits contain the seed used for the SPI Mode. The default SPI CRC is an 8-bit. When the SPI_CRC_LEN[1:0] bits are set to a non-zero value using a Register Write command, the SPI CRC changes as defined in the table. The new polynomial value is enabled for both MISO and MOSI on the next SPI Mode command.

The default seed (SPICRCSEED[3:0] = 0x0) is 0xFF for an 8-bit CRC. When the value is changed to a non-zero value using a Register Write command, the SPI CRC seed changes to the value programmed as shown in the table. The new seed value is enabled for both MISO and MOSI on the next SPI Mode command.

SPI_CRC_LEN[1:0]		SPICRCSEED	CRC Polynomial	CRC Seed
0	0	0	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111, 1111
		Non-Zero		1111, SPICRCSEED[3:0]
0	1	0	$x^4 + 1$	1010
		Non-Zero		SPICRCSEED[3:0]
1	0	0	$x^3 + x + 1$	111
		Non-Zero		SPICRCSEED[2:0]
1	1	0	$x^3 + x + 1$	111
		Non-Zero		SPICRCSEED[2:0]

In PSI5 mode, the SPI CRC bits are readable and writable, but have no impact on device operation or performance.

In DSI3 mode, the SPI CRC bits are readable and writable, but have no impact on device operation or performance.

In I^2C mode, the SPI CRC bits are readable and writable, but have no impact on device operation or performance.

6.2.20 Who Am I Register

The Who Am I register is a user programmed read/write register which contains the unique product identifier for I^{2}C mode. The register is readable in all modes. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$3E	WHO_AM_I	WHO_AM_I[7:0]							
Unprogrammed OTP Value		0	0	0	0	0	0	0	0
Unprogrammed Read Value		1	1	0	0	0	1	0	0

The default register value is 0x00. If the register value is 0x00, a value of 0xC4 is transmitted in response to a read command. For all other register values, the actual register value is transmitted in response to a read command.

WHO_AM_I Register Value (HEX)	Response to a Register Read Command
0X00	0xC4
0X01 Through 0xFF	Actual Register Value

6.2.21 I^{2}C Slave Address Register

The I^{2}C Slave Address register is a user programmed read/write register which contains the unique I^{2}C slave address. The register is readable in all modes. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$3F	I2C_ADDRESS	I2C_ADDRESS[7:0]							
Unprogrammed OTP Value		0	0	0	0	0	0	0	0
Unprogrammed Read Value		0	1	1	0	0	0	0	0

The default register value is 0x00. If the register value is 0x00, the I^{2}C slave address is 0x60 and a value of 0x60 is transmitted in response to a read command. For all other register values, the I^{2}C slave address is the lower 7 bits of the actual register value and the actual register value is transmitted in response to a read command.

I2C_ADDRESS Register Value (HEX)	Response to a Register Read Command	I^{2}C Slave Address
0x00, 0x80	0x60	0x60
0x01 Through 0x7F, 0x81 Through 0xFF	Actual Register Value	I2C_ADDRESS[6:0]

6.2.22 Channel 0 and Channel 1 User Configuration #1 Registers (CH0_CFG_U1, CH1_CFG_U1)

The Channel 0 and Channel 1 user configuration #1 registers are user programmable read/write registers which contain channel specific configuration information. These registers are included in the read/write array error detection.

Changes to these registers reset the DSP datapath. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in Section 5.20. Reads of the SNSDATA_x registers and Sensor Data requests should be prevented during this time.

These registers are readable and writable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$40	CH0_CFG_U1	LPF[3:0]				SAMPLERATE[1:0]		USER_SNS_SHIFT[1:0]	
$48	CH1_CFG_U1	LPF[3:0]				SAMPLERATE[1:0]		USER_SNS_SHIFT[1:0]	
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.22.1 Low-Pass Filter and Sample Rate Selection Bits (LPF[3:0], SAMPLERATE[1:0])

The low pass filter selection bits and sample rate bits select the low pass filter for the associated channel. Reference Section 6.6.4.4 for details regarding the low pass filter.

LPF[3]	LPF[2]	LPF[1]	LPF[0]	Low Pass Filter Type		
				SAMPLERATE = 00, 01	SAMPLERATE = 10	SAMPLERATE = 11
				16μs	32μs	64μs
0	0	0	0	400Hz, 4-Pole	200Hz, 4-Pole	100Hz, 4-Pole
0	0	0	1	400Hz, 3-Pole	200Hz, 3-Pole	100Hz, 3-Pole
0	0	1	0	400Hz, 4-Pole	200Hz, 4-Pole	100Hz, 4-Pole
0	0	1	1	400Hz, 3-Pole	200Hz, 3-Pole	100Hz, 3-Pole
0	1	0	0	325Hz, 3-Pole	162.5Hz, 3-Pole	81.25Hz, 3-Pole
0	1	0	1	370Hz, 2-Pole	185Hz, 2-Pole	92.5Hz, 2-Pole
0	1	1	0	180Hz, 2-Pole	90Hz, 2-Pole	45Hz, 2-Pole
0	1	1	1	100Hz, 2-Pole	50Hz, 2-Pole	25Hz, 2-Pole
1	0	0	0	1500Hz, 4-Pole	750Hz, 4-Pole	375Hz, 4-Pole
1	0	0	1	500Hz, 3-Pole	250Hz, 3-Pole	125Hz, 3-Pole
1	0	1	0	800Hz, 4-Pole	400Hz, 4-Pole	200Hz, 4-Pole
1	0	1	1	1200Hz, 4-Pole	600Hz, 4-Pole	300Hz, 4-Pole
1	1	0	0	120Hz, 3-Pole	60Hz, 3-Pole	30Hz, 3-Pole
1	1	0	1	120Hz, 3-Pole	60Hz, 3-Pole	30Hz, 3-Pole
1	1	1	0	120Hz, 2-Pole	60Hz, 2-Pole	30Hz, 2-Pole
1	1	1	1	50Hz, 4-Pole	25Hz, 4-Pole	12.5Hz, 4-Pole

6.2.22.2 User Sensitivity Shift Selection Bits (U_SNS_SHIFT[1:0])

The user sensitivity selection bits are used along with the user sensitivity multiplier bits to scale the output sensitivity of the device. Reference Section 6.2.23.1 for details.

6.2.23 Channel 0 and Channel 1 User Configuration #2 Registers (CH0_CFG_U2, CH1_CFG_U2)

The Channel 0 and Channel 1 user configuration #2 registers are user programmable read/write registers which contain channel specific configuration information. The registers are included in the read/write array error detection.

Changes to these registers reset the DSP datapath. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in Section 5.20. Reads of the SNSDATA_x registers and Sensor Data requests should be prevented during this time.

These registers are readable and writable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$41	CH0_CFG_U2	U_SNS_MULT[7]	U_SNS_MULT[6]	U_SNS_MULT[5]	U_SNS_MULT[4]	U_SNS_MULT[3]	U_SNS_MULT[2]	U_SNS_MULT[1]	U_SNS_MULT[0]
$49	CH1_CFG_U2	U_SNS_MULT[7]	U_SNS_MULT[6]	U_SNS_MULT[5]	U_SNS_MULT[4]	U_SNS_MULT[3]	U_SNS_MULT[2]	U_SNS_MULT[1]	U_SNS_MULT[0]
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.23.1 User Sensitivity Multiplier Bits (U_SNS_MULT[7:0])

The user sensitivity multiplier bits are used along with the user sensitivity shift bits to scale the output sensitivity of the device. The equation below describes the scaling:

$$OutputSensitivity(12bit) = TrimSensitivity \times SensitivityShiftFactor \times \frac{256 + SensitivityMultiplier}{256}$$

Where:

- $TrimSensitivity$ = The default trimmed sensitivity of the device, as specified in Section 5.6
- $SensitivityMultiplier$ = The unsigned multiplier value contained in the U_SNS_MULT[7:0] bits
- $SensitivityShiftFactor$ = The Shift Factor selected by the U_SNS_SHIFT[1:0] bits as described in the table below

Device Type	U_SNS_SHIFT[1]	U_SNS_SHIFT[0]	Sensitivity Shift Factor
Normal Range	0	0	0.25
Normal Range	0	1	0.50
Normal Range	1	0	1
Normal Range	1	1	2

Note: This table includes some typical device ranges. Other ranges are possible with the user selected shift and multiplier values.

Device Type	Desired Range (g)	Desired Sensitivity (12-Bit, LSB/g)	NXP Trim (12-Bit, LSB/g)	User Sensitivity Shift Factor		User Multiplier Value		Actual Sensitivity 16-Bit Register Chx_SNS-DATAx LSB/g)	Actual Sensitivity 10-Bit Sensor Data Request, LSB/g	Actual Sensitivity 12-Bit Sensor Data Request, LSB/g	Actual Sensitivity 16-Bit Sensor Data Request, LSB/g
				U_SNS_SHIFT (HEX)	Shift Factor	U_SNS_-MULT (HEX)	Multiplier Value (Dec)				
Medium g	15.5	131.7246	33.0161	0x3	2	0xFF	255	263.6130	32.9516	131.8065	2108.904
	16	127.9375	33.0161	0x3	2	0xF0	240	255.8748	31.9844	127.9374	2046.998
	20	102.3500	33.0161	0x3	2	0x8D	141	204.8030	25.6004	102.4015	1638.424
	25	81.8800	33.0161	0x3	2	0x3D	61	163.5328	20.4416	81.7664	1308.262
	35	58.4857	33.0161	0x2	1	0xC5	197	116.8460	14.6058	58.4230	934.7680
	50	40.9400	33.0161	0x2	1	0x3D	61	81.7664	10.2208	40.8832	654.1312
	60	34.1167	33.0161	0x2	1	0x09	9	68.3536	8.5442	34.1768	546.8288
	62	33.0161	33.0161	0x2	1	0x00	0	66.0322	8.2540	33.0161	528.2576
	62.5	32.7520	33.0161	0x1	0.5	0xFC	252	65.5164	8.1896	32.7582	524.1312
	75	27.2933	33.0161	0x1	0.5	0xA7	167	54.5540	6.8193	27.2770	436.4320
	85.3	24.0000	33.0161	0x1	0.5	0x74	116	47.9766	5.9971	23.9883	383.8128
	100	20.4700	33.0161	0x1	0.5	0x3D	61	40.8832	5.1104	20.4416	327.0656
	105	19.5000	33.0161	0x1	0.5	0x2E	46	38.9486	4.8686	19.4743	311.5888
	112.5	18.2000	33.0161	0x1	0.5	0x1A	26	36.3692	4.5462	18.1846	290.9536
	125	16.3760	33.0161	0x0	0.25	0xFC	252	32.7582	4.0948	16.3791	262.0656
	128	16.0000	33.0161	0x0	0.25	0xF0	240	31.9844	3.998	15.9922	255.8752
	150	13.6467	33.0161	0x0	0.25	0xA7	167	27.2770	3.4096	13.6385	218.2160
High g	50	40.9400	10.9465	0x3	2	0xDF	223	81.9278	10.2410	40.9639	655.4224
	60	34.1167	10.9465	0x3	2	0x8F	143	68.2446	8.5306	34.1223	545.9568
	62	33.0161	10.9465	0x3	2	0x82	130	66.0210	8.2526	33.0105	528.1680
	62.5	32.7520	10.9465	0x3	2	0x7F	127	65.5080	8.1885	32.7540	524.0640
	100	20.4700	10.9465	0x2	1	0xDF	223	40.9638	5.1205	20.4819	327.7104
	105	19.5000	10.9465	0x2	1	0xC8	200	38.9970	4.8746	19.4985	311.9760
	112.5	18.2000	10.9465	0x2	1	0xAA	170	36.4314	4.5539	18.2157	291.4512
	125	16.3760	10.9465	0x2	1	0x7F	127	32.7540	4.0943	16.3770	262.0320
	128	16.0000	10.9465	0x2	1	0x76	118	31.9844	3.9981	15.9922	255.8752
	150	13.6467	10.9465	0x2	1	0x3F	63	27.2808	3.4101	13.6404	218.2464
	187	10.9465	10.9465	0x2	1	0x00	0	21.8930	2.7366	10.9465	175.1440
	250	8.1880	10.9465	0x1	0.5	0x7F	127	16.3770	2.0471	8.1885	131.0160
	312.5	6.5504	10.9465	0x1	0.5	0x32	50	13.0844	1.6356	6.5422	104.6752
	375	5.4587	10.9465	0x0	0.25	0xFF	255	10.9252	1.3657	5.4626	87.4016
	500	4.0940	10.9465	0x0	0.25	0x7F	127	8.1884	1.0236	4.0942	65.5072

The table below shows some example user shift and multiplier values for typical PSI5 full scale ranges (+/- 480, 10-bit):

Note: This table includes some typical device ranges. Other ranges are possible with the user selected shift and multiplier values.

Device Type	Desired Range (g)	Desired Sensitivity (10-Bit, LSB/g)	NXP Trim (10-Bit, LSB/g)	User Sensitivity Shift Factor		User Multiplier Value		Actual Sensitivity (PSI5 10-Bit, LSB/g)	Actual Sensitivity (PSI5 16-Bit, LSB/g)
				U_SNS_SHIFT (HEX)	Shift Factor	U_SNS_MULT (HEX)	Multiplier Value (Dec)		
Medium g	15	32.0000	8.2540	0x3	2	0xF0	240	31.9844	2047.00
	20	24.0000	8.2540	0x3	2	0x74	116	23.9883	1535.25
	30	16.0000	8.2540	0x2	1	0xF0	240	15.9922	1023.50
	60	8.0000	8.2540	0x1	0.5	0xF0	240	7.9961	511.500
	120	4.0000	8.2540	0x0	0.25	0xF0	240	3.9980	255.875
High g	60	8.0000	2.7366	0x3	2	0x76	118	7.9961	511.749
	120	4.0000	2.7366	0x2	1	0x76	118	3.9980	255.874
	240	2.0000	2.7366	0x1	0.5	0x76	118	1.9990	127.937
	480	1.0000	2.7366	0x0	0.25	0x76	118	0.9995	63.9686

6.2.24 Channel 0 and Channel 1 User Configuration #3 Registers (CH0_CFG_U3, CH1_CFG_U3)

The Channel 0 and Channel 1 user configuration #3 registers are user programmable read/write registers which contain channel specific configuration information. The registers are included in the read/write array error detection.

Changes to these registers reset the DSP datapath. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in Section 5.20. Reads of the SNSDATA_x registers and Sensor Data requests should be prevented during this time.

These registers are readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$42	CH0_CFG_U3	UNSIGNEDDATA	DATATYPE0[1:0]		DATATYPE1[2:0]			MOVEAVG[1:0]	
$4A	CH1_CFG_U3	UNSIGNEDDATA	DATATYPE0[1:0]		DATATYPE1[2:0]			MOVEAVG[1:0]	
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.24.1 Unsigned Data Select Bit (UNSIGNEDDATA)

The unsigned data selection bit selects signed or unsigned data for the register and sensor data transmissions.

UNSIGNEDDATA	Register Values		DATATYPE Transmissions	
	CHx_SNSDATA0	CHx_SNSDATA1	Sensor Data (DSI, SPI)	Sensor Data (PSI5)
Channel Sensor Data				
0	Signed Data	Signed Data	Signed Data	Signed Data
1	Unsigned Data	Unsigned Data	Unsigned Data	
Temperature Sensor Data				
0	As specified in Section 6.7.2			0x1EA
1				

6.2.24.2 Channel Data Type 0 Selection Bits (CHxDATATYPE0)

The Channel Data Type 0 Selection Bits select the type of data to be included in the SNSDATA0_L and SNSDATA0_H registers for each channel.

CHxDATATYPE0[1]	CHxDATATYPE0[0]	Data Transmitted			
		Data Transmitted	Offset Cancelled?	Moving Average?	Interpolation?
0	0	CHx Sensor Data	Selected by OC_-FILT[1:0]	Selected by MOVEAVG[1:0]	Selected by MOVEAVG[1:0]
0	1	CHx Sensor Data	No		
1	0	Temperature Sensor Data (As specified in Section 6.7.2)			
1	1				

6.2.24.3 Channel Data Type 1 Selection Bits (CHxDATATYPE1)

The Channel Data Type 1 Selection Bits select the type of data to be included in the SNSDATA1_L and SNSDATA1_H registers for each channel.

CHxDATATYPE1[2]	CHxDATATYPE1[1]	CHxDATATYPE1[0]	Data Transmitted			
			Data Transmitted	Offset Cancelled?	Moving Average?	Interpolation?
0	0	0	CHx Sensor Data	Selected by OC_-FILT[1:0]	Selected by MOVEAVG[1:0]	No
0	0	1	CHx Sensor Data	No	Selected by MOVEAVG[1:0]	No
0	1	0	Temperature Sensor Data (As specified in Section 6.7.2)			
0	1	1				
1	0	0	CHx Sensor Data	Selected by OC_-FILT[1:0]	No	No
1	0	1	CHx Sensor Data	No	Selected by MOVEAVG[1:0]	No
1	1	0	Temperature Sensor Data (As specified in Section 6.7.2)			
1	1	1				

In PSI5 Mode, Temperature Sensor Data cannot be transmitted. If Temperature Sensor Data is selected with the CHxDATATYPE selection bits, the Sensor Defect Error will be transmitted in place of sensor data.

6.2.24.4 Signal Chain Moving Average Selection Bits (MOVEAVG[1:0])

The signal chain moving average selection bits determine the input sample period to be used for the signal chain moving average filter.

MOVEAVG[1]	MOVEAVG[0]	Typical Signal Sampling Period (Dependent on Oscillator) (μs)	Signal Chain Moving Average	Interpolation
0	0	Determined by LPF	Bypassed	Enabled
0	1	32	8 Sample Moving Average	Disabled
1	0	64	8 Sample Moving Average	Disabled
1	1	128	8 Sample Moving Average	Disabled

6.2.25 Channel 0 and Channel 1 User Configuration #4 Registers (CH0_CFG_U4, CH1_CFG_U4)

The Channel 0 and Channel 1 user configuration #4 registers are user programmable read/write registers which contain channel specific configuration information. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$43	CH0_CFG_U4	RESERVED	INVERT	OC_FILT[1:0]		PCM	ARM_CFG[2:0]		
$4B	CH1_CFG_U4	RESERVED	INVERT	OC_FILT[1:0]		PCM	ARM_CFG[2:0]		
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.25.1 Signal Inversion Bit (INVERT)

The signal inversion bit provides the option to invert the polarity of the sensor signals as shown below.

INVERT	Acceleration Sensor Data	Fixed Pattern Self-Test	Digital Self-Test	Analog Self-Test		Temperature
0	As shown in Section 3.	As specified in Section 6.2.26.1	Digital Self-Test Activation results in the values specified in Section 5.8.	Positive Self-Test:	Delta from Offset as specified in Section 5.8	As specified in Section 6.7.2
				Negative Self-Test:	Delta from Offset inverted from the specified values in Section 5.8 (Negative Values)	
1	Inverted polarity from that shown in Section 3		Digital Self-Test Activation results in the 2s complement of the values specified in Section 5.8.	Positive Self-Test:	Delta from Offset inverted from the specified values in Section 5.8 (Negative Values)	
				Negative Self-Test:	Delta from Offset as specified in Section 5.8	

6.2.25.2 Offset Cancellation Filter Selection Bits (OC_FILT[1:0])

The offset cancellation filter selection bits provides the option to bypass the offset cancellation filter and the rate limiting for the associated channel. Reference Section 6.6.4.6 for details regarding offset cancellation.

OC_FILT[1]	OC_FILT[0]	Offset Cancellation IIR Filter	Offset Cancellation Rate Limiting
0	0	Enabled	Enabled
0	1	Enabled	Bypassed
1	0	Bypassed	Bypassed
1	1	Bypassed	Bypassed

6.2.25.3 Arming Pin Configuration Bits (ARM_CFG[2:0]) and PCM Range Selection Bit (PCM)

The ARM Configuration Bits (ARM_CFG[2:0]) select the mode of operation for the Arming pins.

ARM_CFG[2]	ARM_CFG[1]	ARM_CFG[0]	PCM	Operating Mode	Output Type	Reference
0	0	0	x	Arm/PCM Output Disabled	Hi Impedance	
0	0	1	0	Arm/PCM Output Disabled	Driven Low	
0	0	1	1	PCM Output	Digital Output	Section 6.8
0	1	0	x	Moving Average Mode	Open Drain, Active High with Pull-down Current	Section 6.9.1
0	1	1	x	Moving Average Mode	Open Drain, Active Low with Pull-up Current	Section 6.9.1
1	0	0	x	Count Mode	Open Drain, Active High with Pull-down Current	Section 6.9.2
1	0	1	x	Count Mode	Open Drain, Active Low with Pull-up Current	Section 6.9.2
1	1	0	x	Unfiltered Mode	Open Drain, Active High with Pull-down Current	Section 6.9.3
1	1	1	x	Unfiltered Mode	Open Drain, Active Low with Pull-up Current	Section 6.9.3

Note: The arming function is reset on a change to the ARM_CFG bits. This includes the downsampling state and all history registers.

When the PCM output is enabled, a Pulse Code Modulated signal proportional to the data selected by the DATATYPE0 selection bits is output on the ARM/PCM pin. Reference Section 6.8 for more information regarding the PCM output.

6.2.26 Channel 0 and Channel 1 User Configuration #5 Register (CH0_CFG_U5, CH1_CFG_U5)

The Channel 0 and Channel 1 user configuration #5 registers are user programmable read/write registers which contain channel specific configuration information. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$44	CH0_CFG_U5	ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
$4C	CH1_CFG_U5	ST_CTRL[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.26.1 Self Test Control Bits (ST_CTRL[3:0])

The self test control bits select one of the various analog and digital self test features of the device as shown in the table below.

The self test control bits are writable in DSI3 Command and Response Mode.

The self test control bits are writable in SPI Mode.

The self test control bits are writable in I^2C Mode.

The self test control bits are writable in PSI5 Programming Mode.

ST_CTRL[3]	ST_CTRL[2]	ST_CTRL[1]	ST_CTRL[0]	Function	16-Bit SNSDATAx Register Value Signed	ST_INCMPLT	ST_ACTIVE
0	0	0	0	DSP writes to the SNS_DATAx_X registers as configured in the ChxDATATYPEx registers.	Sensor Data	No Effect	Clear when Active
0	0	0	1			Clear on Activation	Set When Active
0	0	1	0			Clear on Activation	Set When Active
0	0	1	1			Clear on Activation	Set When Active
0	1	0	0	DSP write to registers inhibited.	0x0000	Clear on Activation	Set When Active
0	1	0	1		0xAAAA	Clear on Activation	Set When Active
0	1	1	0		0x5555	Clear on Activation	Set When Active
0	1	1	1		0xFFFF	Clear on Activation	Set When Active
1	0	0	0	RESERVED	RESERVED	Clear on Activation	Set When Active
1	0	0	1			Clear on Activation	Set When Active
1	0	1	0	Positive Analog Self Test - High	Sensor Data	Clear on Activation	Set When Active
1	0	1	1	Negative Analog Self Test - High		Clear on Activation	Set When Active
1	1	0	0	Digital Self Test: DSP write to registers inhibited Values scale with gain changes	Reference Section 5.8	Clear on Activation	Set When Active
1	1	0	1			Clear on Activation	Set When Active
1	1	1	0			Clear on Activation	Set When Active
1	1	1	1			Clear on Activation	Set When Active

6.2.27 Channel 0 and Channel 1 Arming Configuration Registers (CH0_ARM_CFG, CH1_ARM_CFG)

The arming configuration registers contain configuration information for the arming function. The values in these registers are only relevant if the arming function is operating in moving average mode, or count mode.

Note: The arming function is reset on a change to the CHx_ARM_CFG bits. This includes the downsampling state and all history registers.

These registers can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 6.2.5. The registers are included in the read/write array error detection.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$45	CH0_ARM_CFG	ARM_DS[1:0]		ARM_PS[1:0]		ARM_WS_N[1:0]		ARM_WS_P[1:0]	
$4D	CH1_ARM_CFG	ARM_DS[1:0]		ARM_PS[1:0]		ARM_WS_N[1:0]		ARM_WS_P[1:0]	
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.27.1 Arming Function Down Sampling Selection Bits (ARM_DS[1:0])

The arming function down sampling selection bits select the down sampling rate for the arming function. Reference Section 6.9.4.

ARM_DS[1]	ARM_DS[0]	Down Sampling
0	0	Provide every Sensor Data Request sample to the arming function for the relevant channel
0	1	Provide every other Sensor Data Request sample to the arming function for the relevant channel
1	0	Provide every 4th Sensor Data Request sample to the arming function for the relevant channel
1	1	Provide every 8th Sensor Data Request sample to the arming function for the relevant channel

6.2.27.2 Arming Pulse Stretch (ARM_PS[1:0])

The ARM_PS[1:0] bits set the programmable pulse stretch time for the arming outputs. Refer to Section 6.9 for more details regarding the arming function. Pulse stretch times are derived from the internal oscillator, so the tolerance on this oscillator applies.

ARM_PS[1]	ARM_PS[0]	Pulse Stretch Time (Typical Oscillator)
0	0	0 ms
0	1	128.000 ms - 130.048 ms
1	0	512.000ms - 514.048 ms
1	1	2048.000ms - 2050.048 ms

6.2.27.3 Arming Window Size (ARM_WS_N[1:0], A_WS_P[1:0])

The ARM_WS_N[1:0] and ARM_WS_P[1:0] bits have a different function depending on the state of the ARM_CFG bits in the CHx_CFG_U4 registers. Refer to Section 6.9 for more details regarding the arming function. If the arming function is set to moving average mode, the ARM_WS bits set the number of sensor samples used for the arming function moving average. The number of samples is set independently for each channel and polarity. If the arming function is set to count mode, the ARM_WS bits set the sample count limit for the arming function. The sample count limit is set independently for each channel.

Positive Arming Window Size Definitions (Moving Average Mode)		
ARM_WS_P[1]	ARM_WS_P[0]	Positive Window Size
0	0	2
0	1	4
1	0	8
1	1	16

Negative Arming Window Size Definitions (Moving Average Mode)		
ARM_WS_N[1]	ARM_WS_N[0]	Negative Window Size
0	0	2
0	1	4
1	0	8
1	1	16

Arming Count Limit Definitions (Count Mode)				
ARM_WS_N[1]	ARM_WS_N[0]	ARM_WS_P[1]	ARM_WS_P[0]	Sample Count Limit
Don't Care	Don't Care	0	0	1
Don't Care	Don't Care	0	1	3
Don't Care	Don't Care	1	0	7
Don't Care	Don't Care	1	1	15

6.2.28 Arming Threshold Registers (CHx_ARM_T_P, CHx_ARM_T_N)

The arming threshold registers contain the positive and negative thresholds to be used by the arming function for each channel. Refer to Section 6.9 for more details regarding the arming function.

These registers can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 6.2.5. The registers are included in the read/write array error detection.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$46	CH0_ARM_T_P	ARM_T_P[7:0]							
$47	CH0_ARM_T_N	ARM_T_N[7:0]							
$4E	CH1_ARM_T_P	ARM_T_P[7:0]							
$4F	CH1_ARM_T_N	ARM_T_N[7:0]							
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

The values programmed into the threshold registers are the threshold values used for the arming function as described in Section 6.9. The threshold registers hold independent unsigned 8-bit values for each channel and polarity.

For Part Numbers beginning with FXLS0 through FXLS4, each threshold increment is equivalent to 1 output LSB, 10-bit. The table below shows examples of some threshold register values and the corresponding threshold.

Device Range (g)	Sensitivity (12-Bit, LSB/g)	Arming Threshold Resolution (10-Bit, LSB/g)	Range of Arm Threshold (g)	Programmed Thresholds			
				Positive (Decimal)	Negative (Decimal)	Positive Threshold (g)	Negative Threshold (g)
125	16.3760	4.0940	62.2863	40	12	10	-3
62	33.0161	8.2540	30.8940	123	24	15	-3
50	40.9400	10.2350	24.9145	245	61	24	-6
25	81.8800	20.4700	12.4573	245	61	12	-3
16	127.9375	31.9844	7.9726	223	95	7	-3

For Part Numbers beginning with FXLS5 through FXLS9, each threshold increment is equivalent to 2 output LSB, 10-bit. The table below shows examples of some threshold register values and the corresponding threshold.

Device Range (g)	Sensitivity (12-Bit, LSB/g)	Arming Threshold Resolution (10-Bit, LSB/g)	Range of Arm Threshold (g)	Programmed Thresholds			
				Positive (Decimal)	Negative (Decimal)	Positive Threshold (g)	Negative Threshold (g)
125	16.3760	2.047	124.57	40	12	19.5	-5.86
62	33.0161	4.127	61.788	123	24	29.8	-5.82
50	40.9400	5.118	49.824	245	61	47.9	-11.91
25	81.8800	10.235	24.915	245	61	23.9	-5.96
16	127.9375	15.992	15.945	223	95	13.9	-5.94

If either the positive or negative threshold for one channel is programmed to 0x00, comparisons are disabled for only that polarity. The arming function still operates for the opposite polarity. If both the positive and negative arming thresholds for one channel are programmed to 0x00, the arming function for the associated channel is disabled and the output pin is set to high impedance, regardless of the value of the ARM_CFG bits in the CHx_CFG_U4 register.

6.2.29 Channel Specific Status Register (CH0_STAT, CH1_STAT)

The channel specific status registers are read only registers which contain sensor data specific status information.

These registers are readable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$60	CH0_STAT	SIGNALCLIP	OCPHASE[2:0]			ST_INCMPLT	ST_ACTIVE	OFFSET_ERR	ST_ERROR
$70	CH1_STAT	SIGNALCLIP	OCPHASE[2:0]			ST_INCMPLT	ST_ACTIVE	OFFSET_ERR	ST_ERROR
Reset Value		0	0	0	0	1	0	0	0

6.2.29.1 Signal Clipped Status Bit (SIGNALCLIP)

The signal clipped status bit is set if the output of the sinc filter reaches either the maximum or minimum value. The SIGNAL-CLIP bit is cleared on a read of the CHx_STAT register through any communication interface or on a data transmission that includes the error in the status field.

6.2.29.2 Offset Cancellation Phase Status (OCPHASE[2:0])

The offset cancellation phase status bits indicate the current phase of the offset cancellation filter as described in Section 6.6.4.6.

OCPHASE[2:0]	Offset Cancellation Startup Phase	Offset Low Pass Filter Frequency (Hz)
000	Phase 0	163.8
001	Phase 1	40.96
010	Phase 2	10.24
011	Phase 3	2.560
100	Phase 4	0.640
101	Phase 5	0.160
110	Phase 6 / Normal Mode	0.04
111	Not Applicable	

6.2.29.3 Self Test Incomplete (ST_INCMPLT)

The self test incomplete bit is set after a device reset and is cleared when one of the analog or digital self tests modes is enabled in the ST_CTRL register (ST_CTRL[3] = ‘1’ | ST_CTRL[2] = ‘1’ | | ST_CTRL[1] = ‘1’ | | ST_CTRL[0] = ‘1’) or the PSI5 internal self test procedure has started.

ST_INCMPLT	Condition
0	An Analog or Digital Self Test has been activated since the last reset
1	No Analog or Digital Self Test has not been activated since the last reset AND the PSI5 internal self test procedure has not completed

6.2.29.4 Self Test Active Flag (ST_ACTIVE)

The self test active bit is set if any self test mode is currently active, including the PSI5 internal self test or a self test voltage is applied to the transducer. The self test active bit is cleared when no self test mode is active and no self test voltage is applied to the transducer.

ST_ACTIVE = ST_CTRL[3] | ST_CTRL[2] |ST_CTRL[1] | ST_CTRL[0] | (self test voltage applied to transducer)

6.2.29.5 Offset Error Flag (OFFSET_ERR)

The offset error flag is set if the sensor signal reaches the offset limit specified in Section 5.7. The OFFSET_ERR bit is cleared on a read of the CHx_STAT register through any communication interface or on a data transmission that includes the error in the status field.

OFFSET_ERR	Error Condition
0	No error detected
1	Offset error detected

6.2.29.6 Self Test Error Flag (ST_ERROR)

The self test error flag is set if the PSI5 startup self test fails as described in Section 6.6.2.3. This bit can only be cleared by a device reset.

6.2.30 Device Status Copy Register (DEVSTAT_COPY)

The device status copy register is a read-only register which contains a copy of the device status information contained in the DEVSTAT register. Reference Section 6.2.2 for details regarding the DEVSTAT register contents.

This register is readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode. A read of the DEVSTAT_COPY register has the same effect as a read of the DEVSTAT register.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$61	DEVSTAT_COPY	CH0_ERR	CH1_ERR	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT

6.2.31 Sensor Data #0 Registers (CHx_SNSDATA0_L, CHx_SNSDATA0_H)

The sensor data #0 registers are read only registers which contain the 16-bit sensor data. The data type for the sensor data #0 registers is selected by the DATATYPE0 bits in the CHx_CFG_U3 register. Reference Section 6.2.24.2. Reference Section 6.6.4.9 for details regarding the 16-bit sensor data.

These registers are readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode. In I^2C mode the SNSDATA0_H register value is latched on a read of the SNSDATA0_L register value until the SNSDATA0_H register is read. To avoid data mismatch, it is required that the user always read the registers in sequence, SNSDATA0_L register first, followed by the SNSDATA0_H register.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$62	CH0_SNSDATA0_L	SNSDATA0[7:0]							
$63	CH0_SNSDATA0_H	SNSDATA0[15:8]							
$72	CH1_SNSDATA0_L	SNSDATA0[7:0]							
$73	CH1_SNSDATA0_H	SNSDATA0[15:8]							
Reset Value		0	0	0	0	0	0	0	0

6.2.32 Sensor Data #1 Registers (CHx_SNSDATA1_L, CHx_SNSDATA1_H)

The sensor data #1 registers are read only registers which contain the 16-bit sensor data. The data type for the sensor data #1 registers is selected by the DATATYPE1 bits in the CHx_CFG_U3 register. Reference Section 6.2.24.3. Reference Section 6.6.4.9 for details regarding the 16-bit sensor data.

These registers are readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode. In I^2C mode the SNSDATA1_H register value is latched on a read of the SNSDATA1_L register value until the SNSDATA1_H register is read. To avoid data mismatch, it is required that the user always read the registers in sequence, SNSDATA1_L register first, followed by the SNSDATA1_H register.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$64	CH0_SNSDATA1_L	SNSDATA1[7:0]							
$65	CH0_SNSDATA1_H	SNSDATA1[15:8]							
$74	CH1_SNSDATA1_L	SNSDATA1[7:0]							
$75	CH1_SNSDATA1_H	SNSDATA1[15:8]							
Reset Value		0	0	0	0	0	0	0	0

6.2.33 Channel Specific Factory Configuration Register (CHx_CFG_F)

The channel specific configuration registers are factory programmable OTP registers which contain channel specific configuration information. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for this register.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$A0	CH0_CFG_F	DEV_RANGE[3:0]				RESERVED	RESERVED	AXIS[1:0]	
$B0	CH1_CFG_F	DEV_RANGE[3:0]				RESERVED	RESERVED	AXIS[1:0]	

6.2.33.1 Range Indication Bits (RANGE[3:0])

The range indication bits indicate the full scale range of the channel as shown below.

RANGE[3]	RANGE[2]	RANGE[1]	RANGE[0]	Acceleration Range
0	0	0	0	RESERVED
0	0	0	1	RESERVED
0	0	1	0	Medium
0	0	1	1	RESERVED
0	1	0	0	High
0	1	0	1	RESERVED
0	1	1	0	RESERVED
0	1	1	1	RESERVED
1	0	0	0	RESERVED
1	0	0	1	RESERVED
1	0	1	0	RESERVED
1	0	1	1	RESERVED
1	1	0	0	RESERVED
1	1	0	1	RESERVED
1	1	1	0	RESERVED
1	1	1	1	RESERVED

6.2.33.2 Axis Indication Bits (AXIS[1:0])

The axis indication bits indicate the axes of sensitivity for the channel as shown below.

AXIS[1]	AXIS[0]	Axis of Sensitivity
0	0	X
0	1	Y
1	0	Z
1	1	RESERVED for -X

6.2.34 Self Test Deflection Storage Registers

The self test deflection registers are factory programmable OTP registers which contain the nominal self test values for the various self tests at 25C. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for these registers.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$A2	RESERVED	RESERVED							
$A3	RESERVED	RESERVED							
$A4	CH0_STH_P_L	CH0_STH_P[7:0]							
$A5	CH0_STH_P_H	CH0_STH_P[15:8]							
$A6	RESERVED	RESERVED							
$A7	RESERVED	RESERVED							
$A8	CH0_STH_N_L	CH0_STH_N[7:0]							
$A9	CH0_STH_N_H	CH0_STH_N[15:8]							
$B2	RESERVED	RESERVED							
$B3	RESERVED	RESERVED							
$B4	CH1_STH_P_L	CH1_STH_P[7:0]							
$B5	CH1_STH_P_H	CH1_STH_P[15:8]							
$B6	RESERVED	RESERVED							
$B7	RESERVED	RESERVED							
$B8	CH1_STH_N_L	CH1_STH_N[7:0]							
$B9	CH1_STH_N_H	CH1_STH_N[15:8]							

The self test values are positive and negative deflection values, measured at the factory, and factory programmed for each device. The stored value is equal to one half of the absolute value of the difference between the factory measured Chx-_SNSDATA0 register value with the analog self test active and the factory measured CHx_SNSDATA0 register value for off-set at nominal temperature (Data is aligned to the 12-bit sensor data). Both the self test and offset values are measured with the user scaling set to 1: U_SNS_SHIFT[1:0] = 0x2 and U_SNS_MULT[7:0] = 0x00.

$$CH0\_STH\_P = 0.5 * [\ CH0\_SNSDATA0_{ST\_CTRL=0xA} - CH0\_SNSDATA0_{ST\_CTRL=0x0}\ ]$$

$$CH0\_STH\_N = 0.5 * [\ CH0\_SNSDATA0_{ST\_CTRL=0x0} - CH0\_SNSDATA0_{ST\_CTRL=0xB}\ ]$$

$$CH1\_STH\_P = 0.5 * [\ CH1\_SNSDATA0_{ST\_CTRL=0xA} - CH1\_SNSDATA0_{ST\_CTRL=0x0}\ ]$$

$$CH1\_STH\_N = 0.5 * [\ CH1\_SNSDATA0_{ST\_CTRL=0x0} - CH1\_SNSDATA0_{ST\_CTRL=0xB}\ ]$$

The self test value is controlled by the user via the ST_CTRL[3:0] bits in the CHx_CFG_U5 registers as described in Section 6.2.26.1.

When self test is activated, the sensor data can be compared to the values in the appropriate registers. The difference from the measured deflection value, and the nominal deflection value stored in the register shall not fall outside the self test accuracy limits specified in Section 5.8 (ΔST_{ACC}). Reference Section 6.6.2 for more details on calculating the self test limits.

6.2.35 IC Type Register

The IC type register is a factory programmable OTP register which contains the IC type as defined below. This register is included in the factory programmed OTP array error detection.

This register is readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for this register.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$C0	ICTYPEID	0	0	0	0	0	0	1	1

6.2.36 IC Revision Register

The IC revision register is a factory programmable OTP register which contains the IC revision. The upper nibble contains the main IC revision. The lower nibble contains the sub IC revision. This register is included in the factory programmed OTP array error detection.

This register is readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for this register.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$C1	ICREVID	ICREVID[7:0]							

6.2.37 IC Manufacturer Identification Register

The IC manufacturer identification register is a factory programmable OTP register which identifies NXP as the IC manufacturer. This register is included in the factory programmed OTP array error detection.

This register is readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for this register.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$C2	ICMFGID	0	0	0	0	0	0	1	0

6.2.38 Part Number Register

The part number registers are factory programmed OTP registers which include the numeric portion of the device part number. These registers are included in the factory programmed OTP array error detection.

These register are readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for these registers.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$C4	PN0	PN0[7:0]							
$C5	PN1	PN1[7:0]							

PN1[7:4]	Protocol Type	Offset Cancellation Rate Limiting	Arming Function Threshold Resolution
0	User Selectable	1 LSB / 8s, 10-Bit	1 LSB, 10-Bit
1	SPI32		
2	DSI3		
3	PSI5		
4	I2C		
5	User Selectable	1 LSB / 4s, 10-Bit	2 LSB, 10-Bit
6	SPI32		
7	DSI3		
8	PSI5		
9	I2C		
10-15	RESERVED	RESERVED	RESERVED

PN1[3:0]	Channel 0 Axis	Channel 1 Axis
0	RESERVED	
1	RESERVED	
2	RESERVED	
3	X	Y
4	X	Z
5	RESERVED	
6	RESERVED	
7	RESERVED	
8 - 15	RESERVED	
PN0[7:4]	**Channel 0 Range**	
0	RESERVED	
1	RESERVED	
2	Medium g, X-Axis	
	Medium g, Z-Axis Bumper	
3	High g, X-Axis	
	High g, Z-Axis Bumper	
4	RESERVED	
5	Medium g, Z-Axis Geometric Stop	
6	High , Z-Axis Geometric Stop	
7 - 15	RESERVED	
PN0[3:0]	**Channel 1 Range**	
0	RESERVED	
1	RESERVED	
2	Medium g, X-Axis	
	Medium g, Z-Axis Bumper	
3	High g, X-Axis	
	High g, Z-Axis Bumper	
4	RESERVED	
5	Medium g, Z-Axis Geometric Stop	
6	High , Z-Axis Geometric Stop	
7 - 15	RESERVED	

6.2.39 Device Serial Number Registers

The serial number registers are factory programmed OTP registers which include the unique serial number of the device. A serial number is assigned to the lowest 14 bits. Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. A lot number is programmed to the next 22 bits. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 14-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned. A test configuration revision counter is programmed into the upper 4 bits. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for these registers.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$C6	SN0	SN[7:0]							
$C7	SN1	SN[15:8]							
$C8	SN2	SN[23:16]							
$C9	SN3	SN[31:24]							
$CA	SN4	SN[39:36] = DEVICE_REV[3:0]				SN[35:32]			

The table below shows and example serial number decoding:

<table>
<tr><th>Serial Number</th><th colspan="20">Full Serial Number</th></tr>
<tr><td>Stored Data Format</td><td colspan="4">SN4</td><td colspan="4">SN3</td><td colspan="4">SN2</td><td colspan="4">SN1</td><td colspan="4">SN0</td></tr>
<tr><td>Serial Number Mapping</td><td colspan="2">Test ID</td><td colspan="11">Lot Number</td><td colspan="7">Serial Number within a lot</td></tr>
<tr><td>Example SN (Hex)</td><td colspan="2">1</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">5</td><td colspan="2">2</td><td colspan="2">0</td><td colspan="2">0</td><td colspan="2">5</td><td colspan="2">0</td></tr>
<tr><td>Example SN (Binary)</td><td>00</td><td>01</td><td>00</td><td>00</td><td>00</td><td>00</td><td>00</td><td>00</td><td>01</td><td>01</td><td>00</td><td>10</td><td>00</td><td>00</td><td>00</td><td>00</td><td>01</td><td>01</td><td>00</td><td>00</td></tr>
<tr><td>Device Rev</td><td colspan="20">4’b0000 = 0x0 = 0d: Revision 1 Transducer, Original Programming
4’b0001 = 0x1 = 1d: Revision 1 Transducer, Programming Change for Arming Data Alignment
4’b0010 = 0x2 = 2d: Geometric Stop Transducer, Programming Change for Arming Data Alignment</td></tr>
<tr><td>Example Lot Number</td><td colspan="20">4’b00 00 00 00 00 00 01 01 00 10 00 = 0x000148 = 328d</td></tr>
<tr><td>Example Serial Number</td><td colspan="20">14’b00 00 00 01 01 00 00 = 0x0050 = 80d</td></tr>
</table>

6.2.40 ASIC Wafer ID Registers

The ASIC Wafer ID Registers are factory programmed OTP registers which include the wafer number, wafer X and Y coordinates and the wafer lot number for the device ASIC. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for these registers.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$CB	ASICWFR#	ASICWFR#[7:0]							
$CC	ASICWFR_X	ASICWFR_X[7:0]							
$CD	ASICWFR_Y	ASICWFR_Y[7:0]							
$D0	ASICWLOT_L	ASICWLOT[7:0]							
$D1	ASICWLOT_H	ASICWLOT[15:8]							

6.2.41 Transducer Wafer ID Registers

The Transducer Wafer ID Registers are factory programmed OTP registers which include the wafer number, wafer X and Y coordinates and the wafer lot number for the device transducers. The upper 3 bits of the TRNSWFR# register include a transducer and assembly revision counter. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for these registers.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$D2	TRNS1WFR_X	TRNS1WFR_X[7:0]							
$D3	TRNS1WFR_Y	TRNS1WFR_Y[7:0]							
$D4	TRNS1LOT_L	TRNS1LOT[7:0]							
$D5	TRNS1LOT_H	TRNS1LOT[15:8]							
$DA	TRNS1WFR#	TRNS_ASSY_REV[2:0]			TRNS1WFR#[4:0]				

6.2.42 User Data Registers (USERDATA_0 - USERDATA_E)

User Data registers are user programmable OTP registers which contains user specific information. These registers are included in the user programmed OTP array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I^{2}C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for these registers.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$E0	USERDATA_0	USERDATA_0[7:0]							
$E1	USERDATA_1	USERDATA_1[7:0]							
$E2	USERDATA_2	USERDATA_2[7:0]							
$E3	USERDATA_3	USERDATA_3[7:0]							
$E4	USERDATA_4	USERDATA_4[7:0]							
$E5	USERDATA_5	USERDATA_5[7:0]							
$E6	USERDATA_6	USERDATA_6[7:0]							
$E7	USERDATA_7	USERDATA_7[7:0]							
$E8	USERDATA_8	USERDATA_8[7:0]							
$E9	USERDATA_9	USERDATA_9[7:0]							
$EA	USERDATA_A	USERDATA_A[7:0]							
$EB	USERDATA_B	USERDATA_B[7:0]							
$EC	USERDATA_C	USERDATA_C[7:0]							
$ED	USERDATA_D	USERDATA_D[7:0]							
$EE	USERDATA_E	USERDATA_E[7:0]							
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.42.1 PSI5 Initialization Phase 2 Data Transmissions of User Data

In PSI5 Mode, the values of the User Data registers are transmitted in Initialization Phase 2 as shown in the table below. Reference Section 8.4.2.1 for details on the PSI5 Initialization Phase 2 Transmissions.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$E0	USERDATA_0	Channel 1 F1: D1				Channel 0 F1: D1			
$E1	USERDATA_1	Channel 0 F3: D5				Channel 0 F3: D4			
$E2	USERDATA_2	Channel 0 F4: D7				Channel 0 F4: D6			
$E3	USERDATA_3	Channel 0 F5: D9				Channel 0 F5: D8			
$E4	USERDATA_4	Channel 0 F6: D11				Channel 0 F6: D10			
$E5	USERDATA_5	Channel 0 F7: D13				Channel 0 F7: D12			
$E6	USERDATA_6	Channel 0 F9: D32				Channel 0 F7: D14			
$E7	USERDATA_7	Channel 0 F8: D16 = Channel 1 F8: D16				Channel 0 F8: D15 = Channel 1 F8: D15			
$E8	USERDATA_8	Channel 0 F8: D18 = Channel 1 F8: D18				Channel 0 F8: D17 = Channel 1 F8: D17			
$E9	USERDATA_9	Channel 1 F3: D5				Channel 1 F3: D4			
$EA	USERDATA_A	Channel 1 F4: D7				Channel 1 F4: D6			
$EB	USERDATA_B	Channel 1 F5: D9				Channel 1 F5: D8			
$EC	USERDATA_C	Channel 1 F6: D11				Channel 1 F6: D10			
$ED	USERDATA_D	Channel 1 F7: D13				Channel 1 F7: D12			
$EE	USERDATA_E	Channel 1 F9: D32				Channel 1 F7: D14			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.43 User Data Registers (USERDATA_10 - USERDATA_1E)

User Data registers are user programmable OTP registers which contains user specific information. These registers are included in the user programmed OTP array error detection.

These registers are readable and writable in DSI3 mode, SPI mode, I^2C mode or PSI5 Programming Mode when ENDINIT is not set. Reference Section 6.2.9 for details on the register read process for these registers.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$F0	USERDATA_10	USERDATA_10[7:0]							
$F1	USERDATA_11	USERDATA_11[7:0]							
$F2	USERDATA_12	USERDATA_12[7:0]							
$F3	USERDATA_13	USERDATA_13[7:0]							
$F4	USERDATA_14	USERDATA_14[7:0]							
$F5	USERDATA_15	USERDATA_15[7:0]							
$F6	USERDATA_16	USERDATA_16[7:0]							
$F7	USERDATA_17	USERDATA_17[7:0]							
$F8	USERDATA_18	USERDATA_18[7:0]							
$F9	USERDATA_19	USERDATA_19[7:0]							
$FA	USERDATA_1A	USERDATA_1A[7:0]							
$FB	USERDATA_1B	USERDATA_1B[7:0]							
$FC	USERDATA_1C	USERDATA_1C[7:0]							
$FD	USERDATA_1D	USERDATA_1D[7:0]							
$FE	USERDATA_1E	USERDATA_1E[7:0]							
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

6.2.44 Lock and CRC Registers

The lock and CRC Registers are automatically programmed OTP registers which include the lock bit, the block identifier and the block OTP array CRC use for error detection.

These registers are automatically programmed when the corresponding data array is programmed to OTP using the Write OTP Enable register as documented in Section 6.2.6.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$5F	CRC_UF2	LOCK_UF2	0	0	0	CRC_UF2[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0
$AF	CRC_F_A	LOCK_F_A	REGA_BLOCKID[2:0]			CRC_F_A[3:0]			
Reset Value		1	0	0	1	Varies			
$BF	CRC_F_B	LOCK_F_B	REGB_BLOCKID[2:0]			CRC_F_B[3:0]			
Reset Value		1	0	1	0	Varies			
$CF	CRC_F_C	LOCK_F_C	REGC_BLOCKID[2:0]			CRC_F_C[3:0]			
Reset Value		1	0	1	1	Varies			
$DF	CRC_F_D	LOCK_F_D	REGD_BLOCKID[2:0]			CRC_F_D[3:0]			
Reset Value		1	1	0	0	Varies			
$EF	CRC_F_E	LOCK_F_E	REGE_BLOCKID[2:0]			CRC_F_E[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0
$FF	CRC_F_F	LOCK_F_F	REGF_BLOCKID[2:0]			CRC_F_F[3:0]			
Unprogrammed OTP Value		0	0	0	0	0	0	0	0

The table below shows the state of the lock bits, the block identifiers and the CRC for each register block before and after programming.

Register Block Address	Lock Bit bit[7]		Block Identifier bits[6:4]		CRC bits[3:0]	
	Before Programming	After Programming	Before Programming	After Programming	Before Programming	After Programming
UF2	0	1	000	000	0000	Varies
$Ax	0	1	N/A	001	N/A	Varies
$Bx	0	1	N/A	010	N/A	Varies
$Cx	0	1	N/A	011	N/A	Varies
$Dx	0	1	N/A	100	N/A	Varies
$Ex	0	1	000	101	0000	Varies
$Fx	0	1	000	110	0000	Varies

6.2.45 Reserved Registers

A register read command to a reserved register or a register with reserved bits will result in a valid response. The data for reserved bits may be ‘0’ or ‘1’.

A register write command to a reserved register or a register with reserved bits will execute and result in a valid response. The data for the reserved bits may be ‘0’ or ‘1’. A write to the reserved bits must always be ‘0’ for normal device operation and performance.

6.2.46 Invalid Register Addresses

A register read command to a register address outside of the addresses listed in Section 6.1 will result in a valid response. The data for the registers will be ‘0x00’.

A register write command to a register address outside of the addresses listed in Section 6.1 will not execute, but will result in a valid response. The data for the registers will be ‘0x00’.

A register write command to a read only register will not execute, but will result in a valid response. The data for the registers will be the current contents of the register.

6.3 OTP and Read/Write Register Array CRC Verification

6.3.1 NXP OTP Registers

The following registers are internal OTP registers. These registers are verified by the OTP ECC as well as an independent 4-bit CRC for each 16 byte block.

Memory Type Codes	
F	User Readable Register with OTP

6.3.2 User OTP Only Registers

The following registers are user OTP registers. These registers are verified by the OTP ECC as well as an independent 4-bit CRC for each 16 byte block. The CRC verification uses a generator polynomial of $g(x) = X^4+X^3+1$, with a seed value = ‘0000’. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

Memory Type Codes	
UF0	One Time User Programmable OTP Region 0
UF1	One Time User Programmable OTP Region 1

6.3.3 OTP Modifiable Registers

The following registers are user read/write registers as well as OTP registers with writable mirror registers. The OTP registers are verified by the OTP ECC as well as an independent 4 bit CRC stored in the CRC_UF2 register.

The values read from OTP can be over-written while ENDINIT is not set. Once ENDINIT is set, the writable registers (all registers in the R/W and UF2 regions with the exception of the DEVLOCK_WR register) are verified by an additional continuous 4-bit CRC that is calculated on the entire array. The CRC verification uses a generator polynomial of $g(x) = X^4+X^3+1$, with a seed value = ‘0000’. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

Registers verified by the OTP CRC:

Memory Type Codes	
UF2	One Time User Programmable OTP Region 3 with modifiable mirror registers

Registers verified by the ENDINIT calculated CRC:

Memory Type Codes	
UF2	One Time User Programmable OTP Region 3 with modifiable mirror registers
R/W	User Writable Register, with the exception of the DEVLOCK_WR register

6.4 Voltage Regulators

The device derives its internal supply voltage from the V_{CC}/BUS_I and V_{SS} pins. The internal regulators are supplied by a buffer regulator (V_{BUF}) to provide immunity from EMC and supply dropouts on BUS_I. An external filter capacitor is required for V_{BUF}, as shown in Section 1.

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the internal voltages have increased above the under-voltage detection thresholds. The voltage monitor asserts internal reset when the external supply or internally regulated voltages fall below the under-voltage detection thresholds. A reference generator provides a reference voltage for the ΣΔ converter.

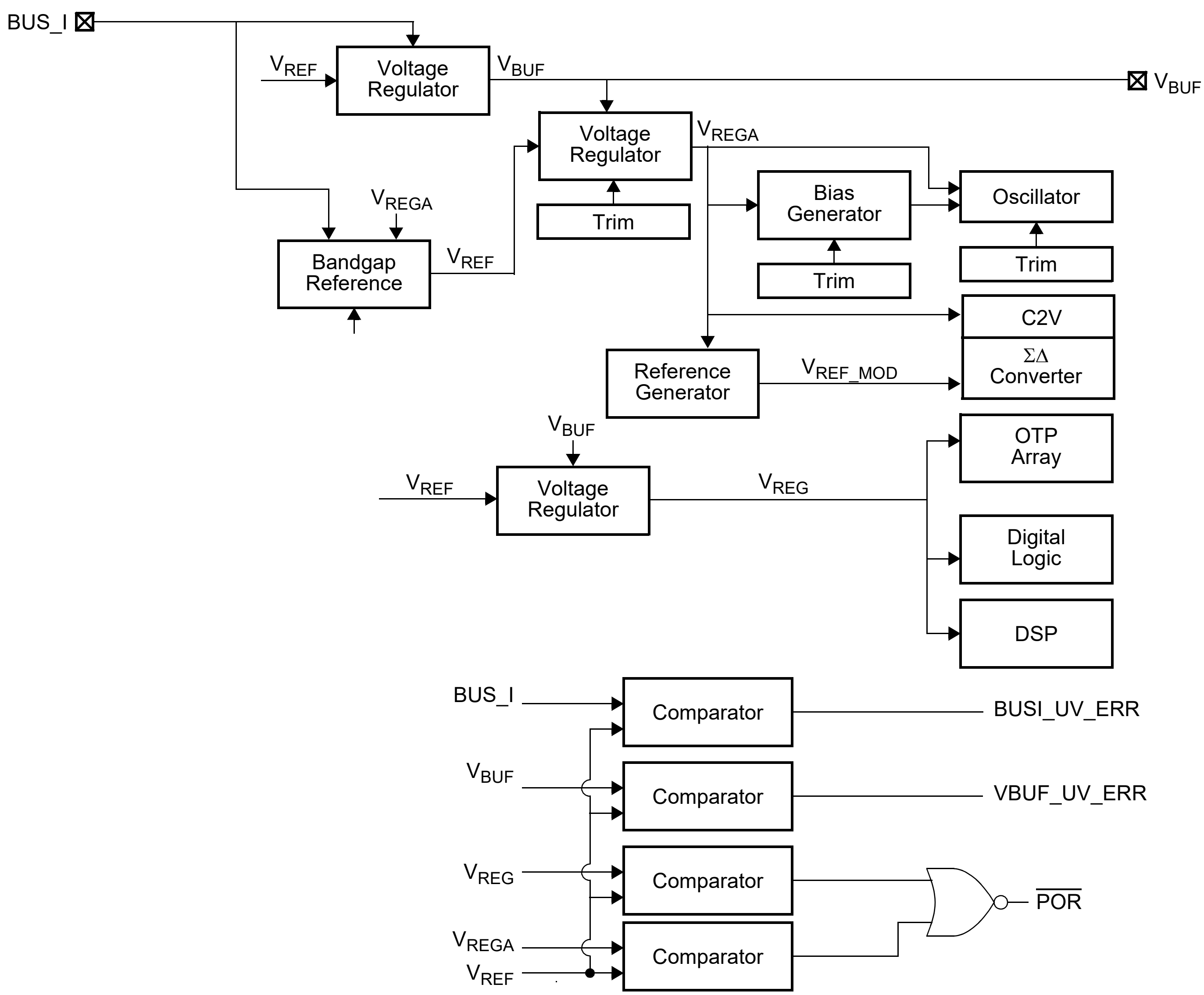


Figure 6-1 Voltage Regulation and Monitoring

6.4.1 V_{BUF} Regulator Capacitor and Capacitor Monitor

In DSI3 and PSI5 modes, the buffer regulator requires an external capacitor between the V_{BUF} pin and the V_{SS} pin. Section 1 shows the recommended types and values for each of these capacitors. A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{BUF} capacitor becomes open. If the external capacitor is not present, the regulator voltage will fall below the threshold specified in Section 5.4 causing the VBUF_ERR bit to be set in the DEVSTAT1 register.

The V_{BUF} capacitor is tested synchronous to the protocol transmissions as shown in the diagrams below.

6.4.1.1 V_{BUF} Capacitance Monitor Timing, DSI3

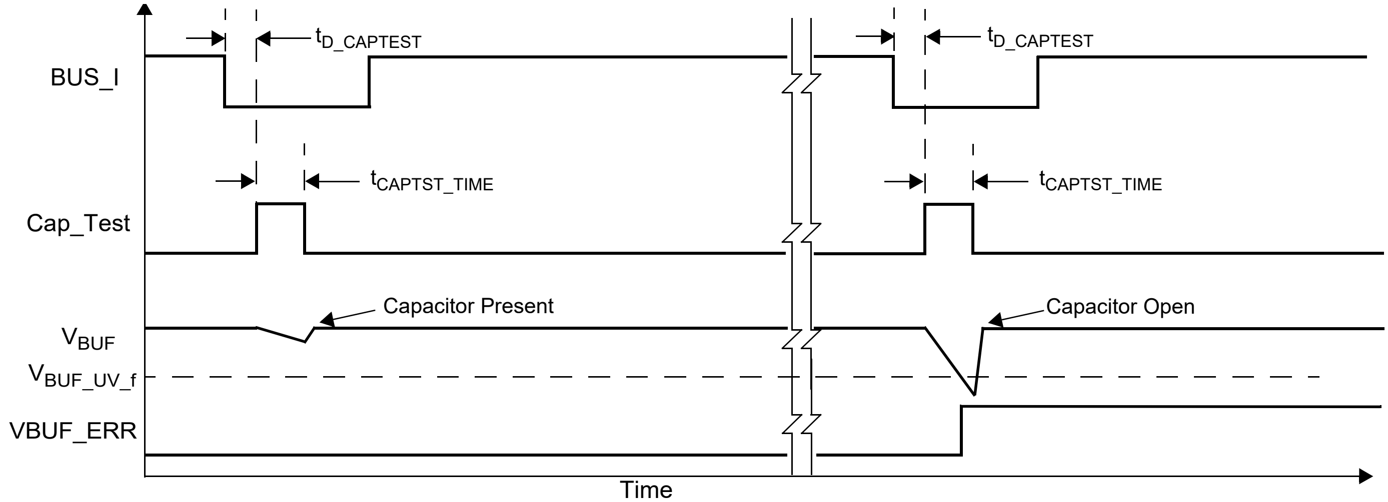


Figure 6-2 V_{BUF} Capacitor Monitor Timing, DSI3

6.4.1.2 V_{BUF} Capacitance Monitor Timing, PSI5 Synchronous Mode

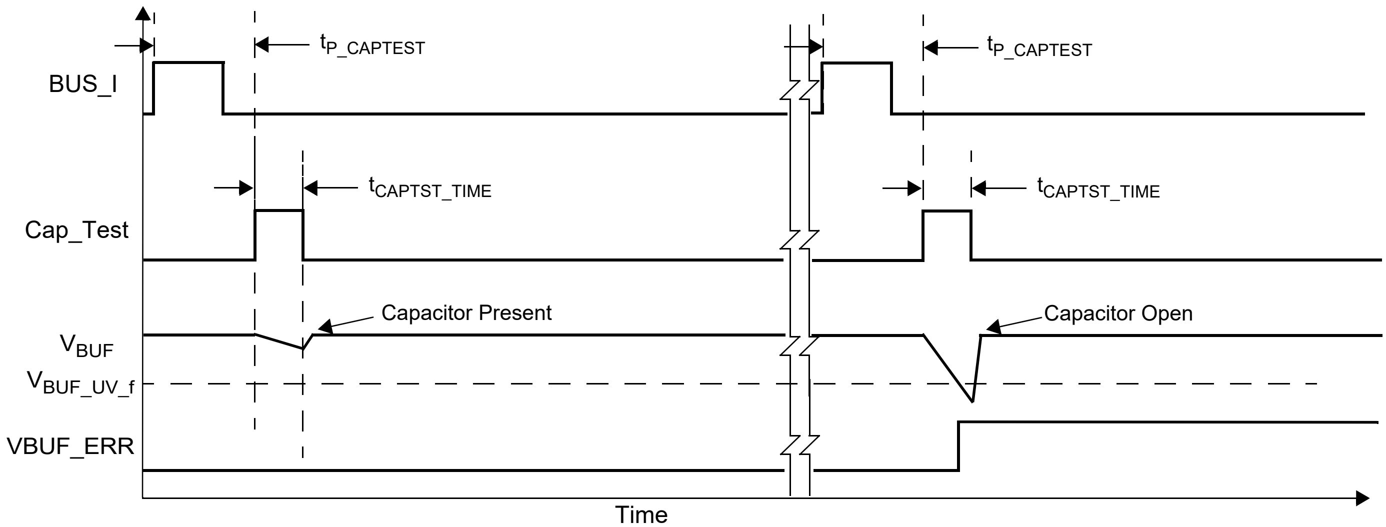


Figure 6-3 V_{BUF} Capacitor Monitor Timing, PSI5 Synchronous Mode

6.4.1.3 V_{BUF} Capacitance Monitor Timing, PSI5 Asynchronous Mode

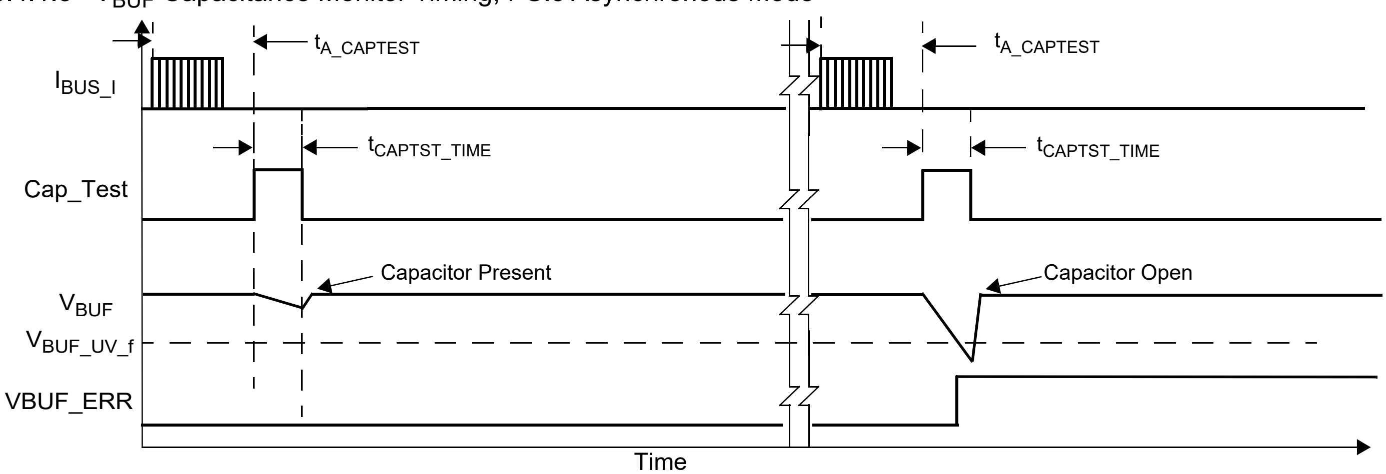


Figure 6-4 V_{BUF} Capacitor Monitor Timing, PSI5 Asynchronous Mode

6.4.2 BUS_I, V_{BUF}, V_{REG}, V_{REGA}, Undervoltage Monitor

A circuit is incorporated to monitor the BUS_I supply voltage and the internally regulated voltages, V_{BUF}, V_{REG} and V_{REGA}. If any of the voltages fall below the specified under-voltage thresholds in Section 5.4, the device will be react as listed below.

- DSI3
  - If any supply falls below the specified threshold during a command transmission in Command and Response Mode, the command is ignored, and no DSI3 response transmission occurs. Once the supply returns above the threshold, the device will resume decoding commands as specified in Section 6.2.2.5.
  - If any supply falls below the specified threshold during a response transmission in Command and Response Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume decoding commands as specified in Section 6.2.2.5.
  - If any supply falls below the specified threshold during a command transmission in Periodic Data Collection Mode, the command is ignored and no periodic response occurs during that period. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 6.2.2.5. Any partially received Background Diagnostic Mode command is flushed and the device will begin decoding a new Background Diagnostic Mode command.
  - If any supply falls below the specified threshold during a periodic response transmission in Periodic Data Collection Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 6.2.2.5. Any partially received Background Diagnostic Mode command is flushed and the device will begin decoding a new Background Diagnostic Mode command.
  - If any supply falls below the specified threshold during a Background Diagnostic Mode response transmission in Periodic Data Collection Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 6.2.2.5. Any partially received Background Diagnostic Mode command is flushed and the device will begin decoding a new Background Diagnostic Mode command.
- PSI5
  - If any supply falls below the specified threshold, all PSI5 transmissions are terminated for the present sync pulse or asynchronous transmission cycle. Once the supply returns above the threshold, the device will resume responses as specified in Section 6.2.2.5.
- SPI
  - If any supply falls below the specified threshold, SPI responses are terminated. Once the supply returns above the threshold, the device will resume command decode and response transmissions as specified in Section 6.2.2.5.
- I^2C
  - If any supply falls below the specified threshold, I^2C transactions are terminated.Once the supply returns above the threshold, the device will resume responses as specified in Section 6.2.2.5.

Reference Figure 6-5 for an example of a supply line interruption during a DSI3 or PSI5 response.

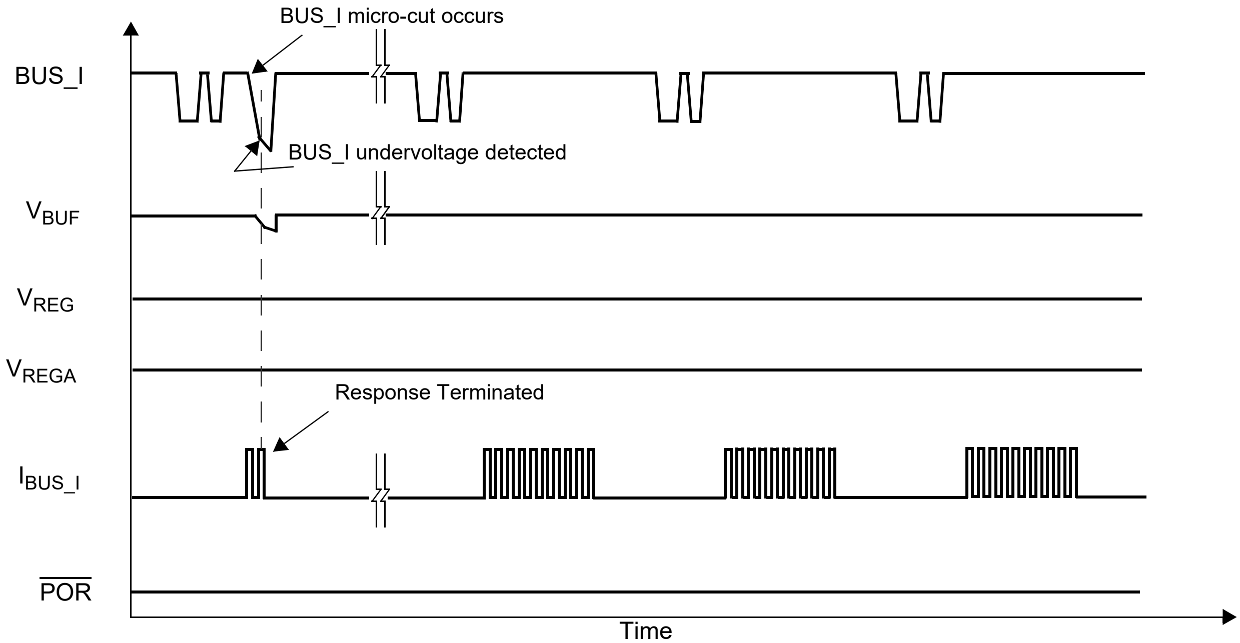


Figure 6-5 BUS_I Micro-Cut Response (DSI3 or PSI5)

6.5 Internal Oscillator

The device includes a factory trimmed oscillator as specified in Section 5.20.

6.5.1 Oscillator Training

The device includes a feature to train the oscillator to a tighter accuracy than the factory trimmed capability assuming the system master has a tighter oscillator accuracy than the slave factory trimmed capability. This feature can be enabled for all modes: DSI3, PSI5, SPI and I^2C.

Note: Oscillator training should not be used in systems that employ spread spectrum communication methods to reduce emissions.

6.5.1.1 DSI3 Oscillator Training

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic transmissions from the master against the values stored in the CRM_PER[1:0] and PDCM_PER[2:0] bits of the user read/write register array. The master programs the intended Periodic Data Collection Mode command period into the PDCM_PER[2:0] bits and the intended Command and Response Mode command period into the CRM_PER[1:0] bits. The device then calculates the number of transmission periods for every 4ms ($n_{CRM\_PER\_4ms\_TYP}$ and $n_{PDCM\_PER\_4ms\_TYP}$).

In Command and Response Mode, oscillator training is completed over 4ms periods if and only if the CK_CAL_EN bit is set and the Command and Response Mode period is between 500us and 4ms, inclusive. The following procedure is used to train the oscillator (Reference Figure 6-6):

1. The device counts the number of oscillator cycles in $n_{CRM\_PER\_4ms\_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 5.20, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If n_{OSC_4ms} is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If n_{OSC_4ms} is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{CRM\_PER\_OSC}$ calculation.

If the CK_CAL_EN bit is cleared after oscillator training has already been initiated, the state of the oscillator is determined by the state of the CK_CAL_RST bit in the TIMING_CFG register. If the CK_CAL_RST bit is cleared, the last adjustment value for the oscillator is maintained. If the CK_CAL_RST bit is set, the oscillator is reset to its untrained value with the untrained tolerance specified in Section 5.20.

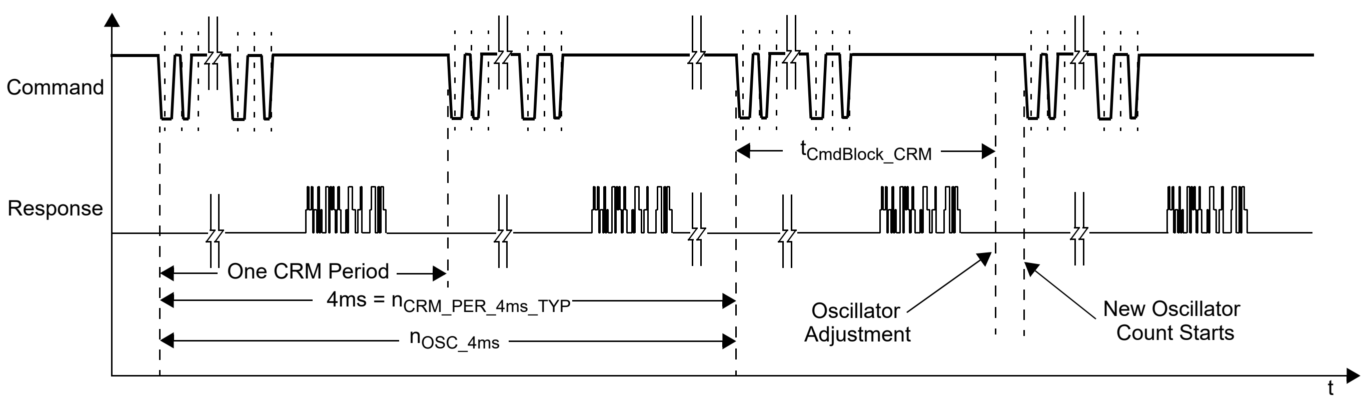


Figure 6-6 Command and Response Mode Oscillator Training Timing Diagram

In Periodic Data Collection Mode, oscillator training is completed over 4ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator (reference Figure 6-7):

1. The device counts the number of oscillator cycles in $n_{PDCM\_PER\_4ms\_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 5.20, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If n_{OSC_4ms} is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If n_{OSC_4ms} is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{PDCM\_PER\_OSC}$ calculation.

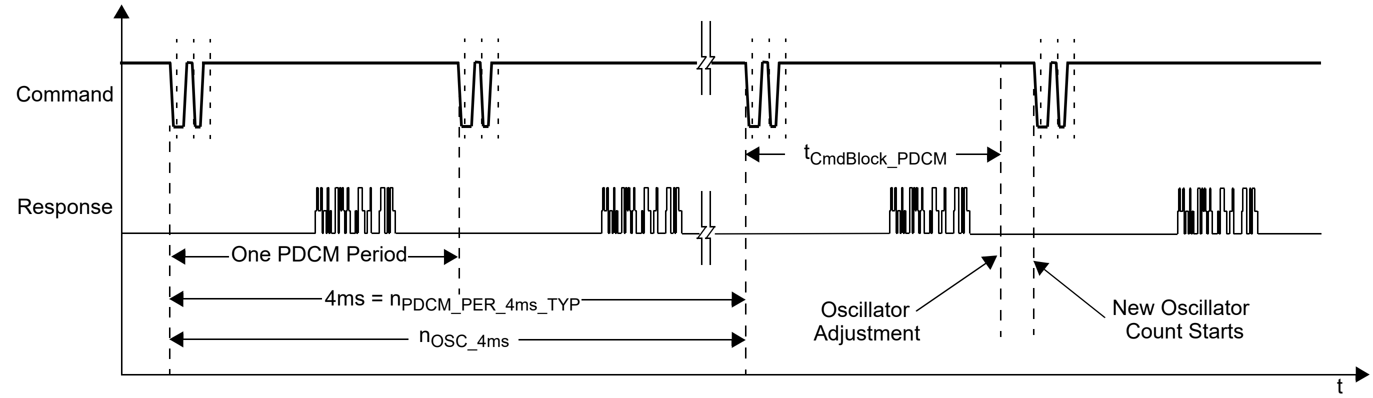


Figure 6-7 Periodic Data Collection Mode Oscillator Training Timing Diagram

6.5.1.2 PSI5 Oscillator Training

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic transmissions from the master against the values stored in the PDCM_PER[2:0] bits of the user read/write register array. The sync pulse period is pre-programmed into the PDCM_PER[2:0] bits. The device then calculates the number of transmission periods for every 4ms ($n_{PSI5\_PER\_4ms\_TYP}$).

Oscillator training is completed over 4ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator (reference Figure 6-8):

1. The device counts the number of oscillator cycles in $n_{PSI5\_PER\_4ms\_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 5.20, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If n_{OSC_4ms} is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If n_{OSC_4ms} is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{PDCM\_PER\_OSC}$ calculation.

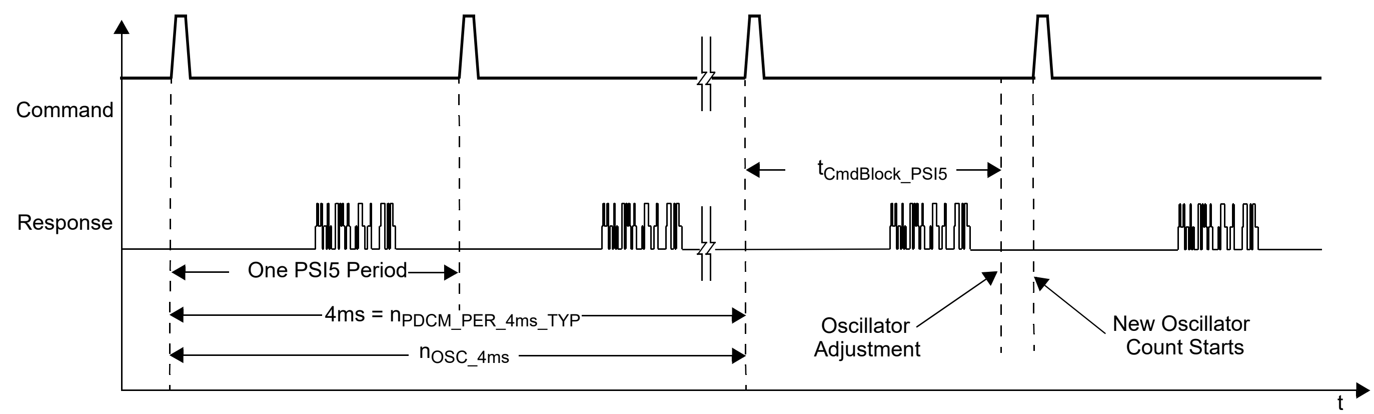


Figure 6-8 PSI5 Oscillator Training Timing Diagram

Notes:

- In order to benefit from the PSI5 oscillator training accuracy improvements, the oscillator must be trained prior to data transmissions in Initialization phase 2. For this reason, if oscillator training is enabled in PSI5 mode, the device will not respond to sync pulses during initialization phase 1, but oscillator training will be enabled t_{RS_PM} after reset.
- Oscillator training will only function properly during initialization phase 1 with a sync pulse period greater than or equal to 500µs.

6.5.1.3 SPI Oscillator Training

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic SOURCEID_0 sensor data request SPI commands from the master against the value stored in the PDCM_PER[2:0] bits of the user read/write register array. The master programs the intended command period into the PDCM_PER[2:0] bits. The device then calculates the number of transmission periods for every 4ms ($n_{SPI\_PER\_4ms\_TYP}$).

In SPI Mode, oscillator training is completed over 4ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator:

1. The device counts the number of oscillator cycles in $n_{SPI\_PER\_4ms\_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 5.20, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If n_{OSC_4ms} is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If n_{OSC_4ms} is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed.

6.5.1.4 I^{2}C Oscillator Training

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic I^{2}C reads of the SNSDATA0_L register from the master against the value stored in the PDCM_PER[2:0] bits of the user read/write register array. The master programs the intended command period into the PDCM_PER[2:0] bits. The device then calculates the number of transmission periods for every 4ms ($n_{SPI\_PER\_4ms\_TYP}$).

In I^{2}C Mode, oscillator training is completed over 4ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator:

1. The device counts the number of oscillator cycles in $n_{I2C\_PER\_4ms\_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC\_4ms\_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 5.20, an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If n_{OSC_4ms} is greater than $n_{OSC\_4ms\_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
   b. If n_{OSC_4ms} is less than $n_{OSC\_4ms\_TYP}$ - $OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed.

6.5.2 Oscillator Training Error Handling

If oscillator training is enabled by the user, but the conditions are not correct to complete oscillator training, the OSCTRAIN_ERR bit is set in the DEVSTAT register. The following conditions will result in the OSCTRAIN_ERR bit being set.

- The CLK_CAL_EN bit in the TIMING_CFG register is set and the measured period (n_{OSC_4ms}) for any mode is outside of the Oscillator Training Window ($OscTrain_{WIN}$).
- The result of the comparison is filtered with an up and down counter.
- If n_{OSC_4ms} is outside the oscillator training window, the counter is incremented.
- If n_{OSC_4ms} is inside the oscillator training window, the counter is decremented.
- If the counter reaches 64 counts, the OSCTRAIN_ERR bit is set.
- The up and down counter has a maximum value of 127 and a minimum value of 0.
- The Command and Response Mode period established by the PDCM_PER and CRM_PER settings does not fall within the 500µs to 4ms window.
- The Command and Response Mode period established by the PDCM_PER and CRM_PER settings is not a whole number divisor of 4ms.

6.6 Inertial Sensor Signal Path

6.6.1 Inertial Sensor Transducer

The device transducer is an overdamped mass-spring-damper system defined by the following transfer function:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

Where:

ζ = Damping Ratio

ω_n = Natural Frequency = $2*\Pi*f_n$

Reference Section 5.19 for transducer parameters.

6.6.2 Inertial Sensor Self Test Interface

The analog self test interface applies a voltage to the g-cell, causing deflection of the proof mass. The resulting sensor data can be compared against the values stored in the Self Test Deflection Registers (Reference Section 6.2.34). The self test interface is controlled through register write operations to the ST_CTRL[3:0] bits in the CHx_CFG_U5 register described in Section 6.2.26. A diagram of the self test interface is shown in Figure 6-9.

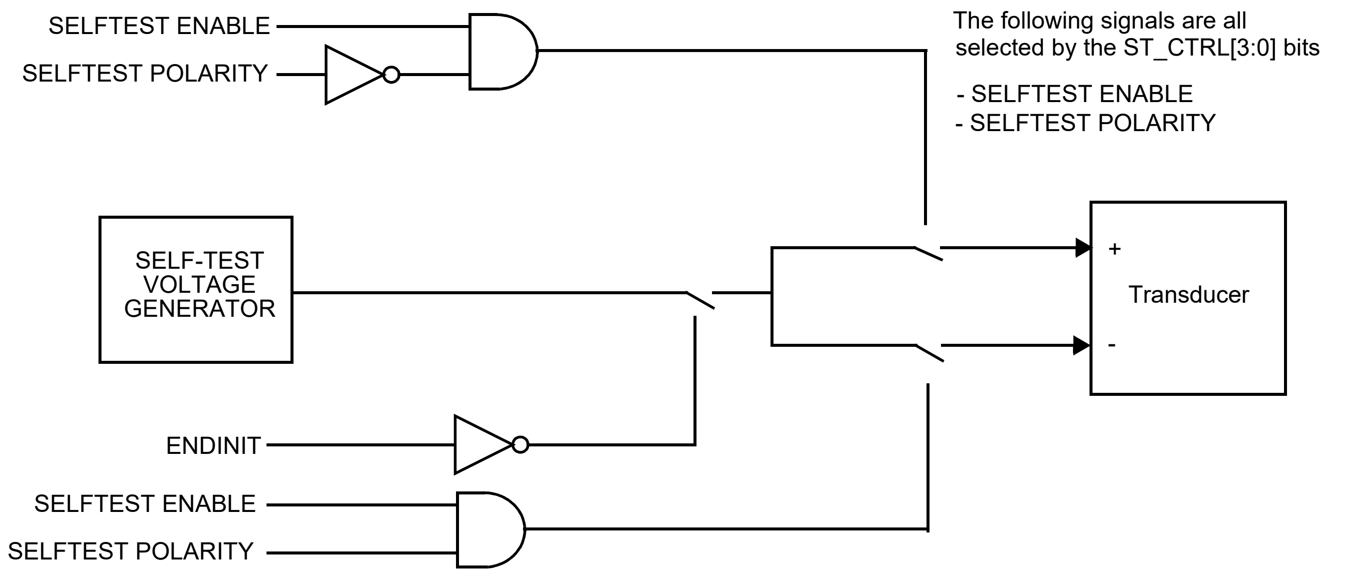


Figure 6-9 Self Test Interface

Self test can be verified via the following methods:

6.6.2.1 Raw Self Test Deflection Verification

In DSI3 mode, SPI mode or I^2C mode, the raw self test deflection can be verified against raw self test limits in Section 5.8.

6.6.2.2 Delta Self Test Deflection Verification

In DSI3 mode, SPI mode or I^2C mode, the raw self test deflection can be verified against the nominal temperature self test deflection value recorded at the time the device was produced. The production self test deflection is stored in the CHx_STy_z register as defined in Section 6.2.34. The Delta Self Test Deflection limits can then be determined by the following equations:

$$\Delta ST_{ACCMINLIMIT} = STDATA \times (1 - \Delta ST_{ACC})$$

Note: This value is truncated.

$$\Delta ST_{ACCMAXLIMIT} = STDATA \times (1 + \Delta ST_{ACC})$$

Note: This value is rounded up.

Where:

	ΔST_{ACC}	The accuracy of the self test deflection relative to the stored deflection as specified in Section 5.8.
	STDATA	The value stored in the appropriate CHx_STy_z register as defined in Section 6.2.34.

6.6.2.3 Startup Digital Self-Test

In DSI3 mode, SPI mode or I^2C mode, during device initialization (ENDINIT not set), the user can activate a digital self-test by writing to the ST_CTRL[3:0] bits in the CHx_CFG_U5 register. The digital self test inputs a known signal stream into the front end of the DSP. After a delay defined by the low pass filter selected, the output sensor data reaches a fixed value which can be verified by the user. The digital self-test values are listed in Section 6.2.26.1.

Note: when any digital self-test is deasserted, the TEMPx_ERR bit for the associated channel is set. This bit is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

6.6.2.4 Fixed Pattern Self-Test

In DSI3 mode, SPI mode or I^2C mode, during device initialization (ENDINIT not set), the user can activate a fixed pattern self-test by writing to the ST_CTRL[3:0] bits in the CHx_CFG_U5 register. Fixed pattern self tests force the DSP output to a set of known values, enabling the user to verify each bit of the sensor data. Fixed pattern self-test values are listed in Section 6.2.26.1.

6.6.2.5 PSI5 Automatic Start Up Self Test Procedure

The following procedure is run automatically on start up for each channel if the device is enabled as a PSI5 device. The minimum gain settings are used during this procedure: U_SNS_SHIFT = ‘00’, U_SNS_MULT = 0x00.

1. Delay t_{PSI5ST_START} (Until Initialization Phase 1 is complete).
2. Suspend the offset cancellation filter.
3. With self test disabled (ST_CTRL = ‘000’), sample the DSP output value every 500μs for 8ms. Compute the average of the 16 DSP output values as the offset.
4. Enable the positive high g self test by automatically setting the ST_CTRL bits in the CHx_CFG_U5 register to the appropriate value.
5. Delay 16 ms.
6. Sample the DSP output value every 500μs for 8ms. Compute the average of the 16 DSP output values. Record the lower 8-bits of the 10-bit PSI5 value.
7. Compare the result to the minimum and maximum self test limits. If the difference is outside of the limits specified in Section 5.8, set the REPEAT_ST flag indicating the test must be repeated.
8. Disable self test (ST_CTRL = ‘000’).
9. Delay 16ms.
10. Sample the DSP output value every 500μs for 8ms. Compute the average of the 16 DSP output values as the offset.
11. Enable the negative high g self test by automatically setting the ST_CTRL bits in the CHx_CFG_U5 register to the appropriate value.
12. Delay 16 ms.
13. Sample the DSP output value every 500μs for 8ms. Compute the average of the 16 DSP output values. Record the lower 8-bits of the 10-bit PSI5 value.
14. Compare the result to the minimum and maximum self test limits. If the difference is outside of the limits specified in Section 5.8, set the REPEAT_ST flag indicating the test must be repeated.
15. Disable Self Test.
16. Delay 16 ms.
17. Sample the DSP output value every 500μs for 8ms. Compute the average of the 16 DSP output values as the offset.
18. If the REPEAT_ST flag is cleared, exit with ST_ERROR cleared. If the REPEAT_ST flag is set, clear the flag, increment the self test repeat counter and compare it to ST_RPT.
    a. If the counter is less than ST_RPT repeat steps 2 - 18.
    b. If the counter is equal to or greater than ST_RPT, set the ST_ERROR flag in the CHx_STAT register.
19. Resume the offset cancellation filter startup.

If the ST_ERROR flag in the CHx_STAT register is set once this test is complete, the device will exit PSI5 initialization phase 2 with a self test error and the self test error message will be transmitted instead of sensor data. In this case, the ST_ERROR bit can only be cleared by a device reset.

6.6.3 Inertial Sensor ΣΔ Converter

A second order sigma delta modulator converts the differential capacitance of the transducer to a data stream that is input to the DSP. The sigma delta modulator operates at a frequency of 1MHz. A simplified block diagram is shown in Figure 6-10.

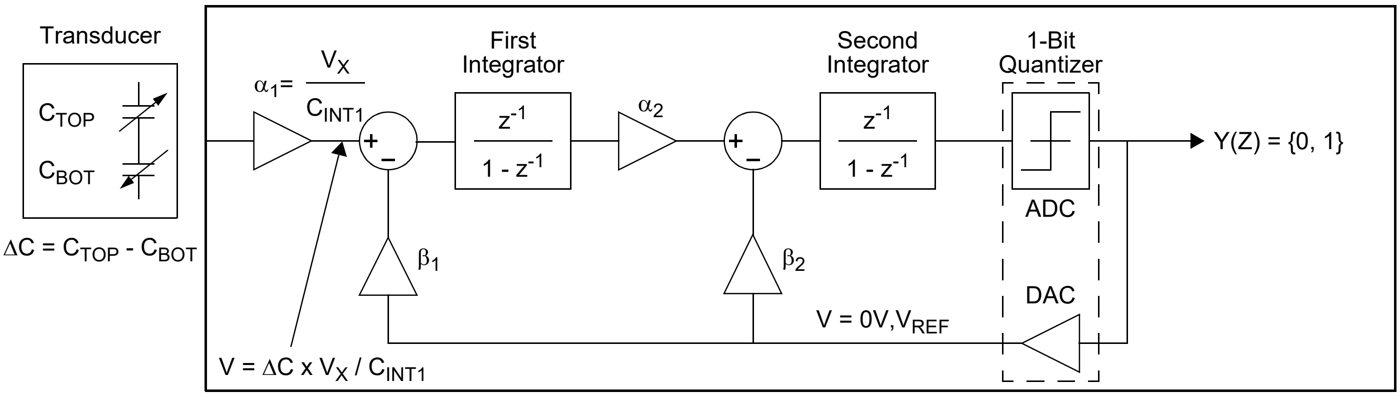


Figure 6-10 ΣΔ Converter Block Diagram

6.6.4 Inertial Sensor Digital Signal Processor

A digital signal processor (DSP) is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP is shown in Figure 6-11.

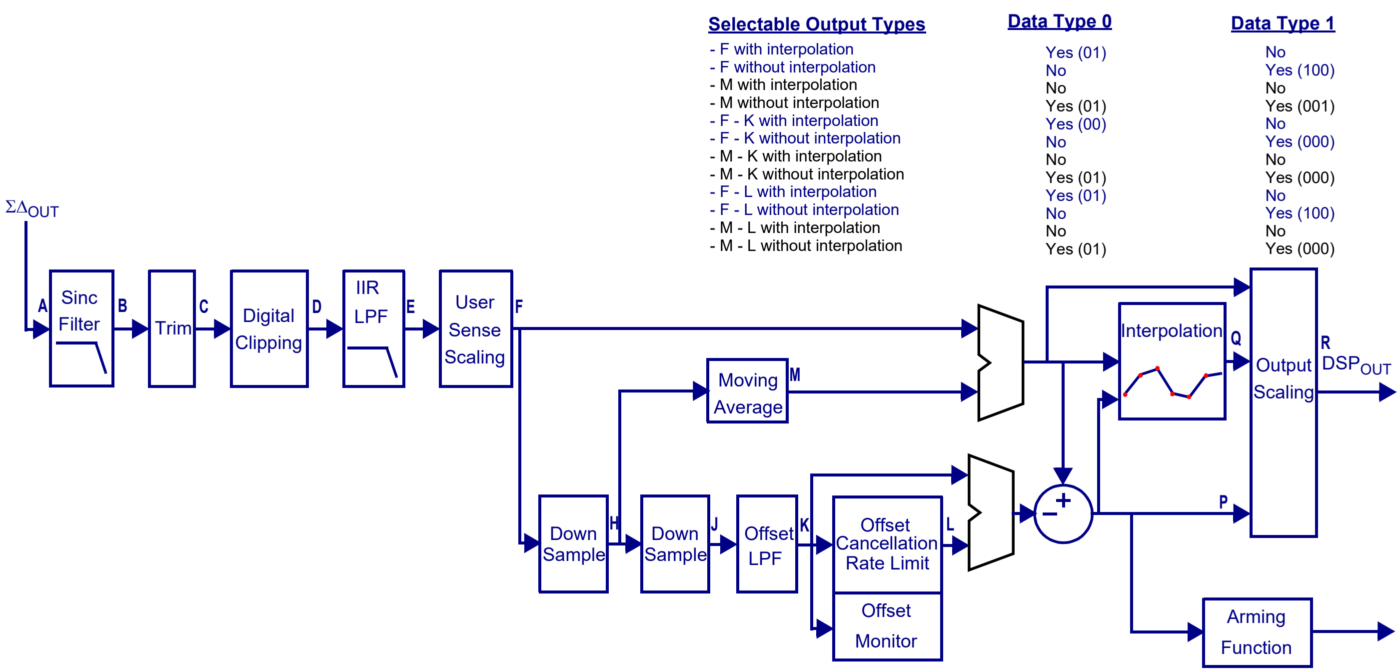


Figure 6-11 Signal Chain Diagram

	Description	Sample Time (µs)	Data Width (Bits)	Sign (Bits)	Over Range (Bits)	Signal Width (Bits)	Signal Margin (Bits)	Typical Block Latency	Reference
A	ΣΔ	1	1	1	NA	1	NA	2.5µs	Section 6.6.3
B	SINC Filter	16, 32, 64	23	1	NA	21	NA	22.5µs	Section 6.6.4.1
C	Trim	16, 32, 64	32	1	2	18	11	N/A	Section 6.6.4.2
D	Digital Clipping	16, 32, 64	32	1	2	18	11	N/A	Section 6.6.4.3
E	Low Pass Filter	16, 32, 64	32	1	2	18	11	Filter Dependent	Section 6.6.4.4
F	User Scaling	16, 32, 64	32	1	2	18	11	N/A	Section 6.6.4.5
H	Down Sample	32, 64, 128	32	1	NA	31	NA	N/A	Section 6.6.4.7
J	Secondary Down Sample	256	32	1	NA	31	NA	N/A	Section 6.6.4.6
K	Offset Low Pass Filter	256	16	1	2	11	2	N/A	Section 6.6.4.6
L	Offset Rate Limiting	256	16	1	2	11	2	N/A	Section 6.6.4.6
M	Moving Average Filter	32, 64, 128	24	1	2	18	3	Filter Dependent	Section 6.6.4.7
P	Offset Subtraction	32, 64, 128	24	1	2	18	3	N/A	Section 6.6.4.6
Q	Interpolation	1, 2, 4	24	1	2	18	3	$t_{SigChainXX}$	Section 6.6.4.8
R	Output Range Selection	1, 2, 4	18	User Selectable				N/A	Section 6.6.4.9

6.6.4.1 Decimation Sinc Filter

The output of the ΣΔ modulator is decimated and converted to a parallel value by a 3rd order Sinc Filter with a decimation ratio of 16:

$$H(Z) = \left(\frac{1}{16^3}\right) \times \left(\frac{1 - Z^{-16}}{1 - Z^{-1}}\right)^3$$

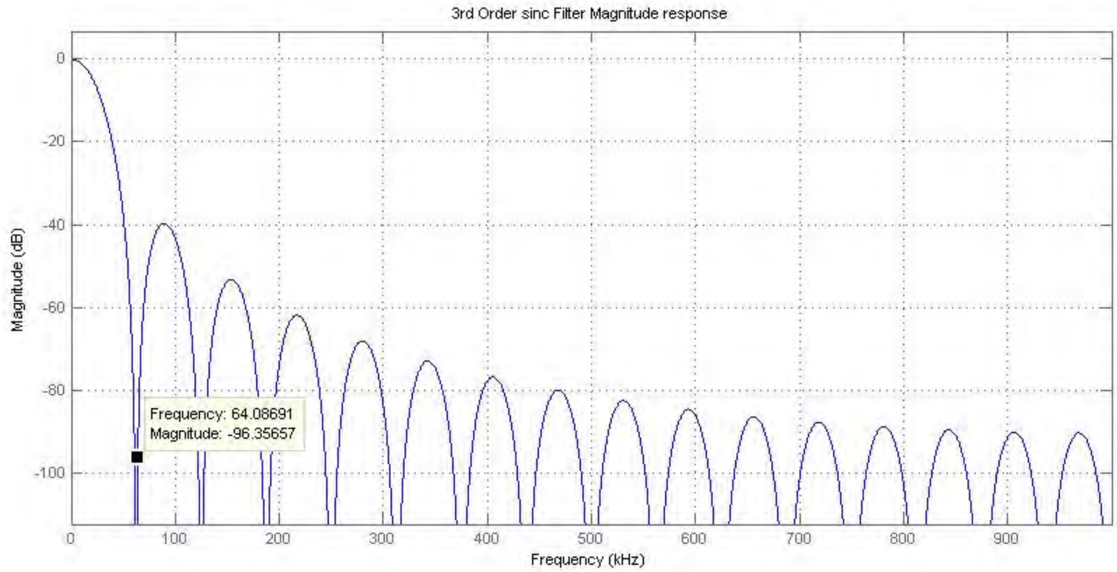


Figure 6-12 Sinc Filter Response

6.6.4.2 Signal Trim and Compensation

The device includes digital trim to compensate for sensor offset, sensitivity and non-linearity over temperature. The following equations are used for the trim compensation:

$$Offset_{Trim} = A_0 + B_2 \times (T - T_{25}) + C_{22} \times (T - T_{25})^2$$

$$Sensitivity_{Trim} = B_1 + (T - T_{25}) \times C_{12}$$

$$Linearity_{Trim} = C_{11}$$

$$Trim_{OUT} = Trim_{In} \times [Sensitivity_{Trim} + Trim_{In} \times Linearity_{Trim}] + Offset_{Trim}$$

Variable Name	Description	Range (Real)	Variable Size (Bits)	Resolution (Real)
A_0	Offset Compensation	-1.0 to +1.0	12	4.8852e-04
B_2	Offset Compensation with First Order Temperature Compensation	-1.0 to +1.0	12	4.8852e-04
C_{22}	Offset Compensation with Second Order Temperature Compensation	-1.0 to +1.0	12	4.8852e-04
B_1	Sensitivity Compensation	-1.0 to +1.0	12	4.8852e-04
C_{12}	Sensitivity Compensation with First Order Temperature Compensation	-1.0 to +1.0	12	4.8852e-04
C_{11}	Linearity Compensation	-1.0 to +1.0	12	4.8852e-04
T	Temperature Sensor Digital Output Value	-1.0 to +1.0	12	4.8852e-04
T_{25}	Temperature Sensor Output Value stored at the Ambient Test Insertion	-1.0 to +1.0	12	4.8852e-04
$Trim_{In}$	Output of the Sinc Filter			
$Trim_{Out}$	Output of the Trim Block			

6.6.4.3 Digital Clipping

The device includes a digital clipping block to maximize the symmetry between the positive and negative electrical dynamic range of the device. Digital clipping values are specified in Section 5.8.

6.6.4.4 Low Pass Filter

Data from the Sinc filter is processed by an infinite impulse response (IIR) low pass filter.

$$H(z) = a_0 \cdot \frac{(n_{11} \cdot z^0) + (n_{12} \cdot z^{-1}) + (n_{13} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{12} \cdot z^{-1}) + (d_{13} \cdot z^{-2})} \cdot \frac{(n_{21} \cdot z^0) + (n_{22} \cdot z^{-1}) + (n_{23} \cdot z^{-2})}{(d_{21} \cdot z^0) + (d_{22} \cdot z^{-1}) + (d_{23} \cdot z^{-2})}$$

The device provides the option for one of several low-pass filters. The filter coefficients are selected with the LPF[3:0] bits in the CHx_CFG_U1 registers.

The filter selection options are listed in Section 6.2.22.1. Response parameters for the low-pass filter are specified in Section 5.18. Filter characteristics for the highest sample rate are illustrated in the figures below.

LPF #0 and LPF #2

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (μs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)	Filter Coefficients			
		00 or 01	400Hz	16μs		839	-19.5	1.59	a_0	0.003143225986084408		
									n_{11}	0.0009951105668343345	d_{11}	1
									n_{12}	0.002003487780064749	d_{12}	-1.892328151433503
0,2	0000 or 0010	10	200Hz	32μs	4	1678	-42.3	3.18	n_{13}	0.001008466113720278	d_{13}	0.8954713774195870
									n_{21}	0.2516720624825626	d_{21}	1
									n_{22}	0.4999888752940916	d_{22}	-1.918978239761011
		11	100Hz	64μs		3356	-66.0	6.36	n_{23}	0.2483390622233452	d_{23}	0.9229853042218408

LPF #1 and LPF #3

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (μs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)	Filter Coefficients			
		00 or 01	400Hz	16μs		697	-16.6	1.49	a_0	0.05189235225042199		
									n_{11}	0.001629077582099646	d_{11}	1
									n_{12}	0.001630351547919014	d_{12}	-0.9481076477495780
1,3	0001 or 0011	10	200Hz	32μs	3	1394	-33.5	2.98	n_{13}	0	d_{13}	0
									n_{21}	0.2500977520825902	d_{21}	1
									n_{22}	0.4999999235890745	d_{22}	-1.915847097557409
		11	100Hz	64μs		2788	-51.5	5.96	n_{23}	0.2499023243303036	d_{23}	0.9191065266874253

LPF #4

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (μs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)	Filter Coefficients			
		00 or 01	325Hz	16μs		856	-21.4	1.84	a_0	0.0424754749983549118		
									n_{11}	0.0010903775691986084	d_{11}	1
									n_{12}	0.00108939409255981445	d_{12}	-0.95752453804016113281
4	0100	10	162.5Hz	32μs	4	1712	-38.7	3.68	n_{13}	0	d_{13}	0
									n_{21}	0.24988752603530883789	d_{21}	1
									n_{22}	0.49999989569187164307	d_{22}	-1.93140876293182373047
		11	81.25Hz	64μs		3424	-56.8	7.36	n_{23}	0.2501125633716583252	d_{23}	0.93358850479125976562

LPF #5

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (μs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)	Filter Coefficients			
		00 or 01	370Hz	16μs		586	-14.1	1.55	a_0	0.00220982858445495367		
									n_{11}	0.25	d_{11}	1
									n_{12}	0.49999998509883880615	d_{12}	-1.91803151369094848633
5	0101	10	185Hz	32μs	2	1172	-25.2	3.10	n_{13}	0.25	d_{13}	0.92024135589599609375
									n_{21}	1	d_{21}	1
									n_{22}	0	d_{22}	0
		11	92.5Hz	64μs		2344	-37.2	6.20	n_{23}	0	d_{23}	0

LPF #6

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (μs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)	Filter Coefficients			
		00 or 01	180Hz	16μs		1187	-25.6	3.19	a_0	0.00053406920051202178		
									n_{11}	0.25	d_{11}	1
									n_{12}	0.50	d_{12}	-1.95983958244323730469
6	0110	10	90Hz	32μs	2	2374	-37.5	6.38	n_{13}	0.25	d_{13}	0.96037364006042480469
									n_{21}	1	d_{21}	1
									n_{22}	0	d_{22}	0
		11	45Hz	64μs		4748	-49.7	12.8	n_{23}	0	d_{23}	0

LPF #7

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (µs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)
7	0111	00 or 01	100Hz	16µs	2	2167	-35.7	5.75
		10	50Hz	32µs		4334	-47.7	11.5
		11	25Hz	64µs		8668	-60.0	23.0

Filter Coefficients			
a_0	0.00016630983736831695		
n_{11}	0.25	d_{11}	1
n_{12}	0.5	d_{12}	-1.97762179374694824219
n_{13}	0.25	d_{13}	0.97778809070587158203
n_{21}	1	d_{21}	1
n_{22}	0	d_{22}	0
n_{23}	0	d_{23}	0

LPF #8

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (µs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)
8	1000	00 or 01	1500Hz	16µs	4	223	-1.26	0.420
		10	750Hz	32µs		446	-5.70	0.840
		11	375Hz	64µs		892	-21.7	1.68

Filter Coefficients			
a_0	0.03834337295612844088		
n_{11}	0.01260285855167835381	d_{11}	1
n_{12}	0.02520581295635351826	d_{12}	-1.62182206187479138748
n_{13}	0.01260284171453899225	d_{13}	0.66016543483091971734
n_{21}	0.25000039185483757809	d_{21}	1
n_{22}	0.49999888229656874739	d_{22}	-1.69136566438039781524
n_{23}	0.25000072584865173919	d_{23}	0.74177717760299266558

LPF #9

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (µs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)
9	1001	00 or 01	500Hz	16µs	3	558	-12.0	1.18
		10	250Hz	32µs		1116	-27.9	2.36
		11	125Hz	64µs		2232	-45.8	4.72

Filter Coefficients			
a_0	0.06461570392887561187		
n_{11}	0.00253228358602412005	d_{11}	1
n_{12}	0.00253382455746249506	d_{12}	-0.93538429607112438813
n_{13}	0.0	d_{13}	0.0
n_{21}	0.25007606629379214302	d_{21}	1
n_{22}	0.49999995372560029905	d_{22}	-1.89461887839771225828
n_{23}	0.24992397997755622097	d_{23}	0.89968498654120099278

LPF #A

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (µs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)
A	1010	00 or 01	800Hz	16µs	4	419	-4.92	0.795
		10	400Hz	32µs		838	-19.5	1.59
		11	200Hz	64µs		1676	-42.3	3.18

Filter Coefficients			
a_0	0.01190410984205714229		
n_{11}	0.00384158186528944052	d_{11}	1
n_{12}	0.00768325414507123675	d_{12}	-1.79000462719285069468
n_{13}	0.00384155498534484614	d_{13}	0.80190873703490794799
n_{21}	0.25000103366513437564	d_{21}	1
n_{22}	0.49999618339874751793	d_{22}	-1.83684943491757790568
n_{23}	0.25000278293126343421	d_{23}	0.85221582591330946599

LPF #B

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (µs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)
B	1011	00 or 01	1200Hz	16µs	4	279	-2.00	0.530
		10	600Hz	32µs		558	-9.30	1.06
		11	300Hz	64µs		1116	-28.8	2.12

Filter Coefficients			
a_0	0.02546195827091324651		
n_{11}	0.00830769458672901175	d_{11}	1
n_{12}	0.01661549341945577768	d_{12}	-1.69226073394381204551
n_{13}	0.00830767373784346147	d_{13}	0.71772269221472528855
n_{21}	0.25000062740839573694	d_{21}	1
n_{22}	0.49999811778583796995	d_{22}	-1.75385062639799738093
n_{23}	0.25000125480314383530	d_{23}	0.78708148814205258770

LPF #C and LPF #D

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (µs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)
C,D	1100 or 1101	00 or 01	120Hz	16µs	3	2325	-46.5	5.00
		10	60Hz	32µs		4650	-64.5	10.0
		11	30Hz	64µs		9300	-82.8	20.0

Filter Coefficients			
a_0	0.01589500145947964072		
n_{11}	0.00015161988544501960	d_{11}	1
n_{12}	0.00015200954845361584	d_{12}	-0.98410499854052035928
n_{13}	0.0	d_{13}	0.0
n_{21}	0.25032124994306603760	d_{21}	1
n_{22}	0.49999917553953604488	d_{22}	-1.97464045392631648568
n_{23}	0.24967957470143059551	d_{23}	0.97494408336020621508

LPF #E

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (µs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)	Filter Coefficients			
		00 or 01	120Hz	16µs		1804	-32.8	4.85	a_0	0.00023895280210650682		
									n_{11}	0.25	d_{11}	1
									n_{12}	0.50	d_{12}	-1.97316625013962188007
E	1110	10	60Hz	32µs	2	3608	-44.7	9.70	n_{13}	0.25	d_{13}	0.97340520294172827587
									n_{21}	1	d_{21}	1
									n_{22}	0	d_{22}	0
		11	30Hz	64µs		7216	-57.0	19.4	n_{23}	0	d_{23}	0

LPF #F

Filter #	LPF[3:0]	SAMPLERATE[1:0]	Typical -3dB Frequency	Sample Time	Filter Order	Group Delay (µs)	1000 Hz Attenuation (dB)	Step Response Activation to 99% (ms)	Filter Coefficients			
		00 or 01	50Hz	16µs		6726	-89.7	12.8	a_0	0.00005137322664827693		
									n_{11}	0.00001504124143177110	d_{11}	1
									n_{12}	0.00003226111162087577	d_{12}	-1.98626319205697576820
F	1111	10	25Hz	32µs	4	13,452	-114	25.6	n_{13}	0.00001738720648386979	d_{13}	0.98631456528362415614
									n_{21}	0.26880063911477075633	d_{21}	1
									n_{22}	0.49866318155607519680	d_{22}	-1.98997568035769623052
		11	12.5Hz	64µs		26,904	-138	51.2	n_{23}	0.23253587866496652770	d_{23}	0.99004036988244481510

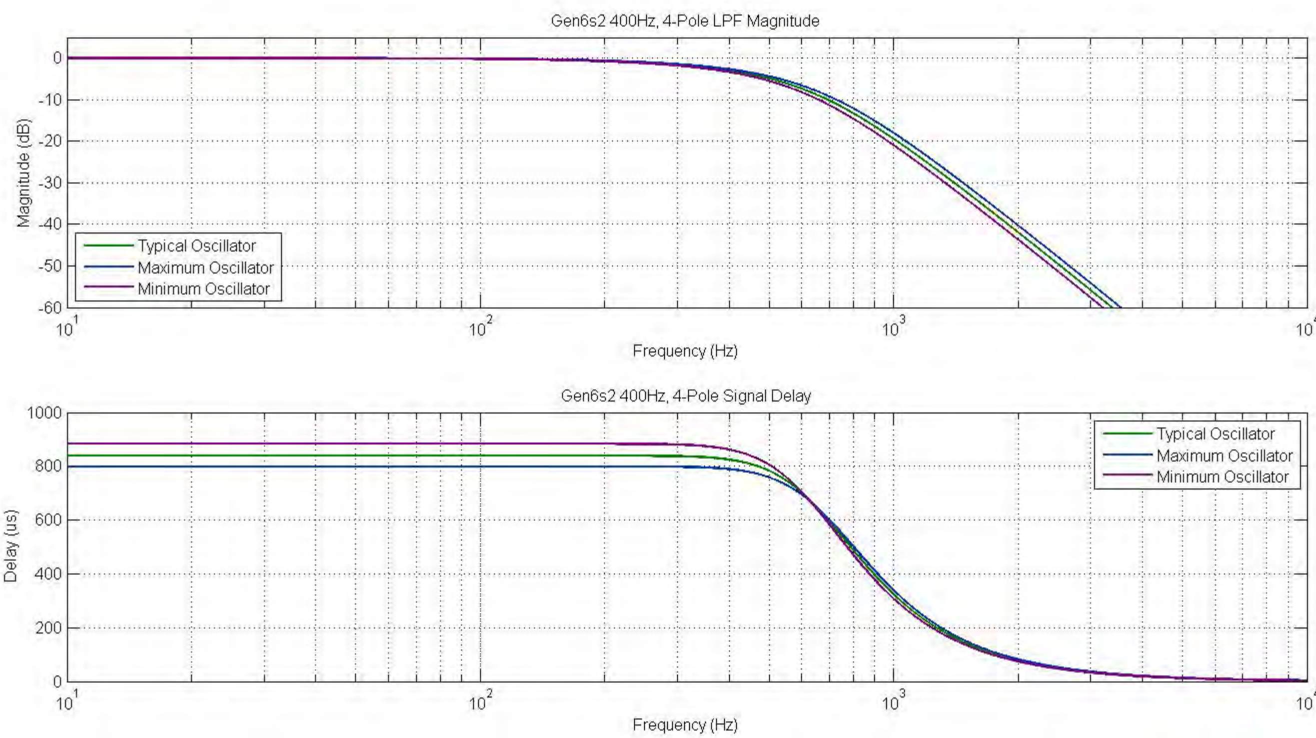


Figure 6-13 400Hz, 4-Pole Low-Pass Filter Response

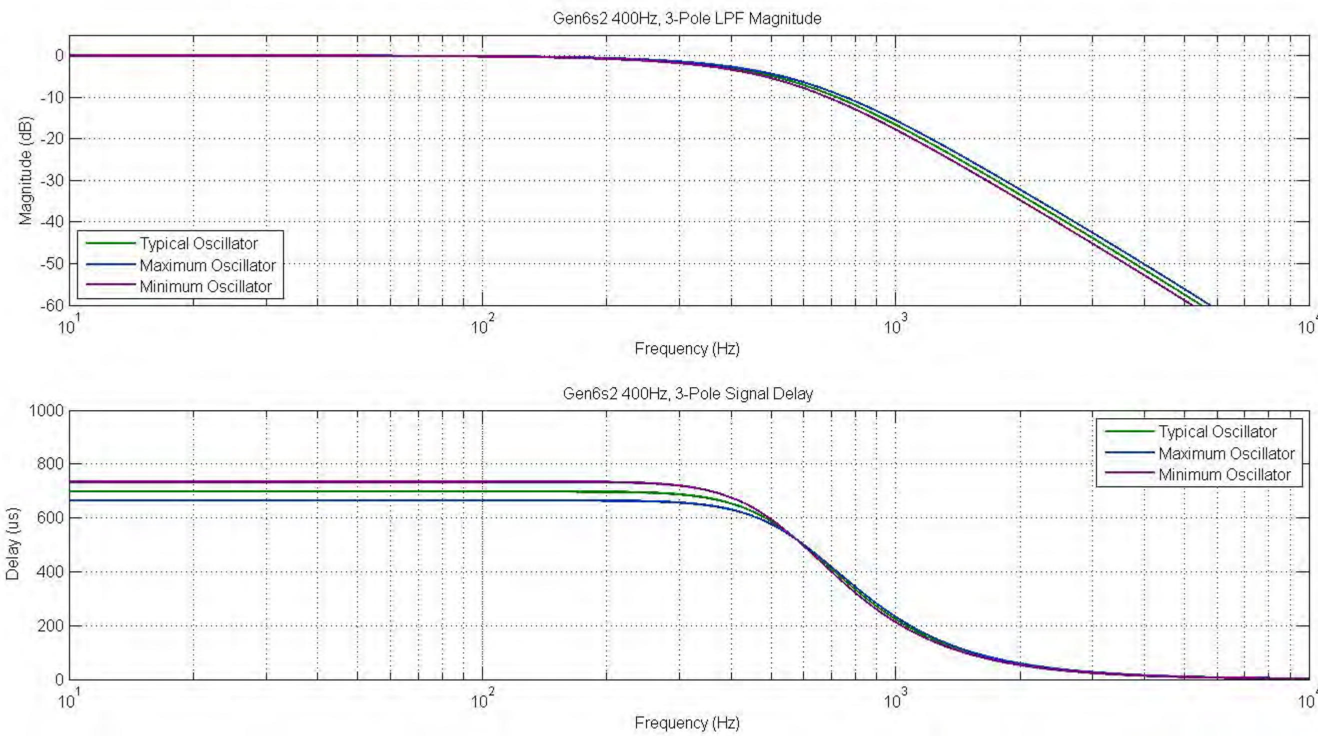


Figure 6-14 400Hz, 3-Pole Low-Pass Filter Response

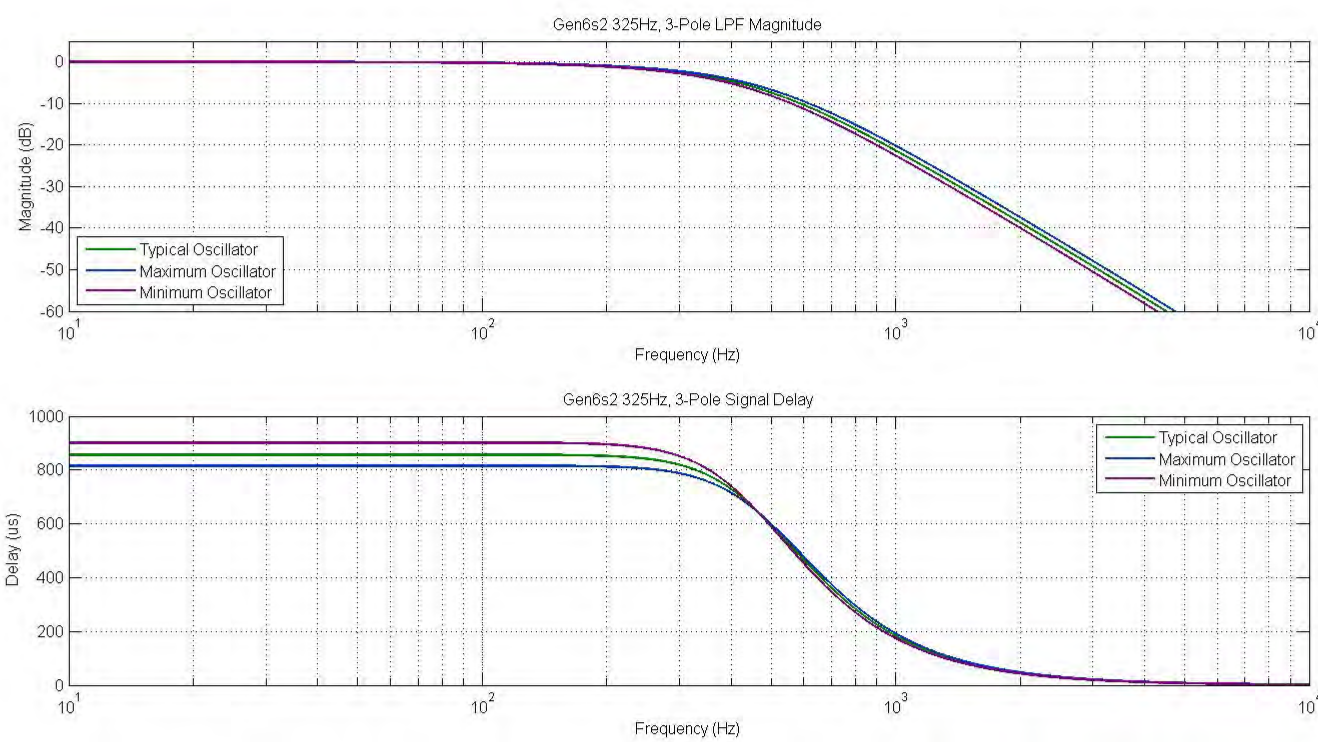


Figure 6-15 325Hz, 3-Pole Low-Pass Filter Response

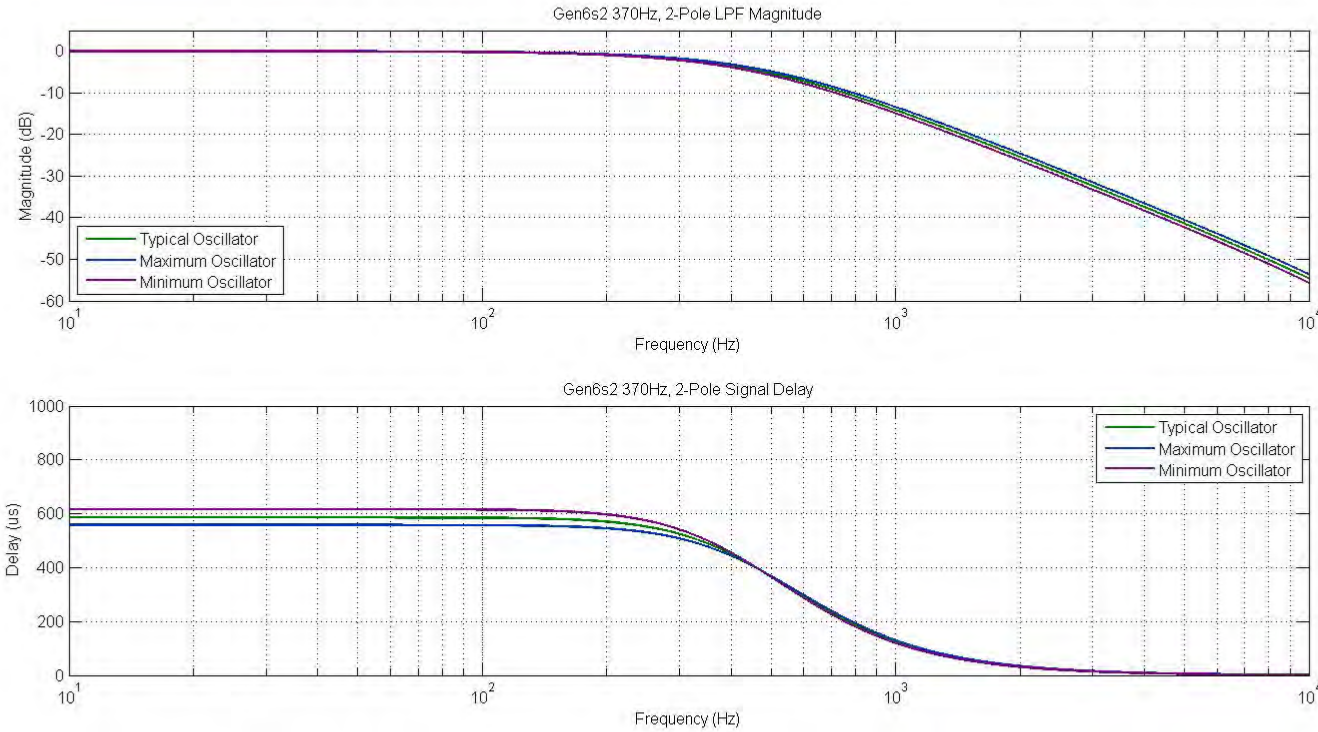


Figure 6-16 370Hz, 2-Pole Low-Pass Filter Response

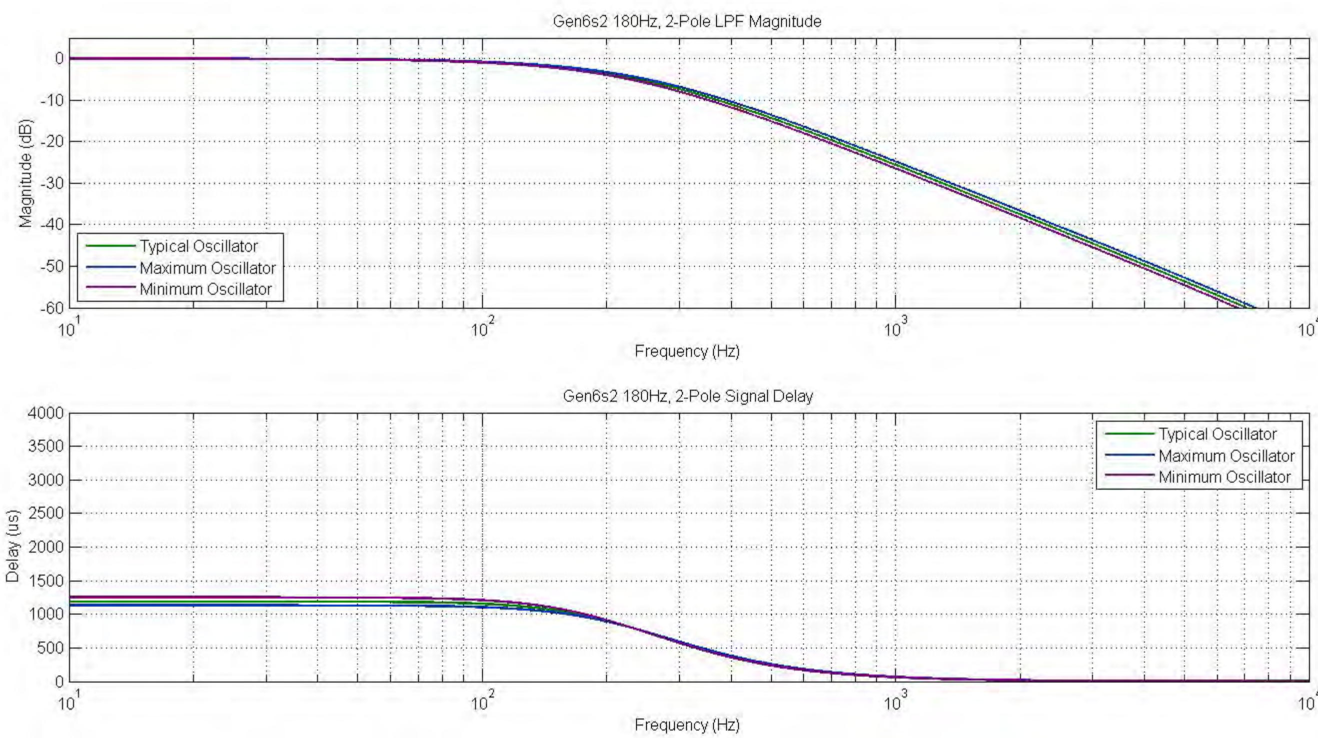


Figure 6-17 180Hz, 2-Pole Low-Pass Filter Response

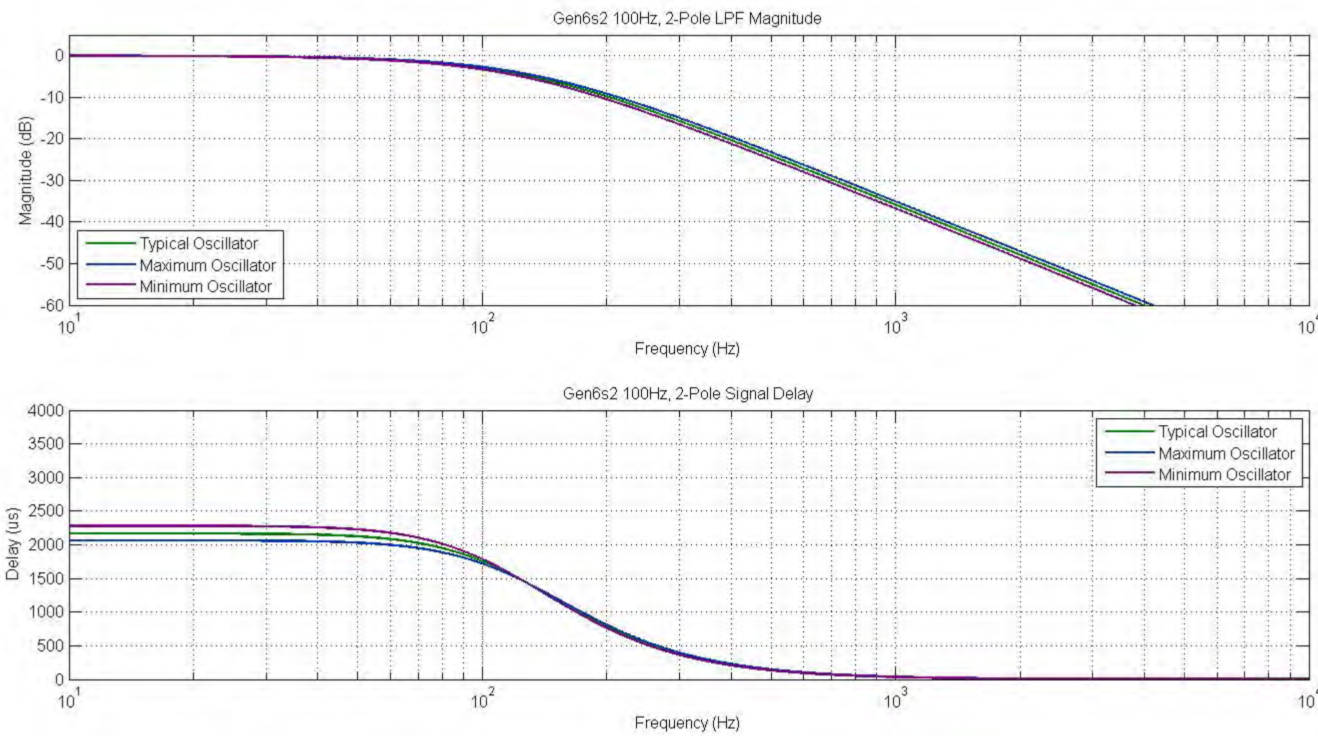


Figure 6-18 100Hz, 2-Pole Low-Pass Filter Response

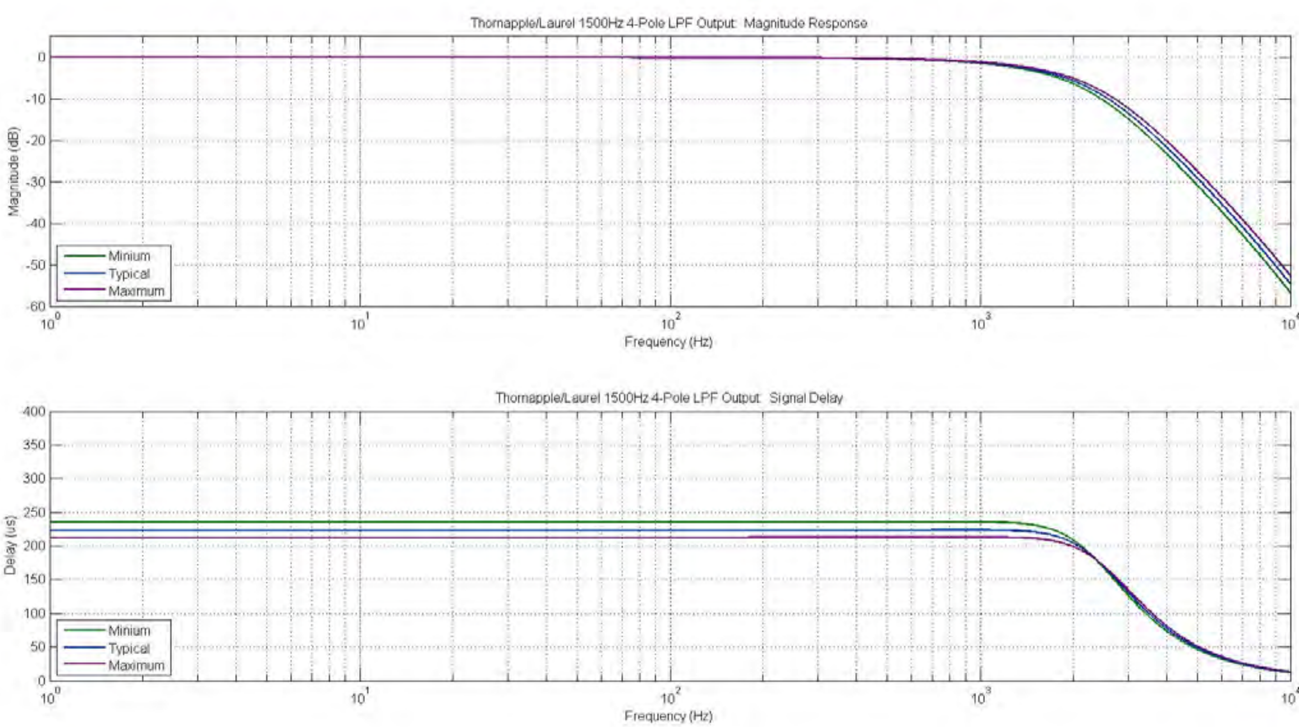


Figure 6-19 1500Hz, 4-Pole Low-Pass Filter Response

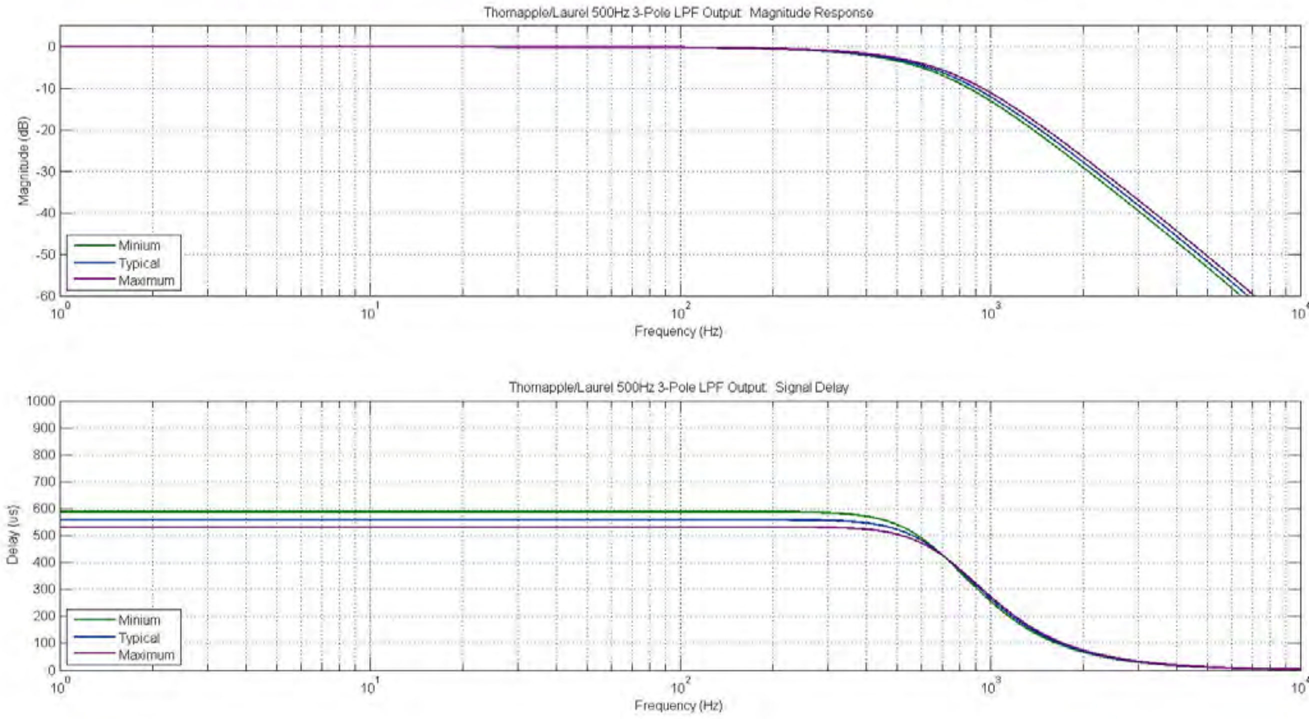


Figure 6-20 500Hz, 3-Pole Low-Pass Filter Response

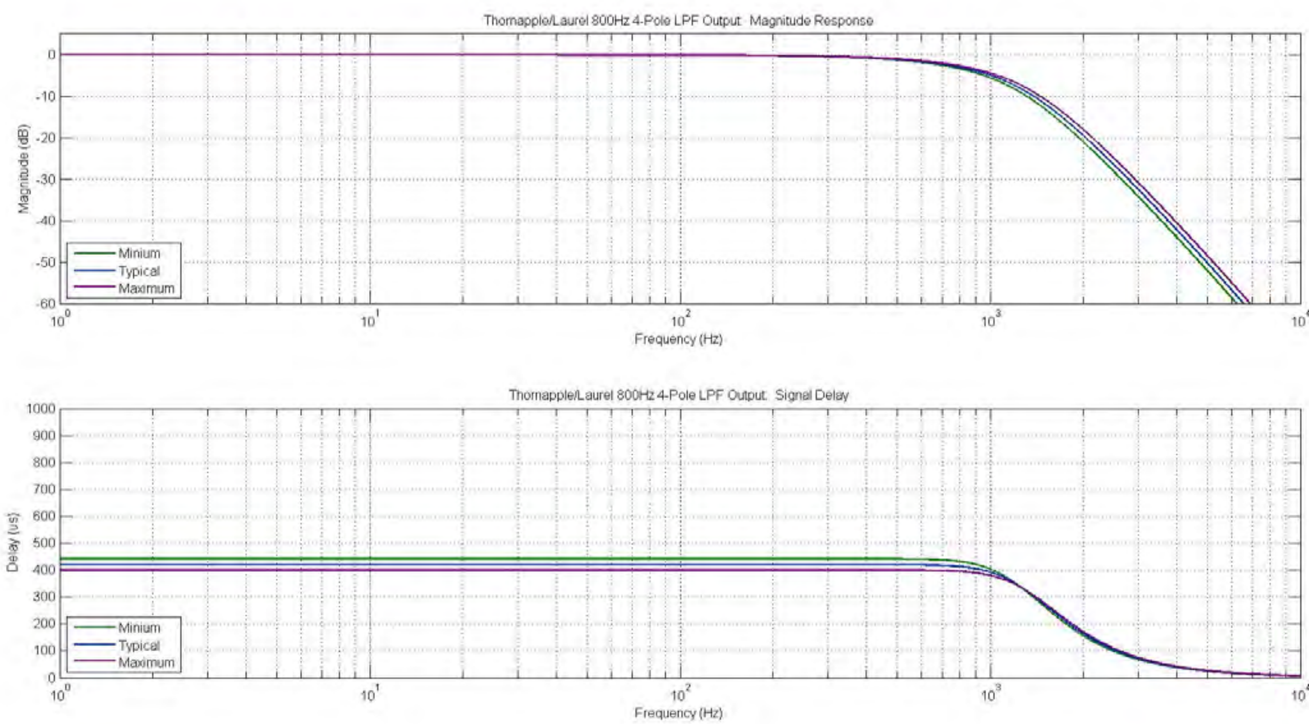


Figure 6-21 800Hz, 4-Pole Low-Pass Filter Response

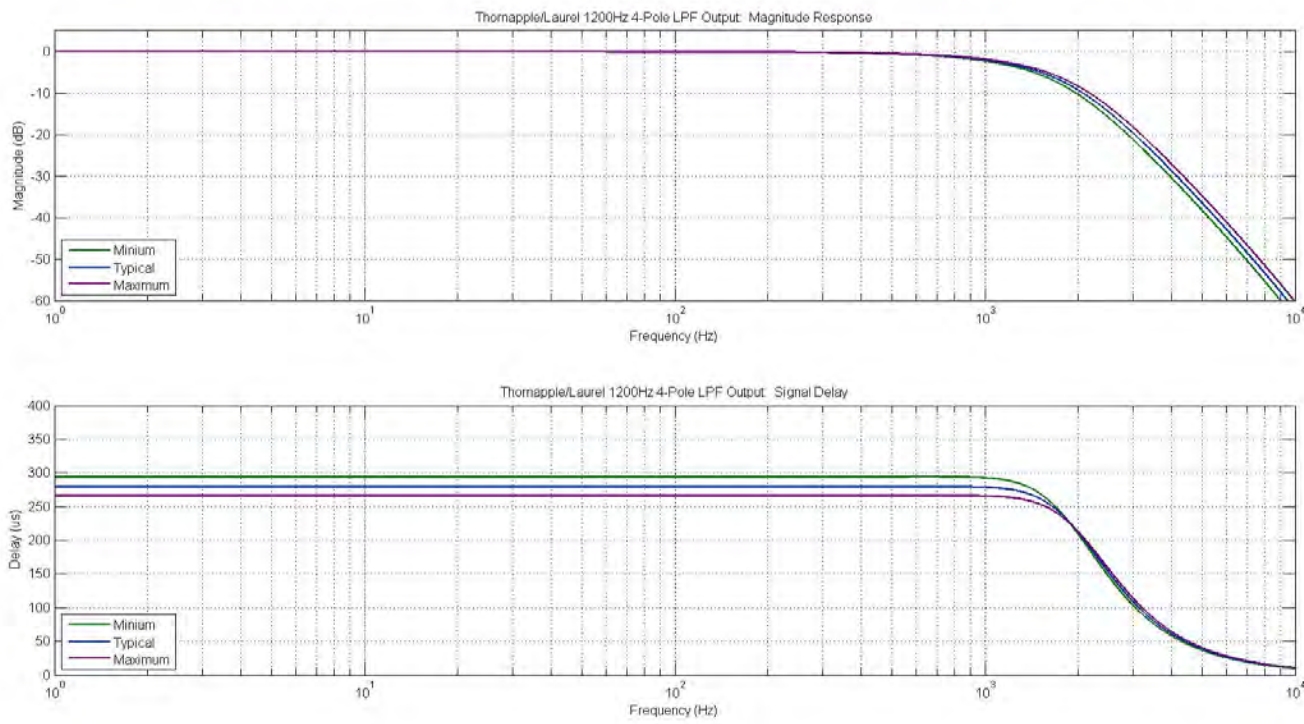


Figure 6-22 1200Hz, 4-Pole Low-Pass Filter Response

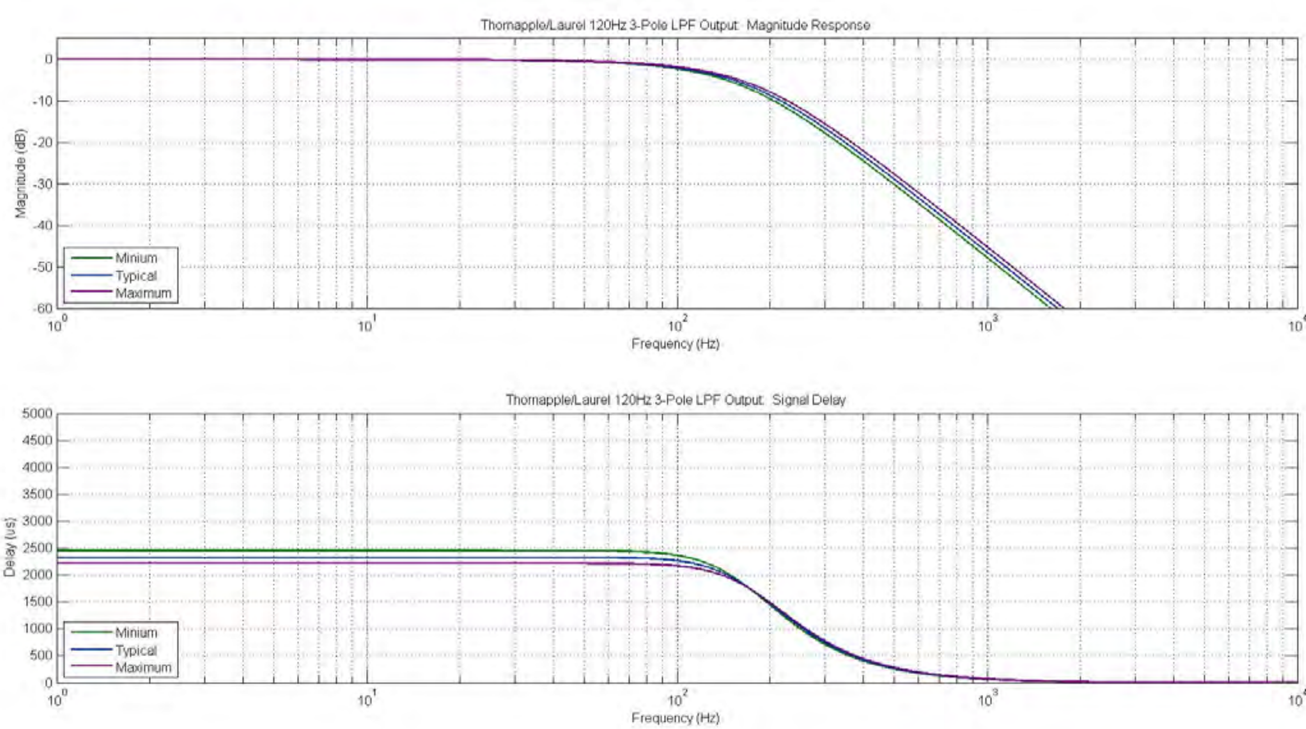


Figure 6-23 120Hz, 3-Pole Low-Pass Filter Response

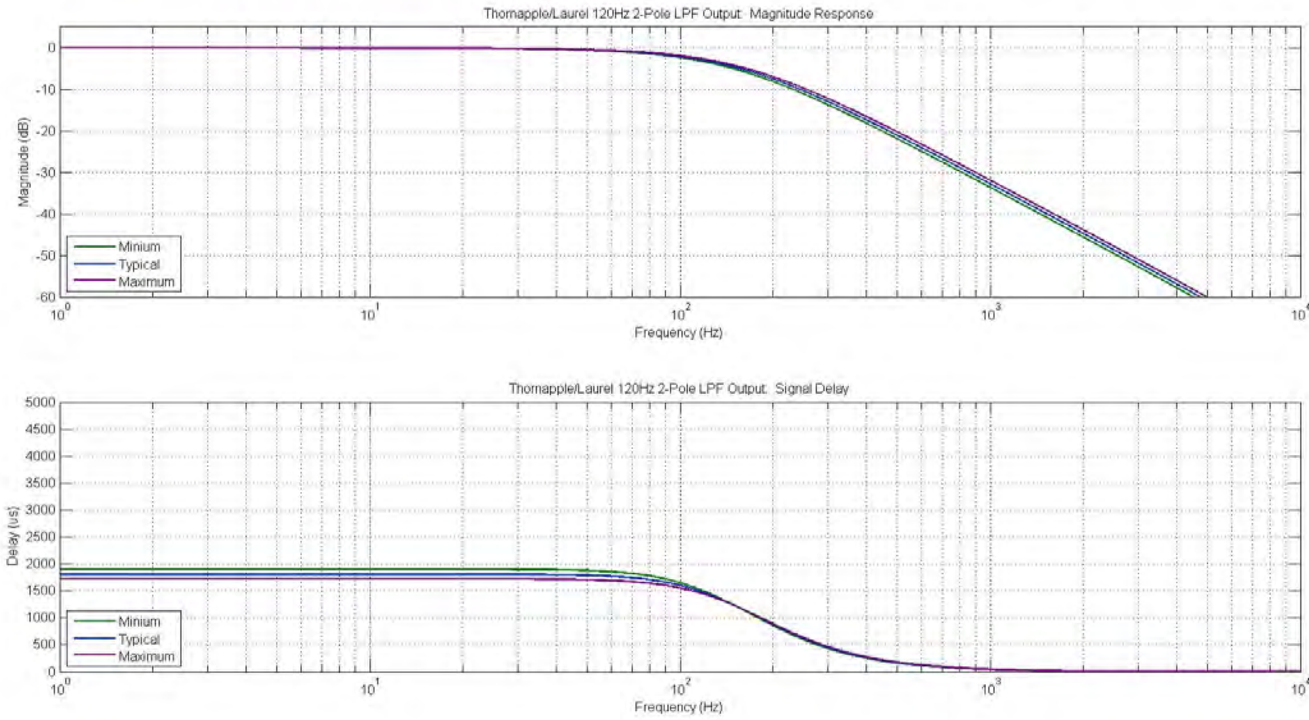


Figure 6-24 120Hz, 2-Pole Low-Pass Filter Response

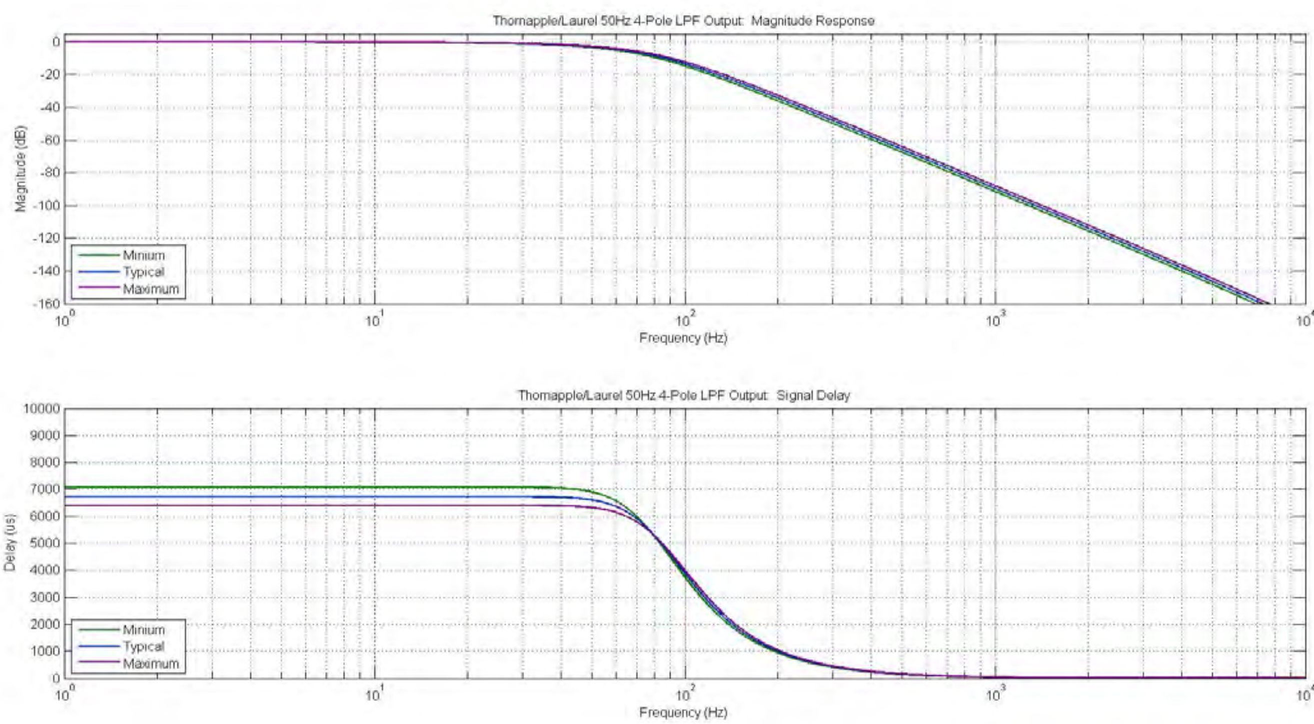


Figure 6-25 50Hz, 4-Pole Low-Pass Filter Response

6.6.4.5 User Sensitivity Scaling

The device includes a user controlled sensitivity scaling as described in Section 6.2.23.1.

6.6.4.6 Offset Cancellation

The device provides an optional offset cancellation circuit to remove internal offset error. A simplified block diagram of the offset cancellation is shown in Figure 6-26.

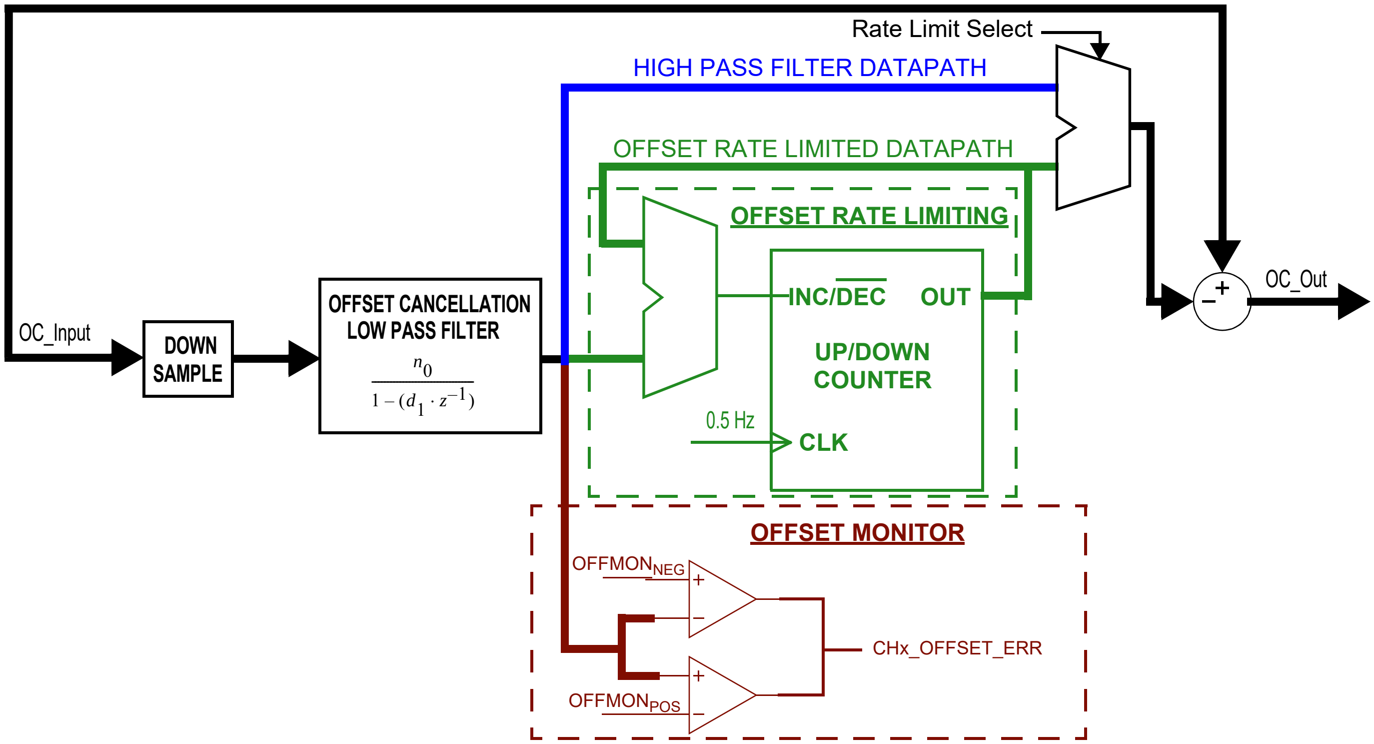


Figure 6-26 Offset Cancellation Block Diagram

The transfer function for the offset low pass filter is:

$$H(z) = a_0 \times \frac{n_0 + (n_1 \cdot z^{-1})}{d_0 + (d_1 \cdot z^{-1})}$$

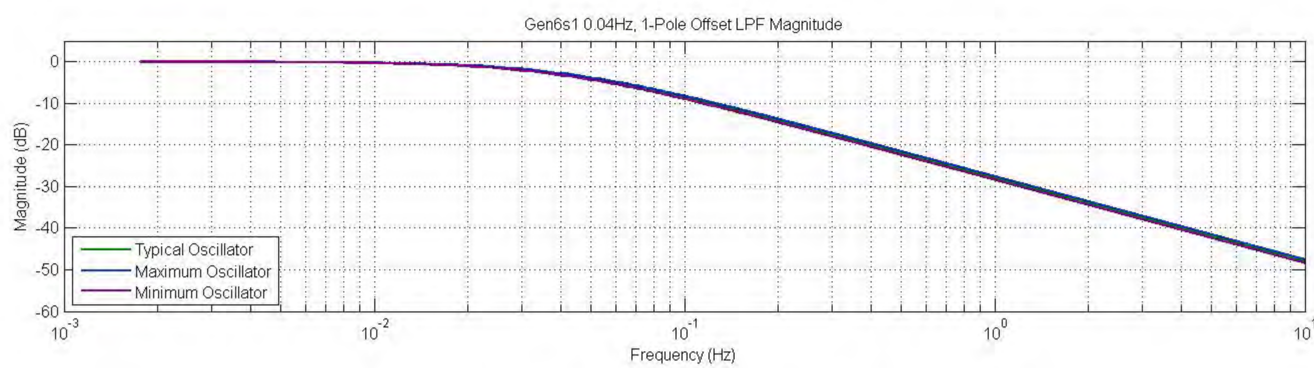
Response parameters are specified in Section 5 and the offset low pass filter coefficients are specified in the table below.

During start up multiple phases of the offset low pass filter are used to allow for fast convergence of the internal offset error during initialization. The offset rate limiting is also bypassed regardless of the state of the OC_FILT bits in the CHx_CFG_U4 register. The low pass filter details and timing for the start up phases is shown in the table below.

In normal mode, output rate limiting can be applied to the output of the offset low pass filter via the OC_FILT bits in the CHx_CFG_U4 register. If rate limiting is enabled, the offset cancellation output is updated by OFF_{Step} LSB every t_{RL_Rate} seconds.

The offset cancellation circuit output value is frozen when self test is active regardless of the offset cancellation phase.

Offset LPF Start Up Phase	Time from Reset to Start of Phase (ms)	Sample Time (us)	Coefficients (24-Bit)				LPF Corner Frequency (-3dB) (Hz)	Time Constant (τ) (ms)	Rate Limiting
0	0	256	a_0	0.234051465988159			163.8	0.9714	Bypassed
			n_0	0.49999988079071	n_1	0.49999988079071			
			d_0	1.0	d_1	-0.765948414802551			
1	4.096	256	a_0	0.063805103302002			40.96	3.886	Bypassed
			n_0	0.49999988079071	n_1	0.49999988079071			
			d_0	1.0	d_1	-0.936194777488708			
2	8.192	256	a_0	0.0163367986679077			10.24	15.54	Bypassed
			n_0	0.49999988079071	n_1	0.49999988079071			
			d_0	1.0	d_1	-0.983663082122802			
3	24.58	256	a_0	0.00410926342010498			2.560	62.17	Bypassed
			n_0	0.49999988079071	n_1	0.49999988079071			
			d_0	1.0	d_1	-0.995890617370605			
4	90.11	256	a_0	0.00102889537811279			0.6400	248.7	Bypassed
			n_0	0.49999988079071	n_1	0.49999988079071			
			d_0	1.0	d_1	-0.998970985412597			
5	352.3	256	a_0	0.000257253646850586			0.1600	994.7	Bypassed
			n_0	0.49999988079071	n_1	0.49999988079071			
			d_0	1.0	d_1	-0.999742627143859			
6	1401	256	a_0	0.0000643377478321934			0.0400	3979	Controlled by OC_FILT[1:0]
			n_0	0.49999988079071	n_1	0.49999988079071			
			d_0	1.0	d_1	-0.9999356623			
Self Test Active	Output Frozen								



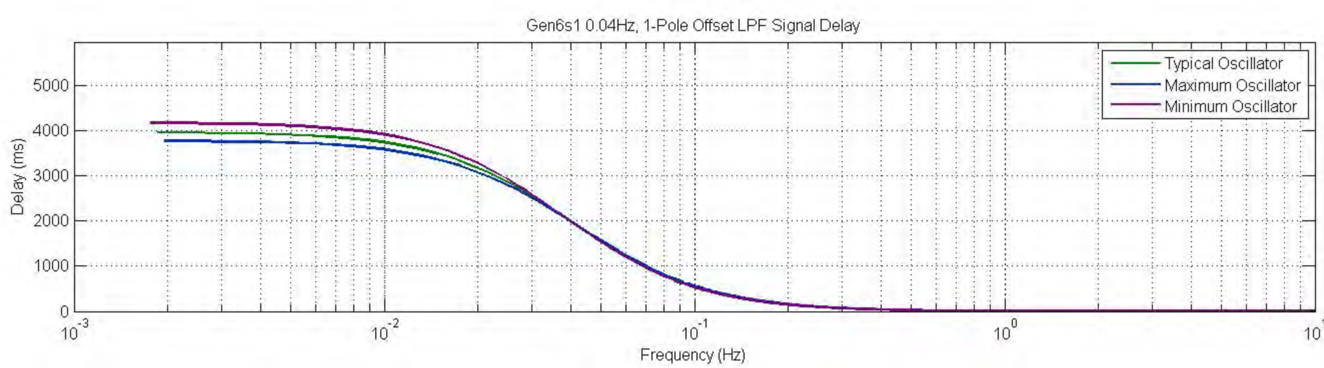


Figure 6-27 0.04Hz Offset Cancellation Low Pass Filter Characteristics

6.6.4.7 Moving Average

The device includes an optional moving average function. Reference Section 6.2.24.4 for details regarding the moving average function. If the moving average function is enabled, interpolation is disabled.

6.6.4.8 Data Interpolation

The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time. Transmitted data is interpolated from the 2 previous samples, resulting in a latency of one sample time, and a maximum signal jitter of 1/16 of the sample time. The device uses the following functions for calculating the interpolation:

$$DataInterpOut_i = DataInterpOut_{i-1} + \frac{DSPOut_{Current} - DataInterpOut_{i-1}}{16 - (i-1)}$$

$$DataInterpOut_0 = DSPOut_{Previous}$$

An example of the output interpolation is shown in Figure 6-28.

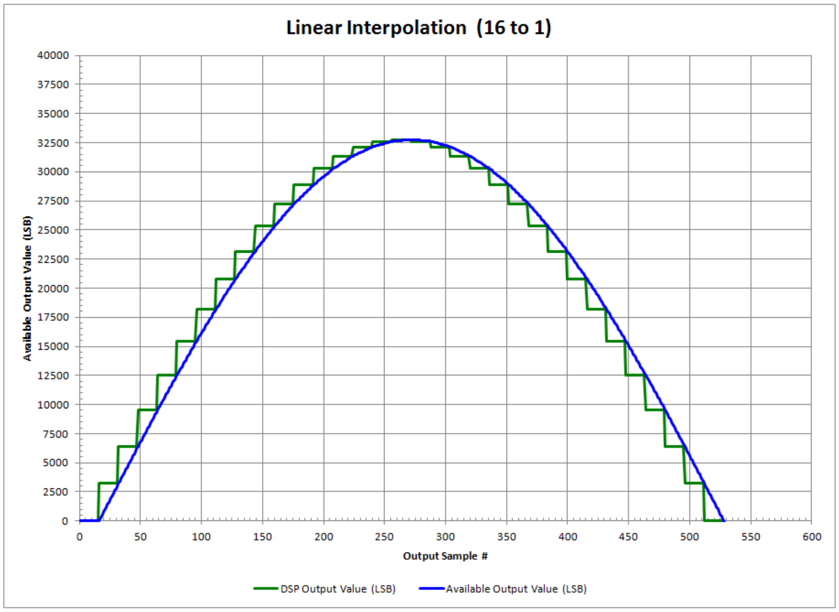


Figure 6-28 Output Interpolation Example

6.6.4.9 Output Scaling

The table below shows the output scaling for each output data type and protocol.

Data Type	PCM	SPI	DSI	PSI5	I²C	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-Bit Register Read		x	x	x	x																								
16-bit			x																										
16-bit		x		x																									
12-bit		x	x																										
10-bit	x		x	x																									

Readable Data
Noise Bits
Clipped Bits

The following equation is used to convert sensor data readings to acceleration using the variables specified in the table below. Note, the values listed apply for a user gain of 1x (U_SNS_SHIFT = ‘10’ and U_SNS_MULT = 0x00).

$$Acceleration_g = \frac{SensorData_{LSB} - SensorDataOFF_{LSB}}{SENSE_{ACCEL}}$$

Where:

$Acceleration_g$	=	The acceleration output in g
$SensorData_{LSB}$	=	The acceleration output in LSB
$SensorDataOFF_{LSB}$	=	The acceleration output value at 0g in LSB
$SENSE_{ACCEL}$	=	The expected sensitivity in LSB/g

g Range Type	Data Reading	Typical $SensorDataOFF_{LSB}$ (LSB)	$SENSE_{ACCEL}$ (LSB/g)	Minimum Sensor Data Value (Signed LSB)	Maximum Sensor Data Value (Signed LSB)
Medium g	16-Bit Register Read	0	66.0322	0x8000 (-32768)	0x7FFF (+32767)
	16-Bit DSI3 PDCM Data	0	66.0322	0x8001 (-32767)	0x7FFF (+32767)
	16-Bit SPI Sensor Data	0	528.258	0x8010 (-32752)	0x7FFF (+32767)
	16-Bit PSI5 Sensor Data	0	528.258	0x8800 (-30720)	0x7800 (+30720)
	12-Bit DSI3 PDCM Data	0	33.0161	0x801 (-2047)	0x7FF (+2047)
	12-Bit SPI Sensor Data	0	33.0161	0x801 (-2047)	0x7FF (+2047)
	10-Bit DSI3 PDCM Data	0	8.25403	0x201 (-511)	0x1FF (+511)
	10-Bit PSI5 Sensor Data	0	8.25403	0x220 (-480)	0x1E0 (+480)
High g	16-Bit Register Read	0	21.8930	0x8000 (-32768)	0x7FFF (+32767)
	16-Bit DSI3 PDCM Data	0	21.8930	0x8001 (-32767)	0x7FFF (+32767)
	16-Bit SPI Sensor Data	0	175.144	0x8010 (-32752)	0x7FFF (+32767)
	16-Bit PSI5 Sensor Data	0	175.144	0x8800 (-30720)	0x7800 (+30720)
	12-Bit DSI3 PDCM Data	0	10.9465	0x801 (-2047)	0x7FF (+2047)
	12-Bit SPI Sensor Data	0	10.9465	0x801 (-2047)	0x7FF (+2047)
	10-Bit DSI3 PDCM Data	0	2.73663	0x201 (-511)	0x1FF (+511)
	10-Bit PSI5 Sensor Data	0	2.73663	0x220 (-480)	0x1E0 (+480)

6.7 Temperature Sensor

6.7.1 Temperature Sensor Signal Chain

The device includes an independent temperature sensor for each channel for signal compensation. The output of the channel 0 temperature sensor is provided for user readability. A simplified block diagram is shown in Figure 6-29. Temperature sensor parameters are specified in Section 5.5 and Section 5.18.

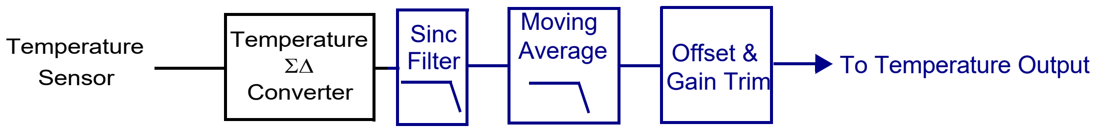


Figure 6-29 Temperature Sensor Signal Chain Block Diagram

6.7.2 Temperature Sensor Output Scaling Equations

The following equation is used to convert temperature readings with the variables as specified in the table below:

$$T_{DEGC} = \frac{T_{LSB} - T0_{LSB}}{T_{SENSE}}$$

Where:

T_{DEGC} = The temperature output in degrees C
T_{LSB} = The temperature output in LSB
$T0_{LSB}$ = The expected temperature output in LSB at 0 C
T_{SENSE} = The expected temperature sensitivity in LSB/C

Data Reading	$T0_{LSB}$ (LSB)	T_{SENSE} (LSB/C)
8-Bit Register Read	68	1
16-Bit Register Read	17408	256
16-Bit DSI3 PDCM Data	17408	256
16-Bit SPI Sensor Data	17408	256
12-Bit DSI3 PDCM Data	1100	16
12-Bit SPI Sensor Data	1100	16
10-Bit DSI3 PDCM Data	276	4
10-Bit PSI5 Data	-27	1

6.8 PCM Output Function

The device provides the option for a PCM output function. The PCM output is enabled if the ARM_CFG bits in the CHx_CFG_U4 registers are configured for PCM output. Selecting the PCM output enables the following functions:

- The non-interpolated sensor data output as defined in the DATATYPE0 bits in the Chx_CFG_U3 register is saturated to 10-bits as shown in Section 6.6.4.9 and converted to an unsigned value.
- The 10-bit sensor value is input into a summer clocked at 10MHz.
- The carry from the summer circuit is output to the PCM pin.

A block diagram of the PCM output is shown in Figure 6-30.

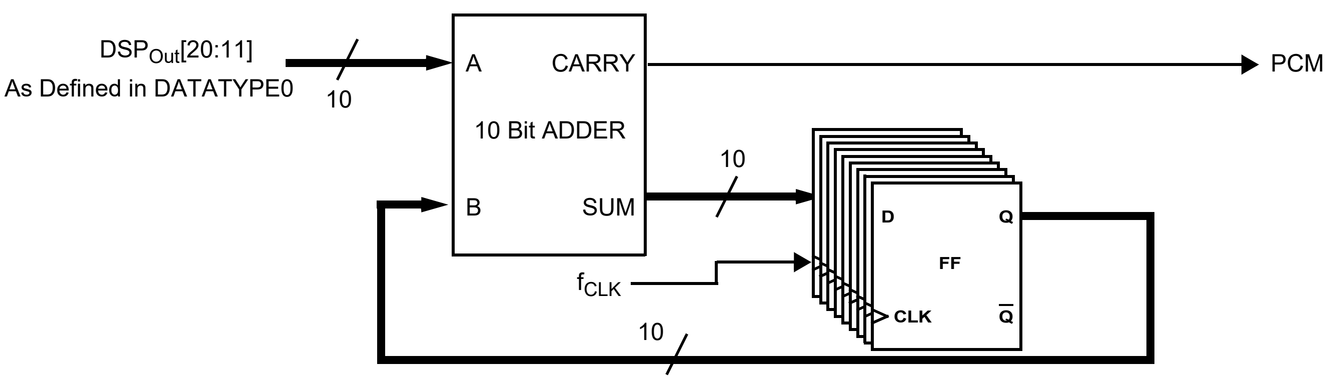


Figure 6-30 PCM Output Function Block Diagram

6.9 Arming Function

When SPI mode is enabled via the COMMTYPE register, the device provides the option for an arming function with 3 modes of operation. The operation of the arming function is selected by the state of the ARM_CFG bits in the CHx_CFG_U4 registers.

Reference Section 9.4 for the operation of the Arming function with exception conditions. Error conditions do not impact prior arming function responses. If an error occurs after an arming activation, the corresponding pulse stretch for the existing arming condition will continue. However, new sensor reads will not update the arming function regardless of the sensor value.

6.9.1 Arming Function: Moving Average Mode

In moving average mode, the arming function runs a moving average on the offset cancelled output of the associated sensor channel DATATYPE0. The number of samples used for the moving average (k) is programmable via the ARM_WS[1:0] bits in the CHx_ARM_CFG registers. Reference Section 6.2.27.3 for register details.

$$ARM\_MA_n = (OC_n + OC_{n-1} + ... + OC_{n+1-k})/k$$

Where n is the current sample

The sample rate for each channel is determined by the rate of the SPI sensor data requests. At the falling edge of SS_B for a sensor data SPI response for SOURCEID_0 (channel 0) or SOURCEID_2 (channel 1), the moving average for the associated channel is updated with a new sample. Reference Figure 6-31. The arming function input data rate can be down sampled as described in Section 6.9.4. The SPI sensor data sample rate must meet the minimum time between requests ($t_{ACC\_REQ\_x}$) specified in Section 5.13.

The moving average output is compared against positive and negative thresholds that are individually programmed for each channel via the CHx_ARMT_x registers. Reference Section 6.2.28 for register details. If the moving average equals or exceeds either threshold, an arming condition is indicated, the arming pin output is asserted for the associated channel and the pulse stretch counter is set as described in Section 6.9.5.

The arming pin output is de-asserted only when the pulse stretch counter expires. Figure 6-33 shows the arming output operation for different SPI conditions.

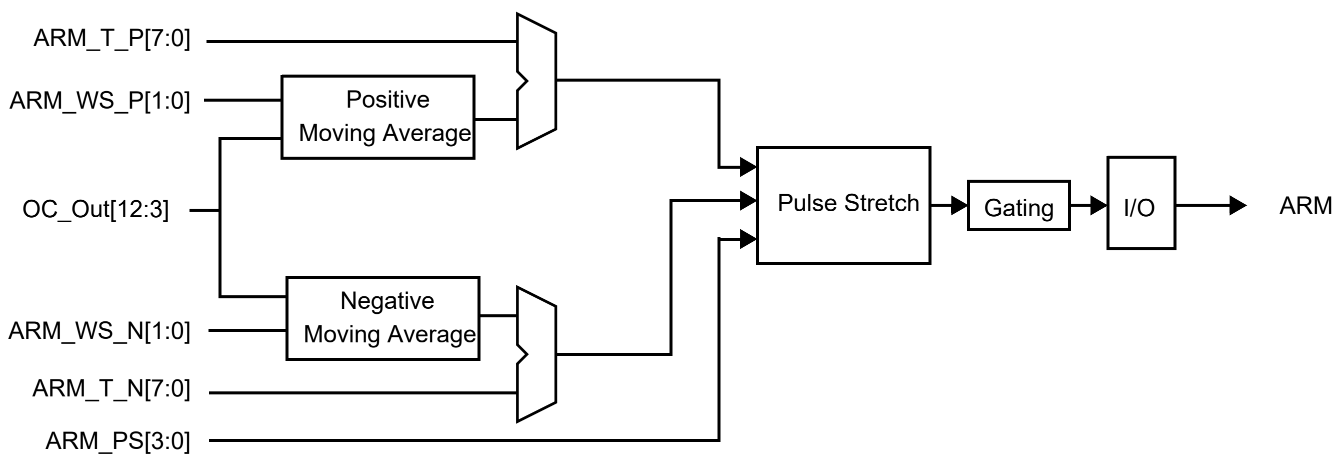


Figure 6-31 Arming Function Block Diagram - Moving Average Mode

6.9.2 Arming Function: Count Mode

In count mode, the arming function compares each offset cancelled sample against positive and negative thresholds that are individually programmed for each channel via the CHx_ARMT_x_x and CHx_ARMT_x_x registers. Reference Section 6.2.28 for register details. If the sample equals or exceeds either threshold, a sample counter is incremented. If the sample does not exceed either threshold, the sample counter is reset to zero.

The sample rate for each channel is determined by the SPI sensor data sample rate. At the falling edge of SS_B for a sensor data SPI response for SOURCEID_0 (channel 0) or SOURCEID_2 (channel 1), a new sample for the associated channel is compared against the thresholds. Reference Figure 6-32. The arming function input data rate can be down sampled as described in Section 6.9.4. The SPI sensor data sample rate must meet the minimum time between requests ($t_{ACC\_REQ\_x}$) specified in Section 5.13.

A sample count limit is programmable via the ARM_WS[1:0] bits in the CHx_ARM_CFG registers. If the sample count reaches the programmable sample count limit, an arming condition is indicated, the associated arm pin output is asserted and the pulse stretch counter is set as described in Section 6.9.5.

The associated arm pin output is de-asserted only when the pulse stretch counter expires. Figure 6-33 shows the arming output operation for different SPI conditions.

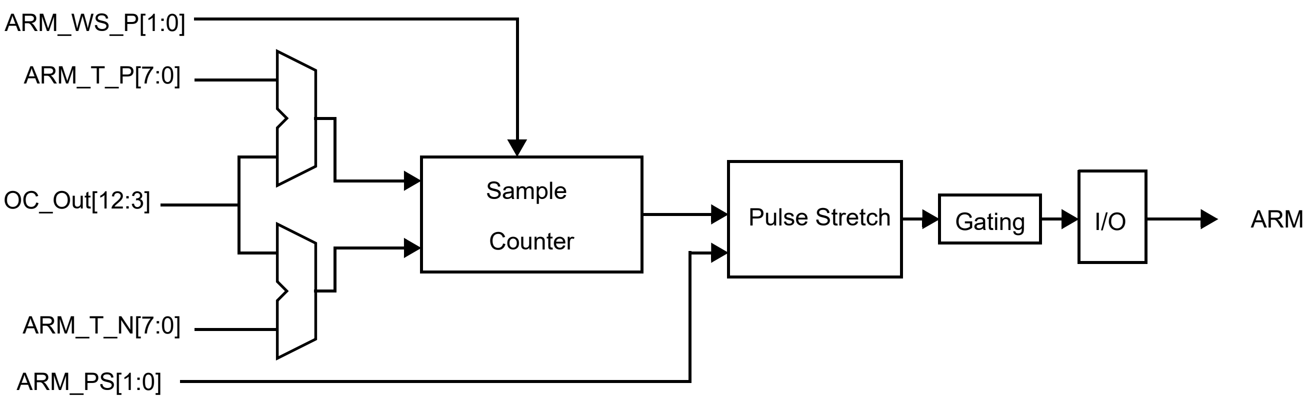


Figure 6-32 Arming Function Block Diagram - Count Mode

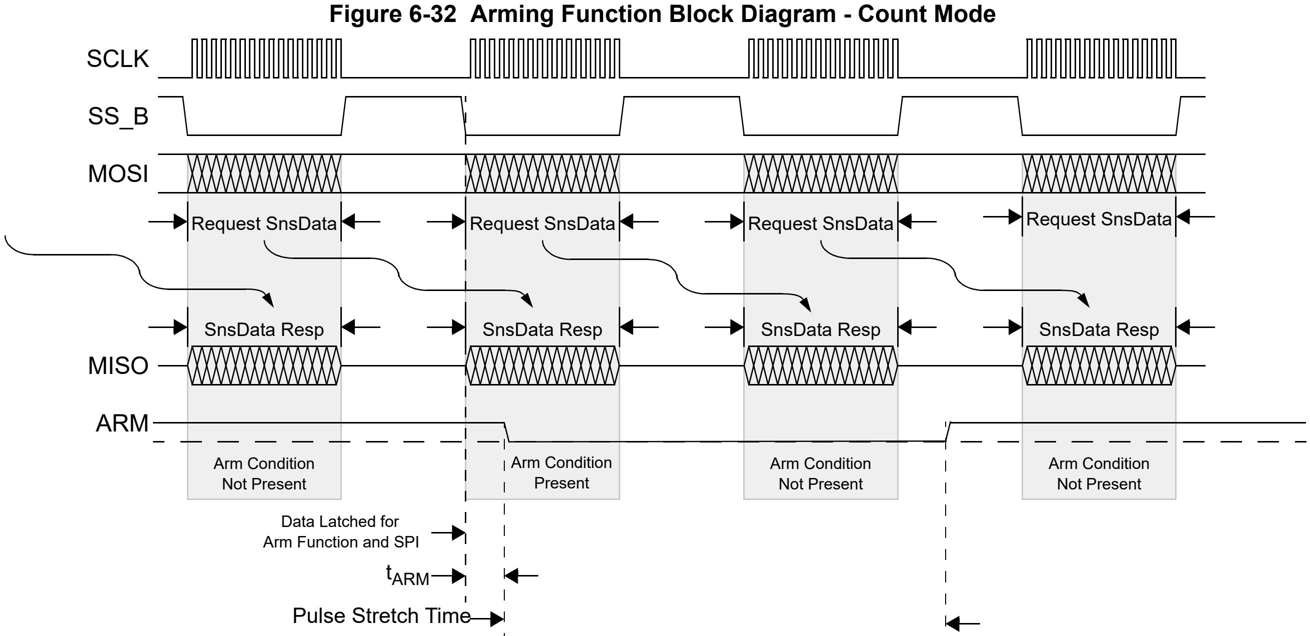


Figure 6-33 Arming Condition, Moving Average and Count Mode

6.9.3 Arming Function: Unfiltered Mode

At the falling edge of SS_B for a sensor data SPI response for SOURCEID_0 (channel 0) or SOURCEID_2 (channel 1), the most recent available offset cancelled sample for the requested channel is compared against positive and negative thresholds that are individually programmed for each channel via the CHx_ARM_T_x and CHx_ARM_T_x registers. Reference Section 6.2.28 for register details. If the sample equals or exceeds either threshold, an arming condition is indicated.

Once an arming condition is indicated for the associated channel, the arm pin output for that channel is asserted when SS_B is asserted and the MISO data includes a sensor data response for that channel. The pulse stretch function is not applied in Unfiltered mode.

Figure 6-34 contain a block diagram of the Arming Function operation in Unfiltered Mode. Figure 6-35 shows the Arming output operation under the different SPI request conditions.

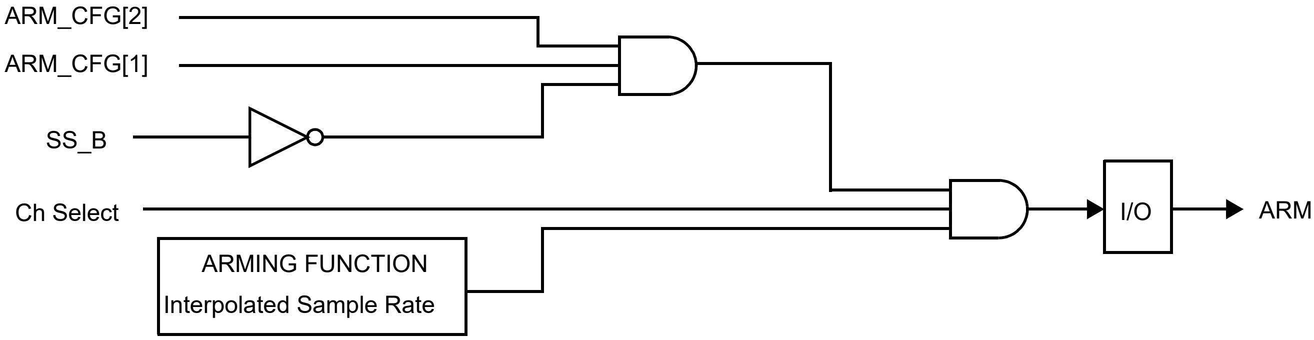


Figure 6-34 Arming Function Block Diagram - Unfiltered Mode

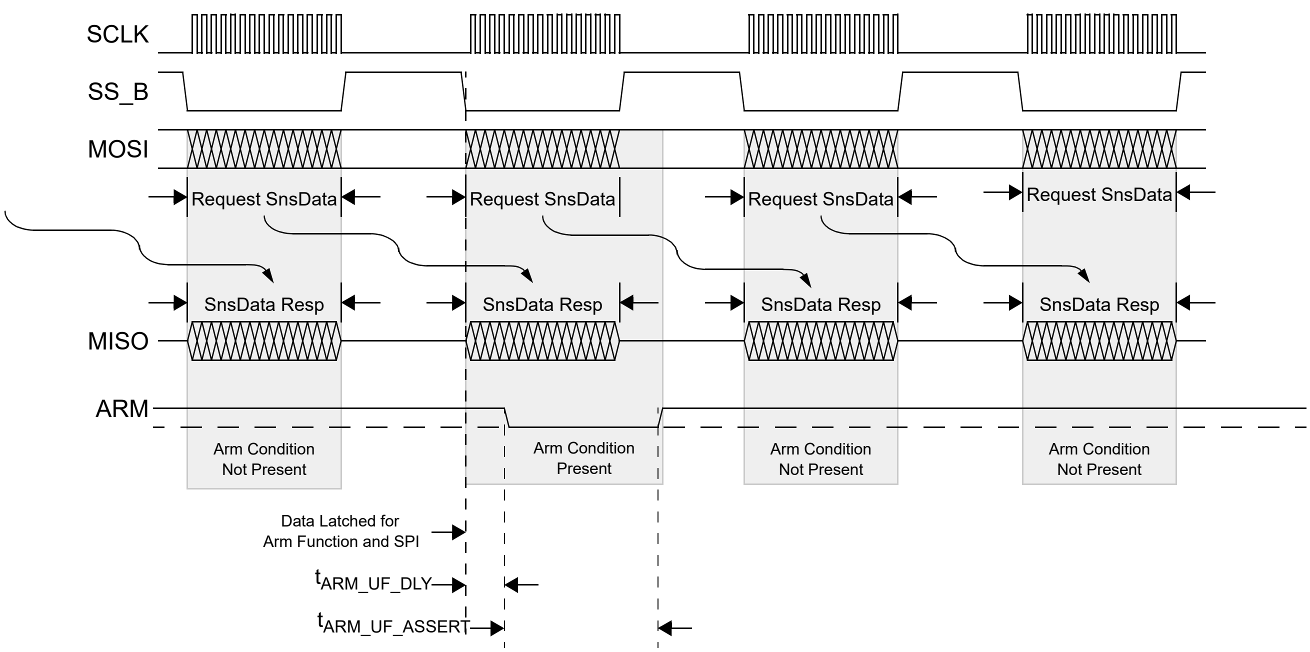


Figure 6-35 Arming Condition, Unfiltered Mode

6.9.4 Arming Function Down Sampling

The data provided to the arming function can be down sampled using the ARM_DS[1:0] bits in the CHx_ARM_CFG registers.

The initial value of the counter is '00'. At the falling edge of SS_B for a sensor data SPI response, if the counter value is equal to '00', the arming function is updated with the new sample as described in Section 6.9.1 or Section 6.9.2. The counter is then incremented by '1'. The counter rolls over to '00' after the maximum value specified in the ARM_DS[1:0] bits is reached.

6.9.5 Arming Pulse Stretch Function

A pulse stretch function can be applied to the arming outputs in moving average mode, or count mode.

If the pulse stretch function is not used (ARM_PS[1:0] = '00'), the arming output is asserted if and only if an arming condition exists for the associated channel after the most recent evaluated sample. The arming output is de-asserted if and only if an arming condition does not exist for the associated channel after the most recent evaluated sample.

If the pulse stretch function is used, (ARM_PS[1:0] not equal '00'), the arming output is controlled only by the value of the pulse stretch timer value. If the pulse stretch timer value is non-zero, the arming output is asserted. If the pulse stretch timer is zero, the arming output is de-asserted. The pulse stretch counter continuously decrements until it reaches zero. The pulse stretch counter is reset to the programmed pulse stretch value if and only if an arming condition exists for the associated channel after the most recent evaluated sample. Reference Figure 6-33.

Exception conditions listed in Section 9.5 do not impact prior arming function responses. If an exception occurs after an arming activation, the corresponding pulse stretch for the existing arming condition will continue. However, new sensor reads will not reset the pulse stretch counter regardless of the sensor value.

6.9.6 Arming Pin Output Structure

The arming output pin structure can be set to active high, or active low with the ARM_CFG bits in the CHx_CFG_U4 registers as described in Section 6.2.25.3. The active high and active low pin output structures are shown in Figure 6-36.

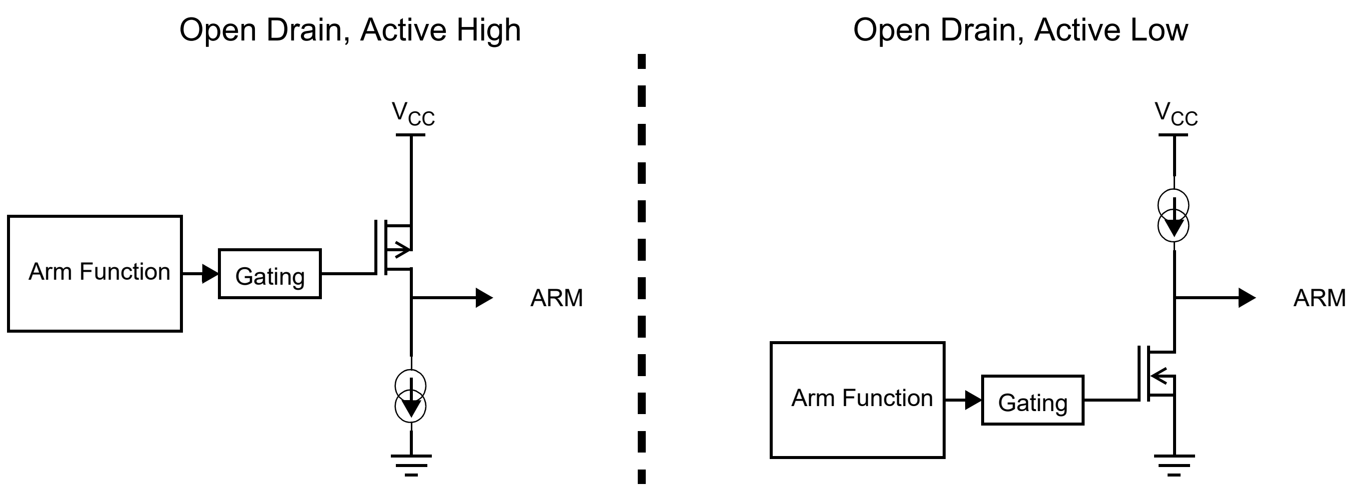


Figure 6-36 Arming Function - Pin Output Structure

SECTION 7 DSI3 PROTOCOL

The DSI3 standard describes two function classes: Signal Function Class and Power Function Class. The device is a slave conforming to the Signal Function Class requirements. The device does not support Power Function Class. The following sections describe the DSI3 Signal Function Class features supported by the device.

7.1 DSI3 Physical Layer

7.1.1 Command Receiver

The command receive block converts voltage transitions on the BUS_I pin to a digital pulse train for decoding by the DSI data link layer.

The supply voltage can vary throughout the specified range, so the communication high voltage (V_{HIGH}) must be sampled and averaged with a low pass filter. The communication low voltage is then determined by comparing the supply voltage to the sampled and averaged V_{HIGH} voltage. Figure 7-1 shows a block diagram of the command receiver physical layer.

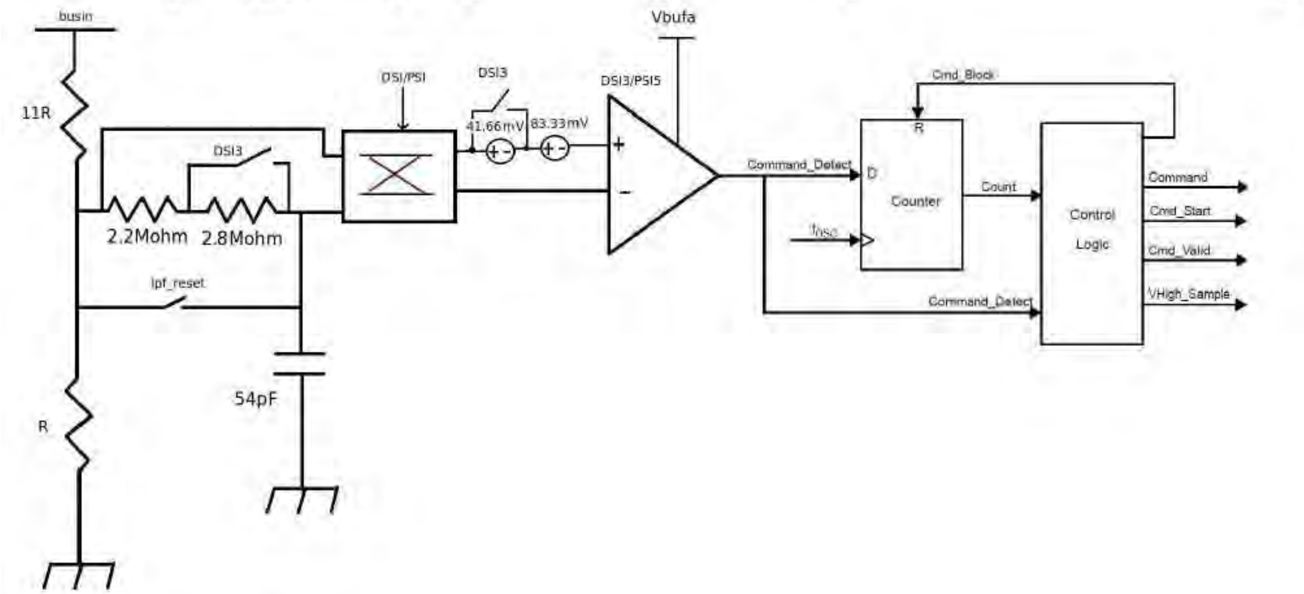


Figure 7-1 Command Receiver Physical Layer

The start of a command is detected when the comparator output (Command_Detect) is low. The comparator output is input to a counter that is updated at the internal oscillator frequency. Control logic monitors the counter output and generates the necessary internal signals for the logic.

Figure 7-2 shows a timing diagram of the command receiver when a valid command is received, and Figure 7-3 shows a timing diagram of the command receiver when a micro-cut is received during the command window. Voltage values and timing parameters are specified in Section 5.4 and Section 5.20.

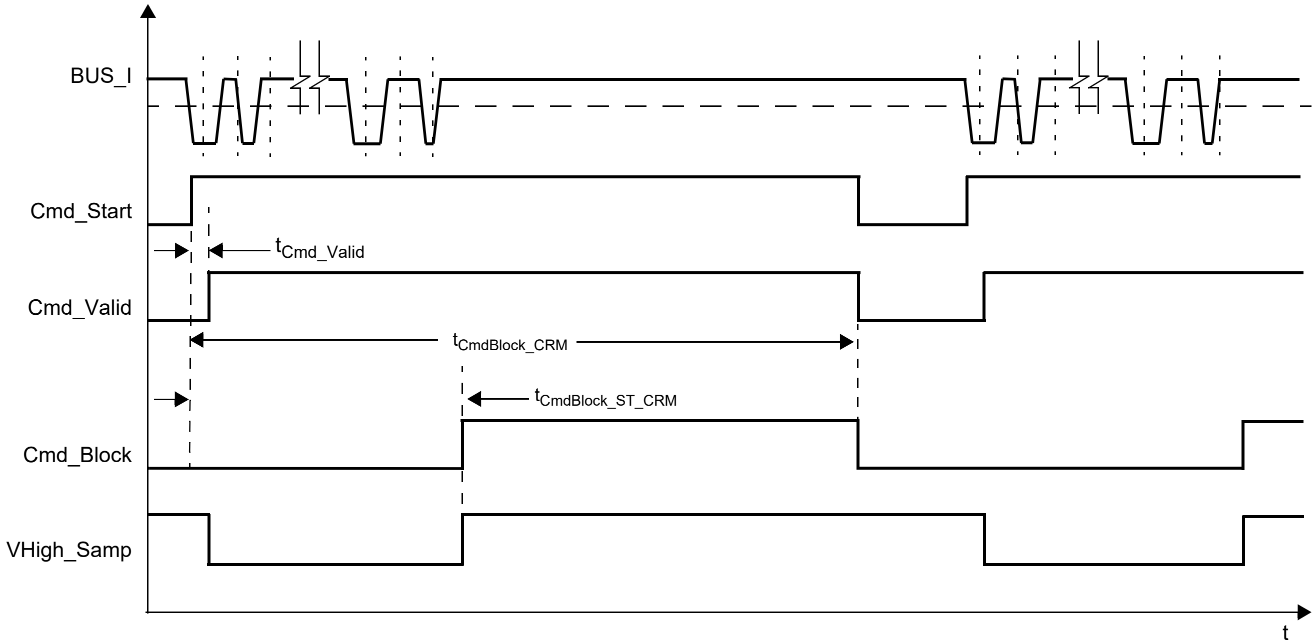


Figure 7-2 DSI3 Command Receiver Timing Diagram: Valid Command

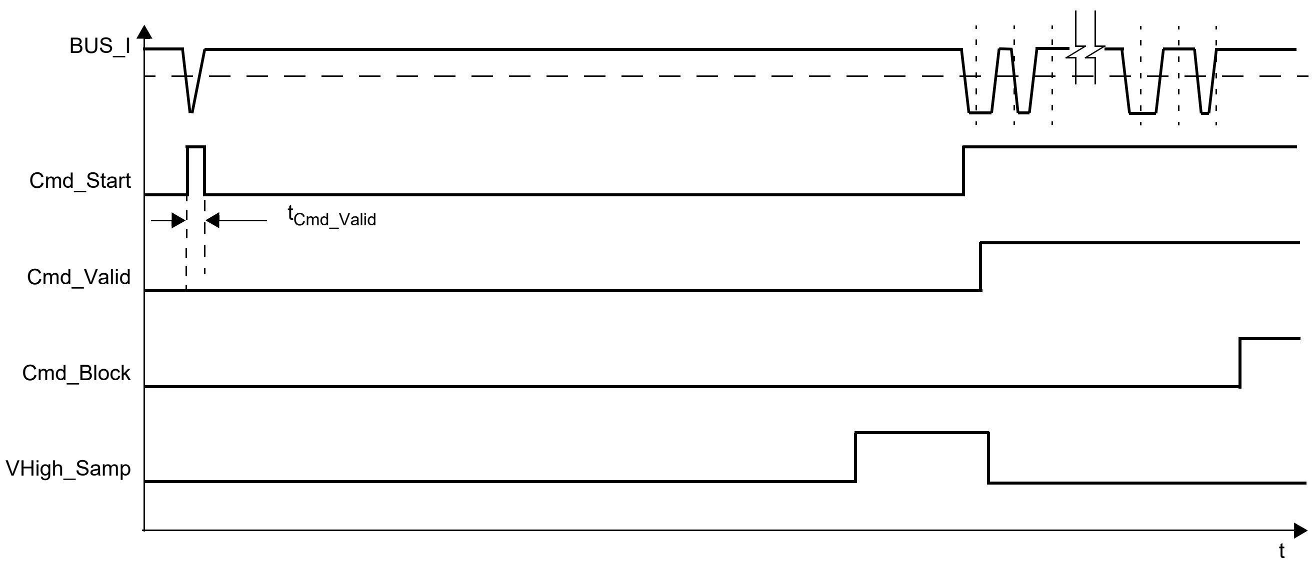


Figure 7-3 DSI3 Command Receiver Timing Diagram: Micro-cut

7.1.2 Response Transmitter

The response transmitter block converts two digital signals into two supply modulation current. The response currents are generated such that the rise and fall times are the same whether the I_{RESP} current is being transmitted or the 2 x I_{RESP} current is being transmitted. A diagram of the response transmitter is shown in Figure 7-2. Current values and timing parameters are specified in Section 5.4 and Section 5.11.

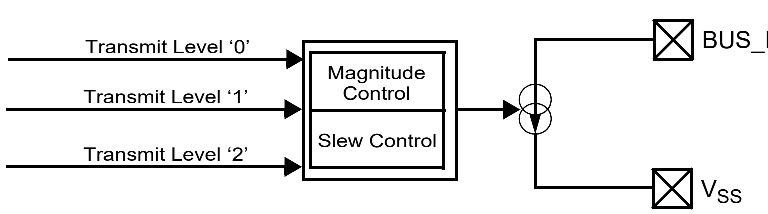


Figure 7-4 DSI3 Transmitter Block Diagram

7.1.3 Discovery Mode Current Sense

The current sense circuit is used during Discovery Mode to determine if any additional slaves are connected to the BUS_O pin of the device. A diagram of the current sense circuit is shown in Figure 7-5. Current values and timing parameters are specified in Section 5.4 and Section 5.11. Details regarding Discovery Mode are included in Section 7.2.3.

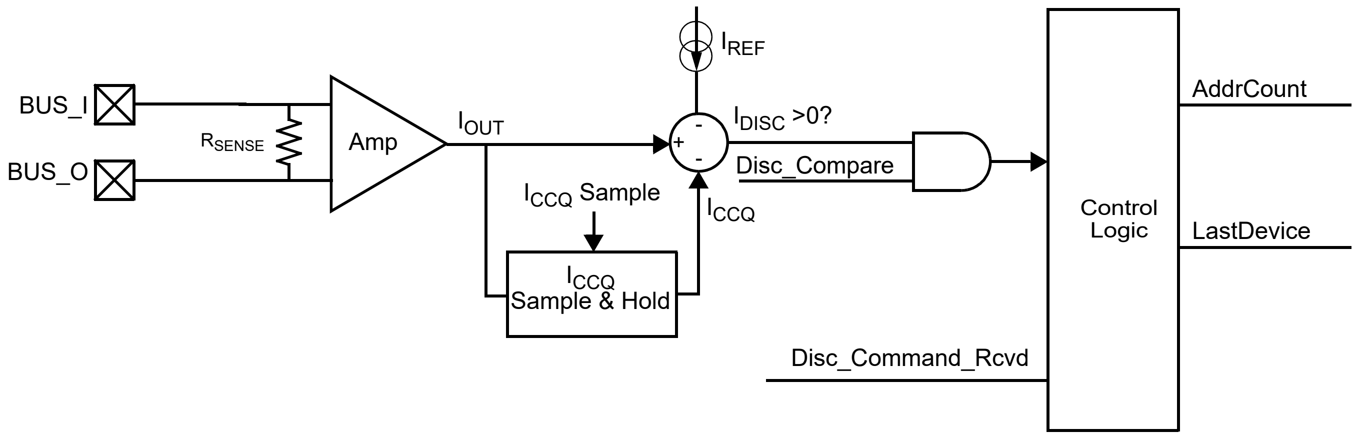


Figure 7-5 Discovery Mode Current Sense Circuit Block Diagram

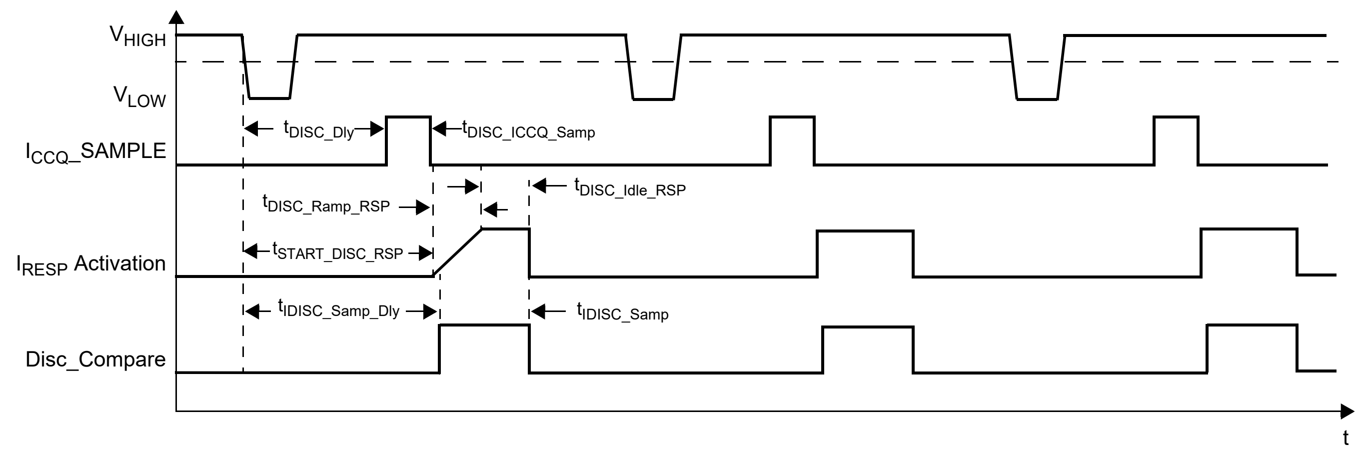


Figure 7-6 DSI3 Discovery Mode Sensing Timing Diagram

7.2 Address Assignment

The device supports all 3 address assignment methods described in the DSI3 standard as described below.

7.2.1 Address Assignment Method for Parallel Connected Slaves

Devices connected in parallel must have pre-programmed addresses by storing a non-zero value into the PADDR[3:0] bits of the PHYSADDR OTP register. If a non-zero value is stored in this OTP register, The device does not participate in any other address assignment method and waits for Command and Response Mode for further configuration. Reference Section 7.3 for details regarding Command and Response Mode.

7.2.2 Address Assignment Method for Bus Switch Connected Daisy Chain Devices

A device connected in daisy chain by a bus switch may have either a pre-programmed address as described in Section 7.2.1, or an un-programmed address.

If the address is pre-programmed, the device does not participate in any other address assignment method and waits for Command and Response Mode for further configuration information, including activating the bus switch to connect the next device on the bus. Reference Section 7.3 for details regarding Command and Response Mode.

If the address is un-programmed, once power is applied, the device is the only device on the segment which requires an address assignment. The device will accept a Command and Response Mode register write command addressed to Address $0 (global command), which writes the PADDR[3:0] bits to a non-zero value. Once a physical address is assigned to the device, Command and Response Mode is used with the assigned physical address for further configuration.

On power up, the device bus switch output defaults to de-activated.

7.2.3 DSI3 Discovery Mode: Address Assignment Method for Resistor Connected Daisy Chain Devices

A device connected in daisy chain via a resistor has an un-programmed address and uses Discovery Mode to obtain its physical address (PADDR[3:0]).

The Master device must initiate Discovery Mode automatically after power is applied to the bus segment by sending a sequence of Discovery Commands. Discovery mode timing is defined in Section 5.11. If the ENDINIT bit is not set and the PADDR[3:0] field is set to ‘0000’, the device will detect a Discovery Command t_{START_DISC} after a power on reset and for intervals of t_{PER_Disc} until Discovery Mode has ended (the maximum value of t_{START_DISC}).

Discovery Mode follows the sequence listed below. Figure 7-7 shows a timing diagram of the Discover Protocol for a 4 device segment.

1. The master powers up the bus segment to a known state.
2. The Master transmits the Discovery Command.
3. After a predetermined delay ($t_{START\_DISC\_RSP}$), all devices without a physical address activate a current ramp to the 2x response current at a ramp rate of i_{DISC_RAMP}.
4. Each device monitors the current through its sense resistor (Δi_{SENSE}).
   a. If the current is above i_{RESP}, the device disables its response current, increments its physical address counter and waits for the next Discovery Command.
   b. If the current is low (Δi_{SENSE} less than i_{RESP}), the device continues to ramp its response current to 2* i_{RESP} in time $t_{DISC\_RAMP\_RSP}$ and maintains the current at 2* i_{RESP} for time $t_{DISC\_IDLE\_RSP}$.
   c. After time $t_{DISC\_IDLE\_RSP}$, if a device has not detected a current through its current sense resistor of i_{RESP}, the device accepts physical address '1' and disables its response current.
5. After a pre-defined period (t_{PER_DISC}), the master transmits another Discovery Command.
6. Steps 3 and 4 are repeated, with the device accepting the address in its address assignment counter if the sense current is low.
7. The Master repeats step 5 until it has transmitted Discovery Commands for all the devices it expects on the bus.
8. Device initialization can now begin using Command and Response Mode.

Once the Discovery Mode is complete, a physical address is assigned to the device, and Command and Response Mode is used with the assigned physical address for further configuration.

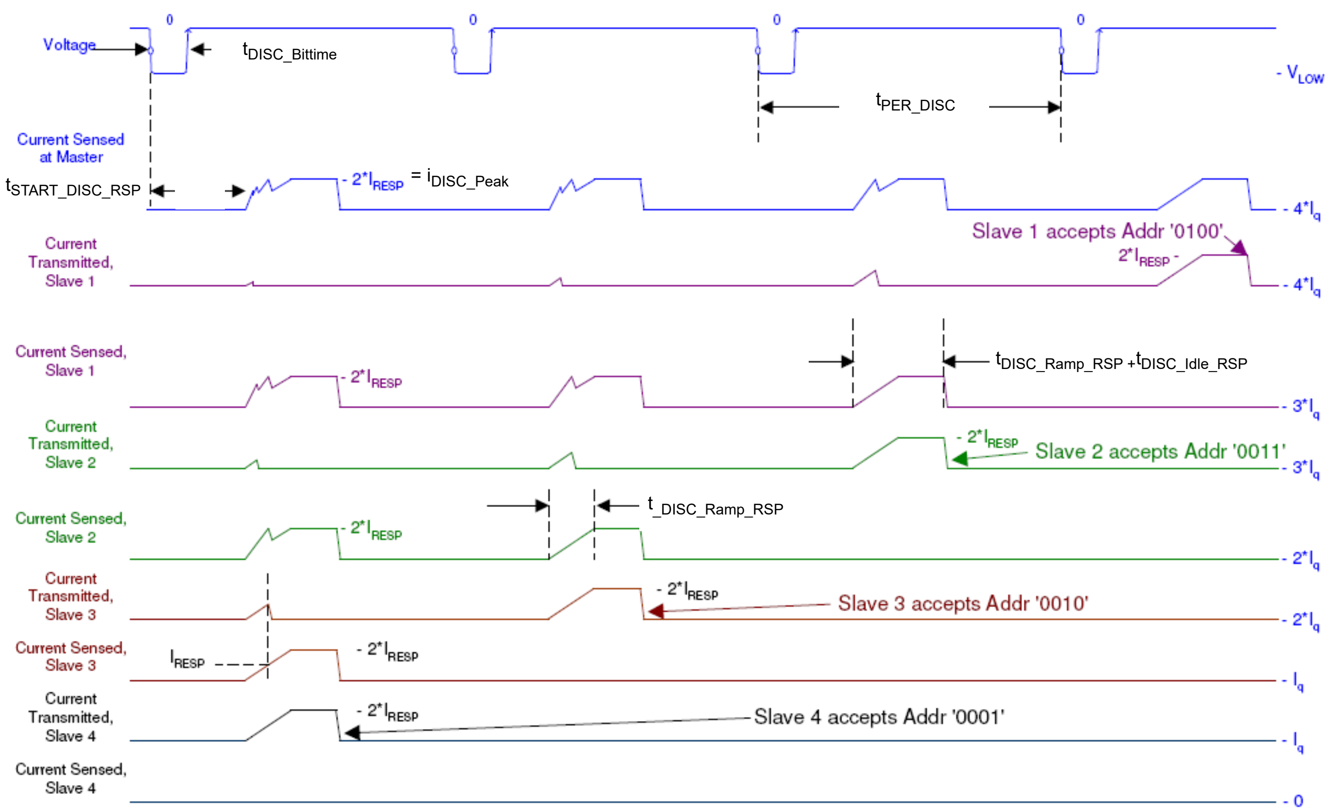


Figure 7-7 DSI3 Discovery Mode Timing Diagram

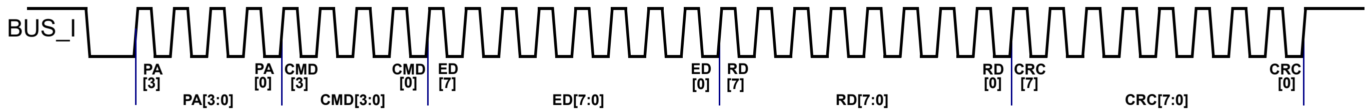
7.3 DSI3 Command and Response Mode

DSI3 Command and Response Mode is the main communication method used for initialization of the device.

7.3.1 DSI3 Command and Response Mode Command Reception

Command and Response Mode data packets are exchanged between a single master and a single slave. The primary purpose of command and response transactions are to read from and write to registers within the device memory structure.

An example Command and Response Mode Command is shown in Figure 7-8. The command consists of 32 bits of data broken up into multiple fields as described in Section 7.3.1.2.



Physical Address				Command				Extended Data								Register Data								Error Checking							
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E7	E6	E5	E4	E3	E2	E1	E0
0	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0	1	1	0	0	0	0	1	1	0	1	1	0

Figure 7-8 Command and Response Mode Example Command

7.3.1.1 Bit Encoding

Figure 7-9 shows the bit encoding used for Command and Response Mode Commands from the Master device.

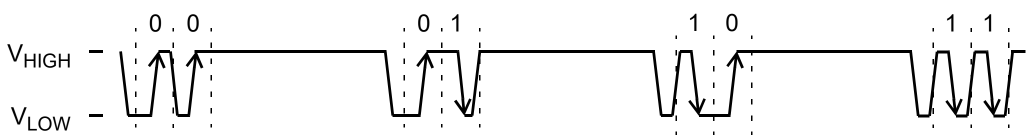


Figure 7-9 Command and Response Mode Command Bit Encoding

7.3.1.2 Command Message Format

The Command and Response Mode Command format is shown in Table 7-1.

Physical Address	Command	Extended Data	Register Data	CRC
PA[3:0]	CMD[3:0]	ED[7:0]	RD[7:0]	CRC[7:0]

Table 7-1 Command and Response Mode - Command Format

Field	Length (Bits)	Definition
PA[3:0]	4	Physical Address Must match the value in the PADDR[3:0] of the PHYSADDR register
CMD[3:0]	4	Command (reference Section 7.3.4)
ED[7:0]	8	Extended Data (reference Section 7.3.4)
RD[7:0]	8	Register Data (reference Section 7.3.4)
CRC[7:0]	8	Error Checking (reference Section 7.3.1.3)

Table 7-2 Command and Response Mode - Field Definitions

7.3.1.3 Error Checking

The device calculates an 8-bit CRC on the entire 32-bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device does not respond.

The CRC decoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and Seed for Command and Response Mode are shown in Table 7-3.

Mode	Default Polynomial	Non-Direct Seed
Command and Response Mode	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111

Table 7-3 Command and Response Mode Command CRC

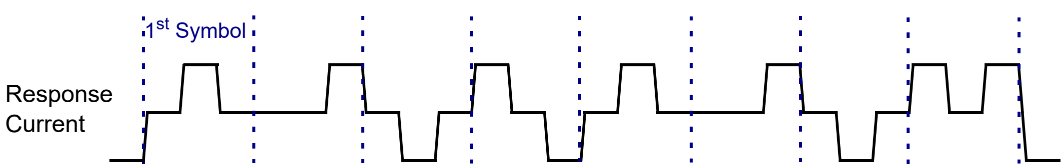
Some example CRC calculations are shown in Table 7-4.

Physical Address	Command	Extended Data	Register Data	Non-Direct Seed	8 Bit CRC
0x01	0x08	0x11	0x86	0xFF	0xB0
0x02	0x01	0x25	0xFF	0xFF	0x38
0x03	0x0F	0x1A	0x41	0xFF	0x2C
0x04	0x01	0x01	0x01	0xFF	0xD4

Table 7-4 Command and Response Mode - CRC Calculation Examples

7.3.2 DSI3 Command and Response Mode Response Transmission

An example Command and Response Mode response is shown in Figure 7-10. The response consists of 32 bits of data broken up into multiple fields as described in Section 7.3.2.2.



Physical Address				Command				Extended Data								Register Data								Error Checking							
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E7	E6	E5	E4	E3	E2	E1	E0
0	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0	1	1	0	0	0	0	1	1	0	1	1	0

Figure 7-10 Command and Response Mode Response Example

7.3.2.1 Symbol Encoding

The device response to a Command and Response Mode Command uses multi-level source coding where data nibbles are first encoded into symbols and then the symbols are encoded into current levels. The symbols are assembled from three consecutive three-level current pulses called chips. Within a symbol there are 3 consecutive chips that can assume one of three discrete current levels as described in Section 5.5: i_q, $i_q + i_{RESP}$, and iq + 2 x i_{RESP}. Figure 7-11 shows the chip transmissions and an example of a 3 symbol (9 chip), 12-bit data packet.

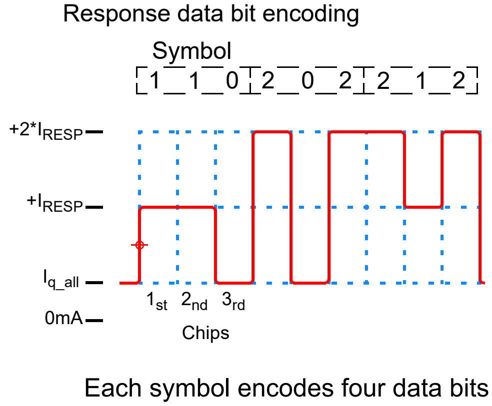


Figure 7-11 Response Symbol Encoding

Of the 27 possible combinations for three consecutive tri-level chips, the combinations that begin with the null current level (i_q) are discarded. Of the remaining 18 symbols, the two symbols that contain the same value for all three chips are also discarded. The remaining 16 symbols all begin with a non-null current level and have at least one transition. These characteristics guarantee that any response packet has a transition at the beginning of a packet and at least one transition in every symbol. Each 3-chip symbol encodes the information of 4-bits. Table 7-5 shows the symbol encoding used by the device.

Encoded Data (4 Bits)		Symbol Transmitted		
Binary	HEX	1st Chip	2nd Chip	3rd Chip
0000	0	1	1	0
0001	1	2	1	1
0010	2	1	0	2
0011	3	2	0	2
0100	4	1	0	0
0101	5	2	1	2
0110	6	1	1	2
0111	7	2	0	1
1000	8	2	2	0
1001	9	2	1	0
1010	A	1	2	2
1011	B	2	2	1
1100	C	1	2	0
1101	D	2	0	0
1110	E	1	0	1
1111	F	1	2	1

Table 7-5 Symbol Mapping

Where:

0 = iq

1= i_{RESP}

2= 2 x i_{RESP}

7.3.2.2 Response Message Format

The Command and Response Mode response format is shown in Table 7-6.

Physical Address	Command	Register + 1 Data	Register Data	CRC
PA[3:0]	CMD[3:0]	RD1[7:0]	RD[7:0]	CRC[7:0]

Table 7-6 Command and Response Mode - Response Format

Field	Length (Bits)	Definition
PA[3:0]	4	Physical Address Matches the value in the PADDR[3:0] of the PHYSADDR register
CMD[3:0]	4	An echo of the received command
ED[7:0]	8	The data contained in the register addressed by RA[7:1] + 1 (High Byte, reference Section 7.3.4)
RD[7:0]	8	The data contained in the register addressed by RA[7:1] + 0 (Low Byte, reference Section 7.3.4)
CRC[7:0]	8	Error Checking (reference Section 7.3.2.3)

Table 7-7 Command and Response Mode - Field Definitions

7.3.2.3 Error Checking

The device calculates a CRC on the entire 32-bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and Seed for Command and Response Mode are shown in Table 7-8.

Mode	Default Polynomial	Non-Direct Seed
Command and Response Mode	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111

Table 7-8 Command and Response Mode Response CRC

Some example CRC calculations are shown in Table 7-4.

7.3.3 DSI3 Command and Response Mode Timing

A timing diagram for Command and Response Mode is shown in Figure 7-12. Timing parameters are specified in Section 5.11.

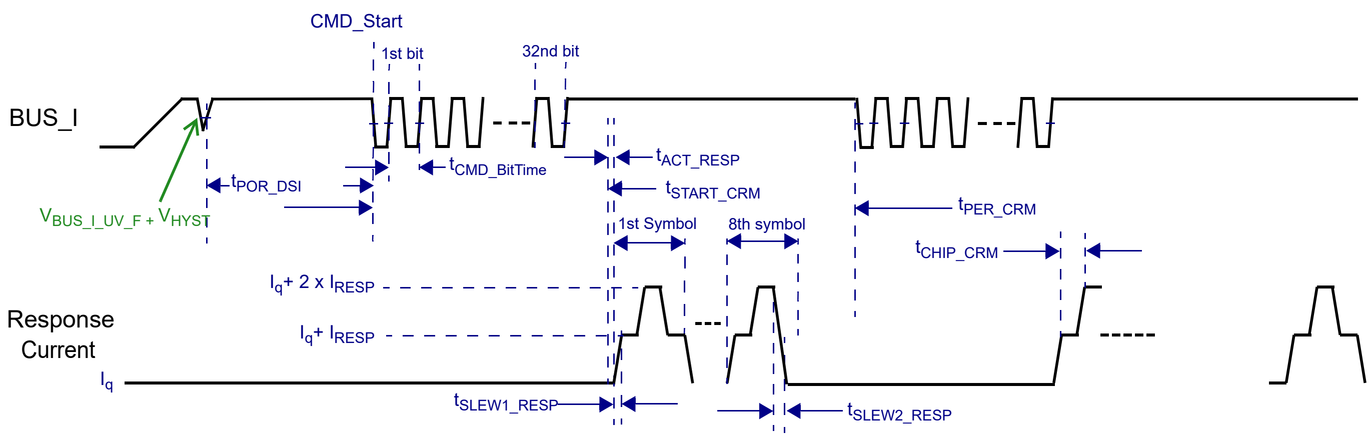


Figure 7-12 Command and Response Mode Timing Diagram

7.3.4 DSI3 Command and Response Mode Command Summary

Command						Data															
C3	C2	C1	C0	Hex	Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	$0	Register Read	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	x	x	x	x	x	x	x	x	x
0	0	0	1	$1	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	0	1	0	$2	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	0	1	1	$3	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	0	0	$4	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	0	1	$5	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	1	0	$6	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	1	1	$7	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	0	0	$8	Register Write	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]
1	0	0	1	$9	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	1	0	$A	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	1	1	$B	Enter PDCM	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	0	0	$C	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	0	1	$D	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	1	0	$E	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	1	1	$F	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

7.3.4.1 Register Read Command

The device supports the Register Read command as a device address specific command only. If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register and a valid CRC is calculated, the device responds to the command.

The device ignores the Register Read command if the command is sent to any other physical address, including the DSI Global Device Address of ‘0000’.

The Register Read command uses the byte address definitions shown in Section 6.1. The Register Read response includes the register contents at the time the Register Read command decode is complete. Readable registers along with their byte addresses are shown in Section 6.1. If an attempt is made to read a register that is not readable, the device will respond with all zero data.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	0	0	0	0	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	x	0	0	0	0	0	0	0	0	8 bits

Bit Field	Definition
PA[3:0]	DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored.
C[3:0]	Register Read Command = ‘0000’
RA[7:1]	RA[7:1] contains the upper 7 bits of the byte address for the register to be read.

Table 7-9 Register Read Command Format

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	0	0	0	0	RD[15]	RD[14]	RD[13]	RD[12]	RD[11]	RD[10]	RD[9]	RD[8]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Bit Field	Definition
PA[3:0]	DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register.
C[3:0]	Register Read Command = ‘0000’
RD[15:8]	The data contained in the register addressed by RA[7:1] + 1 (High Byte)
RD[7:0]	The data contained in the register addressed by RA[7:1] + 0 (Low Byte)

Table 7-10 Register Read Command: Response Format

A register read command to a register address outside of the addresses listed in Section 6.1 will result in a valid response. The data for the registers will be ‘0x0000’.

7.3.4.2 Register Write Command

The device supports the Register Write command as a device address specific command. If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device will execute the register write and respond to the command.

The device ignores the Register Write command if the command is sent to any other physical address, including the DSI Global Device Address of ‘0000’, with one exception as explained in Section 7.3.4.3.

The Register Write command uses the byte address definitions shown in Section 6.1. Writable registers along with their Byte addresses are shown in Section 6.1.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	0	0	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Bit Field	Definition
PA[3:0]	DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored.
C[3:0]	Register Write Command = 1000’
RA[7:0]	RA[7:0] contains the byte address of the register to be read.
RD[7:0]	RD[7:0] contains the data to be written to the register addressed by RA[7:0].

Table 7-11 Register Write Command Format

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	0	0	RD[15]	RD[14]	RD[13]	RD[12]	RD[11]	RD[10]	RD[9]	RD[8]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Bit Field	Definition
PA[3:0]	DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register.
C[3:0]	Register Write Command = ‘1000’
RD[15:8]	The data contained in the register addressed by RA[7:1] + 1 (High Byte) (after the register write is executed)
RD[7:0]	The data contained in the register addressed by RA[7:1] + 0 (Low Byte) (after the register write is executed)

Table 7-12 Register Write Command: Response Format

A register write command to a register address outside of the addresses listed in Section 6.1 will not execute, but will result in a valid response. The data for the registers will be ‘0x0000’.

A register write command to a read only register will not execute, but will result in a valid response. The data for the registers will be the current contents of the register.

7.3.4.3 Global Register Write Command to the PHYSADDR register

The device supports the Register Write command as a global address under the following conditions:

1. The Register Write command is written to the PHYSADDR register.
2. The PADDR[3:0] bits of the PHYSADDR register are equal to ‘0000’ prior to the register write being executed.

If these conditions are met, the device will execute the register write and respond to the command.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Bit Field	Definition
PA[3:0]	The DSI Global address of ‘0000’.
C[3:0]	Register Write Command = 1000’
RA[7:0]	RA[7:0] must be set to the PHYSADDR register address.
RD[3:0]	RD[3:0] contains the new physical address for the device.

Table 7-13 Global Register Write Command Format

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	0	0	RD[15]	RD[14]	RD[13]	RD[12]	RD[11]	RD[10]	RD[9]	RD[8]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Bit Field	Definition
PA[3:0]	The new DSI physical address programmed to the PADDR[3:0] bits in the PHYSADDR register.
C[3:0]	Register Write Command = 1000’
RD[15:8]	The data contained in register after PHYSADDR
RD[7:0]	The data contained in the PHYSADDR register after the register write is executed.

Table 7-14 Global Register Write Command: Response Format

7.3.4.4 Enter Periodic Data Collection Mode Command

The device supports an Enter PDCM command as a device address specific command and as a Global Command.

If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device will set the ENDINIT bit in the DEVLOCK_WR register, enter Periodic Data Collection Mode and respond to the command as shown below. If the PA[3:0] field in the command matches the Global address of '0000', the device will set the ENDINIT bit in the DEVLOCK_RW register and enter Periodic Data Collection Mode regardless of the value of the PADDR[3:0] bits in the PHYSADDR register (this includes PADDR = 0x0). No response is transmitted for a global command. The device ignores the Enter PDCM command if the command is sent to any other physical address.

The various DSI3 communication modes are controlled by the PDCM enable command and the BDM_EN bit in the BDM_CFG register as shown below:

PDCM Enabled?	BDM_EN	Command and Response Mode	Periodic Data Collection Mode	Background Diagnostic Mode
No	0	Enabled	Disabled	Disabled
No	1	Enabled	Disabled	Disabled
Yes	0	Disabled	Enabled	Disabled
Yes	1	Disabled	Enabled	Enabled

Once the ENDINIT bit is set, the registers listed in Section 6.3.3 are locked and the user array read/write register array verification is enabled. The ENDINIT bit can only be cleared by a device reset.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8 bits

Bit Field	Definition
PA[3:0]	DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register or the Global Address of '0000'. Otherwise, the command is ignored.
C[3:0]	Enter PDCM Command = 1011'

Table 7-15 Enter Periodic Data Collection Mode Command Format

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	1	1	0	0	0	0	Ch[3]	Ch[2]	Ch[1]	Ch[0]	0	0	0	0	0	0	0	0	8 bits

Bit Field	Definition
PA[3:0]	DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register.
Ch[3:0]	CHIPTIME[3:0] in the CHIPTIME register
C[3:0]	Enter Periodic Data Collection Mode Command = '1011'

Table 7-16 Enter Periodic Data Collection Mode Command: Response Format

7.3.4.5 Reserved Commands

If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register and a valid CRC is calculated, the device will respond to reserved commands. The physical address and command will be echoed and the correct CRC will be transmitted. The data included in the response is undefined.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits

Bit Field	Definition
PA[3:0]	DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored.
C[3:0]	Invalid Commands
x	Don't Care

Table 7-17 Reserved Commands

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	C[3]	C[2]	C[1]	C[0]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits

Bit Field	Definition
PA[3:0]	DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register.
C[3:0]	Reserved Command Echo

Table 7-18 Reserved Command Response Format

7.4 DSI3 Periodic Data Collection Mode and Background Diagnostic Mode

When the ENDINIT bit in the DEVLOCK_WR register is set, Periodic Data Collection Mode is enabled and the optional Background Diagnostic Mode is enabled.

7.4.1 DSI3 Periodic Data Collection Mode and Background Diagnostic Mode Command Reception

When Periodic Data Collection Mode is enabled, the device will decode the DSI3 Broadcast Read command as well as Background Diagnostic Mode command fragments as described below.

7.4.1.1 Bit Encoding

The Command Bit encoding for Periodic Data Collection Mode and Background Diagnostic Mode is the same as the bit encoding for Command and Response Mode, as described in Section 7.3.1.1.

7.4.1.2 Command Message Format

The command message format for Periodic Data Collection Mode and Background Diagnostic Mode is the same as the command message format for Command and Response Mode, as described in Section 7.3.1.2.

If Background Diagnostic Mode is disabled, then the device responds with the Periodic Data Collection Mode response only if the command is the single bit Broadcast Read Command. A Broadcast Read Command may be either a ‘1’ or a ‘0’. Figure 7-13 shows the Broadcast Read Commands supported by the device.

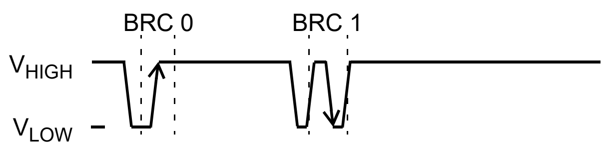


Figure 7-13 Background Diagnostic Mode Command Bit Encoding

If Background Diagnostic Mode is enabled:

- Background Diagnostic Mode commands are transmitted and decoded in 2 or 4 bit fragments depending on the state of the BDM_FRAGSIZE bit in the BDM_CFG register.
- The device responds with the Periodic Data Collection Mode response if and only if the command is a Broadcast Read Command or a command fragment.
- A Broadcast Read Command or any command length other than 2 or 4 bits resets the Background Diagnostic Mode command decode.
- The device responds with a Background Diagnostic Mode response only when a full 32-bit command is received and the decoded command is a valid Command and Response Mode command.

Reference section Section 7.4.4 for additional details on Background Diagnostic Mode timing.

7.4.1.3 Error Checking

The error checking for Background Diagnostic Mode commands is the same as the error checking for Command and Response Mode, and described in Section 7.3.1.3.

No error checking is employed for the Broadcast Read Commands.

7.4.2 DSI3 Periodic Data Collection Mode Response Transmission

When Periodic Data Collection Mode is enabled and the device receives either a Broadcast Read or Background Diagnostic command, the device will respond with periodic data as shown in Figure 7-14 and described in the following sections.

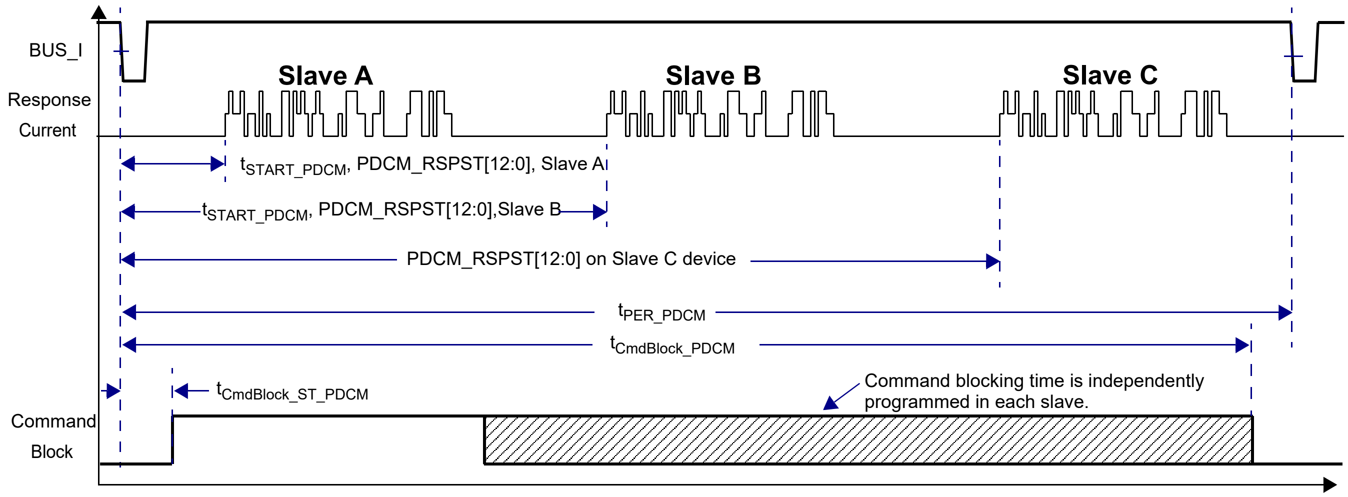


Figure 7-14 Periodic Data Mode Response Transmission

7.4.2.1 Symbol Encoding

The symbol encoding used for Periodic Data Collection Mode Responses is the same as for Command and Response Mode responses, and described in Section 7.3.2.1.

7.4.2.2 Response Message Format

The Periodic Data Collection Mode response format is shown below. Field sizes are defined by the PDCMFORMAT[2:0] bits in the SOURCEID_x register in Section 6.2.12.

Source ID	Keep Alive Counter	Status	Sensor Data	CRC
SOURCEID	KAC	S	D	CRC[7:0]

- If enabled in the PDCMFORMAT[2:0] bits, the SOURCEID field includes the value stored in the SOURCEID_x[3:0] bits of the SOURCEID_x register.
- If enabled in the PDCMFORMAT[2:0] bits, the Keep Alive Counter field is a 2-bit rolling message counter that is independently incremented for each SOURCEID. The initial value of the counter is '00'.
- If enabled, the status field is transmitted as listed in Table 7-19. Reference Section 7.7 for details on exception handling.
- The Sensor Data field includes the sensor data as selected by the DATATYPEx bits for the SOURCEID.
- The CRC field includes an 8-bit CRC as defined in Section 7.4.2.3.

s[3:0]				Description	DEVSTAT State	SUP_ER-R_DIS State	Error Priority	Sensor Data Field Value	
								STATUS Field Size = 4	STATUS Field Size = 0
0	0	0	0	Normal Mode	N/A	N/A	16	Sensor Data	
0	0	0	1	Normal Mode, User Array Not Locked (UF2 region has not been locked)	N/A	N/A	15	Sensor Data	The Sensor Data Field Error Code is transmitted for a minimum of one transmission
0	0	1	0	Self Test Incomplete or Self Test Active or Self Test Error Present	Bit set in CHx_STAT: ST_INCMPLT or ST_ACTIVE or ST_ERROR	N/A	14	Sensor Data	The Sensor Data Field Error Code is transmitted for a minimum of one transmission
0	0	1	1	Oscillator Training Error	Bit set in DEVSTAT3	N/A	13	Sensor Data	The Sensor Data Field Error Code is transmitted for a minimum of one transmission
0	1	0	0	Offset Error	Bit set in CHx_STAT: SIGNALCLIP or OFFSET_ERR	N/A	12	Sensor Data	The Sensor Data Field Error Code is transmitted for a minimum of one transmission
0	1	0	1	Temperature Error	Bit set in DEVSTAT2	N/A	11	Sensor Data	The Sensor Data Field Error Code is transmitted for a minimum of one transmission
0110 to 0111				RESERVED	N/A	N/A	9.10	Sensor Data	The Sensor Data Field Error Code is transmitted for a minimum of one transmission
1	0	0	0	User OTP Memory Error (UF2)	U_OTP_ERR set in DEVSTAT2	N/A	8	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	
1	0	0	1	User R/W Memory Error (UF2)	U_RW_ERR set in DEVSTAT2	N/A	7	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	
1	0	1	0	NXP OTP Memory Error	F_OTP_ERR set in DEVSTAT2	N/A	6	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	
1	0	1	1	Test Mode Active	TESTMODE bit set in DEVSTAT	N/A	5	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	
1	1	0	0	Supply Error	Bit set in DEVSTAT1	0	4	No Response until the supply monitor timer expires The Sensor Data Field Error Code is transmitted for a minimum of one transmission (Reference Section 6.2.2.5)	
						1		No Response until the supply monitor timer expires (Reference Section 6.2.2.5)	
1	1	0	1	Reset Error	DEVRES Set	N/A	3	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	
1110 to 1111				RESERVED	N/A	N/A	1,2	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	

Table 7-19 Periodic Data Collection Mode Status Field Definition

7.4.2.3 Error Checking

The device calculates a CRC on the entire response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and Seed for Periodic Data Collection Mode are shown in Table 7-20.

Mode	Default Polynomial	Non-Direct Seed
Periodic Data Collection Mode	$x^8 + x^5 + x^3 + x^2 + x + 1$	0000, SOURCEID_x[3:0]

Table 7-20 Periodic Data Collection Mode Response CRC

Some example CRC calculations are shown in Table 7-21.

Source Identification (4 Bits)	Keep Alive Counter (2 Bits)	Status (4 Bits)	Sensor Data (10 Bits)	Non-Direct Seed	8 Bit CRC
0x1	0x3	0x0	0x1FF	0x01	0xD6
0x2	0x2	0x0	0x1FE	0x02	0x70
0x3	0x1	0x0	0x20D	0x03	0xB0
0x4	0x0	0x0	0x1EA	0x04	0x5F

Table 7-21 Periodic Data Collection Mode - CRC Calculation Examples

7.4.3 DSI3 Periodic Data Collection Mode Timing

A timing diagram for Periodic Data Collection Mode is shown in Figure 7-15. Timing parameters are specified in Section 5.11.

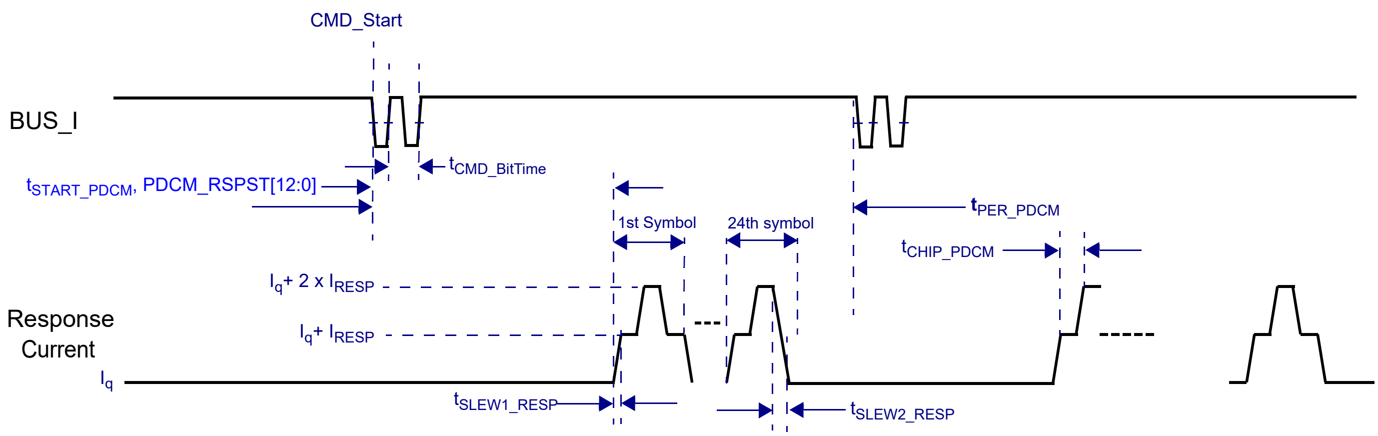


Figure 7-15 Periodic Data Collection Mode Timing Diagram

7.4.4 Background Diagnostic Mode Response Transmission

7.4.4.1 Symbol Encoding

The Background Diagnostic Mode response symbol encoding is the same as the symbol encoding used for Command and Response Mode responses and is described in Section 7.3.2.1.

7.4.4.2 Response Message Format

The Background Diagnostic Mode response message format is the same as the format used for Command and Response Mode responses and is described in Section 7.3.2.2.

- If a complete 32-bit command is received and decoded to a valid Command and Response Mode command the device provides a Background Diagnostic Mode response.
- Responses are initiated by the master transmitting 1 bit Broadcast Read Commands following a completed Background Diagnostic Mode command transmission.
- Response are transmitted in one or two symbol fragments (depending on the state of the BDM_FRAGSIZE bit) following the 1-bit Broadcast Read Command, using the same timing window within the frame that the Background Diagnostic Mode Command used.
- Responses are transmitted if and only if Broadcast Read Commands are received.
- Four or eight consecutive Broadcast Read Commands are required following a valid Background Diagnostic Mode command to complete a response transmission (depending on the state of the BDM_FRAGSIZE bit).
- If any command other than the Broadcast Read Command is received, no response is transmitted and the remainder of the Broadcast Read Command response is terminated.
- The data to be transmitted in the response is latched just before the first symbol of the background diagnostic mode response.

Reference Figure 7-16 for Background Diagnostic Mode timing.

7.4.4.3 Error Checking

The error checking for Background Diagnostic Mode responses is the same as used for Command and Response Mode, and described in Section 7.3.1.3.

7.4.5 DSI3 Background Diagnostic Mode Timing

An example timing diagram for Background Diagnostic Mode is shown in Figure 7-16. In this example, BDM_FRAGSIZE is set to ‘1 (4 bits). Timing parameters are specified in Section 5.11.

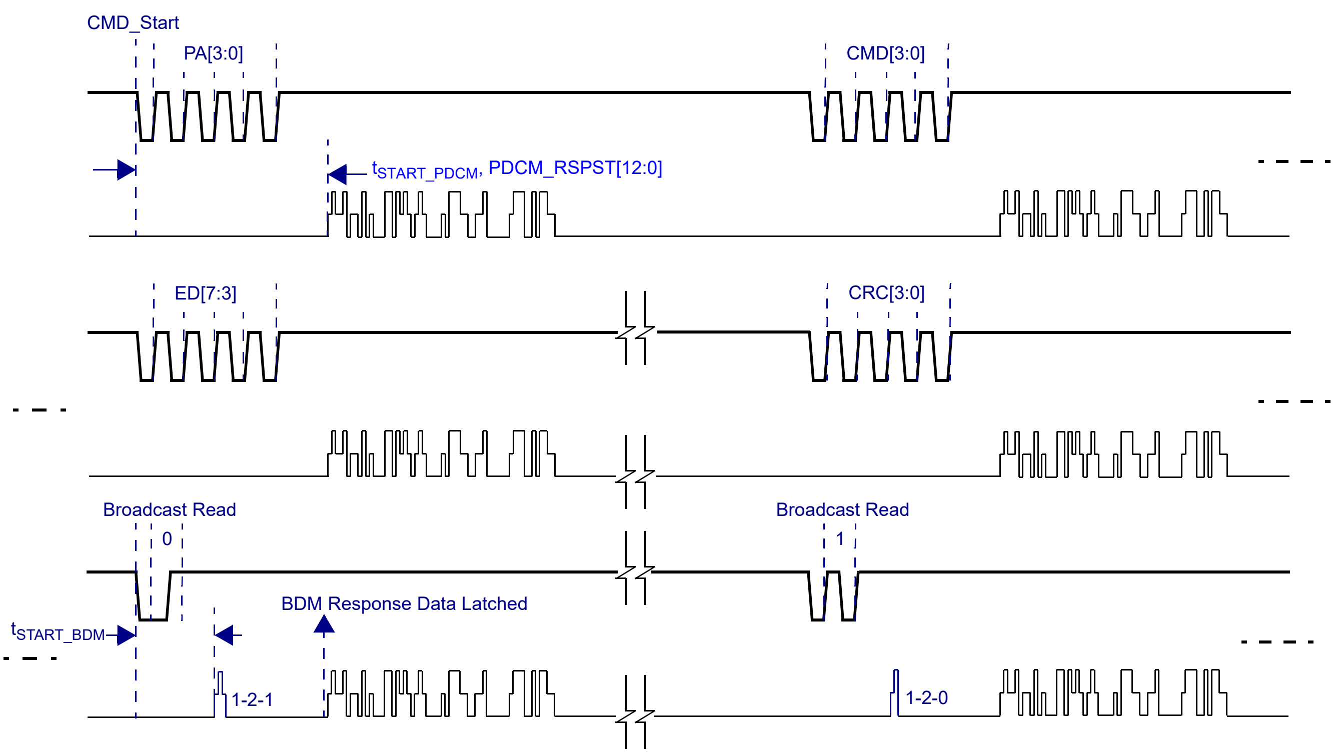


Figure 7-16 Background Diagnostic Mode Timing Diagram

7.4.6 DSI3 Periodic Data Collection Mode and Background Diagnostic Mode Command Summary

When Periodic Data Collection Mode is enabled, the Background Diagnostic Mode supports the Register Read Command as described in the Command and Response Mode Command Summary, Section 7.3.4.1. The Register Write Command is not supported in Background Diagnostic Mode.

7.4.7 DSI3 PDCM Data Transmission Modes

7.4.7.1 Simultaneous Sampling Mode (SS_EN = 1)

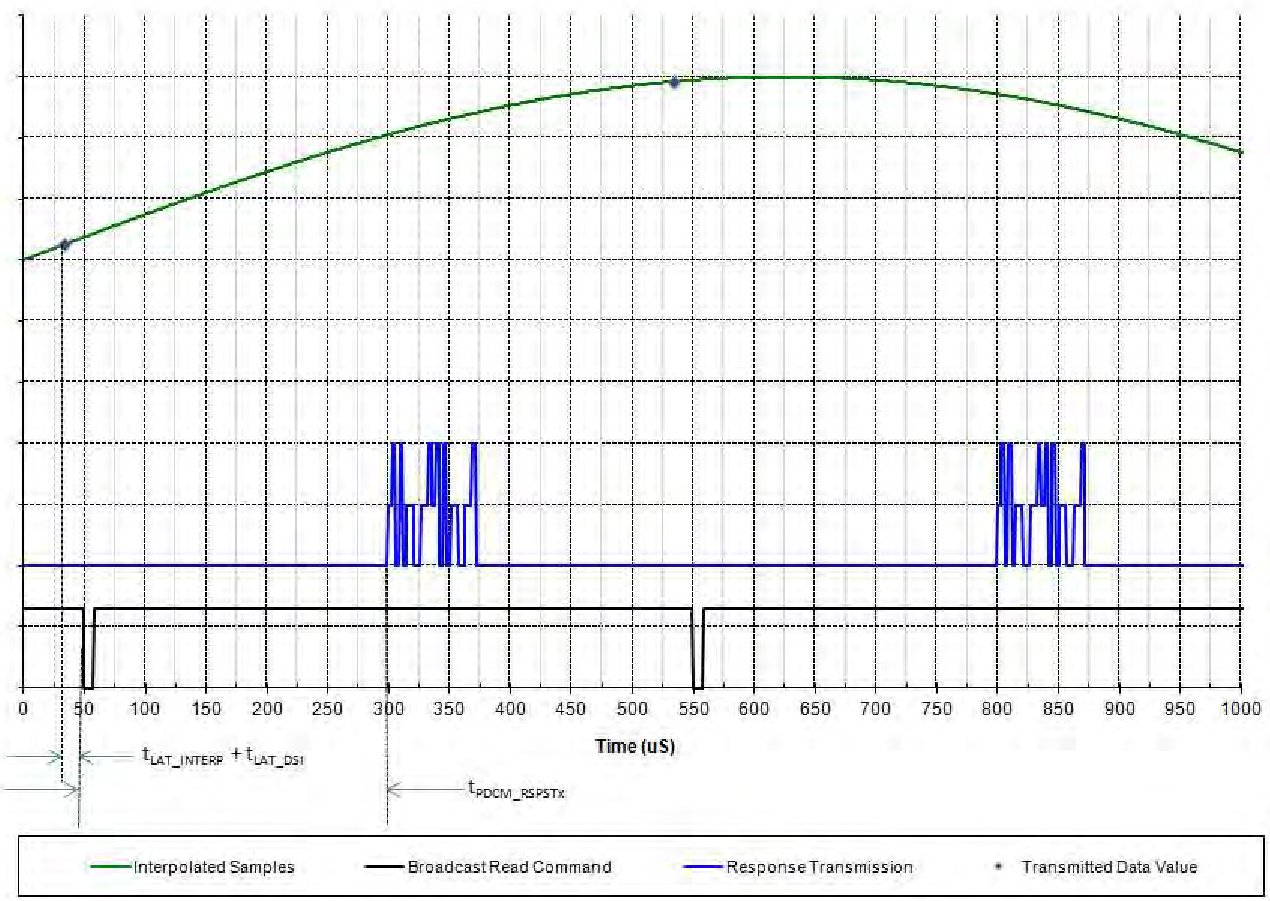


Figure 7-17 Simultaneous Sampling Mode

7.4.7.2 Synchronous Sampling Mode with Minimum Latency (SS_EN = 0)

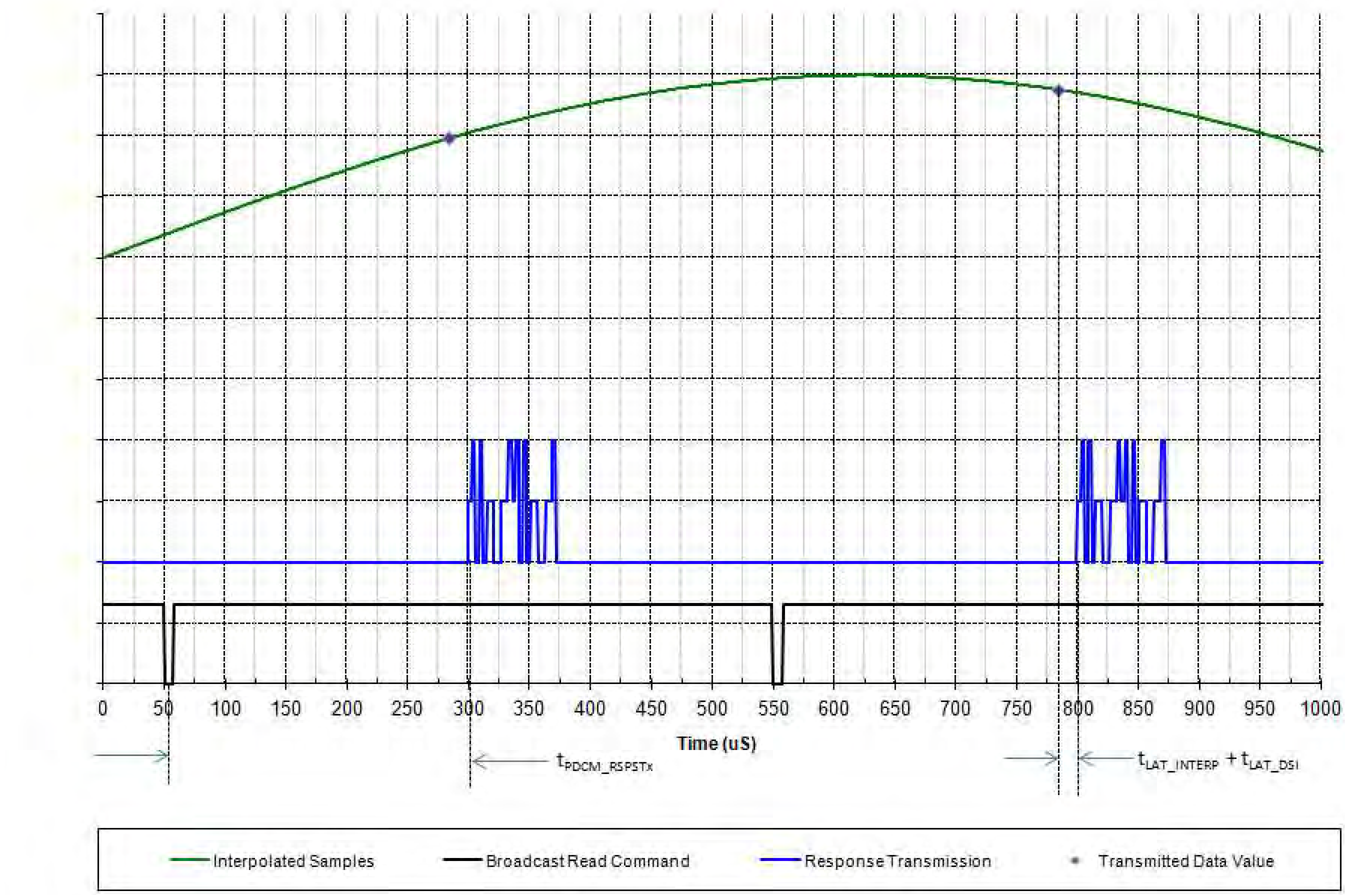


Figure 7-18 Synchronous Sampling Mode with Minimum Latency

7.5 Initialization Timing

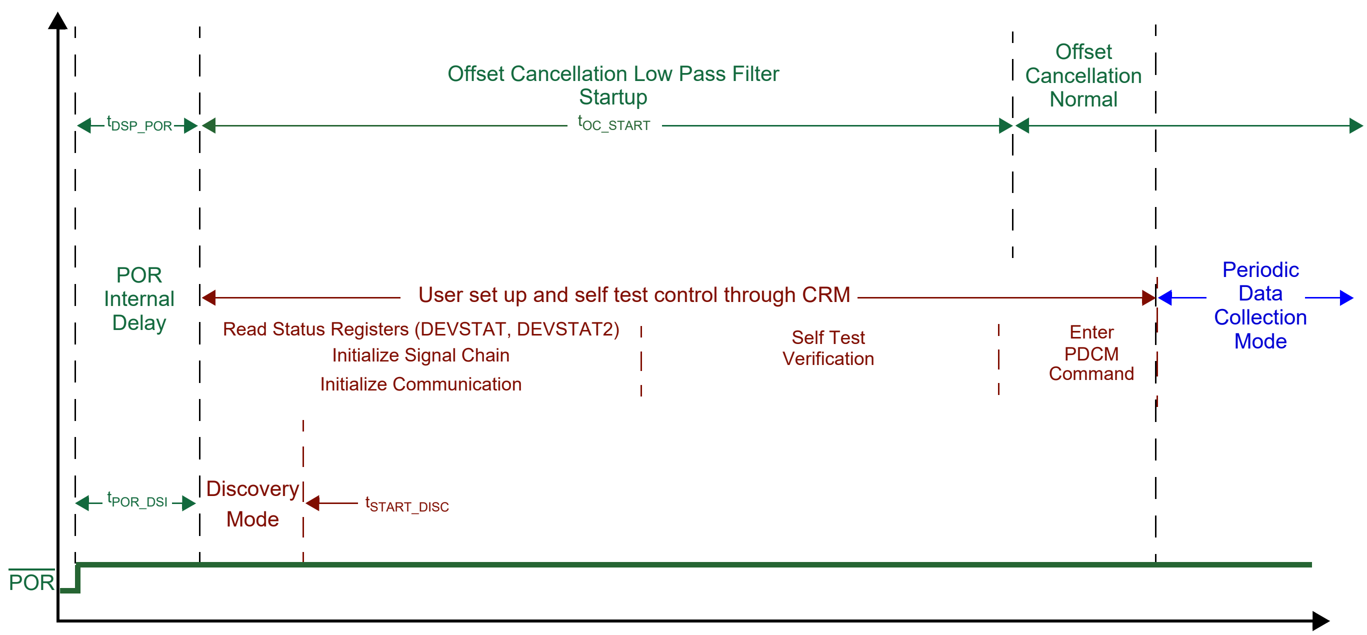


Figure 7-19 Initialization Timing

7.6 Maximum Number of Devices on a Network

The theoretical maximum number of devices on a DSI3 network is 16: 1 master and 15 slaves. The practical limit for the number of devices on a bus is dependent on the minimum common capability of the devices on the bus. The capability of the device is different depending on the bus configuration and operating mode. The impact of the device capability on the practical limit for the number of devices on the network is described in this section.

7.6.1 Pre-Configured, Parallel Connected Network

The number of devices in a pre-configured, parallel connected network is not directly limited by the capability of the device. The practical limit is determined by a combination of the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.

7.6.2 Bus Switch Connected Daisy Chain Network

The number of devices in a bus switch connected daisy chain network is not directly limited by the capability of the device. The practical limit is determined by a combination of the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.
- The current handling capability and resulting voltage drop of the external bus switches in the network.

7.6.3 Resistor Connected Daisy Chain Network Using Discovery Mode

The number of devices in a resistor connected daisy chain network is limited by the capability of the device. The maximum number of equivalent devices connected to the BUS_O pin of a device is 3. This is limited by the total quiescent current drawn from the BUS_O pin during Discovery Mode ($I_{BUS\_O\_q}$).

The practical limit is determined by a combination of the above restriction and the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.
- The maximum allowed quiescent current drawn from the BUS_O pin of other slaves in the system.
- The resulting voltage drop of the Discovery Mode resistors in all slaves in the network.

7.7 DSI3 Exception Handling

The table below summarizes the exception conditions detected by the device and the response for each exception.

Condition		Description	Device Response
Exception	**PDCM Enabled?**		
Power On Reset	N/A	Power Applied	– Reference Section 7.5 – ST_INCMPLT set, PDCM disabled. The device must be re-initialized
V_{BUS_I} Error	N/A	$V_{BUS\_I} < V_{BUS\_I\_UV\_F}$	– Response Current Deactivated – BUSIN_UV_ERR set, PDCM Status set as specified in Section 7.4.2.2 – The device ignores commands in CRM
V_{BUF} Error	N/A	$V_{BUF} < V_{BUF\_UV\_F}$	– Response Current Deactivated – VBUFUV_ERR set, PDCM Status set as specified in Section 7.4.2.2 – The device ignores commands in CRM
Internal Regulator Error	N/A	Internal regulator under-voltage condition	– The device is held in Reset – No response to DSI commands – If activated, BUSSW_L or BUSSW_H is deactivated – The device must be re-initialized when the internal regulator returns above the threshold
OTP Error Detection Fault (Factory Array)	N/A	Error detected in factory programmed OTP array.	– Periodic Data Collection Mode response data set to error response – F_OTP_ERR set, PDCM Status set as specified in Section 7.4.2.2
OTP Error Detection Fault (User Array)	N/A	Error detected in User programmed OTP array and the LOCK_U bit is set.	– Periodic Data Collection Mode response data set to error response – U_OTP_ERR set, PDCM Status set as specified in Section 7.4.2.2
User R/W Array Error Detection Fault	No	N/A	N/A
	Yes	Error detected in user read write registers and the ENDINIT bit is set.	– Periodic Data Collection Mode response data set to error response – U_RW_ERR set, PDCM Status set as specified in Section 7.4.2.2
Self Test Activated	No	ST activated during initialization	– Internal self test circuitry enabled – Self Test Activation Incomplete status cleared – Sensor Data Registers (SNSDATAx_x) contain self test active data – ST_ACTIVE set
	Yes	ST activated in Periodic Data Collection Mode	– Periodic Data Collection Mode sensor response data normal – Self Test Activation ignored
Self Test Never Activated after Reset	No	In initialization, before Self Test	– Normal Responses to Command and Response Mode
	Yes	In PDCM, Self Test incomplete	– Periodic Data Collection Mode sensor response data normal – ST_INCMPLT set, PDCM Status set as specified in Section 7.4.2.2

7.7.1 Daisy Chain and Discovery Mode Error Handling

The table below shows the effect of internal failure modes on the Discovery and Daisy Chain initialization procedures.

Error Condition	Effect on Discovery Mode	Effect on Daisy Chain
Supply Error	Discovery Commands Ignored The device will not participate in Discovery Mode	Daisy Chain Commands Ignored. The device will not participate in Daisy Chain
Memory Error	No Effect The device will attempt to participate in Discovery Mode as programmed.	No Effect The device will attempt to participate in Daisy Chain as programmed.
Temperature Error	No Effect The device will attempt to participate in Discovery Mode as programmed.	No Effect The device will attempt to participate in Daisy Chain as programmed.
Communication Error (Internal)	No Effect The device will participate in Discovery Mode as programmed.	No Effect The device will participate in Daisy Chain as programmed.
Offset Error	No Effect The device will participate in Discovery Mode as programmed.	No Effect The device will participate in Daisy Chain as programmed.
Self Test Incomplete or Self Test Active	Not Applicable	Not Applicable
Device Not Locked	No Effect The device will participate in Discovery Mode as programmed.	No Effect The device will participate in Daisy Chain as programmed.

Table 7-22 DSI3 Error Handling - Discovery Mode and Daisy Chain Mode

SECTION 8 PSI5 PROTOCOL

8.1 Communication Interface Overview

The communication interface between a master device and this slave device in PSI5 mode is established via a PSI5 compatible 2-wire interface, with parallel or serial (daisy-chain) connections to the satellite modules. Figure 8-1 shows one possible system configuration for multiple satellite modules in parallel.

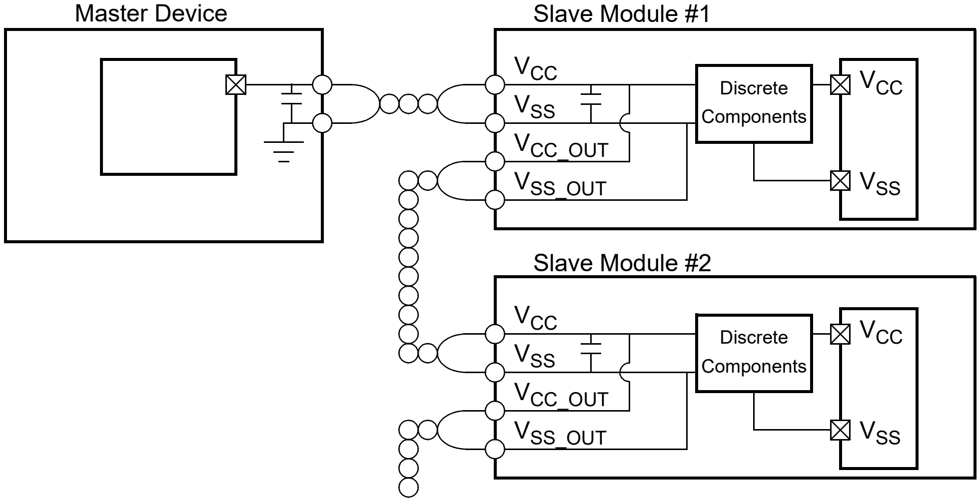


Figure 8-1 PSI5 Satellite Interface Diagram

8.2 Data Transmission Physical Layer

This device uses a two wire interface for both its power supply (V_{CC}), and data transmission. The PSI5 master supplies a pre-regulated voltage to this device. Data transmissions and synchronization control from the PSI5 master to this device are accomplished via modulation of the supply voltage. Data transmissions from this device to the PSI5 master are accomplished via modulation of the current on the power supply line.

8.2.1 Synchronization Pulse

The PSI5 master modulates the supply voltage in the positive direction to provide synchronization of the satellite sensor data. Upon reception of a synchronization pulse, this device delays a specified period of time, called a time slot, before transmitting sensor data. For more details regarding time slots, refer to Section 6.2.17, and Section 5.12.

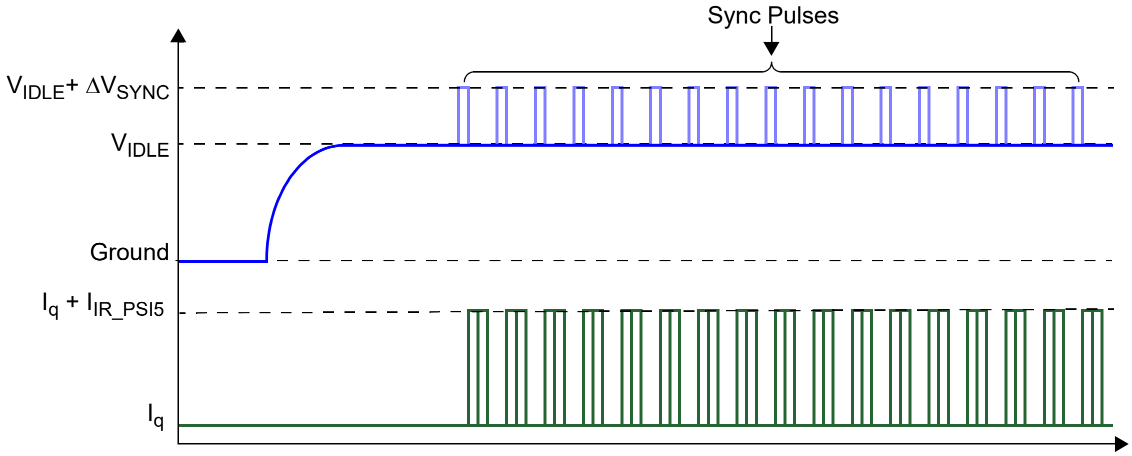


Figure 8-2 Synchronous Communication Overview

8.2.1.1 Synchronization Pulse Detection

The Synchronization (Sync) pulse detection block generates a valid synchronization pulse signal following the detection of an externally generated Sync pulse. This signal resets the Sync pulse time reference (t_{TRIG}), and initiates the timers associated with response messages.

The supply voltage can vary throughout the specified range, so the external Sync pulses may have different absolute voltage levels. Thus, the Sync pulse detection threshold (V_{CC_SYNC}) is dependent not only on the Sync pulse absolute voltage, but also on the supply voltage. Figure 8-3 shows a block diagram of the Sync pulse detection circuit.

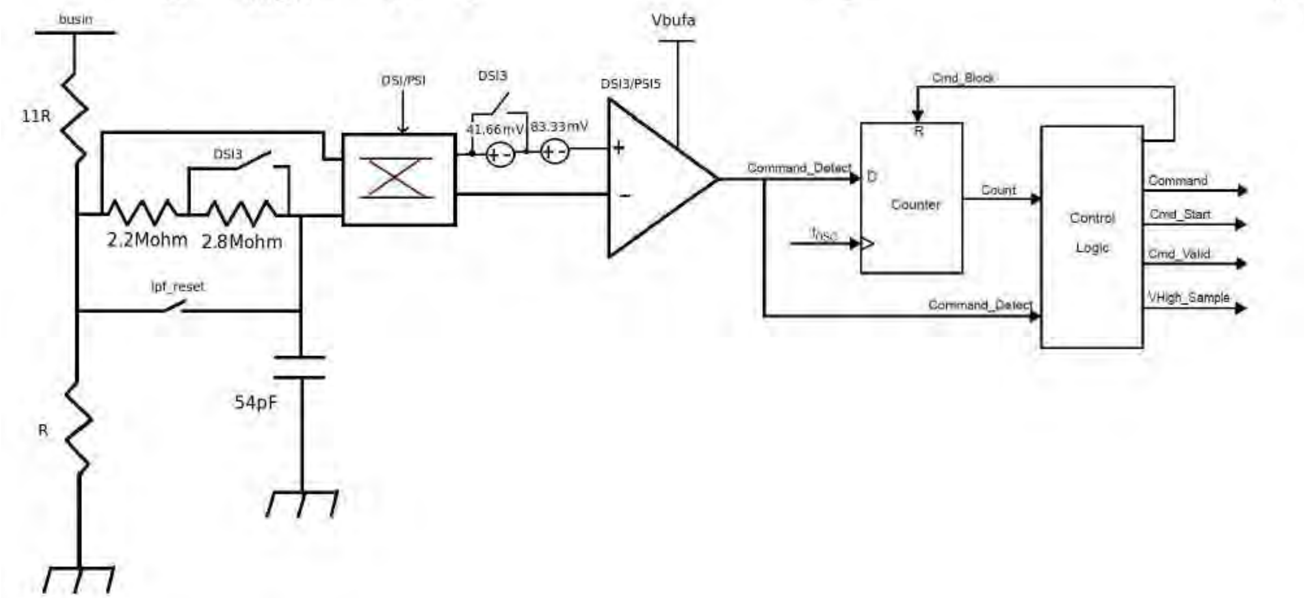


Figure 8-3 Synchronization Pulse Detection Circuit

The start of a Sync pulse is detected when the comparator output is set. The comparator output is input into a counter, and the counter is updated at a fixed frequency. At a fixed time after the initial sync pulse detection, the counter is compared against a limit (the minimum value of t_{SYNC}). If the counter is above the limit, a valid sync pulse is detected.

If the Sync pulse is valid, the following occur:

1. The valid Sync pulse detection signal is set.
2. The detection counter is reset and disabled for t_{SYNC_OFF} (referenced from t_{TRIG}). t_{SYNC_OFF} can be programmed by the user via the PDCM_CMD_B_x registers. Reference Section 6.2.18 for details on the programmable option, and Section 5.12 for timing specifications for each option.
3. The Sync pulse detection low pass filter is reset for a specified time ($t_{SYNC\_LPF\_RESET}$).

If the Sync pulse is invalid, all timers are reset, and the detector becomes sensitive within 2us.

The output of the comparator is monitored at the SampCLK frequency. Once the comparator output goes high, all of the internal timers are started, so that the t_{TRIG} jitter is minimized.

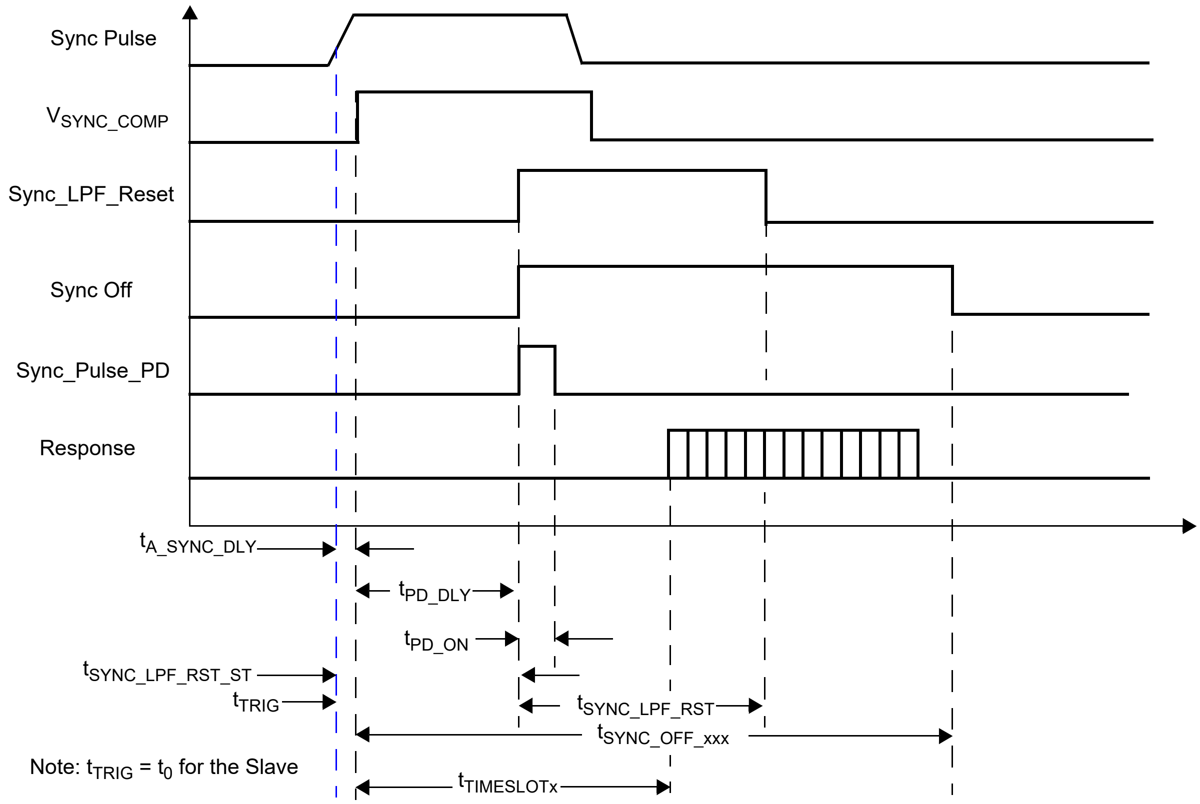


Figure 8-4 Synchronization Pulse Detection Timing

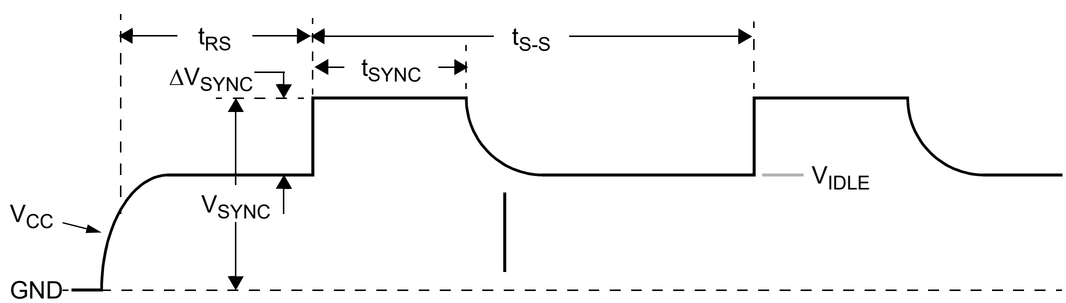


Figure 8-5 Sync Pulse Characteristics

8.2.1.2 Synchronization Pulse Pulldown Function

The device includes an optional Sync pulse pulldown function for systems in which the master device does not include an active pull-down function. The device uses the modulation current pulldown circuit, which sinks I_{R_PSI5} additional current from the BUS_I pin. The pulldown current is activated after t_{PD_DLY} (referenced to t_{TRIG}), and is activated for t_{PD_ON}.

The Sync pulse pulldown function is disabled in Programming Mode, in Initialization Phase 1 and in Daisy Chain Mode until the Run Command is received.

8.3 Data Transmission Data Link Layer

8.3.1 Bit Encoding

The device outputs data by modulation of the V_{CC} current using Manchester Encoding. Data is stored in a transition occurring in the middle of the bit time. The signal idles at the normal quiescent supply current. A logic low is defined as an increase in current at the middle of a bit time. A logic high is defined as a decrease in current at the middle of a bit time. There is always a transition in the middle of the bit time. If consecutive “1” or “0” data are transmitted, There will also be a transition at the start of a bit time.

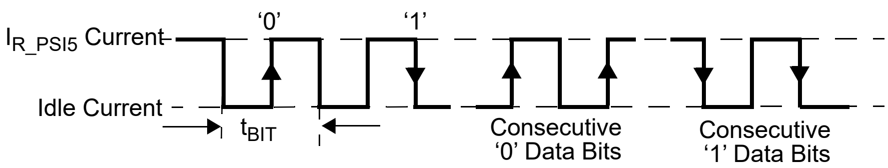


Figure 8-6 Manchester Data Bit Encoding

8.3.2 PSI5 Data Transmission

PSI5 data transmission frames are composed of two start bits, a 10-bit data word, and error detection bit(s). Data words are transmitted least-significant bit (LSB) first. A typical Manchester-encoded transmission frame is illustrated in Figure 8-7.

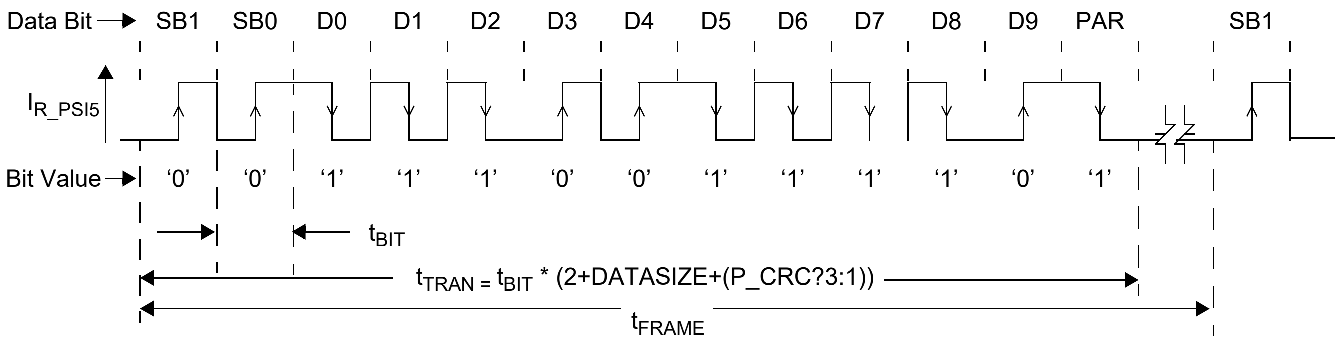


Figure 8-7 Example Manchester Encoded Data Transfer - PSI5-x10x

8.3.2.1 PSI5-x10P Transmission Mode

The device can be configured to transmit 10-bit data with parity by setting the PDCMFORMAT bits in the SOURCEID_x registers and the P_CRC bit in the PSI5_CFG register.

Start Bits		Sensor Data (Reference Section 6.6.4.9)										Parity
S2	S1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	P

Figure 8-8 PSI5-x10P Transmission Mode

8.3.2.2 PSI5-x10C Transmission Mode

The device can be configured to transmit 10-bit data with 3-bit CRC by setting the PDCMFORMAT bits in the SOURCEID_x registers and the P_CRC bit in the PSI5_CFG register.

Start Bits		Sensor Data (Reference Section 6.6.4.9)										CRC		
S2	S1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	C2	C1	C0

Figure 8-9 PSI5-x10C Transmission Mode

8.3.2.3 PSI5-x16P Transmission Mode

The device can be configured to transmit 16-bit data with parity by setting the PDCMFORMAT bits in the SOURCEID_x registers and the P_CRC bit in the PSI5_CFG register. In 16-bit mode, the 10-bit initialization data is transmitted in the upper 10-bits of the data packet and the lower 6-bits are all zeroes.

Start Bits		Sensor Data (Reference Section 6.6.4.9)																Parity
S2	S1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	P
Init Data		0	0	0	0	0	0	10-bit Initialization Data as specified in Section 8.4.2.1										P

Figure 8-10 PSI5-x16P Transmission Mode

8.3.2.4 PSI5-x16C Transmission Mode

The device can be configured to transmit 16-bit data with 3-bit CRC by setting the PDCMFORMAT bits in the SOURCEID_x registers and the P_CRC bit in the PSI5_CFG register. In 16-bit mode, the 10-bit initialization data is transmitted in the upper 10-bits of the data packet and the lower 6-bits are all zeroes.

Start Bits		Sensor Data (Reference Section 6.6.4.9)																CRC		
S2	S1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	C2	C1	C0
Init Data		0	0	0	0	0	0	10-bit Initialization Data as specified in Section 8.4.2.1										C2	C1	C0

Figure 8-11 PSI5-x16C Transmission Mode

8.3.3 Error Detection

Error detection of the transmitted data is accomplished via either a parity bit, or a 3-Bit CRC. The type of error detection used is selected by the P_CRC bit in the PSI5_CFG register.

8.3.3.1 Parity Error Detection

When parity error detection is selected, even parity is employed. The number of logic ‘1’ bits in the transmitted message must be an even number.

8.3.3.2 3-Bit CRC Error Detection

When CRC error detection is selected, a 3-bit CRC is appended to each response message. The 3-bit CRC uses a generator polynomial of $g(x) = X^3+X+1$, with a non-direct seed value = ‘111’. Message data from the transmitted message is read into the CRC calculator LSB first, and the data is augmented with three ‘0’s. Start bits are not used in the CRC calculation. Table 8-1 shows some example CRC calculation values for 10-bit data transmissions.

Data Transmitted											CRC		
HEX	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	C2	C1	C0
0x000	0	0	0	0	0	0	0	0	0	0	1	1	0
0x0CC	0	0	1	1	0	0	1	1	0	0	0	1	1
0x151	0	1	0	1	0	1	0	0	0	1	0	0	0
0x1E0	0	1	1	1	1	0	0	0	0	0	0	1	1
0x1F4	0	1	1	1	1	1	0	1	0	0	0	1	0
0x220	1	0	0	0	1	0	0	0	0	0	1	0	0
0x275	1	0	0	1	1	1	0	1	0	1	1	1	1
0x333	1	1	0	0	1	1	0	0	1	1	0	0	1
0x3FF	1	1	1	1	1	1	1	1	1	1	1	0	0

Table 8-1 PSI5 3-Bit CRC Calculation Examples

8.3.4 PSI5 Data Field and Data Range Values

Table 8-2 shows the details for each data range. The PSI5 data field size is defined by the PDCMFORMAT bits in the SOURCEID_x registers as described in Section 6.2.12.2.

16-Bit Data Values		10-Bit Data Value			Description (EMSG_EXT = 1 in PSI5_CFG)	Description (EMSG_EXT = 0 in PSI5_CFG)
Dec	Hex	Dec	Binary	Hex		
+32704	7FC0	+511		1FF		
+32640	7F80	+510		1FE		
+32576	7F40	+509		1FD		
+32512	7F00	+508		1FC		
+32448	7EC0	+507		1FB		
+32384	7E80	+506		1FA	Reserved	Reserved
+32320	7E40	+505		1F9		
+32256	7E00	+504		1F8		
+32192	7DC0	+503		1F7		
+32128	7D80	+502		1F6		
+32064	7D40	+501		1F5		
+32000	7D00	+500		1F4	Sensor Defect Error	Sensor Defect Error
+31936	7CC0	+499		1F3		
+31872	7C80	+498		1F2	Reserved	Reserved
+31808	7C40	+497		1F1		
+31744	7C00	+496		1F0		
+31680	7BC0	+495		1EF	Communication Error (OSCTRAIN_ERR bit)	
+31616	7B80	+494		1EE	Test Mode Enabled (TESTMODE bit set)	
+31552	7B40	+493		1ED	Offset Error (CH0 or CH1 OFFSET_ERR bit set)	Reserved (Error Mapped to 0x1F4)
+31488	7B00	+492		1EC	Temperature Error (TEMP0_ERR or TEMP1_ERR bit set)	
+31424	7AC0	+491		1EB	Memory Error (F_OTP_ERR, U_OTP_ERR or U_RW_ERR set)	
+31360	7A80	+490		1EA	Sensor Self Test Error (CH0 or CH1 ST_ERROR bit set)	Sensor Self Test Error
+31296	7A40	+489		1E9	Reserved	Reserved
+31232	7A00	+488		1E8	Sensor Busy	Sensor Busy
+31168	79C0	+487		1E7	Sensor Ready	Sensor Ready
+31104	7980	+486		1E6	Sensor Ready, but Unlocked	Sensor Ready, but Unlocked
+31040	7940	+485		1E5		
+30976	7900	+484		1E4	Reserved	Reserved
+30912	78C0	+483		1E3		
+30848	7880	+482		1E2	Bidirectional Communication: RC “Error”	Bidirectional Communication: RC “Error”
+30784	7840	+481		1E1	Bidirectional Communication: RC “OK”	Bidirectional Communication: RC “OK”
+30720	7800	+480		1E0	Maximum positive sensor value	Maximum positive sensor value
• • •	• • •	• • •		• • •		
+129 to +192	0081 to 00C0	+3		003	Positive sensor values	Positive sensor values
+65 to +128	0041 to 0080	+2		002		
+1 to +64	0001 to 0040	+1		001		
0	0000	0		000	Zero	Zero
-1 to -64	FFFF to FFC0	-1		3FF		
-65 to -128	FFBF to FF80	-2		3FE	Negative sensor values	Negative sensor values
-129 to -192	FF7F to FF40	-3		3FD		
• • •	• • •	• • •		• • •		
-30720	8800	-480		220	Maximum negative sensor value	Maximum negative sensor value
-30784	87C0	-481	1000011111	21F	Initialization Data Codes 10-Bit Status Data Nibble 1 - 16 (0000 - 1111) (Dx)	
:	:	:	:	:		
-31744	8400	-496	1000010000	210		
-31808	83C0	-497	1000001111	20F	Initialization Data IDs Block ID 1 - 16 (10-bit Mode) (IDx)	
:	:	:	:	:		
-32767	8000	-512	1000000000	200		

Table 8-2 PSI5 Data Values

8.4 Initialization

Following power-up, the device proceeds through an initialization process which is divided into 3 phases:

- Initialization Phase 1: No Data transmissions occur
- Initialization Phase 2: Sensor self test and transmission of configuration information
- Initialization Phase 3: Transmission of the “Sensor Busy” and/or “Sensor Ready”/“Sensor Defect” messages

Once initialization is completed the device begins normal mode operation, which continues as long as the supply voltage remains within the specified limits.

In asynchronous mode, initialization data is transmitted for Source ID 0 only.

In synchronous mode, the initialization data is transmitted independently for each channel.

In daisy chain mode, initialization data is transmitted in the Source ID 0 and Source ID 2 time slot as defined by the sensor address as documented in Section 8.7.

In Dual Transmission mode, initialization data is transmitted for both Source ID 0 and Source ID 2 in the Source ID 0 timeslot as documented in Section 8.6.

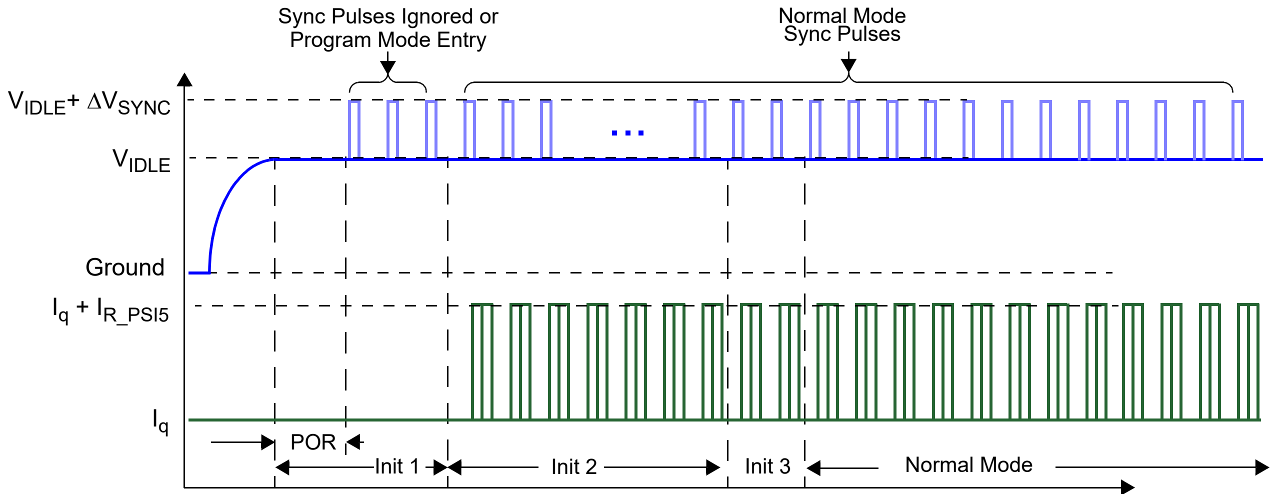


Figure 8-12 PSI5 Sensor 10-Bit Initialization

During PSI5 initialization, the device completes an internal initialization process consisting of the following:

- Power-on Reset
- Device Initialization
- Program Mode Entry Verification
- Offset Cancellation Low Pass Filter Initialization
- Self Test

Figure 8-13 shows the timing for internal and external initialization in synchronous mode. Figure 8-14 shows the timing for internal and external initialization in asynchronous mode. Timing parameters are specified in Section 5.12.

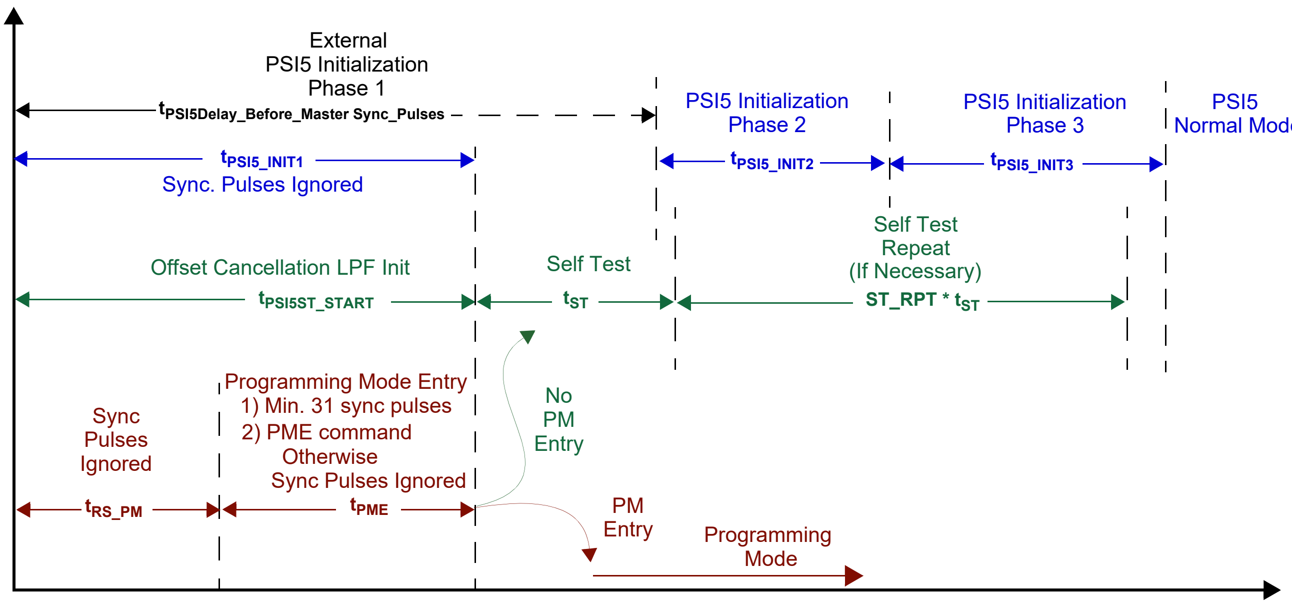


Figure 8-13 PSI5 Initialization Timing, Synchronous Mode

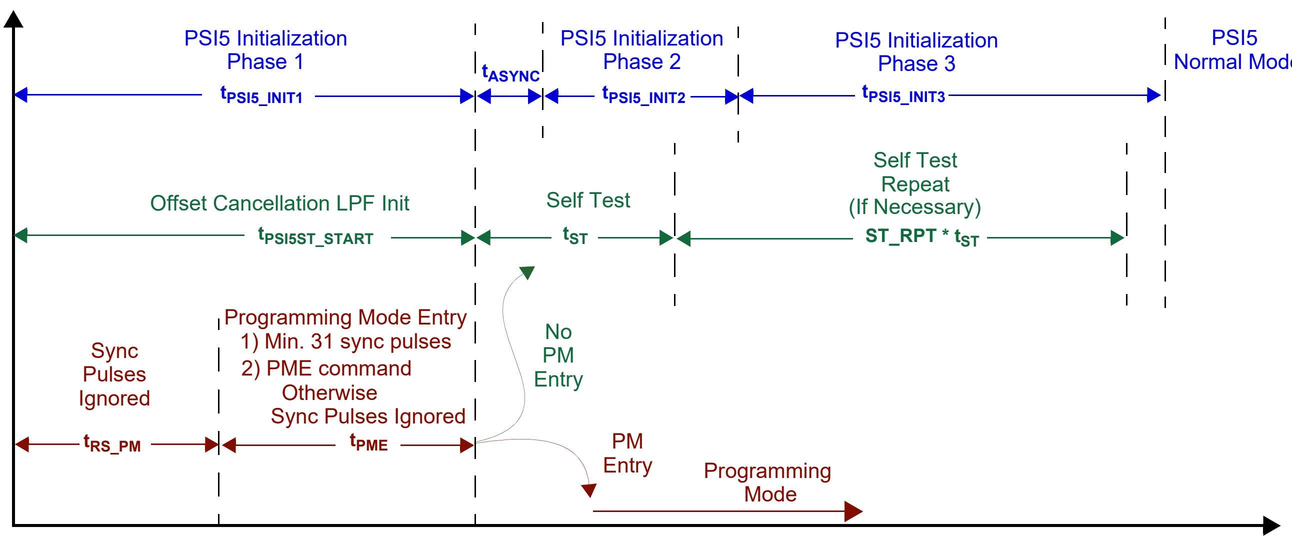


Figure 8-14 PSI5 Initialization Timing, Asynchronous Mode

8.4.1 PSI5 Initialization Phase 1

During PSI5 initialization phase 1, the device begins internal initialization and self checks, but transmits no data. Initialization begins with the sequence below, shown in Figure 8-13:

- Internal Delay to ensure analog circuitry has stabilized (t_{POR_PSI5})
- Offset Cancellation Low Pass Filter Initialization Begins (t_{PSI5ST_START})
- Monitor for the Programming Mode Entry Sequence (t_{PME})
- If the Programming Mode Entry Sequence is not detected, the device enters Initialization Phase 2 (t_{PSI5_INIT2})

8.4.2 PSI5 Initialization Phase 2

During PSI5 initialization phase 2, the device continues its internal self checks and transmits the PSI5 initialization phase 2 data. Initialization data is transmitted using the initialization data codes and IDs specified in Table 8-2, and in the order shown in Figure 8-15.

D1							D2							...	D32						
$ID1_1$	$D1_1$	$ID1_2$	$D1_2$	...	$ID1_k$	$D1_k$	$ID2_1$	$D2_1$	$ID2_2$	$D2_2$	...	$ID2_k$	$D2_k$	...	$ID32_1$	$D32_1$	$ID32_2$	$D32_2$	...	$ID32_k$	$D32_k$
Repeat k times							Repeat k times							...	Repeat k times						

Figure 8-15 PSI5 Initialization Phase 2 Data Transmission Order

The Initialization phase 2 time is calculated with the following equation:

$$t_{Phase2} = Trans_{Nibble} \times k \times (DataFields) \times t_{S-S}$$

Where:

- $Trans_{Nibble}$ = # of Transmissions per Data Nibble
  2: 1 for ID, and 1 for Data
- *k* = The repetition rate for the data fields
- *Data Fields* = 32 data fields or 48 data fields (if INIT2_EXT is set)
- t_{S-S} = Sync Pulse Period

8.4.2.1 PSI5 Initialization Phase 2 Data Transmissions

In PSI5 initialization phase 2, the device transmits a sequence of sensor specific configuration and serial number information. The transmission data is in conformance with the PSI5 specification, Revision 2.1 and AKLV27, Revision 1.20. Unique data content is transmitted for each channel. The data content and transmission format is shown in Table 8-4 and Table 8-5. Table 8-3 shows the phase 2 timing for different operating modes. Times are calculated using the equation in Section 8.4.2.

Operating Mode	Repetition Rate (k)	# of Transmissions	Nominal Phase 2 Time
Asynchronous Mode (228µs)	8	512	116.7ms
Synchronous Mode (500µs)	4	256	128.0ms

Table 8-3 Initialization Phase 2 Time

PSI5 Field ID #	PSI5 Nibble ID #	Page Address	PSI5 Nibble Address	Register Address	PSI5 Description	Value
F1	D1	0	0000	USERDATA_0[3:0]	User Specific Data	User
F2	D2, D3		0001, 0010	NA	Number of Data Blocks: 32: INIT2_EXT=0, 48: INIT2_EXT=1	0010 0000 or 0011 0000
F3	D4, D5		0011, 0100	USERDATA_1[3:0], USERDATA_1[7:4]	User Specific Data	User
F4	D6, D7		0101, 0110	USERDATA_2[3:0], USERDATA_2[7:4]	User Specific Data	User
F5	D8		0111	USERDATA_3[3:0]	User Specific Data	User
	D9		1000	USERDATA_3[7:4]	User Specific Data	User
F6	D10		1001	USERDATA_4[3:0]	User Specific Data	User
	D11		1010	USERDATA_4[7:4]	User Specific Data	User
F7	D12		1011	USERDATA_5[3:0]	User Specific Data	User
	D13		1100	USERDATA_5[7:4]	User Specific Data	User
	D14		1101	USERDATA_6[3:0]	User Specific Data	User
F8	D15		1110	USERDATA_7[3:0]	User Specific Data	User
	D16		1111	USERDATA_7[7:4]	User Specific Data	User
	D17	1	0000	USERDATA_8[3:0]	User Specific Data	User
	D18		0001	USERDATA_8[7:4]	User Specific Data	User
F9	D19		0010	SN4[7:4]	Device Serial Number	Factory
	D20		0011	SN4[3:0]	Device Serial Number	Factory
	D21		0100	SN3[7:4]	Device Serial Number	Factory
	D22		0101	SN3[3:0]	Device Serial Number	Factory
	D23		0110	SN2[7:4]	Device Serial Number	Factory
	D24		0111	SN2[3:0]	Device Serial Number	Factory
	D25		1000	SN1[7:4]	Device Serial Number	Factory
	D26		1001	SN1[3:0]	Device Serial Number	Factory
	D27		1010	SN0[7:4]	Device Serial Number	Factory
	D28		1011	SN0[3:0]	Device Serial Number	Factory
	D29		1100	PN1[3:0]	Device Part Number	Factory
	D30		1101	PN0[7:4]	Device Part Number	Factory
	D31		1110	PN0[3:0]	Device Part Number	Factory
	D32		1111	USERDATA_6[7:4]	User Specific Data	User
F10	D33	2	0000	CH0_STAVG_P[7:4]	Channel 0 Positive Self Test, High Nibble	Varies
	D34		0001	CH0_STAVG_P[3:0]	Channel 0 Positive Self Test, Low Nibble	Varies
	D35		0010	CH0_STOFFSET_P[7:4]	Channel 0 Post Positive Self Test Offset, High Nibble	Varies
	D36		0011	CH0_STOFFSET_P[3:0]	Channel 0 Post Positive Self Test Offset, Low Nibble	Varies
	D37		0100	CH0_STAVG_N[7:4]	Channel 0 Negative Self Test, High Nibble	Varies
	D38		0101	CH0_STAVG_N[3:0]	Channel 0 Negative Self Test, Low Nibble	Varies
	D39		0110	CH0_STOFFSET_N[7:4]	Channel 0 Post Negative Self Test Offset, High Nibble	Varies
	D40		0111	CH0_STOFFSET_N[3:0]	Channel 0 Post Negative Self Test Offset, Low Nibble	Varies
	D41		1000	CH1_STAVG_P[7:4]	Channel 1 Positive Self Test, High Nibble	Varies
	D42		1001	CH1_STAVG_P[3:0]	Channel 1 Positive Self Test, Low Nibble	Varies
	D43		1010	CH1_STOFFSET_P[7:4]	Channel 1 Post Positive Self Test Offset, High Nibble	Varies
	D44		1011	CH1_STOFFSET_P[3:0]	Channel 1 Post Positive Self Test Offset, Low Nibble	Varies
	D45		1100	CH1_STAVG_N[7:4]	Channel 1 Negative Self Test, High Nibble	Varies
	D46		1101	CH1_STAVG_N[3:0]	Channel 1 Negative Self Test, Low Nibble	Varies
	D47		1110	CH1_STOFFSET_N[7:4]	Channel 1 Post Negative Self Test Offset, High Nibble	Varies
	D48		1111	CH1_STOFFSET_N[3:0]	Channel 1 Post Negative Self Test Offset, Low Nibble	Varies

Table 8-4 Channel 0 PSI5 Initialization Phase 2 Data

PSI5 Field ID #	PSI5 Nibble ID #	Page Address	PSI5 Nibble Address	Register Address	Description	Value
F1	D1	0	0000	USERDATA_0[7:4]	User Specific Data	User
F2	D2, D3		0001, 0010	NA	Number of Data Blocks: 32: INIT2_EXT=0, 48: INIT2_EXT=1	0010 0000 or 0011 0000
F3	D4, D5		0011, 0100	USERDATA_9[3:0], USERDATA_9[7:4]	User Specific Data	User
F4	D6, D7		0101, 0110	USERDATA_A[3:0], USERDATA_A[7:4]	User Specific Data	User
F5	D8		0111	USERDATA_B[3:0]	User Specific Data	User
	D9		1000	USERDATA_B[7:4]	User Specific Data	User
F6	D10		1001	USERDATA_C[3:0]	User Specific Data	User
	D11		1010	USERDATA_C[7:4]	User Specific Data	User
F7	D12		1011	USERDATA_D[3:0]	User Specific Data	User
	D13		1100	USERDATA_D[7:4]	User Specific Data	User
	D14		1101	USERDATA_E[3:0]	User Specific Data	User
F8	D15		1110	USERDATA_7[3:0]	User Specific Data	User
	D16		1111	USERDATA_7[7:4]	User Specific Data	User
	D17	1	0000	USERDATA_8[3:0]	User Specific Data	User
	D18		0001	USERDATA_8[7:4]	User Specific Data	User
F9	D19		0010	SN4[7:4]	Device Serial Number	Factory
	D20		0011	SN4[3:0]	Device Serial Number	Factory
	D21		0100	SN3[7:4]	Device Serial Number	Factory
	D22		0101	SN3[3:0]	Device Serial Number	Factory
	D23		0110	SN2[7:4]	Device Serial Number	Factory
	D24		0111	SN2[3:0]	Device Serial Number	Factory
	D25		1000	SN1[7:4]	Device Serial Number	Factory
	D26		1001	SN1[3:0]	Device Serial Number	Factory
	D27		1010	SN0[7:4]	Device Serial Number	Factory
	D28		1011	SN0[3:0]	Device Serial Number	Factory
	D29		1100	PN1[3:0]	Device Part Number	Factory
	D30		1101	PN0[7:4]	Device Part Number	Factory
	D31		1110	PN0[3:0]	Device Part Number	Factory
	D32		1111	USERDATA_E[7:4]	User Specific Data	User
F10	D33	2	0000	CH0_STAVG_P[7:4]	Channel 0 Positive Self Test, High Nibble	Varies
	D34		0001	CH0_STAVG_P[3:0]	Channel 0 Positive Self Test, Low Nibble	Varies
	D35		0010	CH0_STOFFSET_P[7:4]	Channel 0 Post Positive Self Test Offset, High Nibble	Varies
	D36		0011	CH0_STOFFSET_P[3:0]	Channel 0 Post Positive Self Test Offset, Low Nibble	Varies
	D37		0100	CH0_STAVG_N[7:4]	Channel 0 Negative Self Test, High Nibble	Varies
	D38		0101	CH0_STAVG_N[3:0]	Channel 0 Negative Self Test, Low Nibble	Varies
	D39		0110	CH0_STOFFSET_N[7:4]	Channel 0 Post Negative Self Test Offset, High Nibble	Varies
	D40		0111	CH0_STOFFSET_N[3:0]	Channel 0 Post Negative Self Test Offset, Low Nibble	Varies
	D41		1000	CH1_STAVG_P[7:4]	Channel 1 Positive Self Test, High Nibble	Varies
	D42		1001	CH1_STAVG_P[3:0]	Channel 1 Positive Self Test, Low Nibble	Varies
	D43		1010	CH1_STOFFSET_P[7:4]	Channel 1 Post Positive Self Test Offset, High Nibble	Varies
	D44		1011	CH1_STOFFSET_P[3:0]	Channel 1 Post Positive Self Test Offset, Low Nibble	Varies
	D45		1100	CH1_STAVG_N[7:4]	Channel 1 Negative Self Test, High Nibble	Varies
	D46		1101	CH1_STAVG_N[3:0]	Channel 1 Negative Self Test, Low Nibble	Varies
	D47		1110	CH1_STOFFSET_N[7:4]	Channel 1 Post Negative Self Test Offset, High Nibble	Varies
	D48		1111	CH1_STOFFSET_N[3:0]	Channel 1 Post Negative Self Test Offset, Low Nibble	Varies

Table 8-5 Channel 1 PSI5 Initialization Phase 2 Data

Note: Offset and self test data in Field ID#10 is only transmitted if the internal self test for the associated channel has completed and has passed before F10, D33 is to be transmitted. This can only occur if the internal self test sequence passes the first time. If F10, D33 is to be transmitted before the internal self test has completed for a specific channel, 0x0 will be transmitted in place of offset and self test data for that channel only.

Note: If self test has completed all retries and has failed before F10, D33 is to be transmitted, F10, D33 - D48 will include self test data from the last failed attempt.

Note: Constant values are transmitted for all fields marked as “RESERVED”

Note: Initialization phase 2 nibble ID D19 and D32 data transmissions result in a read of the OTP array. The reads are asynchronous to the internal self-test timing. If either of the reads occurs simultaneous to the activation or deactivation of the internal self-test, the device may not respond for one PSI5 sync pulse. No initialization phase 2 data transmissions are skipped, data transmissions resume for the next sync pulse. To avoid the no response, the user should start sync pulse transmissions prior to the internal start of Initialization phase 2. Refer to the latest PSI5 application note for alternative initialization phase 2 start times to avoid the no response.

8.4.3 Internal Self Test

Once Initialization Phase 1 completes, the device begins its internal self test as described in Section 6.6.2.5. If Self Test fails, the device repeats Self Test up to ST_RPT times.

8.4.4 Initialization Phase 3

During PSI5 initialization phase 3, the device completes its internal self checks, and transmits a combination of “Sensor Busy” or “Sensor Ready” messages as defined in Table 8-2. The number of “Sensor Busy” messages transmitted in initialization phase 3 varies depending on the mode of operation, and the number of self test repetitions. Self test is repeated on failure up to ST_RPT times to provide immunity to misuse inputs during initialization. Self test terminates successfully after one successful self test sequence.

Once internal self test is completed, the device transmits 2 “Sensor Ready” commands.

Note: self test repeats are handled independently for each channel. However, both channels will exit initialization phase 3 simultaneously. If only one channel is repeating self tests, both channels will transmit “Sensor Busy” commands until either self-test has passed on both channels or the total number of repeats have completed.

The ENDINIT bit is automatically set when the device exits Initialization Phase 3.

8.5 Normal Mode

8.5.1 Asynchronous Mode

The device can be programmed to respond in asynchronous mode as specified in Section 6.2.17.1.

In asynchronous mode, the device transmits data at a fixed rate (t_{ASYNC}) and will not respond to normal sync pulses. However, during initialization phase 1, the device will monitor sync pulses to decode the Programming Mode Entry Command and allow entry into Programming Mode.

8.5.2 Simultaneous Sampling Mode

The device can be programmed to respond in Simultaneous Sampling Mode by programming the SS_EN bit to “Simultaneous Sampling Mode”.

In Simultaneous Sampling Mode, the most recent interpolated sensor data sample is latched at t_{TRIG} (rising edge of Sync Pulse) and transmitted starting at the time programmed in the PDCM_RSPSTx registers, relative to t_{TRIG}.

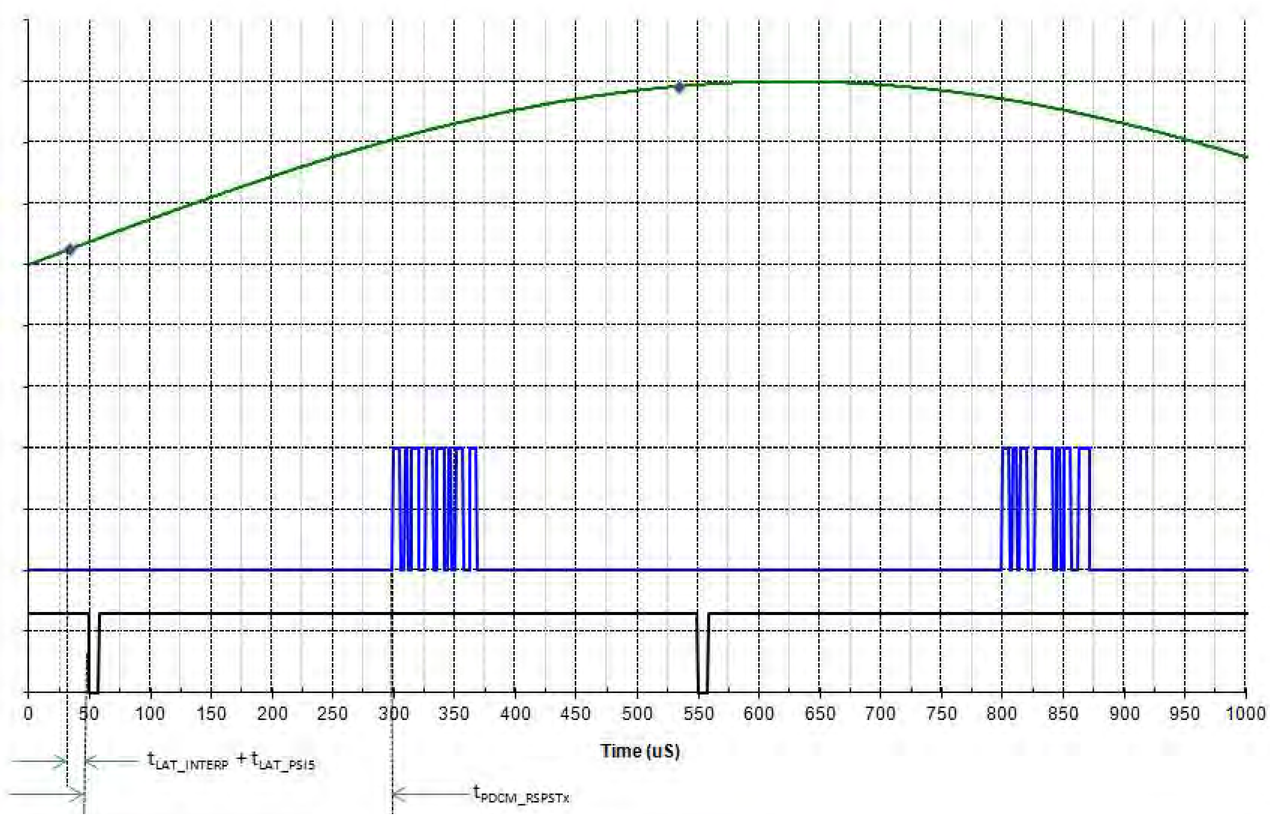


Figure 8-16 Simultaneous Sampling Mode

8.5.3 Synchronous Sampling Mode with Minimum Latency

The device can be programmed to respond in Synchronous Sampling Mode with minimum latency by programming the SS_EN bit to "Synchronous Sampling Mode".

In Synchronous Sampling Mode, the most recent interpolated sensor data sample is latched at the time programmed in the PDCM_RSPSTx registers, relative to t_{TRIG} (rising edge of Sync pulse). The data is transmitted starting at the time programmed in the PDCM_RSPSTx registers, relative to t_{TRIG}.

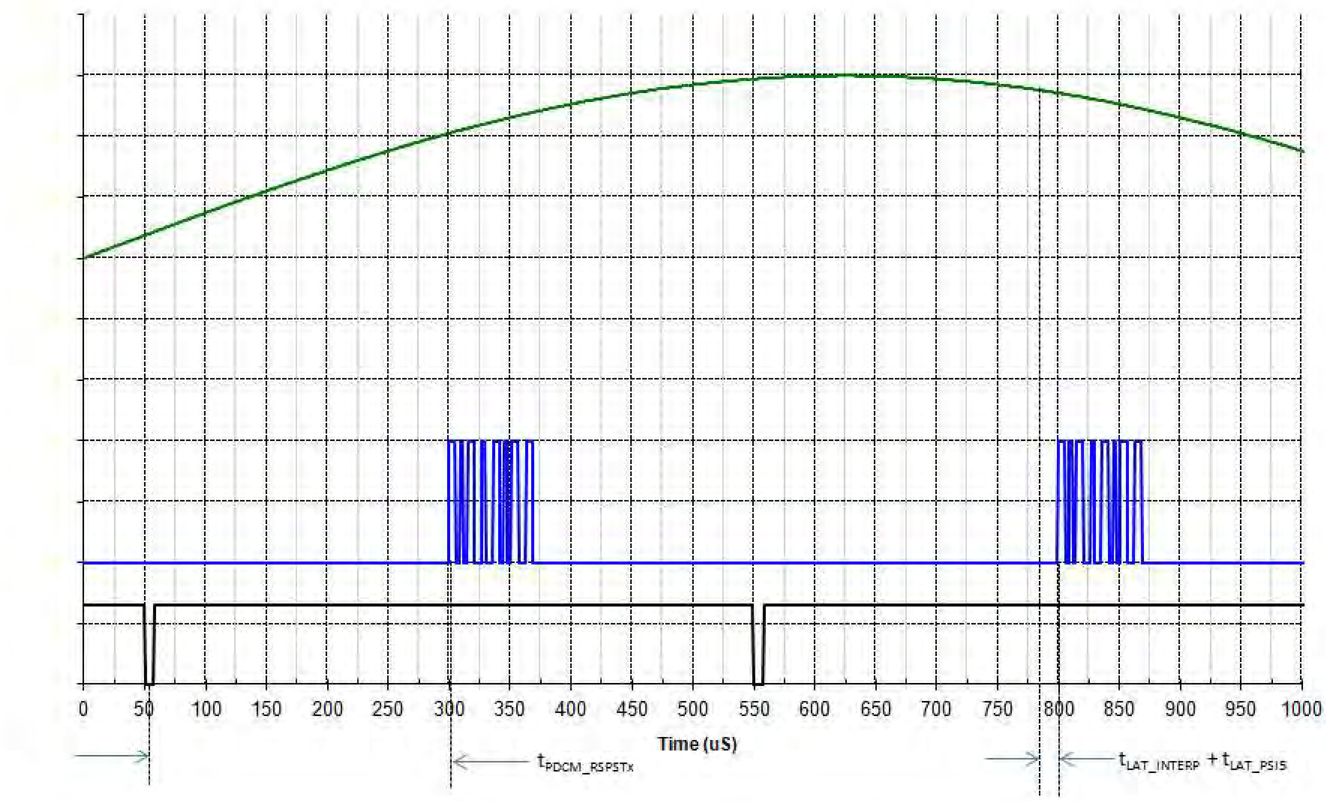


Figure 8-17 Synchronous Sampling Mode with Minimum Latency

8.6 Dual Transmission Mode

The device can be programmed to transmit both channel 0 and channel 1 data in the SOURCEID0 settings if the DUALTRANS bit is set as described in Section 6.2.16.4. In dual transmission mode, the following data is transmitted using the SOURCEID0 settings.

Start Bits		CH1_SNSDATA0										CH0_SNSDATA0										Parity
S2	S1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	P

Figure 8-18 Dual Transmission Mode Transmission Data with Parity

Start Bits		CH1_SNSDATA0										CH0_SNSDATA0										CRC		
S2	S1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	C2	C1	C0

Figure 8-19 Dual Transmission Mode Transmission Data with CRC

8.7 Daisy Chain Mode

The device can be programmed to operate in Daisy Chain Mode by setting the DAISY_CHAIN bit in the PSI5_CFG register. Daisy Chain Mode can be programmed to operate in either “Simultaneous Sampling Mode”, or “Synchronous Sampling Mode” by setting the SS_EN bit to the desired operating mode. In Simultaneous Sampling Mode, the most recent interpolated sensor data sample is latched at t_{TRIG} (rising edge of Sync Pulse). In Synchronous Sampling Mode, the most recent interpolated sensor data sample is latched at the transmission time associated with the programmed sensor address, relative to t_{TRIG} (rising edge of Sync pulse).

When programmed to operate in Daisy Chain Mode, the device follows the procedure below:

- On power-up, the device proceeds through normal PSI5 Initialization Phase 1 as specified in Section 8.4.1. At least one sync pulse must be transmitted during initialization phase 1.
- Upon completion of Initialization Phase 1, the device waits for a PSI5 “Set Address” command defined in Table 8-6 and Table 8-7.
  - The Set Address command must be preceded by at least 31 consecutive sync pulses. All other commands must be preceded by either 31 consecutive sync pulses or 5 consecutive missing sync pulses.
  - The Daisy Chain Programming command and response formats are defined in Section 8.9.2. The response settings are defined in Figure 8-22, with the exception of the time slot.
  - The response to the PSI5 Set Address command and all other valid commands uses the Source ID 0, address based time slot specified in Table 8-8.
  - If a framing error or CRC error is detected on a received command, the device reacts and responds to the error as specified in Section 8.9.4 using the Source ID 0, address based time slot specified in Table 8-8. Address ‘000’ corresponds to the $t_{TIMESLOT\_DCP}$ time slot.
- After receiving a valid address and completing the response, the device will decode and respond to all Table 8-6 commands sent to the sensor address it is set to. All responses will be transmitted in the address based time slot specified in Table 8-8.
- When the “Run Mode” command is received, the device responds to the command using the address based time slot(s) specified in Table 8-8. The device then ignores all commands and proceeds through Initialization Phase 2 and Initialization Phase 3 in response to sync pulses. The following response format is used, regardless of the state of the relevant bits in the Device Configuration Registers:

Parameter	Reference	Value
Time Slot	Section 6.2.17.1	Address based time slot(s) specified in Table 8-8
Data Size	Section 6.2.12.2	Data size controlled by the PDCMFORMAT bits
Error Checking	Section 6.2.16.6	Even Parity
Baud Rate	Section 6.2.14.2	Baud Rate controlled by the CHIPTIME bits

- Upon completion of Initialization Phase 3, the ENDINIT bit is set, the device enters normal mode and responds to all sync pulses with sensor data using the format above.

CMD Type	SAdr			FC			Command	Response (OK)		Response (Error)	
	A2	A1	A0	F2	F1	F0		RC	RD1	RC	RD1
Short	0	0	0	A2	A1	A0	Set Sensor Address (Daisy Chain)	OK	SAdr	Error	ErrN
Short	1	1	1	0	0	0	Broadcast Message - “Run Mode”	OK	0x000	Error	ErrN
Short	SAdr = 1,2,3,4,5,6			0	0	0	Activate Low Side Bus Switch BUSSW_CTRL[1:0] = ‘11’	OK	0x000	Error	ErrN
Short	SAdr = 1,2,3,4,5,6			1	1	1	Activate High Side Bus Switch BUSSW_CTRL[1:0] = ‘10’	OK	0x111	Error	ErrN
Short	SAdr = 1,2,3,4,5,6			A2	A1	A0	Set Sensor Address (Daisy Chain)	OK	SAdr	Error	ErrN

Table 8-6 Daisy Chain Programming Commands and Responses

Response Code	Definition	Value
RC = OK	Command Message Received Properly	0x1E1
RC = Error	Error during transmission of Command Message	0x1E2
SAdr	Programmed Sensor Address, prepended with 0s	Varies

Table 8-7 Daisy Chain Programming Response Code Definitions

Sensor Address (SAdr)			Description	Time Slot Source ID 0	Time Slot Source ID 2
A2	A1	A0			
0	0	0	Un-programmed sensor	N/A	N/A
0	0	1	Sensor Address 1	$t_{TIMESLOT\_DC0}$	$t_{TIMESLOT\_DC1\_L}$
0	1	0	Sensor Address 2	$t_{TIMESLOT\_DC1\_L}$	$t_{TIMESLOT\_DC2\_L}$
0	1	1	Sensor Address 3	$t_{TIMESLOT\_DC2\_L}$	$t_{TIMESLOT\_DC0}$
1	0	0	Sensor Address 4	$t_{TIMESLOT\_DC1\_H}$	$t_{TIMESLOT\_DC2\_H}$
1	0	1	Sensor Address 5	$t_{TIMESLOT\_DC2\_H}$	$t_{TIMESLOT\_DC3\_H}$
1	1	0	Sensor Address 6	$t_{TIMESLOT\_DC3\_H}$	$t_{TIMESLOT\_DC0}$
1	1	1	N/A	N/A	N/A

Table 8-8 Valid Daisy Chain Addresses

Note: Writes to Sensor Address 7 are ignored.

8.8 Error Handling

8.8.1 Daisy Chain Error Handling

The table below shows the effect of internal failure modes on the Daisy Chain initialization procedure.

Error Condition	Effect on Daisy Chain
Supply Error	Daisy Chain Commands Ignored. The device will not participate in Daisy Chain
Communication Error	No Effect. The device will participate in Daisy Chain as programmed.
Test Mode Enabled	Daisy Chain Commands Ignored. The device will not participate in Daisy Chain
Offset Error	No Effect. The device will participate in Daisy Chain as programmed.
Temperature Error	No Effect. The device will participate in Daisy Chain as programmed.
Memory Error	No Effect. The device will participate in Daisy Chain as programmed.
Self Test Error	No Effect. The device will participate in Daisy Chain as programmed.
Device Not Locked	No Effect. The device will participate in Daisy Chain as programmed.

8.8.2 Initialization Phase 2 Error Handling

The table below shows the effect of internal failure modes on the Initialization Phase 2 transmissions. Some errors occurring in Initialization Phase 2 will prevent entry into Initialization Phase 3. Once the error is no longer present, the device will complete Initialization Phase 2 as necessary and then transition to Initialization Phase 3.

Error Condition	Effect on Initialization Phase 2
Supply Error	Temporary, Sync Pulses Ignored
Communication Error	No Effect
Test Mode Enabled	No Effect
Offset Error	No Effect
Temperature Error	No Effect. The device will attempt to transmit Initialization Phase 2 data.
Memory Error	No Effect. The device will attempt to transmit Initialization Phase 2 data.
Self Test Error	No Effect
Device Not Locked	No Effect

8.8.3 Initialization Phase 3 Error Handling

The table below shows the effect of internal failure modes on the Daisy Chain initialization procedures. Some errors occurring in Initialization Phase 3 will prevent entry into Run Mode until the error is no longer present. Once the error is no longer present, one or more Sensor Ready commands will be transmitted before entering Run Mode.

Error Condition	Effect on Initialization Phase 3
Supply Error	Temporary, Sync Pulses Ignored
Communication Error	No Effect
Test Mode Enabled	No Effect
Offset Error	No Effect
Temperature Error	No Effect. The device will attempt to transmit Initialization Phase 3 data.
Memory Error	No Effect. The device will attempt to transmit Initialization Phase 3 data.
Self Test Error	No Effect
Device Not Locked	Sensor Ready replaced with Sensor Ready, but Not Locked Transmission (UF2 Region is un-programmed)

8.8.4 Normal Mode Error Handling

8.8.4.1 Standard Error Reporting

The table below summarizes the error reporting in normal mode if the PSI5 Error Extension option is disabled. A single error transmission clears the device status allowing for temporary error conditions to be cleared once the error condition is removed.

Error Condition	Error Code	Error Response
Supply Error	NA	Temporary (Normal transmissions continue once condition is removed)
Communication Error	0x1F4	
Test Mode Enabled		
Offset Error		
Temperature Error		
Memory Error		
Self Test Error	0x1EA	Latched until reset Note: A self test error on either channel results in a self test error response from both channels.
Device Not Locked	NA	NA

8.8.4.2 PSI5 Error Extension Option

If the PSI5 error extension option is enabled, additional error reporting is available as shown in the table below. A single error transmission clears the device status allowing for temporary error conditions to be cleared once the error condition is removed.

Error Condition	Error Code	Error Response
Supply Error	NA	Temporary (Normal transmissions continue once condition is removed)
Communication Error	0x1EF	
Test Mode Enabled	0x1EE	
Offset Error	0x1ED	
Temperature Error	0x1EC	
Memory Error	0x1EB	
Self Test Error	0x1EA	Latched until reset Note: A self test error on either channel results in a self test error response from both channels.
Device Not Locked	NA	NA

8.9 PSI5 Programming Mode

PSI5 Programming mode is a synchronous communication mode that allows for bidirectional communication with the device. Programming mode is intended for factory programming of the OTP array and reading of diagnostic information. It is not intended for use in normal operation.

8.9.1 PSI5 Programming Mode Entry

The device enters programming mode if and only if the following sequence occurs:

- At least 31 sync pulses are detected, directly preceding the Programming Mode Entry Short Command during the Programming Mode Entry Window shown in Figure 8-13.
  - The window timing is defined in Section 5.12 (t_{PME}).
  - The Sync pulses and Programming Mode Entry command must be received with a sync pulse period of $t_{S\text{-}S\_PM}$

If the Programming Mode entry requirement is not met:

- Programming Mode Entry is blocked until the device is reset.
- The device proceeds with PSI5 Initialization Phase 2, and PSI5 Initialization Phase 3.
- The device enters normal mode, and responds as programmed to normal sync pulses.

If the Programming Mode entry requirement is met:

- Normal transmissions to sync pulses are terminated.
- The device will detect commands if the start condition is met as described in Section 8.9.2.2.
- The device responds only to valid PSI5 Short and XLong Commands addressed to Sensor Address ‘001’, as defined in Section 8.9.3.

8.9.2 PSI5 Programming Mode - Data Link Layer

8.9.2.1 PSI5 Programming Mode - Command Bit Encoding

Commands messages are transmitted via the modulation of the supply voltage. The presence of a sync pulse is a logic '1' and the absence of a sync pulse is a logic '0'. Sync pulses are expected at a rate of $t_{S\text{-}S\_PM}$.

8.9.2.2 PSI5 Programming Mode - Command Message Format

Once Programming Mode is enabled, command message data frames consist of a start condition, 3 Start Bits (S[2:0]), a 3 bit Sensor Address (SAdr[2:0]), a 3-bit Function Code (FC[2:0]), an optional Register Address (RAdr[7:0]), an optional data field (D[7:0]), and a 3-bit CRC (C[2:0]. The start condition consists of one of the following:

1. A minimum of 5 consecutive logic ‘0’s (with no sync bits)
2. A minimum of 31 consecutive logic ‘1’s (this includes logic ‘1’s transmitted for the previous response)

The command message format is shown in Figure 8-20.

Start Bits			**Sensor Addr**			**Function Code**			**Register Address**												**Data**				**CRC**		
S2	S1	S0	SA0	SA1	SA2	FC0	FC1	FC2	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	D0	D1	D2	D3	D4	D5	D6	D7	C2	C1	C0
0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0

Response		
RC	**RD1**	**RD0**
$3FF	$3FF	$3FF

CRC

Data to be written to register (optional)

Register Address (optional)

Function Codes (Reference Section 8.9.3)

Sensor Address - Fixed at 001

Start Bit Sequence = 010

Figure 8-20 Programming Mode Via PSI5 Command Data Format

Bit stuffing is necessary to maintain a synchronized time base between the command master and the device. A logic ‘1’ Sync bit is added every 4th bit in the command message to ensure there will never be more than 3 logic '0' bits in a row.

Start Bits				**Sensor Address**				**Function Code**				**Register Address**											**Data**										**CRC**			
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	RA6	RA7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0

Response		
RC	RD1	RD0
$1E2	$3FF	$3FF

Figure 8-21 Programming Mode Via PSI5 XLONG Command Data Format with Sync Bits

Once a command is received and verified, the device expects 2 to 3 consecutive sync pulses (depending upon the command message lengths described below). There is no delay restriction between the command and the first sync pulse for the response. Once the first sync pulse for the response is received, each successive response sync pulse must be received within the programming mode sync pulse period specified ($t_{S\text{-}S\_PM}$) or a framing error may occur.

For each of these sync pulses, The device will respond with the following settings:

Parameter	Value
Time Slot	$t_{TIMESLOT\_DC1\_L}$
Data Size	10 Bit data
Error Checking	Even Parity
Baud Rate	125kBaud
Sync Pulse Pulldown	Disabled

Figure 8-22 Programming Mode Via PSI5 Response Message Settings

8.9.2.3 Short Frame Command and Response Format

Short frames are the simplest type of command message. No data is transmitted in a short frame command. Only specific instructions are performed in response to short frame commands. The Short Frame format is shown in Figure 8-23. Short Frame commands and responses are defined in Section 8.9.3.

The device only supports a short command for Programming Mode Entry.

Start Bits				Sensor Address				Function Code				CRC		
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	C2	C1	C0
0	1	0	1	1	0	0	1	0	0	1	1	0	0	0

Response	
RC	RD1
$1E2	$3FF

Figure 8-23 Programming Mode Via PSI5 Short Command and Response Format

8.9.2.4 Long Frame Command and Response Format

Long frames allow for the transmission of data nibbles for register writes. The device can provide register data in response to a read or write request. The Long Frame format is shown in Figure 8-25. The device does not support the Long Frame Command.

Start Bits				Sensor Address				Function Code				Register Address								Data					CRC			
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	D0	D1	D2	Sy	D3	C2	C1	Sy	C0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	1	0

Response		
RC	RD1	RD0
$1E2	$3FF	$3FF

Figure 8-24 Programming Mode Via PSI5 Long Command and Response Format

8.9.2.5 Extra Long Frame Command and Response Format

Extra Long Frames allow for the transmission of address and data bytes for register reads and writes. The device can provide register data in response to a read or write request. The Extra Long Frame format is shown in Figure 8-25. Extra Long Frame commands and responses are defined in Section 8.9.3.

The device supports Register Read and Register Write Extra Long commands.

Start Bits				Sensor Address				Function Code				Register Address										Data											CRC			
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	RA6	RA7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0

Response		
RC	RD1	RD0
$1E2	$3FF	$3FF

Figure 8-25 Programming Mode Via PSI5 Long Command and Response Format

8.9.2.6 Command Message CRC

Programming mode command error checking is accomplished by a 3-bit CRC. The 3-bit CRC is calculated using all message bits except start bits and sync bits. The CRC verification uses a generator polynomial of $g(x) = X^3+X+1$, with a non-direct seed value = ‘111’. The message data is provided to the CRC calculator in the order received (LSB first, SAdr, FC, RAdr, Data), and then augmented with three ‘0’s. Table 8-1 shows some example CRC calculation values for 10-bit data transmissions.

The calculated CRC is then compared against the received 3-bit CRC (received MSB first). If a CRC mismatch is detected, the device responds with a CRC Error response as defined in Section 8.9.4.

8.9.2.7 Command Sync Pulse Blanking Time

In Programming Mode and Programming Mode Entry, the device employs a fixed Sync Pulse blanking time of $t_{SYNC\_OFF\_500}$ regardless of the state of the PDCM_CMD_B register value.

8.9.2.8 Command Timeout

In the event that the device does not detect a sync pulse within a 4-bit window time, the command reception will be terminated and the device will respond to the next sync pulse with a Short Frame Framing Error response as defined in Section 8.9.4.

8.9.3 PSI5 Programming Mode Command and Response Summary

CMD Type	SAdr	FC FC[2:0]	Command	Register Address	Data Field	Response (OK)			Response (Error)		
						RC	RD1	RD0	RC	RD1	RD0
Short	001	100	Invalid Command	N/A	N/A	No Response			No Response		
Short		101	Invalid Command	N/A	N/A	No Response			No Response		
Short		110	Invalid Command	N/A	N/A	No Response			No Response		
Short		111	Enter Programming Mode	N/A	N/A	OK	0x0CA	N/A	No Response		
Long		010	Invalid Command	N/A	N/A	No Response			No Response		
Long		011	Invalid Command	N/A	N/A	No Response			No Response		
XLong		000	Read register located at address RA7:RA0	Varies	Varies	OK	RData	RData+1	Error	ErrN	0x000
XLong		001	Write WData to register RA7:RA0	Varies	Varies	OK	WData	RA7:RA0	Error	ErrN	0x000

Table 8-9 Programming Mode Via PSI5 Commands and Responses

Response Code	Definition	Value
RC = OK	Command Message Received Properly	0x1E1
RC = Error	Error during transmission of Command Message	0x1E2
RData	Byte Contents of Register located at address RA7:RA1 with RA0 = 0 (Low Byte)	Varies
RData + 1	Byte Contents of Register located at address RA7:RA1 with RA0 = 1 (High Byte)	Varies
WData	Byte Contents of Register located at address RA7:RA0	Varies

Table 8-10 Programming Mode Via PSI5 Response Code Definitions

8.9.4 Programming Mode Via PSI5 Error Response Summary

ErrN	Mnemonic	Description	Supported
0000	General	General Error	No
0001	Framing	Framing Error (4 consecutive zeroes)	Yes
0010	CRC	CRC Error on Received Message	Yes
0011	Address	Sensor Address Not Supported	No (Invalid Address is ignored)
0100	FC	Function Code Not Supported	No (N/A)
0101	Reserved	Reserved	No
0110			
0111			
1000	Reserved	Reserved	No
1001			
1010			
1011			
1100			
1101			
1110			
1111			

Table 8-11 Error Response Summary

ErrN is transmitted in the 4 LSBs of RD1. All other bits in the response data field are set to ‘0’.

8.10 PSI5 OTP Programming Procedure

1. Enter Programming Mode.
2. Set $V_{CC} = V_{PP}$
3. Load desired data into the desired registers using PSI5 Write commands.
4. Write the necessary OTP program sequence to the WRITE_OTP_EN register for the desired OTP region to be written.
5. Delay t_{PROG_TIME} after the completion of the Write OTP program to allow for completion of the OTP writes.
6. Read the DEVSTAT and DEVSTAT2 registers to confirm no errors occurred during the OTP writes.
7. Read back the register values that were written and compare to the desired values to confirm successful OTP writes.

Reference the PSI5 OTP Programming Procedure Application Note for further details on OTP Programming.

SECTION 9 STANDARD 32-BIT SPI PROTOCOL

The device includes a standard SPI protocol requiring 32-bit data packets. The device is a slave device requires that the base clock value be low (CPOL = 0) with data captured on the rising edge of the clock and data propagated on the falling edge of the clock (CPHA = 0). The most significant bit is transferred first (MSB first). SPI transfers are completed through a sequence of two phases. During the first phase, the command is transmitted from the SPI master to the device. During the second phase, response data is transmitted from the slave device. MOSI and SCLK transitions are ignored when SS_B is not asserted.

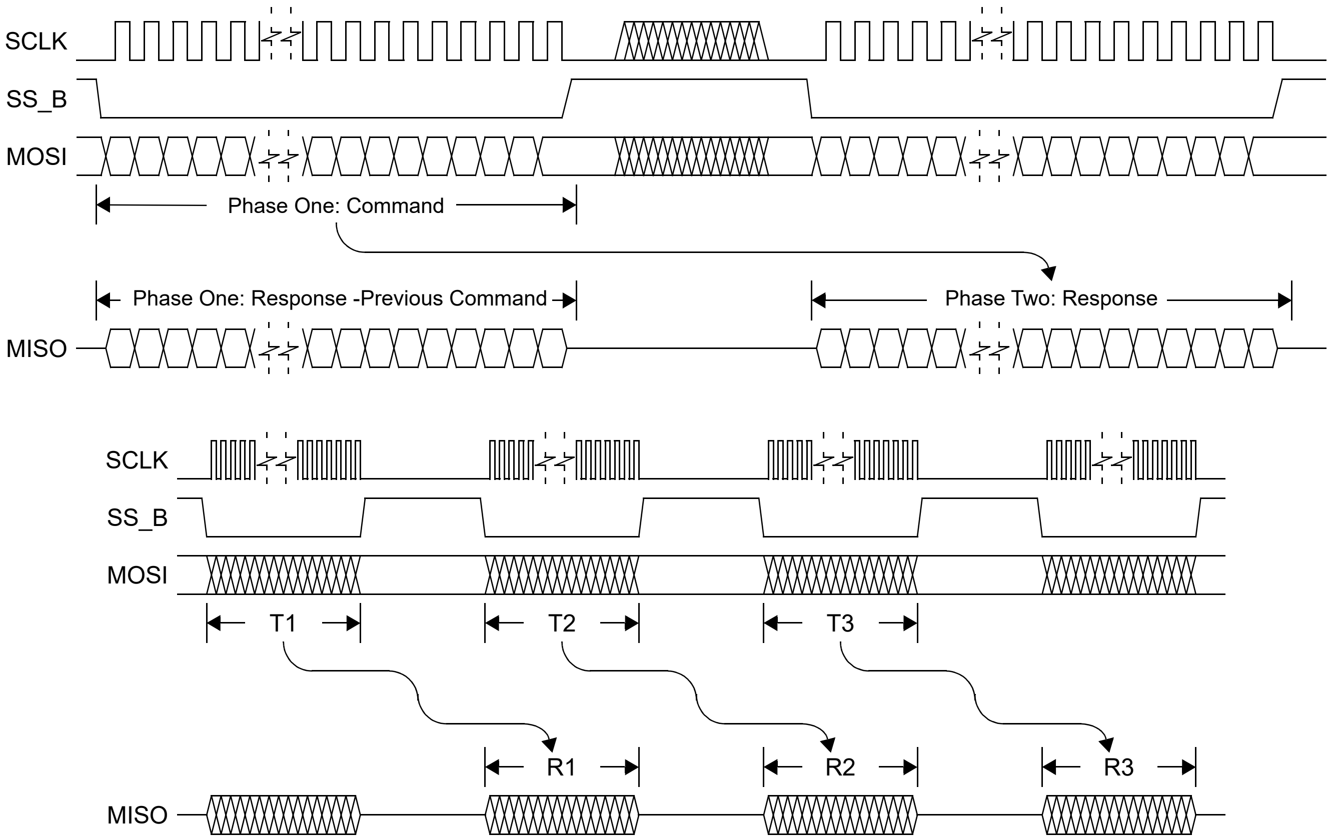


Figure 9-1 Standard 32-Bit SPI Protocol Timing Diagram

9.1 SPI Command Format

MSB … LSB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Access Command																															
Command				Fixed Bits: Must = 0x0				Register Address								Register Data								8-Bit CRC							
C[3:0]				0	0	0	0	RA[7:1]							RA[0]	RD[7:0]								CRC[7:0]							
Sensor Data Command																															
Command				Fixed Bits: Must = 0x00000																				8-Bit CRC							
C[3:0]				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC[7:0]							

9.2 SPI Response Format

MSB … LSB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Response to Register Request																															
Command				Basic Status		Unused Data = 0x0		Register Data: Contents of RA[7:1] High Byte								Register Data: Contents of RA[7:1] Low Byte								8-Bit CRC							
C[0]	C[3]	C[2]	C[1]	ST[1:0]		0	0	RD[15:8]								RD[7:0]								CRC[7:0]							
Response to Sensor Data Request																															
Command				Basic Status		Sensor Data																Detail Status		8-Bit CRC							
C[0]	C[3]	C[2]	C[1]	ST[1:0]		SD[11:0]												Optional SD resolution				SF[1:0]		CRC[7:0]							
Error Response to Register Request																															
Command				Basic Status		Unused Data = 0x0		Register Data: Contents of RA[7:1] High Byte								Register Data: Contents of RA[7:1] Low Byte								8-Bit CRC							
0	0	0	0	1	1	0	0	RD[15:8]								RD[7:0]								CRC[7:0]							
Error Response to Sensor Data Request With Sensor Data																															
Command				Basic Status		Sensor Data																Detail Status		8-Bit CRC							
C[0]	C[3]	C[2]	C[1]	1	1	SD[11:0]												Optional SD resolution				SF[1:0]		CRC[7:0]							
Error Response to Sensor Data Request Without Sensor Data																															
Command				Basic Status		x	Unused Data = 0x0000															Detail Status		8-Bit CRC							
0	0	0	0	1	1	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SF[1:0]		CRC[7:0]							

9.3 Command Summary

C[3:0]				Command Type	Data Source SOURCEID[2:0] = C[3:1]	Reference
0	0	0	0	Unused Command (Reserved for Error Response)	Not Applicable	Not Applicable
0	0	0	1	Sensor Data Request	SOURCEID[3:0] = 0x0	Section 9.3.3
0	0	1	0	Reserved Command	Not Applicable	Not Applicable
0	0	1	1	Sensor Data Request	SOURCEID[3:0] = 0x1	Section 9.3.3
0	1	0	0	Reserved Command	Not Applicable	Not Applicable
0	1	0	1	Sensor Data Request	SOURCEID[3:0] = 0x2	Section 9.3.3
0	1	1	0	Reserved Command	Not Applicable	Not Applicable
0	1	1	1	Sensor Data Request	SOURCEID[3:0] = 0x3	Section 9.3.3
1	0	0	0	Register Write Request	Not Applicable	Section 9.3.2
1	0	0	1	Sensor Data Request	SOURCEID[3:0] = 0x4	Section 9.3.3
1	0	1	0	Reserved Command	Not Applicable	Not Applicable
1	0	1	1	Sensor Data Request	SOURCEID[3:0] = 0x5	Section 9.3.3
1	1	0	0	Register Read Request	Not Applicable	Section 9.3.1
1	1	0	1	Sensor Data Request	SOURCEID[3:0] = 0x6	Section 9.3.3
1	1	1	0	Reserved Command	Not Applicable	Not Applicable
1	1	1	1	Sensor Data Request	SOURCEID[3:0] = 0x7	Section 9.3.3

9.3.1 Register Read Command

The device supports a Register Read command. The Register Read command uses the upper 7 bits of the addresses defined in Section 6.1 to address two 8-bit registers in the register map. The response to the command includes the contents of RA[7:1] high byte (RA[0] = 1) in the upper byte and the contents of RA[7:1] low byte (RA[0] = 0) in the lower byte.

The response to a register read command is shown in Section 9.3.1.2. The response is transmitted on the next SPI message if and only if all of the following conditions are met:

- No SPI Error is detected (Reference Section 9.5.4)
- No MISO Error is detected (Reference Section 9.5.5)

If the above conditions are met, the device responds to the register read request as shown in Section 9.3.1.2. Otherwise, the device responds with the Error Response as defined in Section 9.5.3. The Register Read response includes the register contents at the rising edge of SS_B for the Register Read command.

9.3.1.1 Register Read Command Message Format

MSB **LSB**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command C[3:0]				**Fixed Bits: Must = 0x0**				**Register Address**								**Register Data**								**8-Bit CRC**							
1	1	0	0	0	0	0	0	RA[7:1]							RA[0]	0	0	0	0	0	0	0	0	CRC[7:0]							

Bit Field	Definition
C[3:0]	Register Read Command = ‘1100’
RA[7:1]	RA[7:1] contains the word address of the register to be read.
CRC[7:0]	CRC. Reference Section 9.4

9.3.1.2 Register Read Response Message Format

MSB **LSB**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command C[0], [3:1]				**Basic Status**		**Unused Data = 0x0**		**Register Data: Contents of RA[7:1] High Byte**								**Register Data: Contents of RA[7:1] Low Byte**								**8-Bit CRC**							
0	1	1	0	ST[1:0]		0	0	RD[15:8]								RD[7:0]								CRC[7:0]							

Bit Field	Definition
C[0], [3:1]	Register Read Command = ‘0110’
ST[1:0]	Status. Reference Section 9.5.1
RD[15:8]	The contents of the register addressed by RA[7:1] High Byte (RA[0] = 1)
RD[7:0]	The contents of the register addressed by RA[7:1] Low Byte (RA[0] = 0)
CRC[7:0]	CRC. Reference Section 9.4

9.3.2 Register Write Command

The device supports a Register Write command. The Register Write command writes the value specified in RD[7:0] to the register addressed by RA[7:0]. The response to the command includes the new contents of RA[7:1] high byte (RA[0] = 1) in the upper byte and the contents of RA[7:1] low byte (RA[0] = 0) in the lower byte.

The response to a register write command is shown in Section 9.3.2.2. The register write is executed and a response is transmitted on the next SPI message if and only if all of the following conditions are met:

- No SPI Error is detected (Reference Section 9.5.4)
- The ENDINIT bit is cleared
  - This applies to all registers with the exception of the RESET[1:0] bits in the DEVLOCK_WR register

If the above conditions are met, the register write is executed and the device responds to the register write request as shown in Section 9.3.2.2. Otherwise, no register is written and the device responds with the Error Response as defined in Section 9.2. The register is not written until the transfer during which the register write was requested has been completed.

A register write command to a read only register will not execute, but will result in a valid response.

9.3.2.1 Register Write Command Message Format

MSB **LSB**

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><th colspan="4">Command C[3:0]</th><th colspan="4">Fixed Bits: Must = 0x0</th><th colspan="8">Register Address</th><th colspan="8">Register Data</th><th colspan="8">8-Bit CRC</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="7">RA[7:1]</td><td>RA[0]</td><td colspan="8">RD[7:0]</td><td colspan="8">CRC[7:0]</td></tr>
</table>

Bit Field	Definition
C[3:0]	Register Write Command = ‘1000’
RA[7:0]	RA[7:1] contains the byte address of the register to be written.
RD[7:0]	RD[7:0] contains the data byte to be written to address RA[7:0]
CRC[7:0]	CRC. Reference Section 9.4

9.3.2.2 Register Write Response Message Format

MSB **LSB**

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><th colspan="4">Command C[0], [3:1]</th><th colspan="2">Basic Status</th><th colspan="2">Unused Data = 0x0</th><th colspan="8">Register Data: Contents of RA[7:1] High Byte</th><th colspan="8">Register Data: Contents of RA[7:1] Low Byte</th><th colspan="8">8-Bit CRC</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="2">ST[1:0]</td><td>0</td><td>0</td><td colspan="8">RD[15:8]</td><td colspan="8">RD[7:0]</td><td colspan="8">CRC[7:0]</td></tr>
</table>

Bit Field	Definition
C[0], [3:1]	Register Write Command = ‘0100’
ST[1:0]	Status. Reference Section 9.5.1
RD[15:8]	The contents of the register addressed by RA[7:1] High Byte (RA[0] = 1)
RD[7:0]	The contents of the register addressed by RA[7:1] Low Byte (RA[0] = 0)
CRC[7:0]	CRC. Reference Section 9.4

9.3.3 Sensor Data Request Commands

The device supports standard sensor data request commands. The sensor data request command format is described in Section 9.3.3.1. The response to a sensor data request is shown in Section 9.3.3.2. The response is transmitted on the next SPI message subject to the error handling conditions specified in Section 9.5. The sensor data included in the response is the sensor data at the falling edge of SS_B for the Sensor Data Request response.

9.3.3.1 Sensor Data Request Command Message Format

MSB **LSB**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command				**Fixed Bits: Must = 0x00000**																				**8-Bit CRC**							
C[3:0]				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC[7:0]							

Bit Field	Definition
C[0]	Sensor Data Request Command = ‘1’
C[3:1] = SOURCEID[2:0]	Source Identification code for the requested sensor data. Reference Section 6.2.12.
CRC[7:0]	CRC. Reference Section 9.4

9.3.3.2 Sensor Data Request Response Message Format

MSB **LSB**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command C[0], [3:1]				**Basic Status**		**Sensor Data**																**Detail Status**		**8-Bit CRC**							
1	C[3]	C[2]	C[1]	ST[1:0]		SD[11:0]												Optional SD resolution				SF[1:0]		CRC[7:0]							

Bit Field	Definition
C[0]	Sensor Data Request Command = ‘1’
C[3:1] = SOURCEID[2:0]	Source Identification code for the requested sensor data. Reference Section 6.2.12.
ST[1:0]	Basic Status. Reference Section 9.5.1
SD[11:0]	Sensor Data. Reference Section 6.6.4.9
SF[1:0]	Detailed Status. Reference Section 9.5.2
CRC[7:0]	CRC. Reference Section 9.4

9.3.4 Reserved Commands

The device responds to reserved commands on the next SPI message subject to the error handling conditions specified in Section 9.5.

9.3.4.1 Reserved Command Message Format

MSB LSB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8-Bit CRC							
0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC[7:0]							
0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC[7:0]							
0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC[7:0]							
0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC[7:0]							
1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC[7:0]							
1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC[7:0]							

Bit Field	Definition
C[3:0]	Reserved Command
CRC[7:0]	CRC. Reference Section 9.4

9.3.4.2 Reserved Command Response Message Format

MSB LSB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command Echo				Data																				8-Bit CRC							
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC[7:0]							

Bit Field	Definition
Command Echo	Reserved Command Echo - Undefined
Data	Response Data - Undefined
CRC[7:0]	CRC. Reference Section 9.4

9.4 Error Checking

9.4.1 Default 8-bit CRC

9.4.1.1 Command Error Checking

The device calculates an 8-bit CRC on the entire 32-bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device responds with the SPI Error response.

The CRC decoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and Seed are shown below.

SPICRCSEED[3:0]	Default Polynomial	Default Non-Direct Seed
0000	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111
Non-Zero	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 SPICRCSEED[3:0]

Table 9-1 SPI Command Message CRC

Some example CRC calculations are shown in Table 9-3.

9.4.1.2 Response Error Checking

The device calculates a CRC on the entire 32-bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and Seed are shown below.

SPICRCSEED[3:0]	Default Polynomial	Default Non-Direct Seed
0000	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111
Non-Zero	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 SPICRCSEED[3:0]

Table 9-2 SPI Response Message CRC

Some example CRC calculations are shown in Table 9-3.

Polynomial	Seed	Bits[31:28]	Bits[27:24]	Bits[23:16]	Bits[15:8]	Bits[7:0]
		Command	0x0	Register Address	Register Data	8 Bit CRC
$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111	0x8	0x0	22	C1	0xBD
$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111	0x4	0x0	1F	C1	0x57
$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111	0xC	0x0	22	00	0x66
$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111	0x6	0x0	1F	C1	0xB8
$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111	0x4	0x0	FF	5A	0xE5
$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111	0xC	0x0	3E	00	0x13
$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111	0x6	0x0	FF	5A	0x0A

Table 9-3 SPI 8-Bit CRC Calculation Examples

9.4.2 Selectable 4-bit CRC

The user can select a 4-bit CRC instead of the default 8-bit CRC for the SPI by programming the SPI_CFG register as described in Section 6.2.19.

9.4.2.1 SPI Command Format with 4-bit CRC

MSB LSB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Access Command																															
Command				**Fixed Bits: Must = 0x0**				**Register Address**								**Register Data**								**Fixed Bits: Must = 0x0**				**4-Bit CRC**			
C[3:0]				0	0	0	0	RA[7:1]							RA[0]	RD[7:0]								0	0	0	0	CRC[3:0]			
Sensor Data Command																															
Command				**Fixed Bits: Must = 0x00000**																				**Fixed Bits: Must = 0x0**				**4-Bit CRC**			
C[3:0]				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC[3:0]			

9.4.2.2 SPI Response Format with 4-bit CRC

MSB LSB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Response to Register Request																															
Command				**Basic Status**		**Unused Data = 0x0**		**Register Data: Contents of RA[7:1] High Byte**								**Register Data: Contents of RA[7:1] Low Byte**								**Unused Data = 0x0**				**4-Bit CRC**			
C[0]	C[3]	C[2]	C[1]	ST[1:0]		0	0	RD[15:8]								RD[7:0]								0	0	0	0	CRC[3:0]			
Response to Sensor Data Request																															
Command				**Basic Status**		**Sensor Data**																**Detail Status**		**KAC**				**4-Bit CRC**			
C[0]	C[3]	C[2]	C[1]	ST[1:0]		SD[11:0]												Optional SD resolution				SF[1:0]		KAC[3:0]				CRC[3:0]			
Error Response to Register Request																															
Command				**Basic Status**		**Unused Data = 0x0**		**Register Data: Contents of RA[7:1] High Byte**								**Register Data: Contents of RA[7:1] Low Byte**								**Unused Data = 0x0**				**4-Bit CRC**			
0	0	0	0	1	1	0	0	RD[15:8]								RD[7:0]								0	0	0	0	CRC[3:0]			
Error Response to Sensor Data Request With Sensor Data																															
Command				**Basic Status**		**Sensor Data**																**Detail Status**		**KAC**				**4-Bit CRC**			
C[0]	C[3]	C[2]	C[1]	1	1	SD[11:0]												Optional SD resolution				SF[1:0]		KAC[3:0]				CRC[3:0]			
Error Response to Sensor Data Request Without Sensor Data																															
Command				**Basic Status**		**x**	**Unused Data = 0x0000**															**Detail Status**		**Unused Data = 0x0**				**4-Bit CRC**			
0	0	0	0	1	1	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SF[1:0]		0	0	0	0	CRC[3:0]			

9.4.2.3 Command Error Checking with 4-bit CRC

The device calculates a 4-bit CRC on the entire 32-bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device responds with the SPI Error response.

The CRC decoding procedure is:

1. A seed value determined by the SPICRCSEED[3:0] value in the SPI_CFG register is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and Seed are shown below.

Default Polynomial	Non-Direct Seed
$x^4 + 1$	SPICRCSEED[3:0]

Table 9-4 SPI Command Message CRC, 4-Bit

9.4.2.4 Response Error Checking with 4-bit CRC

The device calculates a CRC on the entire 32-bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value determined by the SPICRCSEED[3:0] value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds four zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and Seed are shown below.

Default Polynomial	Non-Direct Seed
$x^4 + 1$	SPICRCSEED[3:0]

Table 9-5 SPI Response Message CRC, 4-Bit

9.4.2.5 Message Counter (KAC) with 4-bit CRC

If the 4-bit CRC is enabled, a 4-bit message counter field (KAC) is added to the Sensor Data Request Response. The message counter field is a 4-bit rolling message counter that is independently incremented for each SOURCEID. The initial value of the counter is ‘0001’.

9.4.2.6 Example 4-Bit CRC Calculations

Some example CRC calculations for 32-bit SPI commands are shown in Table 9-6.

Polynomial	Seed	Bits[31:28]	Bits[27:24]	Bits[23:16]	Bits[15:8]	Bits[7:4]	Bits[3:0]
		Command	0x0	Register Address	Register Data	0x0	4 Bit CRC
$x^4 + 1$	1010	0x8	0x0	22	C1	0x0	0xF
$x^4 + 1$	1010	0x4	0x0	1F	C1	0x0	0xD
$x^4 + 1$	1010	0xC	0x0	22	00	0x0	0x6
$x^4 + 1$	1010	0x6	0x0	1F	C1	0x0	0xF
$x^4 + 1$	1010	0x4	0x0	FF	5A	0x0	0x1
$x^4 + 1$	1010	0xC	0x0	3E	00	0x0	0xB
$x^4 + 1$	1010	0x6	0x0	FF	5A	0x0	0x3

Table 9-6 SPI 4-Bit CRC Calculation Examples

9.4.3 Selectable 3-bit CRC

The user can select a 3-bit CRC instead of the default 8-bit CRC for the SPI by programming the SPI_CFG register as described in Section 6.2.19.

9.4.3.1 SPI Command Format with 3-bit CRC

MSB LSB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Access Command																															
Command				Fixed Bits: Must = 0x0				Register Address								Register Data								Fixed Bits: Must = 0x00					3-Bit CRC		
C[3:0]				0	0	0	0	RA[7:1]							RA[0]	RD[7:0]								0	0	0	0	0	CRC[2:0]		
Sensor Data Command																															
Command				Fixed Bits: Must = 0x00000																				Fixed Bits: Must = 0x00					3-Bit CRC		
C[3:0]				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC[2:0]		

9.4.3.2 SPI Response Format with 3-bit CRC

MSB LSB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Response to Register Request																															
Command				Basic Status		Unused Data = 0x0		Register Data: Contents of RA[7:1] High Byte								Register Data: Contents of RA[7:1] Low Byte								Unused Data = 0x00					3-Bit CRC		
C[0]	C[3]	C[2]	C[1]	ST[1:0]		0	0	RD[15:8]								RD[7:0]								0	0	0	0	0	CRC[2:0]		
Response to Sensor Data Request																															
Command				Basic Status		Sensor Data																Detail Status		KAC				1	3-Bit CRC		
C[0]	C[3]	C[2]	C[1]	ST[1:0]		SD[11:0]												Optional SD resolution				SF[1:0]		KAC[3:0]				1	CRC[2:0]		
Error Response to Register Request																															
Command				Basic Status		Unused Data = 0x0		Register Data: Contents of RA[7:1] High Byte								Register Data: Contents of RA[7:1] Low Byte								Unused Data = 0x00					3-Bit CRC		
0	0	0	0	1	1	0	0	RD[15:8]								RD[7:0]								0	0	0	0	0	CRC[2:0]		
Error Response to Sensor Data Request With Sensor Data																															
Command				Basic Status		Sensor Data																Detail Status		KAC				1	3-Bit CRC		
C[0]	C[3]	C[2]	C[1]	1	1	SD[11:0]												Optional SD resolution				SF[1:0]		KAC[3:0]				1	CRC[2:0]		
Error Response to Sensor Data Request Without Sensor Data																															
Command				Basic Status		x	Unused Data = 0x0000															Detail Status		Unused Data = 0x00					3-Bit CRC		
0	0	0	0	1	1	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SF[1:0]		0	0	0	0	0	CRC[2:0]		

9.4.3.3 Command Error Checking with 3-bit CRC

The device calculates a 3-bit CRC on the entire 32-bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device responds with the SPI Error response.

The CRC decoding procedure is:

1. A seed value determined by the SPICRCSEED[2:0] value in the SPI_CFG register is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and Seed are shown below.

Default Polynomial	Non-Direct Seed
$x^3 + x + 1$	SPICRCSEED[2:0]

Table 9-7 SPI Command Message CRC, 3-Bit

Some example CRC calculations are shown in Table 8-1.

9.4.3.4 Response Error Checking with 3-bit CRC

The device calculates a CRC on the entire 32-bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value determined by the SPICRCSEED[2:0] value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds three zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and Seed are shown below.

Default Polynomial	Non-Direct Seed
$x^3 + x + 1$	SPICRCSEED[2:0]

Table 9-8 SPI Response Message CRC, 3-Bit

9.4.3.5 Message Counter (KAC) with 3-bit CRC

If the 3-bit CRC is enabled, a 4-bit message counter field (KAC) is added to the Sensor Data Request Response. The message counter field is a 4-bit rolling message counter that is independently incremented for each SOURCEID. The initial value of the counter is ‘0001’.

9.4.3.6 Example 3-Bit CRC Calculations

Some example CRC calculations for 32-bit SPI commands are shown in Table 9-9.

Polynomial	Seed	Bits[31:28]	Bits[27:24]	Bits[23:16]	Bits[15:8]	Bits[7:3]	Bits[2:0]
		Command (Hex)	0x0 (Hex)	Register Address (Hex)	Register Data (Hex)	0b00000 (Binary)	3 Bit CRC (Binary)
$x^3 + x + 1$	111	0x8	0x0	22	C1	0b00000	0b100
$x^3 + x + 1$	111	0x4	0x0	1F	C1	0b00000	0b010
$x^3 + x + 1$	111	0xC	0x0	22	00	0b00000	0b001
$x^3 + x + 1$	111	0x6	0x0	1F	C1	0b00000	0b000
$x^3 + x + 1$	111	0x4	0x0	FF	5A	0b00000	0b000
$x^3 + x + 1$	111	0xC	0x0	3E	00	0b00000	0b101
$x^3 + x + 1$	111	0x6	0x0	FF	5A	0b00000	0b010

Table 9-9 SPI 3-Bit CRC Calculation Examples

9.5 Exception Handling

9.5.1 Basic Status Field

All responses include a basic status field (ST[1:0]) that includes the general status of the device and transmitted data as described below. The basic status includes channel specific data and may be unique by channel but will be common for multiple sources from the same channel. The contents of the basic status field is a representation of the device status at the rising edge of SS_B for the previous SPI command.

9.5.1.1 Basic Status Field for Responses to Register Commands

ST[1:0]		Status	Description	SF[1:0]		Priority
0	0	Device in Initialization	ENDINIT Not Set	0	0	3
0	1	Normal Mode	ENDINIT Set	0	0	4
1	0	Self Test	ST_CTRL[3:0] not equal to '0000' for any channel	0	0	2
1	1	Internal Error Present	Reference Section 9.5.2	Reference Section 9.5.2		1

9.5.1.2 Basic Status Field for Responses to Sensor Data Request Commands

ST[1:0]		Status	Description	SF[1:0]		Sensor Data Field	Priority
0	0	Device in Initialization	ENDINIT Not Set	0	0	Sensor Data	3
0	1	Normal Mode	ENDINIT Set	0	0	Sensor Data	4
1	0	Self Test	ST_CTRL[3:0] not equal to '0000' for the associated channel	0	0	Sensor Data	2
1	1	Internal Error Present	Reference Section 9.5.2	Reference Section 9.5.2		Reference Section 9.5.2	1

Figure 9-2 shows the internal device status mapping by register and the basic status field contents by response type.

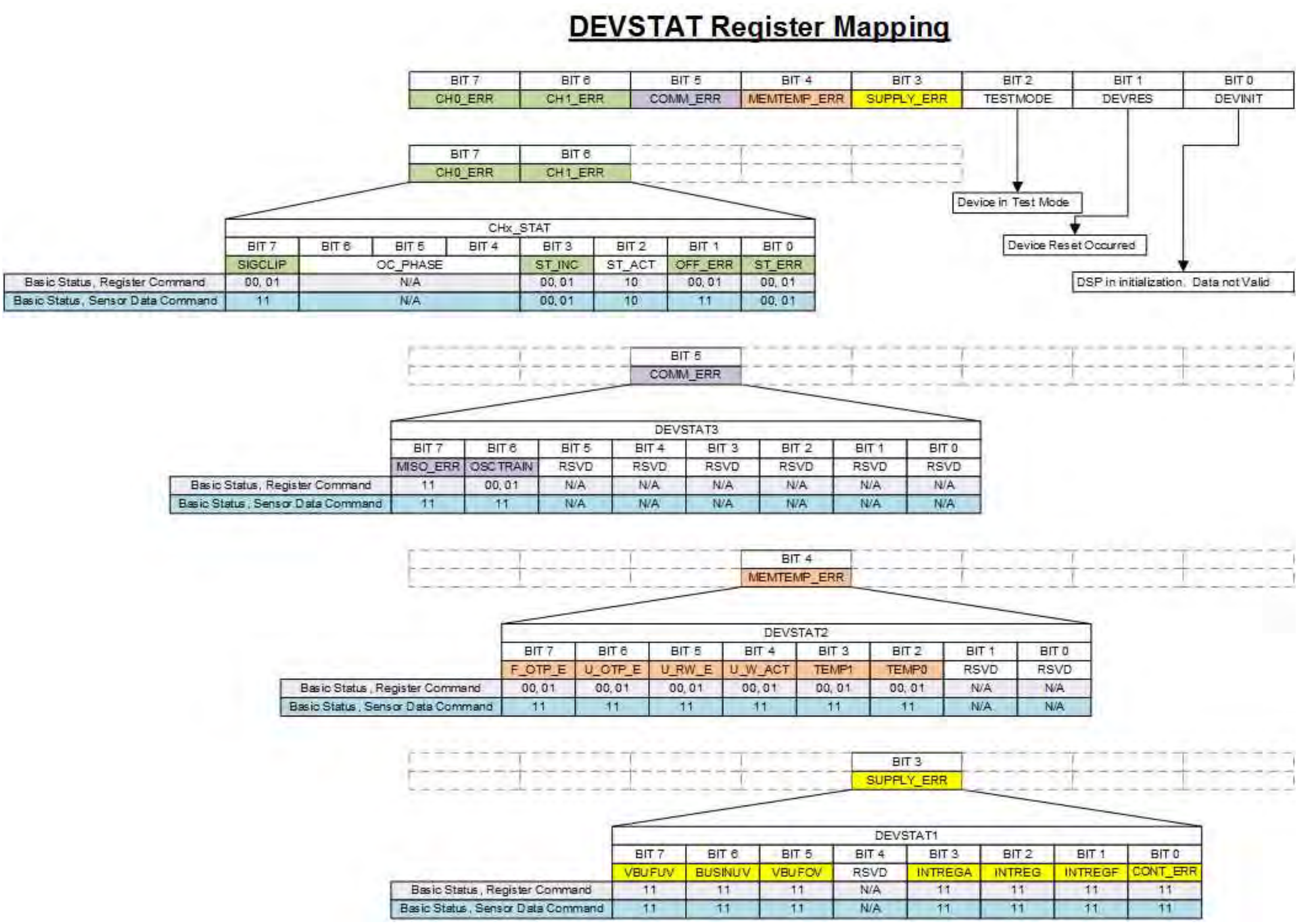


Figure 9-2 Internal Status Mapping and SPI Basic Status Content

9.5.2 Detailed Status Field

The response to sensor data requests includes a detailed status field (SF[1:0]). If the Basic Status indicates an internal error, the contents of the detailed status field provide additional information regarding the error status. The detailed status includes channel specific data and may be unique by channel but will be common for multiple sources from the same channel. The contents of the detailed status field is a representation of the device status at the rising edge of SS_B for the previous SPI command.

ST[1:0]		SF[1:0]		Status Sources	DEVSTAT State	SUPERR_DIS State	Error Priority	Command Echo Field (Source ID)	Sensor Data Request Commands Sensor Data Field Value	Register Access Command Response	PCM
1	1	0	0	Oscillator Training Error	Bit set in DEVSTAT3	N/A	11	C[0], C[3:1]	Sensor Data	Normal	No Effect
				Offset Error	Bit set in CHx_STAT: SIGNALCLIP or OFF-SET_ERR	N/A	10	C[0], C[3:1]	Sensor Data	Normal	No Effect
				Temperature Error	Bit set in DEVSTAT2	N/A	9	C[0], C[3:1]	Sensor Data	Normal	No Effect
1	1	0	1	User OTP Memory Error (UF0 or UF1)	U_OTP_ERR set in DEVSTAT2	N/A	8	0x0	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	Normal	No Effect
				User R/W Memory Error (UF2)	U_RW_ERR set in DEVSTAT2	N/A	7	0x0	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	Normal	No Effect
				NXP OTP Memory Error	F_OTP_ERR set in DEVSTAT2	N/A	6	0x0	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	Normal	No Effect
1	1	1	0	Test Mode Active	TESTMODE bit set in DEVSTAT	N/A	5	0x0	All zero response		No Effect
				Supply Error	Bit set in DEVSTAT1	0	4	0x0	All zero response until the supply monitor timer expires An Error Code is transmitted for a minimum of one transmission (Reference Section 6.2.2.5)		Disabled
						1	4	0x0	All zero response until the supply monitor timer expires (Reference Section 6.2.2.5)		
				Reset Error	DEVRES set	N/A	3	0x0	The Sensor Data Field Error Code is transmitted for a minimum of one transmission		No Effect
1	1	1	1	MISO Error	Bit set in DEVSTAT3	N/A	2	0x0	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	Error Response	No Effect
				SPI Error	N/A	N/A	1	0x0	The Sensor Data Field Error Code is transmitted for a minimum of one transmission	Error Response	No Effect

Table 9-10 SPI Error Response Status Field Definition

9.5.3 Error Responses

MSB **LSB**

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">Error Response to Register Request</td></tr>
<tr><td colspan="4">Command</td><td colspan="2">Basic Status</td><td colspan="2">Unused Data = 0x0</td><td colspan="8">Register Data: Contents of RA[7:1] High Byte</td><td colspan="6">Register Data: Contents of RA[7:1] Low Byte</td><td colspan="2">Detail Status</td><td colspan="8">8-Bit CRC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="8">RD[15:8]</td><td colspan="6">RD[7:0]</td><td colspan="2">SF[1:0]</td><td colspan="8">CRC[7:0]</td></tr>
<tr><td colspan="32">Error Response to Sensor Data Request With Sensor Data</td></tr>
<tr><td colspan="4">Command</td><td colspan="2">Basic Status</td><td colspan="16">Sensor Data</td><td colspan="2">Detail Status</td><td colspan="8">8-Bit CRC</td></tr>
<tr><td>C[0]</td><td>C[3]</td><td>C[2]</td><td>C[1]</td><td>1</td><td>1</td><td colspan="12">SD[11:0]</td><td colspan="4">Optional SD resolution</td><td colspan="2">SF[1:0]</td><td colspan="8">CRC[7:0]</td></tr>
<tr><td colspan="32">Error Response to Sensor Data Request Without Sensor Data</td></tr>
<tr><td colspan="4">Command</td><td colspan="2">Basic Status</td><td>x</td><td colspan="15">Unused Data = 0x0000</td><td colspan="2">Detail Status</td><td colspan="8">8-Bit CRC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">SF[1:0]</td><td colspan="8">CRC[7:0]</td></tr>
</table>

Bit Field	Definition
C[3:0]	Command bits: all 0s or a command echo
SD[11:0]	Sensor Data or the Sensor Data Field Error Code. • For unsigned data, the Sensor Data Field Error Code is 0x000 • For signed data, the Sensor Data Field Error Code is 0x800 Reference Section 9.5.2 for Sensor Data Request commands. For all other commands, all bits are ‘0’.
SF[3:0]	Status. Reference Section 9.5.2

9.5.4 SPI Error

The following external SPI conditions result in a SPI error:

- SCLK is high when SS_B is asserted
- The number of SCLK rising edges detected while SS_B is asserted is not equal to 0 or 32
- SCLK is high when SS_B is deasserted
- A command message CRC error is detected (MOSI)
- A Sensor Data Request is received for a SOURCEID that is not enabled
- A Register Write command to any register other than the DEVLOCK_WR register is received while ENDINIT is set.

If a SPI error is detected, the device responds with the Error Response as described in Section 9.5.3 with the Detailed Status Field set to “SPI Error” as defined in Section 9.5.2.

9.5.5 SPI Data Output Verification Error

The device includes a function to verify the integrity of the data output to the MISO pin. The function compares the data transmitted on the MISO pin to the data intended to be transmitted. If any one bit doesn’t match, a SPI MISO Mismatch Fault is detected and the MISO_ERR flag in the DEVSTAT3 register is set.

If a valid sensor data request message is received during the SPI transfer with the MISO mismatch failure, the request is ignored and the device responds with the Error Response as described in Section 9.5.3 with the Detailed Status Field set to “SPI Error” as defined in Section 9.5.2. during the subsequent SPI message.

If a valid register write request message is received during the SPI transfer with the MISO mismatch failure, the register write is completed as requested, but the device responds with the Error Response as described in Section 9.5.3 with the Detailed Status Field set to “SPI Error” as defined in Section 9.5.2. during the subsequent SPI message.

If a valid register read request message is received during the SPI transfer with the MISO mismatch failure, the register read is ignored and the device responds with the Error Response as described in Section 9.5.3 with the Detailed Status Field set to “SPI Error” as defined in Section 9.5.2. during the subsequent SPI message.

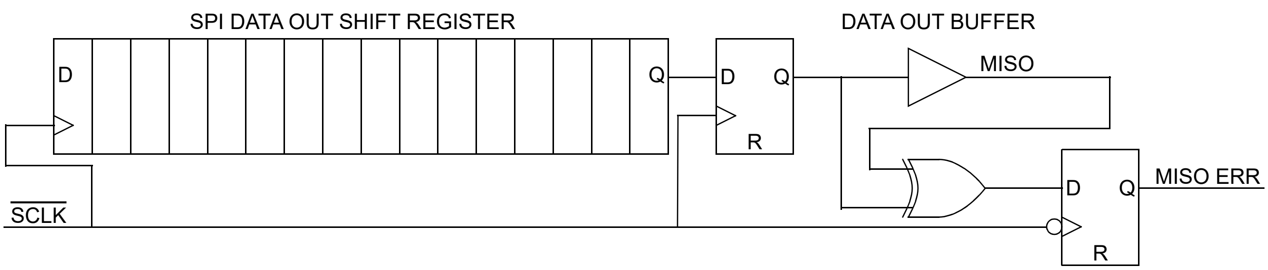


Figure 9-3 SPI Data Output Verification

9.6 SPI Timing Diagram

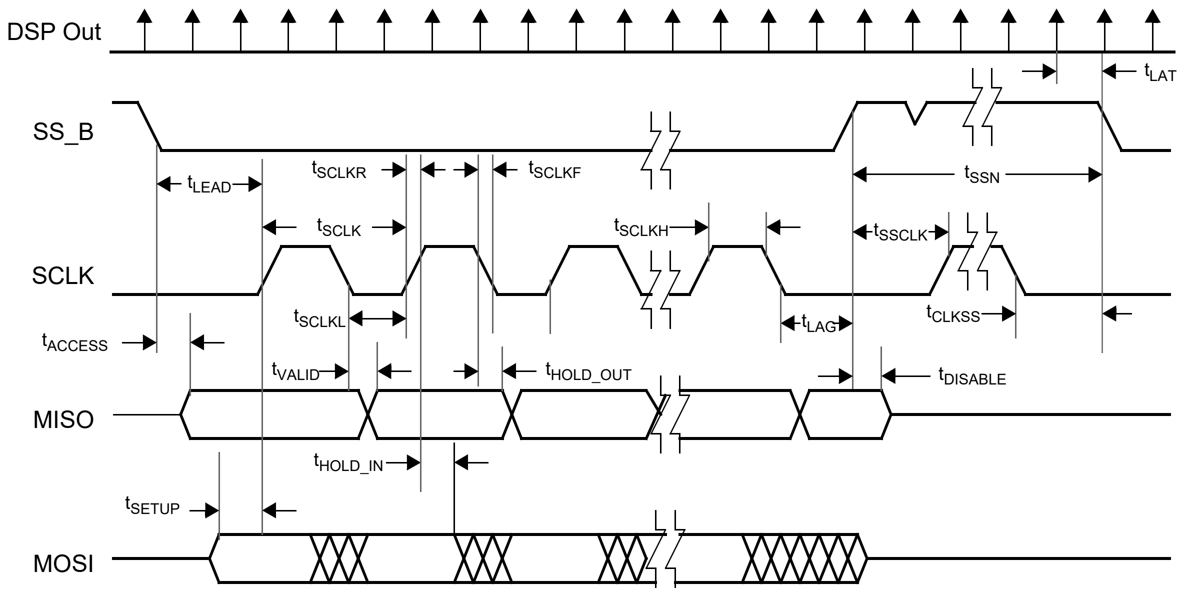


Figure 9-4 SPI Timing Diagram

SECTION 10 INTER INTEGRATED CIRCUIT (I^2C) INTERFACE

The device includes an interface compliant to the NXP I^2C bus specification UM10204, Revision 5. The device operates in slave mode and includes support for Standard Mode, Fast Mode and Fast Mode Plus although the maximum practical operating frequency for I^2C in a given system implementation depends on several factors including the pull-up resistor values and the total bus capacitance.

10.1 I^2C Bit Transmissions

The state of SDA when SCL is high determines the bit value being transmitted. SDA must be stable when SCL is high and change when SCL is low as shown in Figure 10-2. After the START signal has been transmitted by the master, the bus is considered busy. Timing for the start condition is specified in Section 5.14.

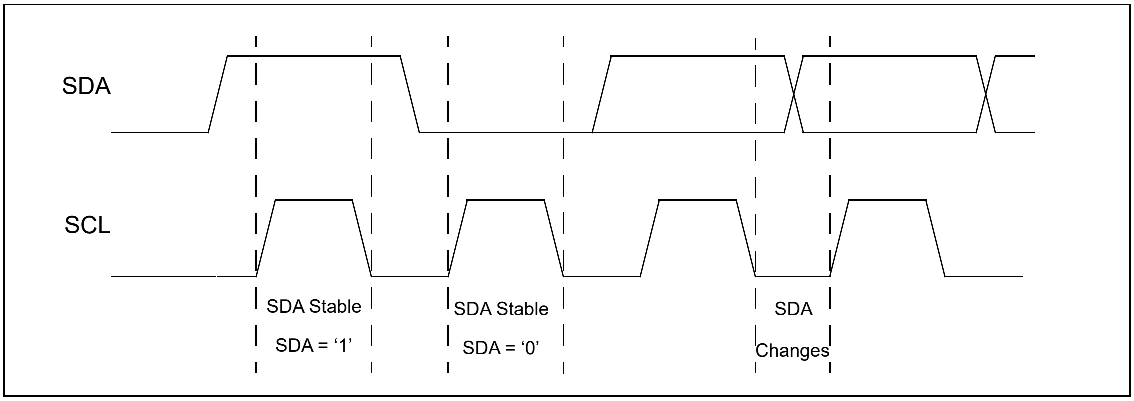


Figure 10-1 I^2C Bit Transmissions

10.2 I^2C Start Condition

A bus operation is always started with a start condition (START) from the master. A START is defined as a high to low transition on SDA while SCL is high as shown in Figure 10-2. After the START signal has been transmitted by the master, the bus is considered busy. Timing for the start condition is specified in Section 5.14.

A start condition (START) and a repeat START condition (rSTART) are identical.

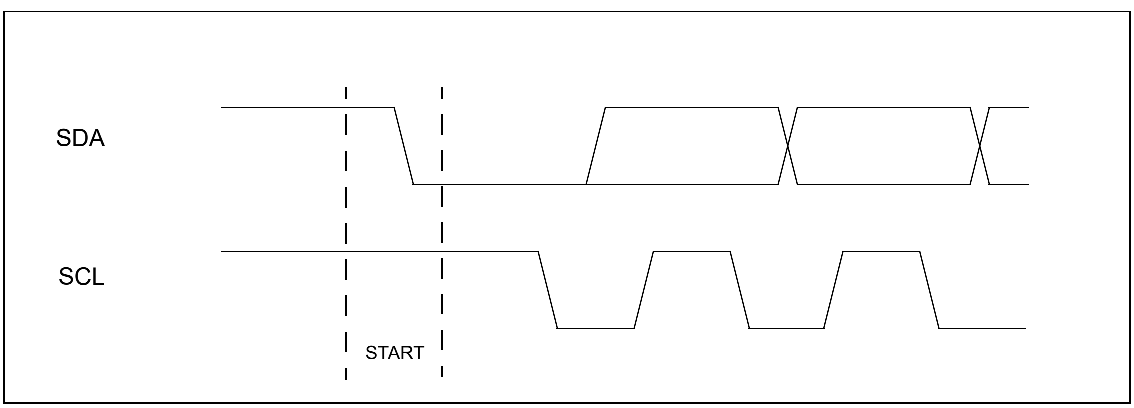


Figure 10-2 I^2C Start Condition

10.3 I²C Byte Transmissions

Data transfers are completed in byte increments. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit (Section 10.4) from the receiver. Data is transferred with the Most Significant Bit (MSB) first (Figure 10-3). The master generates all clock pulses, including the 9th clock for the Acknowledge bit. Timing for the byte transmissions is specified in Section 5.14.

All functions for this device are completed within the Acknowledge clock pulse. Clock Stretching is not used.

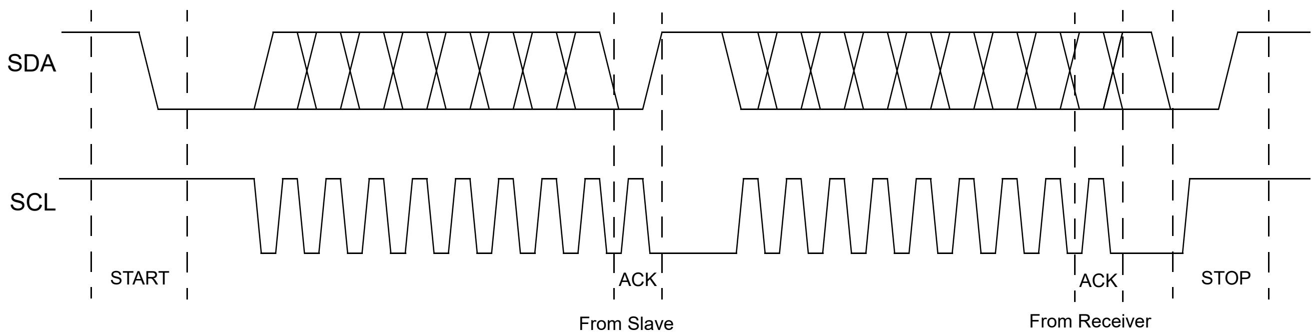


Figure 10-3 I²C Byte Transmissions

10.4 I²C Acknowledge and Not Acknowledge Transmissions

Each byte must be followed by an Acknowledge bit (ACK) from the receiver. For an ACK, the transmitter releases SDA during the acknowledge clock pulse and the receiver pulls SDA low during the high portion of the clock pulse. Set-up and hold times as specified in Section 5.14 must also be taken into account.

For a Not Acknowledge bit (NACK), SDA remains high during the entire acknowledge clock pulse. Five conditions lead to a NACK:

1. No receiver is present on the bus with the transmitted address.
2. The addressed receiver is unable to receive or transmit because it is performing some real-time function and is not ready to start communication with the master.
3. The receiver receives unrecognized data or commands.
4. The receiver cannot receive any more data bytes.
5. The master-receiver signals the end of the transfer to the slave transmitter.

Following a Not Acknowledge bit, the master can transmit either a STOP to terminate the transfer, or a repeated START to initiate a new transfer.

An example ACK and NACK are shown in Figure 10-4.

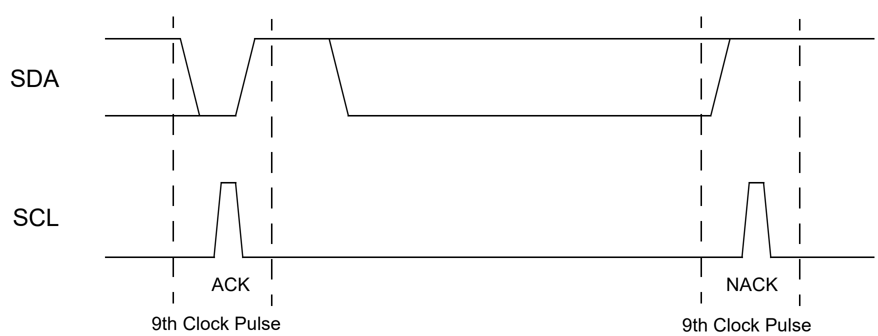


Figure 10-4 I²C Acknowledge and Not Acknowledge Transmission

10.5 I^2C Stop Condition

A bus operation is always terminated with a stop condition (STOP) from the master. A STOP is defined as a Low to high transition on SDA while SCL is high as shown in Figure 10-5. After the STOP has been transmitted by the master, the bus is considered free. Timing for the stop condition is specified in Section 5.14.

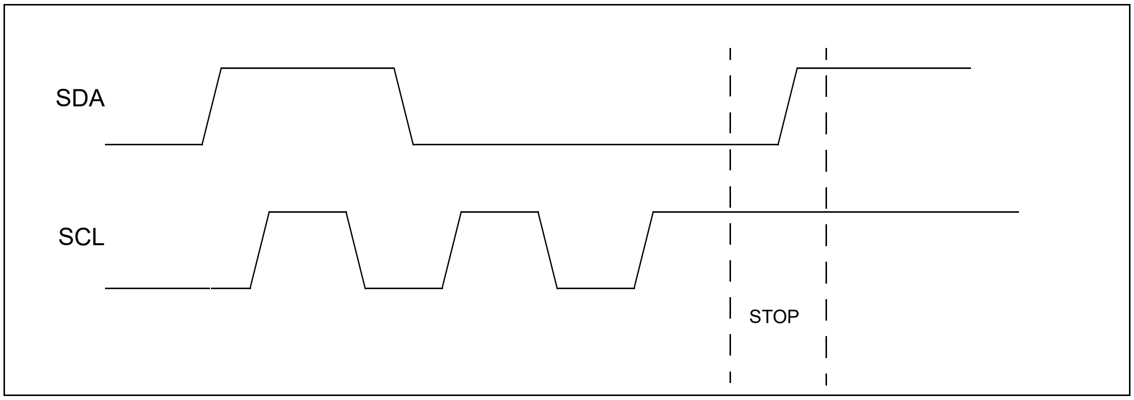


Figure 10-5 I^2C Stop Condition

10.6 I^2C Register Transfers

10.6.1 Register Write Transfers

The device supports I^2C register write data transfers. Register write data transfers are constructed as follows:

1. The Master transmits a START condition
2. The Master transmits the 7-Bit Slave Address
3. The Master transmits a ‘0’ for the Read/Write Bit to indicate a Write operation
4. The Slave transmits an ACK
5. The Master transmits the register address to be written
6. The Slave transmits an ACK
7. The Master transmits the data byte to be written to the register address
8. The Slave transmits an ACK
9. The master transmits a STOP condition

The device automatically increments the register address allowing for multiple register writes to be completed in one transaction. In this case, the register write data transfers are constructed as follows:

1. The Master transmits a START condition
2. The Master transmits the 7-Bit Slave Address
3. The Master transmits a ‘0’ for the Read/Write Bit to indicate a Write operation
4. The Slave transmits an ACK
5. The Master transmits the register address to be written
6. The Slave transmits an ACK
7. The Master transmits the data byte to be written to the register address
8. The Slave transmits an ACK
9. The Master transmits the data byte to be written to the register address +1
10. The Slave transmits an ACK
11. Repeat steps 9 and 10 until all registers are written
12. The master transmits a STOP condition

10.6.2 Register Read Transfers

The device supports I^{2}C register read data transfers. Register read data transfers are constructed as follows:

1. The Master transmits a START condition
2. The Master transmits the 7-Bit Slave Address
3. The Master transmits a ‘0’ for the Read/Write Bit to indicate a Write operation
4. The Slave transmits an ACK
5. The Master transmits the register address to be read
6. The Slave transmits an ACK
7. The Master transmits a repeat START condition
8. The Master transmits the 7-Bit Slave Address
9. The Master transmits a ‘1’ for the Read/Write Bit to indicate a Read operation
10. The Slave transmits an ACK
11. The Slave transmits the data from the register addressed
12. The master transmits a NACK
13. The master transmits a STOP condition

S	SLAVE ADDRESS	$\overline{W}$	A	REGISTER ADDRESS	A	rSTART	SLAVE ADDRESS	R	A	REGISTER DATA	N	P

Master Transmission
Slave Transmission

The device automatically increments the register address allowing for multiple register reads to be completed in one transaction. In this case, the register read data transfers are constructed as follows:

1. The Master transmits a START condition
2. The Master transmits the 7-Bit Slave Address
3. The Master transmits a ‘0’ for the Read/Write Bit to indicate a Write operation
4. The Slave transmits an ACK
5. The Master transmits the register address to be read
6. The Slave transmits an ACK
7. The Master transmits a repeat START condition
8. The Master transmits the 7-Bit Slave Address
9. The Master transmits a ‘1 for the Read/Write Bit to indicate a Read operation
10. The Slave transmits an ACK
11. The Slave transmits the data from the register addressed
12. The Master transmits an ACK
13. The Slave transmits the data byte from register address +1
14. Repeat steps 12 and 13 until all registers are read
15. The Master transmits a NACK
16. The master transmits a STOP condition

10.6.3 Sensor Data Register Read Wrap Around Options

The device includes automatic sensor data register read wrap around features to optimize the number of I2C transactions necessary for continuous reads of sensor data.

10.6.3.1 Single Channel Register Read Wrap Around

Depending on the state of the SIDx_EN bits in the channel 0 and channel 1 SOURCEID_0 and SOURCEID_1 registers, the register address automatically wraps back to the DEVSTAT_COPY register as shown in the table below.

Ch1 SID1_EN	Ch1 SID0_EN	Ch0 SID1_EN	Ch0 SID0_EN	Address Increment and Wrap Around Effect	Optimized Register Read Sequence
0	0	0	0	Address wraps around from $FF to $00	None
0	0	0	1	Address wraps from $63 (CH0_SNSDATA0_H) to $61 (DEVSTAT_COPY)	DEVSTAT_COPY, CH0_SNSDATA0_L, CH0_SNSDATA0_H
0	0	1	x	Address wraps from $65 (CH0_SNSDATA1_H) to $61 (DEVSTAT_COPY)	DEVSTAT_COPY, CH0_SNSDATA0_L, CH0_SNSDATA0_H, CH0_SNSDATA1_L, CH0_SNSDATA1_H
0	1	x	x	Address jumps from $65 (CH0_SNSDATA1_H) to $72 (CH1_SNSDATA0_L) Address wraps from $73 (CH1_SNSDATA1_H) to $61 (DEVSTAT_COPY)	DEVSTAT_COPY, CH0_SNSDATA0_L, CH0_SNSDATA0_H, CH0_SNSDATA1_L, CH0_SNSDATA1_H, CH1_SNSDATA0_L, CH1_SNSDATA0_H
1	x	x	x	Address jumps from $65 (CH0_SNSDATA1_H) to $72 (CH1_SNSDATA0_L) Address wraps from $75 (CH1_SNSDATA1_H) to $61 (DEVSTAT_COPY)	DEVSTAT_COPY, CH0_SNSDATA0_L, CH0_SNSDATA0_H, CH0_SNSDATA1_L, CH0_SNSDATA1_H, CH1_SNSDATA0_L, CH1_SNSDATA0_H, CH1_SNSDATA1_L, CH1_SNSDATA1_H

10.7 I²C Timing Diagram

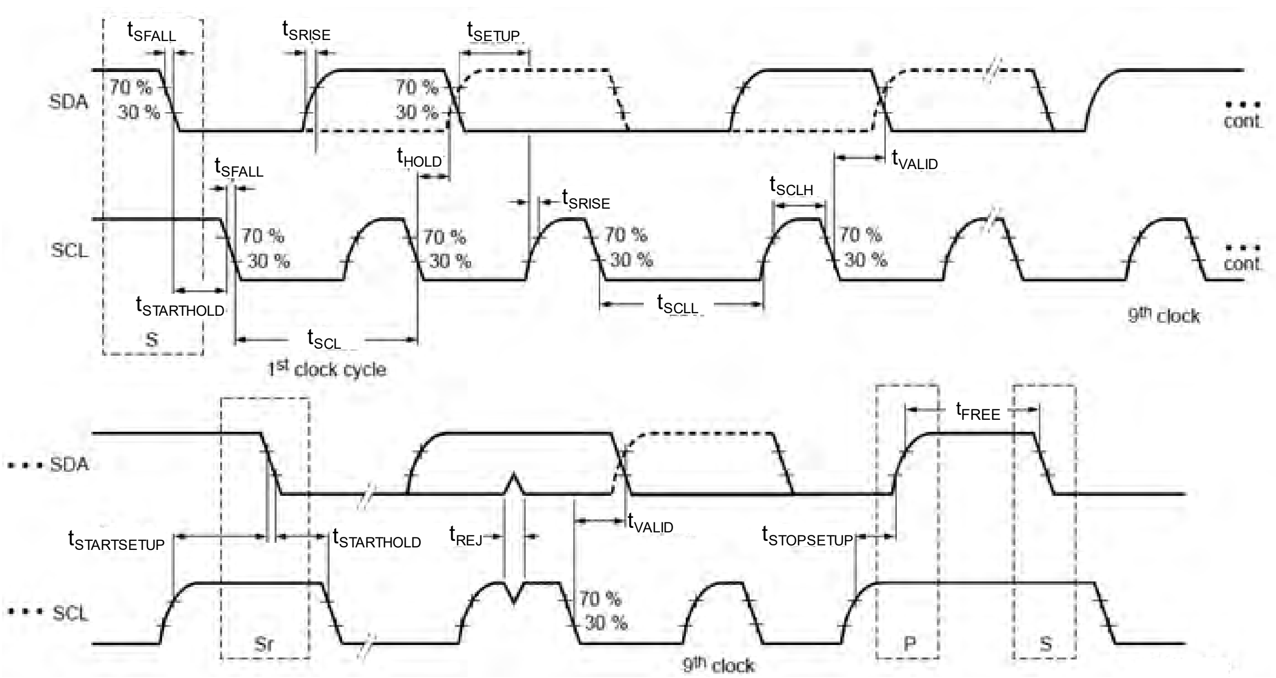


Figure 10-6 I²C Timing Diagram

SECTION 11 PACKAGE DIMENSIONS AND RECOMMENDED FOOTPRINT

Reference the NXP Case Outline Drawing SOT1688 at the following link for package dimensions and recommended footprint information:

http://www.nxp.com/packages

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support