IQS323 DATASHEET

3 Channel Self-Capacitive / 3 Channel Mutual-Capacitive / 2 Channel Inductive sensing controller with Touch and Proximity user interfaces. The device features an I²C communications interface, low power options, wear detection, metal detection and a slider with on-chip gesture calculations

1 Device Overview

The IQS323 ProxFusion® IC is a sensor fusion device for various single and dual-channel sensing requirements. Applications include proximity and touch buttons, sliders, metal sensors and wear detection pairs. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 3 external sensor pad connections
- Configure multiple channels on external pins (Self/Mutual/Inductive).
- External sensor options:
  - 3 self capacitive buttons
  - Up to 2 wear detection pairs (with shared physical reference)
  - 3 mutual capacitive touch/proximity sensors
  - 2 inductive mode sensors
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Differential measurements (reference channels)
  - Debounce & Hysteresis
  - Dual direction trigger indication
  - Halt Mode
- Built-in Signal processing options:
  - Touch/Prox output
  - Slider output
  - Gesture output
  - Reference User Interface
  - Release User Interface
- Design simplicity
  - PC Software for debugging & optimal setup for performance
- Automated system power modes for optimal response vs consumption
  - Distributed ultra low power (ULP) mode
- I²C communication interface with IRQ/RDY(up to fast plus - 1MHz)
- Event and streaming modes
- Supply Voltage 1.8V(-5%)to 3.5V
- Package options
  - WLCSP11 (1.48 x 1.08 x 0.345 mm) - interleaved 0.35mm x 0.35mm ball pitch
  - DFN12 (3 x 3 x 0.75 mm) - 0.5mm pitch

1.2 Applications

- TWS earphones
- Wear Detection
- Waterproof Buttons (Inductive)
- Low power Wake-up Buttons / Proximity
- Watches and fitness bands
- SAR Safety Sensor

1.3 Block Diagram

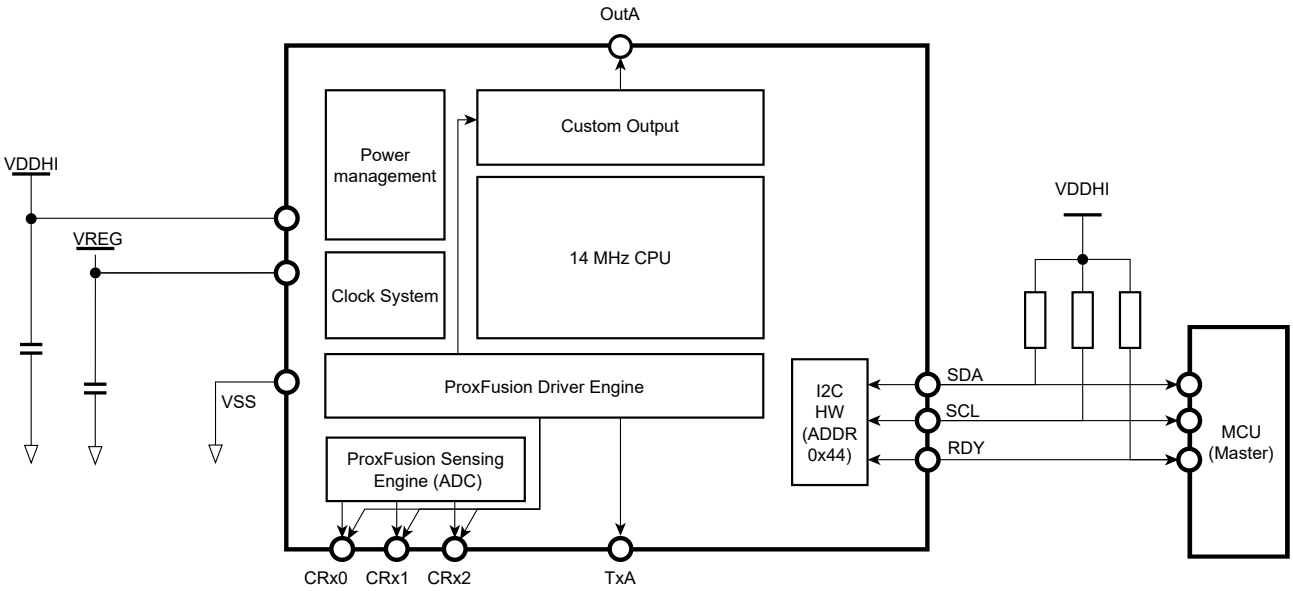

Figure 1.1: Functional Block Diagram

Contents

2 Hardware Connection

2.1 WLCSP11 Pin Diagram

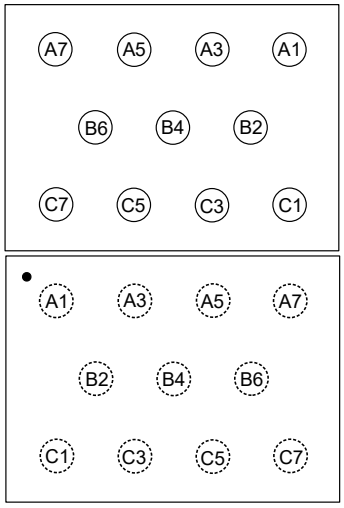

Table 2.1: 11-pin WLCSP11 Package

Pin no.	Signal
A7	VSS
A5	SDA
A3	VREG
A1	CRx1/CTx1
B6	TxA
B4	OutA
B2	CRx0/CTx0
C7	RDY/MCLR
C5	VDD
C3	SCL
C1	CRx2/CTx2/Bias

2.2 DFN12 Pin Diagram

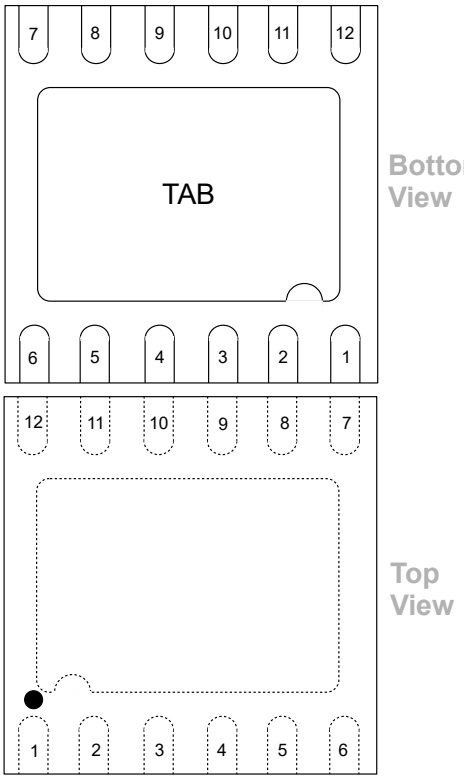

Table 2.2: 12-pin DFN Package

Pin no.	Signal
1	TxA
2	SDA
3	VDD
4	VREG
5	SCL
6	CRx2/CTx2/Bias
7	CRx0/CTx0
8	NC
9	CRx1/CTx1
10	OutA
11	RDY/MCLR
12	VSS

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP11	DFN12				
B6	1	TxA	Digital		VREG
A5	2	SDA	Digital		VDD
C5	3	VDD	Power	Power	N/A
A3	4	VREG	Power	Power	N/A
C3	5	SCL	Digital		VDD
C1	6	CRx2/CTx2/Bias	Analog		VREG
B2	7	CRx0/CTx0	Analog		VREG
-	8	NC	N/A		N/A
A1	9	CRx1/CTx1	Analog		VREG
B4	10	OutA	Digital		VDD
C7	11	RDY/MCLR	Digital		VDD
A7	12	VSS	Power	Power	N/A

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[i]	Description
		WLCSP11	DFN12		
ProxFusion®	CRx0/CTx0	B2	7	IO	ProxFusion® channel
	CRx1/CTx1	A1	9	IO	
	CRx2/CTx2/Bias	C1	6	IO	
	TxA	B6	1	O	TxA pad
	OutA	B4	10	O	OutA pad
GPIO	RDY/MCLR	C7	11	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP
I^2C	SDA	A5	2	IO	I^2C Data
	SCL	C3	5	IO	I^2C Clock
Power	VDD	C5	3	P	Power supply input voltage
	VREG	A3	4	P	Internal regulated supply output
	VSS	A7	12	P	Analog/Digital Ground

[i] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

2.5 Reference Schematic

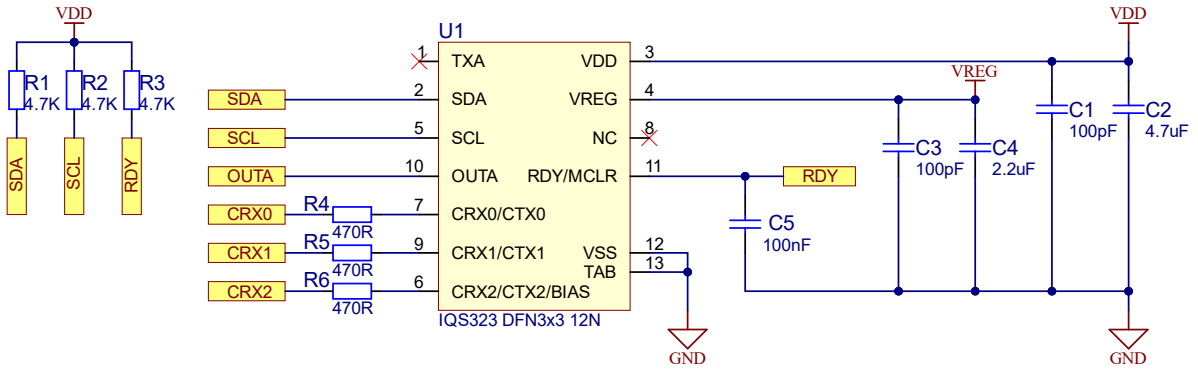

Figure 2.1: 3 Button Self Capacitance Reference Schematic

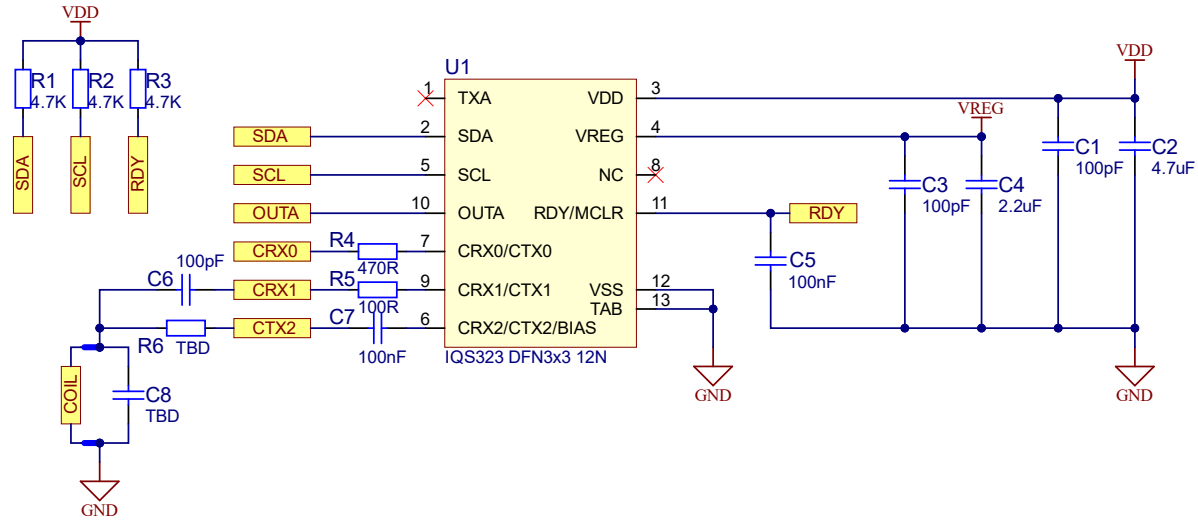

Figure 2.2: Single Proximity/Touch Key and Inductive Sensing Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.5V max)	V
Storage temperature, T_{stg}	-40	85	°C

3.2 Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin	1.71		3.5	V
VREG	Internal regulated supply output for analog domain		1.53		V
VSS	Supply voltage applied at VSS pin	0	0	0	V
T_A	Operating free-air temperature	-40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2*C_{VREG}$	$3*C_{VREG}$		µF
C_{VREG}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	2	5	13	µF
$Cx_{\_SELF\text{-}VSS}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (self-capacitance mode)	-	-	400	pF
$Cm_{\_CTX\text{-}CRX}$	Capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.1	-	9	pF
$Cx_{\_CRX\text{-}VSS\text{-}1M}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @f_{xfer}=1MHz)			100	pF
$Cx_{\_CRX\text{-}VSS\text{-}4M}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @ f_{xfer}=4MHz sensing)			25	pF
$\frac{Cx_{CRX-VSS}}{Cm_{CTX-CRX}}$	Capacitance ratio for optimal SNR in mutual capacitance mode	10		20	n/a
$RCx_{\_CRX/CTX}$	Series (in-line) resistance of all mutual capacitance pins (Tx & Rx pins) in mutual capacitance mode	0[i]	0.47	10[ii]	kΩ
$RCx_{\_SELF}$	Series (in-line) resistance of all self capacitance pins in self capacitance mode	0[i]	0.47	10[ii]	kΩ

3.3 ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[iii]	± 2000	V

[i] Nominal series resistance of 470Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection

[ii] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. R_{max} x C_{max} = $\frac{1}{(6xf_{xfer})}$ where "C" is the pin capacitance to Vss.

[iii] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

3.4 Current Consumption

Inductive Mode Setup: ATI Target = 256, F_{OSC} = 14MHz
Self-capacitive Mode Setup: ATI Target = 512, F_{xfer} = 500kHz
Mutual capacitive Mode Setup: ATI Target = 512, F_{xfer} = 500kHz
Interface Selection: Event mode

Power mode	Active channels	Report rate [ms]	Typical Current [µA]	
			1.8V	3.3V
Normal Power	Inductive (1 coil)	10	127.64	129.27
	Self-capacitive (3 channels)	16	124.64	125.20
	Mutual Capacitive (2 channels)	16	170.83	171.76
Low Power	Inductive (1 coil)	80	10.83	11.38
	Self-capacitive (3 channels)	60	37.08	37.31
	Mutual Capacitive (2 channels)	60	49.76	50.26
Ultra Low Power	Inductive (1 coil)	200	6.39	6.68
	Self-capacitive (3 channels)	160	3.85	3.88
	Mutual Capacitive (2 channels)	160	8.89	9.26
Halt	NA	3000	1.74	1.75

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Typ	Max	Unit
V_{VDD}	Power-up/down level (Reset trigger) - slope >100V/s	1.040	1.353	1.568	V
V_{VREG}	Power-up/down level (Reset trigger) - slope >100V/s	0.945	1.122	1.304	V

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3V	VSS – 0.3	-	1.05	V
		VDD = 1.7V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3V	2.25	-	VDD + 0.3	V
		VDD = 1.7V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3V	-	-	15	ns
		VDD = 1.7V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

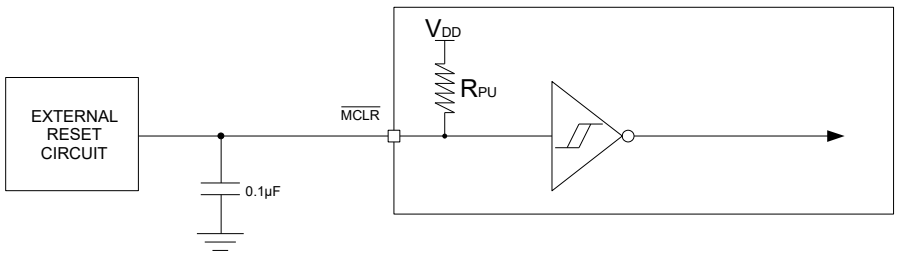

Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	42	500-1500	5000	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20mA			0.3	V
V_{OL}	TxA Output low voltage OutA Output low voltage RDY/MCLR Output low voltage	I_{sink} = 10mA			0.15	V
V_{OH}	Output high voltage	I_{source} = 20mA	VDD - 0.2			V
V_{IL}	Input low voltage		VDD * 0.3			V
V_{IH}	Input high voltage				VDD * 0.7	V
C_{b_max}	SDA & SCL maximum bus capacitance				550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Test Conditions	VDD	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		1.8V, 3.3V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START		1.8V, 3.3V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START		1.8V, 3.3V	0.26			µs
$t_{HD,DAT}$	Data hold time		1.8V, 3.3V	0			ns
$t_{SU,DAT}$	Data setup time		1.8V, 3.3V	50			ns
$t_{SU,STO}$	Setup time for STOP		1.8V, 3.3V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		1.8V, 3.3V	0		50	ns

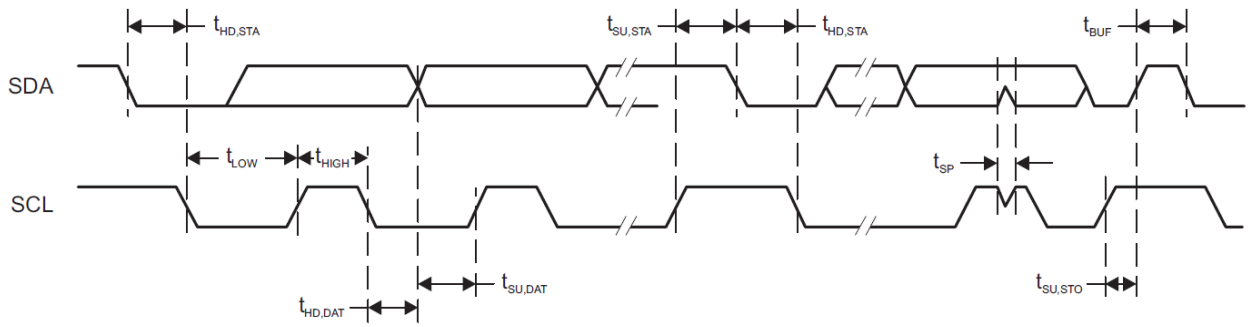

Figure 4.2: I²C Mode Timing Diagram

5 ProxFusion® Module

The IQS323 contains a single ProxFusion® module that uses patented technology to measure and process the sensor data.

5.1 Channel Options

Self-capacitance, Mutual capacitance, Reference tracking and Inductive designs are possible with the IQS323.

- Sensor pad design overview: AZD008
- Mutual capacitance button layout guide: AZD036
- Inductive design layout guide: AZD115

5.2 Low Power Options

The IQS323 offers 3 power modes:

- Normal power mode (NP)
- Low power mode (LP)
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimized firmware setup
  - Intended for rapid wake-up on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
  - Other sensor channels are typically sampled at a slower rate in order to optimize power consumption

5.3 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance/inductance, and all outputs are derived from this.

5.3.1 Max Counts

Each channel is limited to having a count value smaller than the configurable limit *(Max counts)*. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

5.3.2 Linearise Counts

If the *Linearise* option is set the IQS323 linearises the counts before reporting them. If this option is set the counts are inverted and the *Invert* bit must be set to invert the channel logic.

It is recommended to linearise the counts, especially when using the Release UI functionality (Section 7.3).

5.4 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value known as the *LTA*. The LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

5.4.1 Reseed

Since the *LTA* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the *Reseed* bit in Table A.27.

5.5 Power Mode Timeout

In order to optimize power consumption and performance, power modes are "stepped" when the power mode switching is set to 'Automatic'. This moves the device to more power efficient modes when no interaction has been detected for a certain (configurable) time known as the *Power Mode Timeout*. The value for the power mode to never timeout (i.e the current power mode will never progress to a lower power mode), is 0x00.

In addition to 'Automatic' power mode, the IQS323 power mode switching can also be set to 'Automatic No ULP'. This functions identically to 'Automatic' mode except the device will never enter Ultra Low Power (ULP) mode.

5.6 Filter Betas

An Infinite Impulse Response(IIR) filter is applied to the digitized raw input for both the counts value and the LTA.

Damping options for the counts filters are defined in Table A.23, Table A.24, Table A.25 and Table A.26.

Damping options for the LTA filters are defined in Table A.23, Table A.24, Table A.25 and Table A.26.

Damping factor = Beta/256

5.7 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and inductance, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

5.8 Automatic Re-ATI

5.8.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed the *ATI Event* status bit will be set. It is cleared when read by the master through I^2C.

5.8.2 Conditions for Re-ATI to Activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.10.

Re-ATI Boundary = ATI target ± (ATI Band)

For example, assume that the ATI target is 800 and that the and the default boundary value is 1/8*800 = 100. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

LTA > 900 or LTA < 700

The ATI algorithm executes in a short time, and therefore goes unnoticed by the user.

Note that I^2C communications are disabled for the duration of the ATI process.

5.8.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if the following is true for any channel after the ATI has completed:

- Counts are outside the **Re-ATI Boundary** upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set *(ATI Error)*. The flag status is only updated again when a new ATI algorithm is performed.

A Re-ATI will not be automatically triggered if an ATI Error occurs. If an ATI Error occurs the master should manually trigger a Re-ATI using the Re-ATI bit in Table A.27.

5.9 Sensor Setup

To perform a measurement the IQS323 must be configured to display the correct waveform on it's CTx pins. Tables A.8 and A.9 show the register settings Wav Pattern 0, Wav Pattern 1 and Wav Pattern Select.

Wav Pattern 0 and Wav Pattern 1 configure the waveform to be displayed on the CTx pin and Wav Pattern Select selects whether Wav Pattern 0 or Wav Pattern 1 is displayed on each CTx pin. Note that the CTxs must be enabled in the per channel Sensor Setup registers (Table A.4).

Writing a 0 to a bit in Table 5.1 will output the pattern defined in Wav Pattern 0 on the corresponding CTx. Likewise, writing a 1 will output Wav Pattern 1.

Table 5.1: Wav Pattern Select

Bit3	Bit2	Bit1	Bit0
TxA	CTx2	CTx1	CTx0

5.9.1 Self Capacitance, Mutual Capacitance and Inductive Measurements

Table 5.2 shows the values to be written to Wav Pattern 0 and Wav Pattern 1 for each measurement type. In all cases Wav Pattern Select should be set to 0x00.

Table 5.2: Recommended Pattern Values

Measurement Type	Wav Pattern 0	Wav Pattern 1
Self Capacitance	0x03	0x00
Mutual Capacitance	0x0E	0x00
Inductive	0x0B	0x00

5.9.2 Differential Capacitance Measurement

For a Differential Capacitance Measurement two CTxs are used. The waveforms on the CTxs are inverses of one another. Therefore both Wav Pattern 0 and Wav Pattern 1 must be configured and Wav Pattern Select is used to output the correct waveform on the CTx pins.

As an example, CTx0 and CTx1 are configured as Txs for a Differential Capacitance Measurement on Sensor 0. Wav Pattern 0 is set to 0x0E and Wav Pattern 1 is set to 0x0B. Thus, the value 0xBE must be written to he lower byte of register 0x34.

Since Wav Pattern 0 is desired on CTx0 and Wav Pattern 1 on CTx1, 0x02 should be written to the upper byte of register 0x35 (Wav Pattern Select).

Table 5.3 shows these example pattern values.

Table 5.3: Differential Capacitance Example Pattern Values

Wav Pattern 0	Wav Pattern 1	Wav Pattern Select
0x0E	0x0B	0x02

6 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Only certain parameters are described below. The other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.

6.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (*Charge Transfer frequency*) will be provided. For high resistance sensors, it might be needed to decrease f_{xfer}.

6.2 Reset

6.2.1 Reset Indication

After a reset, the *Reset Event* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *(ACK Reset)*. If it becomes set again, the master will know a reset has occurred, and can react appropriately.

While *Reset* bit remains set:

- The device will not be able to enter into I^2C Event mode operation (i.e. streaming communication behavior will be maintained until the Reset bit is cleared)
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in a much longer time to finish the ATI routine.

6.2.2 Software Reset

The IQS323 can be reset by means of an I^2C command *(Soft Reset)*.

6.2.3 Hardware Reset

The MCLR/RDY pin (active LOW) can be used to hard reset the device when outside an I^2C communication window. For more details see Section 4.2.

7 Additional Features

7.1 OutA Functionality

OutA can be used either as a general purpose output pin or as an event indicator. Register *0xD0* controls the behaviour of OutA.

7.1.1 OutA as a General Purpose Output

Writing a value of 0x0000 to *OutA Mask* will set the state of OutA to LOW (0V). Writing a value of 0x7FFF to *OutA Mask* will set the state of OutA to HIGH (VDD). Any other value will result in the behaviour outlined in section 7.1.2.

7.1.2 OutA as an Event Indicator

If the *number of slider channels* is set to zero then *OutA Mask* selects which event in *System Status* controls OutA.

If the *number of slider channels* is greater than zero then the slider is enabled and *OutA Mask* selects which event in *Gesture Status* controls OutA.

In both cases OutA can be configured as either active HIGH or active LOW using the most significant bit (bit 15) in *OutA Mask*. Setting this bit to '1' will configure OutA as an active LOW pin while setting it to '0' will configure it as active HIGH.

For example, suppose the user wishes to have OutA go LOW during a HOLD slider event and HIGH otherwise. With the slider configured, *OutA Mask* selects from the events in *Gesture Status*. Since OutA should go LOW during a HOLD event and HIGH otherwise, OutA must be configured to be active LOW and the HOLD event should be selected by setting the fifth bit in *OutA Mask*. Therefore the value 0x8020 should be written to *OutA Mask*.

7.2 Reference UI

The IQS323 implements a Reference User Interface (Reference UI).

A reference channel adjusts the LTA of the primary sensing channel by subtracting the change in LTA of the reference channel from the LTA of the primary sensing channel. This subtraction is done when the primary sensing channel is in a Touch or Prox state. The Reference UI eliminates the effect of count drift on the measurement.

For example, in wear detect applications the temperature of the sensor is likely to change over time, resulting in poor sensor performance. By using the Reference UI, the drift in counts due to temperature is accounted for and the sensor performance is not affected by the temperature change.

The reference channel sensor should be exposed to the same conditions as the sensing channel, and the user should not be able to affect the counts of the reference channel.

A single reference channel can be configured to have multiple follower channel's. However, a follower channel cannot have multiple references.

7.2.1 Setting Descriptions

Table A.13 shows the register containing the parameters *Channel Mode*, *Reference Sensor ID* and *Follower Event Mask*. The *Follower Weight* is found in Table A.16.

A description of these settings is in Table 7.1.

Table 7.1: Reference UI Setting Descriptions

Setting	Description	Options
Channel mode	Configure channel as reference or follower	Independent Reference Follower
Reference Sensor ID	If a channel is selected as a follower then its Reference Sensor ID should be set to select which channel acts as a reference for it.	Selects a channel as a reference channel for the follower that Reference Sensor ID has been set for. Reference Sensor ID must be set to the channel number of the desired reference channel.
Follower Event Mask	The reference channel should not ATI if the follower is in a Prox or Touch state. This mask must be set to select the follower's Prox and Touch flags in System Status so that ATI is disabled for the reference channel when the follower is in a Prox or Touch state.	
Follower Weight	If the channel is set as a follower channel, this value determines how aggressively it will track the reference channel adjustment.	Bit value/4096

7.2.2 Example Setup

In an example Reference UI setup Channel 0 is set as the follower and Channel 1 is configured as a reference.

Since Channel 0 is the follower and Channel 1 is the reference, the *Reference Sensor ID* for Channel 0 should be set to 0x01. This selects Channel 1 as a reference for Channel 0.

The *Reference Sensor ID* is not used if the *Channel Mode* is set to 'Reference'. Therefore Channel 1's *Reference Sensor ID* is not used and can be set to 0x00.

Since Channel 1 is the reference the *Follower Event Mask* must be set to disable ATI on Channel 1 when Channel 0 is in Prox or Touch. Channel 0's Prox and Touch flags are the first and second bits of the upper byte of *System Status*. To select them, the first and second bits of *Follower Event Mask* should be set to 1. Therefore, 0x03 should be written to *Follower Event Mask* for Channel 1.

The *Follower Event Mask* is not used if the *Channel Mode* is set to 'Follower'. Therefore Channel 0's *Follower Event Mask* is not used and can be set to 0x00.

Follower Weight must be set for the follower channel. Its value is application specific. Setting the bit value to 4096 will result in the follower channel directly tracking the reference. A value greater than 4096 will cause the follower to track the reference aggresively while a value less than 4096 results in slower tracking.

Table 7.2: Reference UI Example Settings

Setting	Channel 0	Channel 1
Channel mode	Follower	Reference
Reference Sensor ID	0x01	0x00
Follower Event Mask	0x00	0x03
Follower Weight	Bit value/4096	0x00

7.3 Release UI

The IQS323 implements a Release User Interface (Release UI) that allows for the detection and release of long term touch and proximity events. In order to do this, the Release UI makes use of an additional LTA, known as the *Activation LTA* (Registers *0x20*, *0x21* and *0x22*).

When a touch or proximity event is detected the LTA is frozen but the Activation LTA is still updated. When the difference between the Counts and Activation LTA is smaller than the *Activation Settling Threshold* (Table A.29) for more than *Delta Snapshot Sample Delay* (Table A.30) samples, then the counts delta between the LTA and Counts value (*Delta Snapshot*) is recorded (registers *0x23*, *0x24*, *0x25*).

A percentage of the Delta Snapshot, as defined by *Release Delta Percentage* (Table A.30), is used to exit touch and prox conditions.

If

$$\textbf{(Counts - Activation LTA) > (Delta Snapshot} \times \frac{\textbf{Release Delta Percentage}}{128}\textbf{)}$$

then the channel is reseeded and therefore any touch or prox conditions are exited.

The Release UI implementation allows for the detection of long term touch events by exiting a touch or prox condition based on the rate at which counts change rather than by comparing the counts to a fixed threshold.

7.4 Watchdog Timer

The IQS323 implements a hardware watchdog timer. The watchdog timer is set to expire after 255ms if not kicked and will trigger a software reset upon expiration.

During I^2C communication the watchdog timer is reset whenever a read or write occurs. Therefore, if the master initiates communication by sending an I^2C START condition and does not complete the I^2C transaction then after 255ms the IQS323 will reset.

The I^2C transaction is completed either when an I^2C STOP notification is sent by the master or when the master ends the communication as described in Section 8.9.

8 I²C Interface

8.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a RDY (ready interrupt) line. The RDY pin also serves as a Master Clear (MCLR) and can be used to hard reset the device (Section 6.2.3). Byte level clock stretching is allowed. The communications interface of the IQS323 supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS323 implements 8-bit addressing with 2 bytes at each address.

8.2 I²C Address

The 7-bit device address is 0x44[i] ('01000100'). The full address byte will thus be 0x89 (read) or 0x88 (write).

8.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

8.4 Communication During ATI

If an ATI event is triggered then I²C communications are disabled for the duration of the ATI process.

8.5 Memory Map Addressing and Data

The memory map implements 8-bit addressing. Data is formatted as 16-bit words meaning that two bytes are stored at each address. For example, address $0x10$ will provide two bytes. The next two bytes read will be from address $0x11$.

The 16-bit data is sent in little endian byte order (least significant byte first).

8.6 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and initiate I²C reads accordingly.

The RDY line allows the master MCU to be woken from low-power/sleep when user presence is detected by the touch device. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

On the IQS323 the RDY line also serves as an MCLR pin. MCLR functionality is described in Section 6.2.3.

[i] The device will also acknowledge an I²C address of 0x45. Writing to this address will cause the IQS323 to enter a debugging mode and should not be done under normal operating conditions. Therefore, both 0x44 and 0x45 are reserved on the I²C bus when using the IQS323.

8.7 Communications Window

When the device has data for the master, it will pull the RDY line LOW. This indicates that the device has opened its *communications window* and is expecting the master to address it. When the communication window is closed the RDY line is released. For information on when the communications window is closed see section 8.9.

Transfer of data between the master and slave must occur during the communications window (RDY is LOW). If the master wishes to initiate communication, a *Force Communications Request* must be made, after which the master should wait for the slave to pull RDY LOW before attempting to read or write. Section 8.12.2 describes the *Force Communications Request* sequence.

8.8 I²C Transaction Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH) and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be missed/lost. The default I²C timeout period is set to 200ms and can be adjusted in register *0xD1*. The I²C transaction timeout period should be set between 2ms and 230ms. The *I²C transaction timeout* is measured from the start of the communications window (RDY goes LOW).

Once communication between the master and the IQS323 has begun (START condition on I²C lines), the I²C transaction timeout is disabled leaving the watchdog timer in control. For more information on the behaviour of the device under these conditions see Section 7.4.

8.9 Terminate Communication

A standard I²C STOP will close the current communication window.

If the stop bit disable (*Stop Bit Disable*) is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF) shown in figure 8.1.

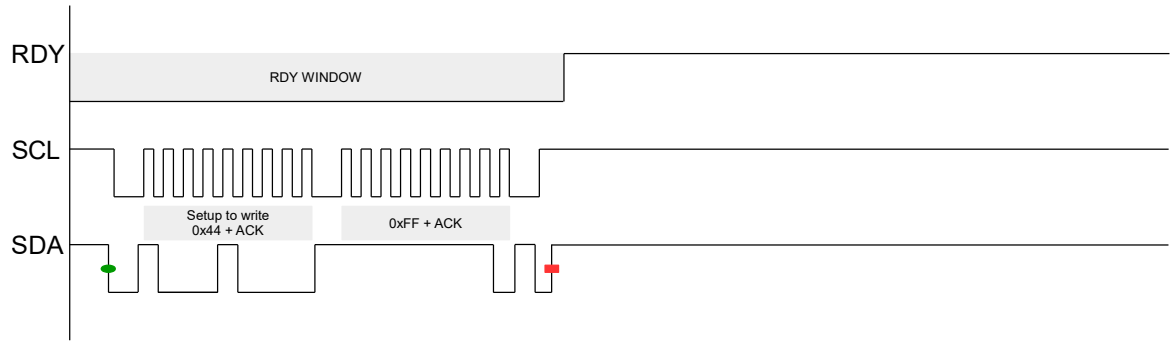

Figure 8.1: Force Stop Communication Sequence

8.10 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY = high)

8.11 I²C Interface

The IQS323 has 2 *Interface Types*, as described in the sections below.

8.11.1 I²C Streaming

I²C Streaming mode refers to constant data reporting at the relevant power mode report rate specified in register *0xC1* (normal power report rate), register *0xC2* (low power report rate) and register *0xC3* (ultra low power report rate) respectively.

8.11.2 I²C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (Event mode). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs.

8.12 Event Mode Communication

For event mode to function correctly the following requirements must be met:

- A device reset, as indicated by the *Reset Event* flag, must be acknowledged by setting the *ACK Reset* bit. Setting the *ACK RESET* bit will clear the *RESET Event* flag in the *System Status* register.
- Enabled events must be serviced by reading from the *System Status* register (0x10) to ensure all event flags are cleared. If these flags are not cleared continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode.

8.12.1 Events

Events can be individually enabled to trigger communication, bit definitions can be found in *System Status* and *Gesture Status*.

Using the *Events Enable* register the following events can be enabled:

- ATI Error
- ATI Active
- ATI event
- Power Mode change
- Slider event
- Prox or Touch event

8.12.2 Force Communication

In streaming mode, the IQ323 I²C will provide Ready (RDY) windows at intervals specified by the power mode report rate. Ideally, communication with the IQS323 should only be initiated in a RDY window. A communication request described in the figure below will force a RDY window to open. In event mode RDY windows are only provided when an event is reported. A RDY window must be requested to write or read settings outside of this provided window. The minimum and maximum time between the communication request and the opening of a RDY window (t_{wait}) is application specific. The average values of t_{wait} are 0.1ms $\leq t_{wait} \leq$ 45ms[ii].

[ii] Please contact Azoteq for an application specific value of t_{wait}

The communication request sequence is shown in figure 8.2.

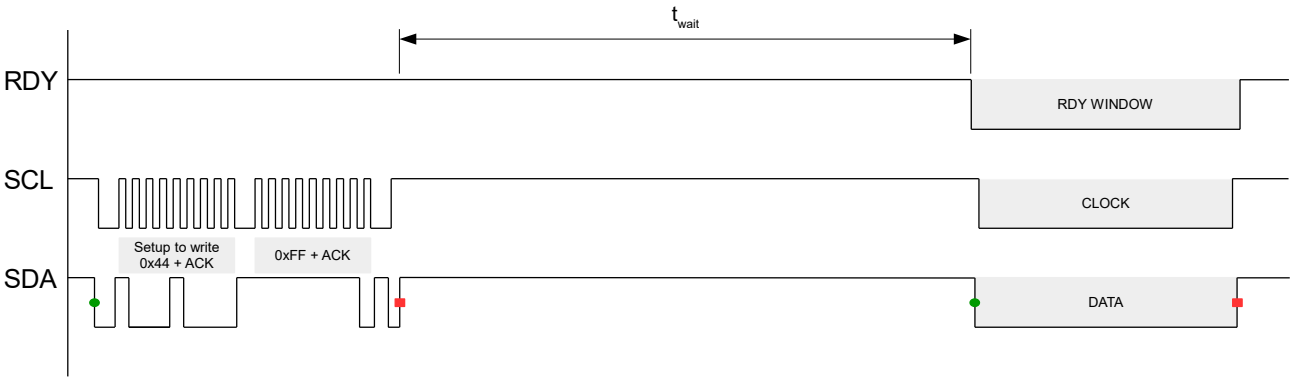

Figure 8.2: Force Communication Sequence

9 Memory Map Register Descriptions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
Read Only	**System Information**	
0x10	Systems Status	See Table A.2
0x11	Gestures	See Table A.3
0x12	Slider Coordinates	16-bit value
0x13	Channel 0 Filtered Counts	16-bit value
0x14	Channel 0 LTA	
0x15	Channel 1 Filtered Counts	
0x16	Channel 1 LTA	
0x17	Channel 2 Filtered Counts	
0x18	Channel 2 LTA	
Read Only	**Release UI**	
0x20	Channel 0 Activation LTA	16-bit value
0x21	Channel 1 Activation LTA	
0x22	Channel 2 Activation LTA	
0x23	Channel 0 Delta Snapshot	
0x24	Channel 1 Delta Snapshot	
0x25	Channel 2 Delta Snapshot	
Read/Write	**Sensor 0 Setup**	
0x30	Sensor Setup 0	See Table A.4
0x31	Conversion Frequency Setup	See Table A.5
0x32	Prox Control	See Table A.6
0x33	Prox Input and Control	See Table A.7
0x34	Pattern Definitions	See Table A.8
0x35	Pattern Selection and Engine Bias Current	See Table A.9
0x36	ATI Setup	See Table A.10
0x37	ATI Base	16-bit value
0x38	ATI Multipliers Selection	See Table A.11
0x39	Compensation	See Table A.12
Read/Write	**Sensor 1 Setup**	
0x40	Sensor Setup	See Table A.4
0x41	Conversion Frequency Setup	See Table A.5
0x42	Prox Control	See Table A.6
0x43	Prox Input and Control	See Table A.7
0x44	Pattern Definitions	See Table A.8
0x45	Pattern Selection and Engine Bias Current	See Table A.9
0x46	ATI Setup	See Table A.10
0x47	ATI Base	16-bit value
0x48	ATI Multipliers and Dividers	See Table A.11
0x49	Compensation	See Table A.12
Read/Write	**Sensor 2 Setup**	
0x50	Sensor Setup	See Table A.4
0x51	Conversion Frequency Setup	See Table A.5
0x52	Prox Control	See Table A.6
0x53	Prox Input and Control	See Table A.7
0x54	Pattern Definitions	See Table A.8
0x55	Pattern Selection and Engine Bias Current	See Table A.9
0x56	ATI Setup	See Table A.10
0x57	ATI Base	16-bit value

0x58	ATI Multipliers and Dividers	See Table A.11
0x59	Compensation	See Table A.12
Read/Write	**Channel 0 Setup**	
0x60	Channel 0 Setup	See Table A.13
0x61	Prox Settings	See Table A.14
0x62	Touch Settings	See Table A.15
0x63	Follower Weight	See Table A.16
Read/Write	**Channel 1 Setup**	
0x70	Channel 1 Setup	See Table A.13
0x71	Prox Settings	See Table A.14
0x72	Touch Settings	See Table A.15
0x73	Follower Weight	See Table A.16
Read/Write	**Channel 2 Setup**	
0x80	Channel 2 Setup	See Table A.13
0x81	Prox Settings	See Table A.14
0x82	Touch Settings	See Table A.15
0x83	Follower Weight	See Table A.16
Read/Write	**Slider Config**	
0x90	Slider Setup and Calibration	See Table A.17
0x91	Slider Calibration and Bottom Speed	See Table A.18
0x92	Slider Top Speed	16-bit value
0x93	Slider Resolution	
0x94	Enable Mask	See Table A.19
0x95	Enable Status Pointer	See Table A.20
0x96	Delta Link 0	See Table A.21
0x97	Delta Link 1	
0x98	Delta Link 2	
Read/Write	**Gesture Config**	
0xA0	Gesture Select	See Table A.22
0xA1	Minimum Time	16-bit value (ms)
0xA2	Max Tap Time	
0xA3	Max Swipe Time	
0xA4	Min Hold Time	
0xA5	Max Tap Distance	16-bit value
0xA6	Min Swipe Distance	
Read/Write	**Filter Betas**	
0xB0	Counts Filter Betas	See Table A.23
0xB1	LTA Filter Betas	See Table A.24
0xB2	LTA Fast Filter Betas	See Table A.25
0xB3	Activation LTA Filter Betas	See Table A.26
0xB4	Fast Filter Band	16 bit value
Read/Write	**System Control**	
0xC0	System Control	See Table A.27
0xC1	Normal Power Mode Report Rate	16-bit value (ms) Range: 0 - 3000
0xC2	Low Power Mode Report Rate	
0xC3	Ultra Low Power Mode Report Rate	
0xC4	HALT Mode Report Rate	
0xC5	Power Mode Timeout	16-bit value (ms) Range: 0 - 65000
Read/Write	**General**	
0xD0	OutA Mask	See Section 7.1

0xD1	I²C Transaction Timeout	16 bit value (ms) Range: 2 - 230
0xD2	Event Timeouts	See Table A.28
0xD3	Events Enable and Activation Settling Threshold	See Table A.29
0xD4	Release UI Settings	See Table A.30
Read/Write	**I²C Settings**	
0xE0	I²C Setup	See Table A.31

10 Ordering Information

10.1 Ordering Code

IQS323 zzz ppb

IC NAME	IQS323	=	IQS323	
DEFAULT CONFIGURATION	zzz	=	001	3 button self capacitance, configurable via I^2C
PACKAGE TYPE	pp	=	CS	WLCSP-11 package
		=	DN	DFN-12 package
BULK PACKAGING	b	=	R	WLCSP-11 Reel (3000pcs/reel) DFN-12 Reel (6000pcs/reel)

Figure 10.1: Order Code Description

10.2 Top Marking

10.2.1 WLCSP11 Package

- IQS323
  pppxx

Product Name
ppp = product code
xx = batchcode

10.2.2 DFN12 Package Marking Option 1

- IQS323
  pppxx

Product Name
ppp = product code
xx = batchcode

10.2.3 DFN12 Package Marking Option 2

- IQS3dd
  pppxx

Product Name
ppp = product code
xx = batchcode

11 Package Specification

11.1 Package Outline Description - WLCSP11

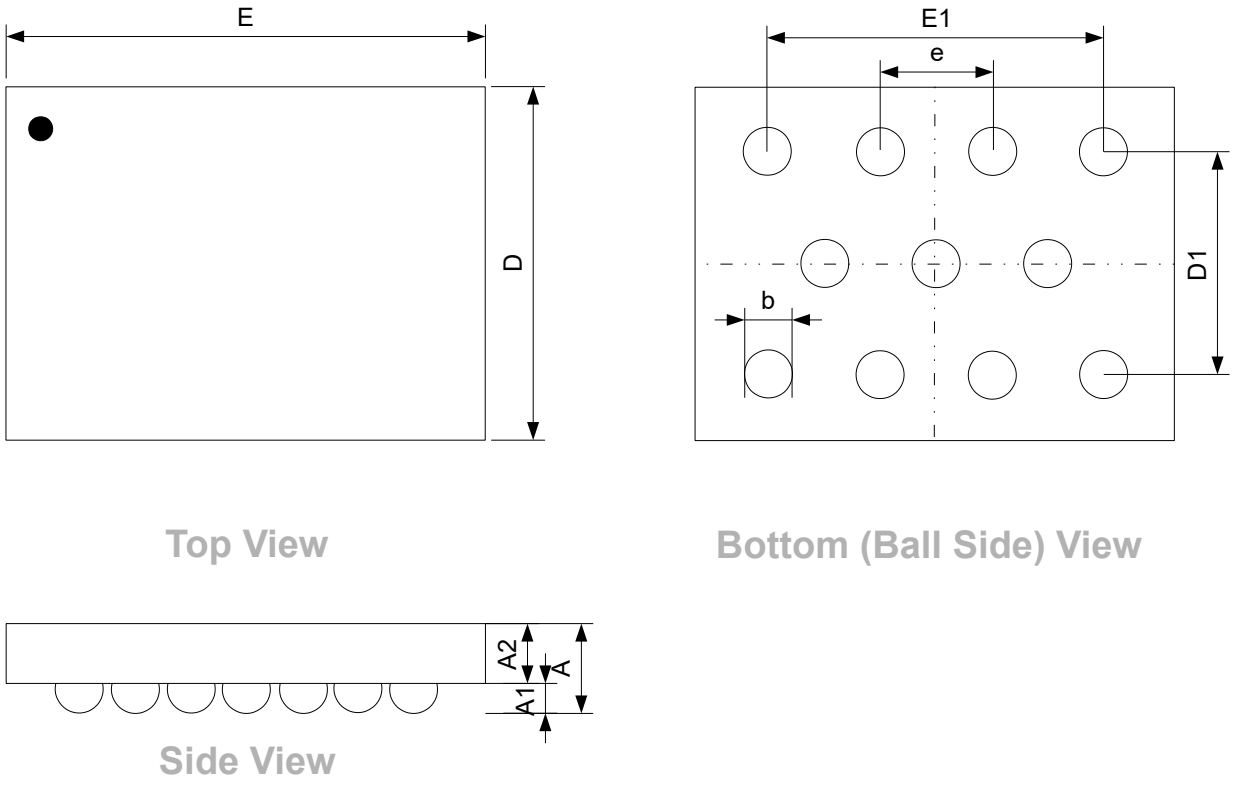

Figure 11.1: WLCSP (1.48x1.08) - 11 Package Outline Visual Description

Table 11.1: WLCSP (1.48x1.08) - 11 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.345±0.042	D1	0.700
A1	0.090±0.014	E	1.480±0.02
A2	0.230±0.025	E1	1.050
b	0.160±0.024	e	0.350
D	1.080±0.020		

11.2 Package Outline Description - DFN12

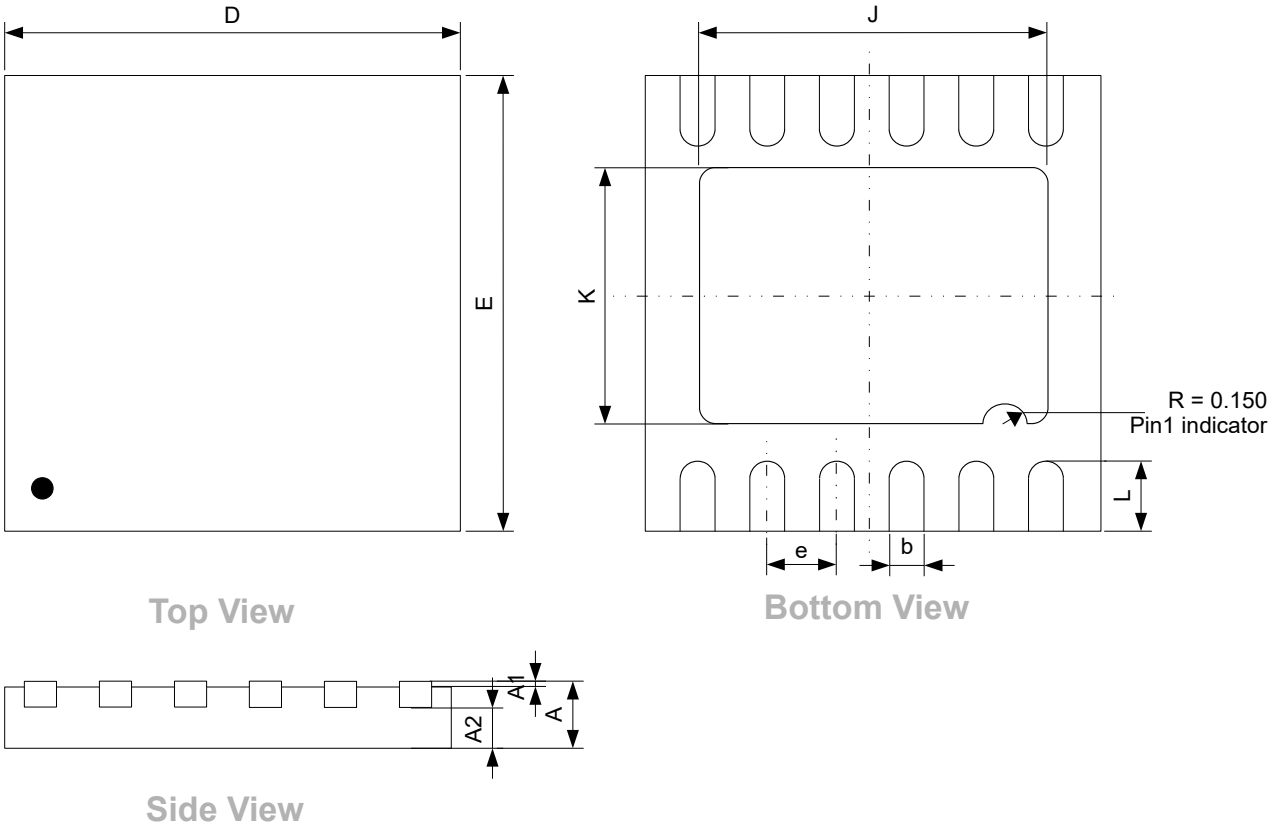

Figure 11.2: DFN (3x3)-12 Package Outline Visual Description

Table 11.2: DFN (3x3)-12 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.750±0.100	J	2.400±0.050
A1	0.025±0.025	K	1.700±0.050
A2	0.547	L	0.450±0.050
D	3.00±0.050	b	0.230
E	3.00±0.050	e	0.500

A Memory Map Descriptions

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Category	Name	Value
0x00	Reserved	Product Number	1106
0x01		Major Version	0
0x02		Minor Version	18
0x03		Reserved	
0x04			
0x05 - 0x09		Reserved	

Table A.2: System Status

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CHANNEL_FLAGS								SYSTEM_FLAGS							
Current Power mode		CH2 Touch	CH2 Prox	CH1 Touch	CH1 Prox	CH0 Touch	CH0 Prox	Reset Event	ATI Error	ATI Active	ATI Event	Power Event	Slider Event	Touch Event	Prox Event

- Bit 15-14: **Current Power Mode**
  - 00: Normal Power
  - 01: Low Power
  - 10: Ultra Low Power
  - 11: Halt Mode
- Bit 13-8: **CHx Touch and Prox**

  For CHx Touch
  - 0: CHx not in Touch
  - 1: CHx in Touch

  For CHx Prox
  - 0: CHx not in Prox
  - 1: CHx in Prox
- Bit 7: **Reset Event**
  - 0: No Reset Event occurred
  - 1: Reset Event occurred
- Bit 6: **ATI Error**
  - 0: No ATI Error occurred
  - 1: ATI Error occurred
- Bit 5: **ATI Active**
  - 0: ATI not active
  - 1: ATI active
- Bit 4: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 3: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 2: **Slider Event**
  - 0: No Slider Event occurred
  - 1: Slider Event occurred
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

Table A.3: Gesture Status

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED								**GESTURE_FLAGS**							
Reserved								Busy	Event	Hold	Flick Negative	Flick Positive	Swipe Negative	Swipe Positive	Tap

- Bit 7: **Busy**
  - 0: Gestures Idle
  - 1: Gestures Busy
- Bit 6: **Event**
  - 0: No Gesture Event occurred
  - 1: Gesture Event occurred
- Bit 5: **Hold**
  - 0: No Hold event detected
  - 1: Hold event detected
- Bit 4: **Flick Negative**
  - 0: No Flick Negative event detected
  - 1: Flick Negative event detected
- Bit 3: **Flick Positive**
  - 0: No Flick Positive event detected
  - 1: Flick Positive event detected
- Bit 2: **Swipe Negative**
  - 0: No Swipe Negative event detected
  - 1: Swipe Negative event detected
- Bit 1: **Swipe Positive**
  - 0: No Swipe Positive event detected
  - 1: Swipe Positive event detected
- Bit 0: **Tap**
  - 0: No Tap Event detected
  - 1: Tap Event detected

Table A.4: Sensor Setup

Register: 0x30, 0x40, 0x50

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TX_SELECT								**SENSOR_SETUP**							
Reserved	CalCap Rx	CalCap Tx	Reserved	TxA	CTx2	CTx1	CTx0	Reserved	Release UI Enable	FOSC Tx Frequency	Vbias	Invert	Dual Direct	Linearise Counts	Enable Channel

- Bit 14: **CalCap Rx**
  - 0: CalCap Rx not selected
  - 1: CalCap Rx selected
- Bit 13: **CalCap Tx**
  - 0: CalCap Tx not selected
  - 1: CalCap Tx selected
- Bit 11: **TxA**
  - 0: TxA disabled
  - 1: TxA enabled
- Bit 10-8: **CTxx**
  - 0: CTxx disabled
  - 1: CTxx enabled
- Bit 6: **Release UI Enable**
  - 0: Release UI disabled
  - 1: Release UI enabled
- Bit 5: **FOSC Tx Frequency**
  - 0: FOSC Tx Frequency disabled
  - 1: FOSC Tx Frequency enabled
- Bit 4: **Vbias**
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 3: **Invert**

- 0: Do not invert channel logic
- 1: Invert channel logic

- Bit 2: **Dual Direct**
  - 0: Single direction thresholds
  - 1: Dual direction thresholds
- Bit 1: **Linearise Counts**
  - 0: Do not Linearise counts
  - 1: Linearise counts
- Bit 0: **Enable Channel**
  - 0: Channel disabled
  - 1: Channel enabled

Table A.5: Conversion Frequency Setup

Register: 0x31, 0x41, 0x51

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONV_FREQ_PERIOD								**CONV_FREQ_FRAC**							
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 15-8: **Conversion Frequency Period**
  - The charge transfer frequency f_{xfer} is determined by the values of the Conversion Frequency Fraction and the Conversion Frequency Period. The required value of the Conversion Frequency Period is dependent on the dead time enabled bit (See Table A.7).
  - Dead time disabled $f_{xfer} = \frac{fosc}{2 \times period + 2}$
  - Dead time enabled $f_{xfer} = \frac{fosc}{2 \times period + 3}$
  - Range: 0 - 127
- Bit 7-0: **Conversion Frequency Fraction**
  - Set to 127
- For F_{OSC} = 14MHz, a fixed conversion frequency fraction of 127 and dead time enabled, the following values of the conversion frequency period are recommended and will result in the indicated conversion frequency:
  - 1: 2MHz
  - 5: 1MHz[i]
  - 12: 500kHz
  - 17: 350kHz
  - 26: 250kHz
  - 53: 125kHz

Table A.6: Prox Control

Register: 0x32, 0x42, 0x52

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PROX_CTRL_1								**PROX_CTRL_0**							
Reserved	0v5 Discharge	Reserved	Cs Size	Reserved	Reserved	S/H Bias Select		Max Counts		PXS Mode					

- Bit 15: **Reserved**
  - Set to 0
- Bit 14: **0v5 Discharge**
  - 0: Disabled
  - 1: Enabled
- Bit 13: **Reserved**
  - Set to 0
- Bit 12: **Cs Size**
  - 0: Use 40pF Cs
  - 1: Use 80pF Cs
- Bit 11: **Reserved**
  - Set to 0
- Bit 10: **Reserved**
  - Set to 0
- Bit 9-8: **S/H Bias Select**

[i]Please note: The maximum charge transfer frequency for mutual-capacitance mode (refer to Table A.6) is 1MHz

- 00: 2μA
- 01: 5μA
- 10: 7μA
- 11: 10μA

› Bit 7-6: **Max Counts**
- 00: 1023
- 01: 2047
- 10: 4095
- 11: 16383

› Bit 5-0: **PXS Mode**
- 0x10: Self-Capacitance
- 0x13: Mutual-Capacitance
- 0x1D: Current Measurement
- 0x3D: Inductive[ii]

Table A.7: Prox Input and Control

Register: 0x33, 0x43, 0x53

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RX_SELECT								TG_CTRL							
Reserved	Reserved	Internal Reference	Prox Engine Bias Current	Calibration Cap Select	Rx2	Rx1	Rx0	Reserved	Dead Time Enable	Reserved	Reserved	Auto Prox Cycle Select		Reserved	

› Bit 15: **Reserved**
- Set to 0

› Bit 14: **Reserved**
- Set to 0

› Bit 13: **Internal Reference**
- 0: Internal Reference disabled
- 1: Internal Reference enabled

› Bit 12: **Prox Engine Bias Current**
- 0: Prox Engine Bias Current disabled
- 1: Prox Engine Bias Current enabled

› Bit 11: **Calibration Capacitor Select**
- 0: Calibration Capacitor enabled
- 1: Calibration Capacitor disabled

› Bit 10-8: **Rxx**
- 0: Rxx Disabled
- 1: Rxx Enabled

› Bit 7: **Reserved**
- Set to 1

› Bit 6: **Dead Time Enable**
- 0: Dead Time Disabled
- 1: Dead Time Enabled

› Bit 4: **Reserved**
- Set to 0

› Bit 3-2: **Auto Prox Cycle Select**
- Number of conversions before each interrupt is generated in Auto Mode
- 00: 4
- 01: 8
- 10: 16
- 11: 32

› Bit 1-0: **Reserved**
- Set to 11

[ii] If CRx2/CTx2/Bias is used as an Rx for an inductive measurement the PXS Mode should be set to *Current Measurement*

Table A.8: Pattern Definitions

Register:	0x34, 0x44, 0x54														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_SETUP								**CALCAP_INACTIVE_RX**							
Wav Pattern 1				Wav Pattern 0				Calibration Capacitor				Inactive Rxs			

- Bit 15-12: **Wav Pattern 1**
  - See Section 5.9
- Bit 11-8: **Wav Pattern 0**
  - See Section 5.9
- Bit 7-4: **Calibration Capacitor**
  - Calibration Capacitor size = 0.5pF x Calibration Capacitor
  - Max value = 7 (Calibration Capacitor size = 3.5pF)
- Bit 3-0: **Inactive Rxs**
  - Selects state of Cx's when not in use
  - 0x00: Floating
  - 0x05: Bias voltage
  - 0x0A: VSS
  - 0x0F: VREG

Table A.9: Pattern Selection and Engine Bias Current

Register:	0x35, 0x45, 0x55														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BIAS_CURRENT								**PATTERN_SELECT**							
Engine Bias Current				Engine Bias Current Trim				Wav Pattern Select							

- Bit 15-12: **Engine Bias Current**
  - Signed value (MSB is sign bit)
  - Bias Current = Engine Bias Current x $3\mu A$ + Engine Bias Current Trim x $200nA$
- Bit 11-8: **Engine Bias Current Trim**
  - 4 bit Engine Bias Current Trim Value
- Bit 7-0: **Wav Pattern Select**
  - Select which pattern is displayed on which Cx
  - See Section 5.9

Table A.10: ATI Setup

Register:	0x36, 0x46, 0x56														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI_SETUP_1								**ATI_SETUP_0**							
ATI Resolution Factor												ATI Band	ATI Mode		

- Bit 15-4: **ATI Resolution Factor**
  - ATI TARGET = ACTUAL ATI BASE x $\frac{\text{ATI Resolution Factor}}{16}$
- Bit 3: **ATI Band**
  - 0: Small ATI Band = ($\frac{1}{16}$ x ATI TARGET)
  - 1: Large ATI Band = ($\frac{1}{8}$ x ATI TARGET)
- Bit 2-0: **ATI Mode**
  - 000: Disabled
  - 001: Compensation Only
  - 010: ATI from Compensation Divider
  - 011: ATI from Fine Fractional Divider
  - 100: Full

Table A.11: ATI Multipliers and Dividers

Register:	0x38, 0x48, 0x58														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI_FINE								**ATI_COARSE**							
Fine Fractional Multiplier		Fine Fractional Divider						Coarse Fractional Multiplier				Coarse Fractional Divider			

Table A.12: Compensation

Register:	0x39, 0x49, 0x59														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI_COMPENSATION_1								**ATI_COMPENSATION_0**							
Compensation Divider					Res-erved	Compensation									

Table A.13: Channel Setup

Register:	0x60, 0x70, 0x80														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FOLLOWER_MASK								**REF_UI_SETUP**							
Follower Event Mask								Reference Sensor ID				Channel Mode			

- Bit 15-8: **Follower Event Mask**
  - Masks the events in the upper byte of System Status
- Bit 7-4: **Reference Sensor ID**
  - Select Reference Sensor
- Bit 3-0: **Channel Mode**
  - 00: Independent
  - 01: Follower
  - 10: Reference

Table A.14: Prox Settings

Register:	0x61, 0x71, 0x81														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PROX_DEBOUNCE								**PROX_THRESHOLD**							
Prox Debounce Exit				Prox Debounce Enter				Prox Threshold							

- Bit 15-12: **Prox Debounce Exit**
  - 0000: Prox Debounce Exit disabled
  - Number of debounce conversions on Prox Exit (4-bit value)
- Bit 11-8: **Prox Debounce Enter**
  - 0000: Prox Debounce Enter disabled
  - Number of debounce conversions on Prox Enter (4-bit value)
- Bit 7-0: **Prox Threshold**
  - 8 bit value

Table A.15: Touch Settings

Register:	0x62, 0x72, 0x82														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TOUCH_HYSTERESIS								**TOUCH_THRESHOLD**							
Touch Hysteresis								Touch Threshold							

- Bit 15-12: **Touch Hysteresis**
  - $Touch\ Hysteresis = \frac{TouchHysteresis}{256}$ x $TouchThreshold$
- Bit 7-0: **Touch Threshold**
  - $Touch\ Threshold = \frac{Threshold \times LTA}{256}$

Table A.16: Follower Weight

Register:	0x63, 0x73, 0x83														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FOLLOWER_WEIGHT_1								**FOLLOWER_WEIGHT_0**							
Follower Weight															

- Bit 15-0: **Follower Weight**
  - $Follower\ Weight = \frac{Weight}{4096}$

Table A.17: Slider Setup and Calibration

Register:	0x90														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LOWER_CALIBRATION								**SLIDER_SETUP**							
Lower Calibration Value								Res-erved	Static Filter	Slow/Static Beta			Total Channels		

- Bit 15-8: **Lower Calibration Value**
  - 8-bit value
- Bit 6: **Static Filter**
  - 0: Static Filter disabled
  - 1: Static Filter enabled
- Bit 5-3: **Slow/Static Beta**
  - 3-bit value
- Bit 2-0: **Total Channels**
  - Number of channels to use for slider

Table A.18: Slider Calibration and Bottom Speed

Register:	0x91														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BOTTOM_SPEED								**UPPER_CALIBRATION**							
Bottom Speed								Upper Calibration							

- Bit 15-8: **Bottom Speed**
  - 8-bit value
- Bit 7-0: **Upper Calibration**
  - 8-bit value

Table A.19: Enable Mask

Register:	0x94														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ENABLE_MASK_1								**ENABLE_MASK_0**							
Enable Mask															

- Bit 0: **Channel 0 Enable**
  - 0: Channel 0 Disabled for Slider
  - 1: Channel 0 Enabled for Slider
- Bit 1: **Channel 1 Enable**
  - 0: Channel 1 Disabled for Slider
  - 1: Channel 1 Enabled for Slider
- Bit 2: **Channel 2 Enable**
  - 0: Channel 2 Disabled for Slider
  - 1: Channel 2 Enabled for Slider

Table A.20: Enable Status Pointer

Register:	0x95														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ENABLE_STATUS_POINTER_1								**ENABLE_STATUS_POINTER_0**							
Enable Status Pointer															

- Bit 15-0: **Enable Status Pointer**
  - 0x552: Slider active in Touch

Table A.21: Delta Links

Register:	0x96, 0x97, 0x98, 0x99														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DELTA_LINKX_1								**DELTA_LINKX_0**							
Delta Link X															

- Bit 15-0: **Delta Link X** - Select element order per channel
  - Delta Link number corresponds with slider element order

- 0x000: Disabled
- 0x430: Channel 0 enabled for element
- 0x472: Channel 1 enabled for element
- 0x4B4: Channel 2 enabled for element

Table A.22: Gesture Select

Register:	0xA0														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED								**GESTURE_SELECT**							
Reserved								Reserved				Hold Enable	Flick Enable	Swipe Enable	Tap Enable

- Bit 3: **Hold Enable**
  - 0: Hold disabled
  - 1: Hold enabled
- Bit 2: **Flick Enable**
  - 0: Flick disabled
  - 1: Flick enabled
- Bit 1: **Swipe Enable**
  - 0: Hold disabled
  - 1: Hold enabled
- Bit 0: **Tap Enable**
  - 0: Tap disabled
  - 1: Tap enabled

Table A.23: Counts Filter Betas

Register:	0xB0														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LP_COUNTS_FILTER								**NP_COUNTS_FILTER**							
Low Power Counts Beta								Normal Power Count Beta							

Table A.24: LTA Filter Betas

Register:	0xB1														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LP_LTA_FILTER								**NP_LTA_FILTER**							
Low Power LTA Beta								Normal Power LTA Beta							

Table A.25: LTA Fast Filter Betas

Register:	0xB2														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LP_LTA_FAST_FILTER								**NP_LTA_FAST_FILTER**							
Low Power LTA Fast Beta								Normal Power LTA Fast Beta							

Table A.26: Activation LTA Filter Betas

Register:	0xB3														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LP_ACTIVATION_LTA_FILTER								**NP_ACTIVATION_LTA_FILTER**							
Low Power Activation LTA Beta								Normal Power Activation LTA Beta							

Table A.27: System Control

Register:	0xC0														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED								**SYSTEM_CONTROL**							
Reserved								Interface Type	Power Mode			Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 7: **Interface Selection**
  - 0: I²C Streaming
  - 1: I²C Events
- Bit 6-4: **Power Mode**
  - 000: Normal Power Mode
  - 001: Low Power Mode
  - 010: Ultra Low Power Mode
  - 011: Halt Mode
  - 100: Automatic
  - 101: Automatic No ULP
- Bit 3: **Reseed**
  - 0: No Reseed
  - 1: Trigger Reseed
- Bit 2: **Re-ATI**
  - 0: No Re-ATI
  - 1: Trigger Re-ATI
- Bit 1: **Soft Reset**
  - 0: No Soft Reset
  - 1: Trigger Soft Reset
- Bit 0: **ACK Reset**
  - 0: No ACK Reset
  - 1: ACK Reset

Table A.28: Event Timeouts

Register: 0xD2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TOUCH_EVENT_TIMEOUT								**PROX_EVENT_TIMEOUT**							
Touch Event Timeout								Prox Event Timeout							

- Bit 15-8: **Touch Event Timeout**
  - *Touch Event Timeout* = Touch Event Timeout x 512ms
- Bit 7-0: **Prox Event Timeout**
  - *Prox Event Timeout* = Prox Event Timeout x 512ms

Table A.29: Events Enable and Activation Settling Threshold

Register: 0xD3

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACTIVATION_THRESHOLD								**EVENTS_ENABLE**							
Activation Settling Threshold								Res-erved	ATI Error	Res-erved	ATI Event	Power Event	Slider Event	Touch Event	Prox Event

- Bit 15-8: **Activation Settling Threshold**
  - 8 bit value
- Bit 6: **ATI Error Mask**
  - 0: ATI Error disabled
  - 1: ATI Error enabled
- Bit 4: **ATI Event Mask**
  - 0: ATI Event disabled
  - 1: ATI Event enabled
- Bit 3: **Power Event Mask**
  - 0: Power Event disabled
  - 1: Power Event enabled
- Bit 2: **Slider Event Mask**
  - 0: Slider Event disabled
  - 1: Slider Event enabled
- Bit 1: **Touch Event Mask**
  - 0: Touch Event disabled
  - 1: Touch Event enabled
- Bit 0: **Prox Event Mask**
  - 0: Prox Event disabled
  - 1: Prox Event enabled

Table A.30: Release UI Settings

Register:	0xD4														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DELTA_SNAP_SAMPLE_DELAY								**RELEASE_DELTA_PERCENTAGE**							
Delta Snapshot Sample Delay								Release Delta Percentage							

- Bit 15-8: **Delta Snapshot Sample Delay**
  - 8-bit value
- Bit 7-0: **Release Delta Percentage**
  - ***Release Delta Percentage*** = $\frac{\text{Release Delta Percentage}}{128}$

Table A.31: I2C Settings

Register:	0xE0														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED								**I2C_SETUP**							
Reserved														R/W Check Dis-able	Stop Bit Dis-able

- Bit 1: **Read/Write Check Disable**
  - 0: Read/Write Check enable
  - 1: Read/Write Check disabled
- Bit 0: **Stop Bit Disable**
  - 0: Stop Bit enabled
  - 1: Stop Bit disabled

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