

Arm® Cortex®-M33 32-bit MCU + TrustZone® + FPU, 375 DMIPS, 250 MHz, 2-Mbyte flash, 640-Kbyte RAM, math accelerators

Datasheet - production data

## Features

**Includes ST state-of-the-art patented technology**

### Core

- Arm® Cortex®-M33 CPU with TrustZone®, FPU, frequency up to 250 MHz, MPU, 375 DMIPS (Dhrystone 2.1)

### ART Accelerator

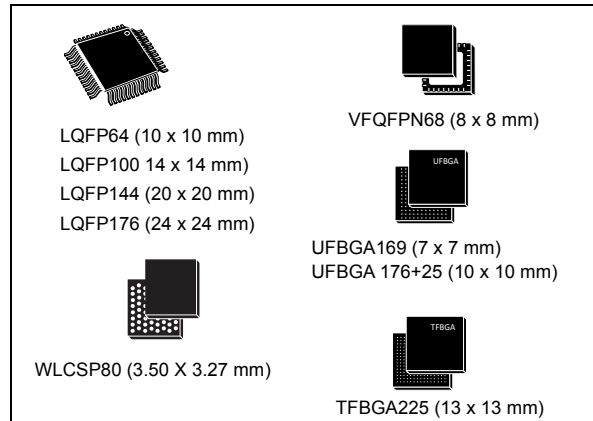
- 8-Kbyte instruction cache for 0-wait-state execution from flash and external memories
- 4-Kbyte data cache for external memories

### Benchmarks

- 1.5 DMIPS/MHz (Dhrystone 2.1)
- 1023 CoreMark® (4.092 CoreMark®/MHz)

### Memories

- Up to 2 Mbytes of embedded flash memory with ECC, two banks read-while-write
- Up to 48-Kbyte per bank with high-cycling capability (100 K cycles) for data flash
- 2-Kbyte OTP (one-time programmable)
- 640 Kbytes of SRAM (64-Kbyte SRAM2 with ECC and 320-Kbyte SRAM3 with flexible ECC)
- 4 Kbytes of backup SRAM available in the lowest power modes
- Flexible external memory controller with up to 16-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, FRAM, NOR/NAND memories
- One Octo-SPI interface with support for serial PSRAM/NAND/NOR, hyper RAM/flash frame formats
- Two SD/SDIO/MMC interfaces



### Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-50 MHz HSE, 32.768 kHz LSE

### General-purpose inputs/outputs

- Up to 140 fast I/Os with interrupt capability (most of them 5 V-tolerant)
- Up to ten I/Os with independent supply down to 1.08 V

### Low-power consumption

- Sleep, Stop, and Standby modes
- V<sub>BAT</sub> supply for RTC, 32 backup registers (32-bit)

### Security

- Arm® TrustZone® with Armv8-M mainline security extension
- Up to eight configurable SAU regions
- TrustZone® aware and securable peripherals
- Flexible life cycle scheme with secure debug authentication
- SFI (secure firmware installation)

- Secure firmware upgrade support with TF-M
- HASH hardware accelerator
- ECDSA signature verification
- True random number generator, NIST SP800-90B compliant
- 96-bit unique ID
- Active tamperers

### Two DMA controllers to offload the CPU

- Two dual-port DMAs with FIFO

### Mathematical acceleration

- CORDIC for trigonometric functions acceleration
- FMAC (filter mathematical accelerator)

### Reset and supply management

- 1.71 V to 3.6 V application supply and I/O
- POR, PDR, PVD, and BOR
- Embedded (LDO) or SMPS step-down converter regulator with configurable scalable output to supply the digital circuitry

### Up to 24 timers

- 18 16-bit timers (including six low-power 16-bit timers available in Stop mode)
- Two 32-bit timers with up to four IC/OC/PWM or pulse counters and quadrature (incremental) encoder input
- Two watchdogs
- Two SysTick timers

### Up to 34 communication interfaces

- Up to four I2Cs Fm+ (SMBus/PMBus®)
- One I3C
- Up to 12 U(S)ARTs (ISO7816 interface, LIN, IrDA, modem control) and one LPUART
- Up to six SPIs, including three muxed in full-duplex I2S audio class accuracy via internal audio PLL or external clock, and up to five additional SPIs from five USARTs when configured in Synchronous mode (one additional SPI with OctoSPI)
- Two SAI
- Two FDCANs
- One 8- to 14-bit camera interface
- One 16-bit parallel slave synchronous interface
- One HDMI-CEC
- One Ethernet MAC interface with DMA controller
- One USB 2.0 full-speed host and device
- One USB Type-C®/USB Power Delivery r3.1

### Analog

- Two 12-bit ADCs with up to 5 Msps in 12-bit
- One 12-bit DAC with two channels
- Digital temperature sensor

### Debug

- Authenticated debug, flexible device life cycle
- Serial wire-debug (SWD), JTAG, Embedded Trace Macrocell™ (ETM)

### ECOPACK2 compliant packages

**Table 1. Device summary**

| Reference   | Part numbers                                                                                                                                               |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STM32H562xx | STM32H562AG, STM32H562AI, STM32H562IG, STM32H562II, STM32H562RG, STM32H562RI, STM32H562VG, STM32H562VI, STM32H562ZG, STM32H562ZI                           |
| STM32H563xx | STM32H563AG, STM32H563AI, STM32H563IG, STM32H563II, STM32H563MI, STM32H563RG, STM32H563RI, STM32H563VG, STM32H563VI, STM32H563ZG, STM32H563ZI, STM32H563LI |

# Contents

|          |                                            |           |
|----------|--------------------------------------------|-----------|
| <b>1</b> | <b>Introduction</b>                        | <b>14</b> |
| <b>2</b> | <b>Description</b>                         | <b>15</b> |
| <b>3</b> | <b>Functional overview</b>                 | <b>20</b> |
| 3.1      | Arm Cortex-M33 core with TrustZone and FPU | 20        |
| 3.2      | ART Accelerator (ICACHE and DCACHE)        | 20        |
| 3.2.1    | Instruction cache (ICACHE)                 | 20        |
| 3.2.2    | Data cache (DCACHE)                        | 21        |
| 3.3      | Memory protection unit                     | 22        |
| 3.4      | Embedded flash memory                      | 22        |
| 3.4.1    | FLASH security and protections             | 23        |
| 3.4.2    | FLASH privilege protection                 | 23        |
| 3.5      | Embedded SRAMs                             | 23        |
| 3.5.1    | SRAMs TrustZone security                   | 23        |
| 3.5.2    | SRAMs privilege protection                 | 24        |
| 3.6      | Security overview                          | 24        |
| 3.7      | Boot modes                                 | 24        |
| 3.7.1    | STM32H562/H563xx boot modes                | 25        |
| 3.8      | Global TrustZone controller (GTZC)         | 26        |
| 3.9      | TrustZone security architecture            | 26        |
| 3.9.1    | TrustZone peripheral classification        | 27        |
| 3.9.2    | Default TrustZone security state           | 27        |
| 3.10     | Power supply management                    | 28        |
| 3.10.1   | Power supply schemes                       | 28        |
| 3.10.2   | Power supply supervisor                    | 32        |
| 3.10.3   | Reset mode                                 | 33        |
| 3.10.4   | VBAT operation                             | 33        |
| 3.10.5   | PWR TrustZone security                     | 34        |
| 3.11     | Peripheral interconnect matrix             | 34        |
| 3.12     | Reset and clock controller (RCC)           | 34        |
| 3.12.1   | RCC TrustZone security                     | 35        |
| 3.13     | Clock recovery system (CRS)                | 35        |

|        |                                                                               |    |
|--------|-------------------------------------------------------------------------------|----|
| 3.14   | General-purpose inputs/outputs (GPIOs) .....                                  | 36 |
| 3.14.1 | GPIOs TrustZone security .....                                                | 36 |
| 3.15   | Multi-AHB bus matrix .....                                                    | 36 |
| 3.16   | General purpose direct memory access controller (GPDMA) .....                 | 36 |
| 3.17   | Interrupts and events .....                                                   | 38 |
| 3.17.1 | Nested vectored interrupt controller (NVIC) .....                             | 38 |
| 3.17.2 | Extended interrupt/event controller (EXTI) .....                              | 38 |
| 3.18   | Cyclic redundancy check calculation unit (CRC) .....                          | 39 |
| 3.19   | CORDIC coprocessor (CORDIC) .....                                             | 39 |
| 3.20   | Filter math accelerator (FMAC) .....                                          | 39 |
| 3.21   | Flexible memory controller (FMC) .....                                        | 40 |
| 3.21.1 | LCD parallel interface .....                                                  | 40 |
| 3.21.2 | FMC TrustZone security .....                                                  | 40 |
| 3.22   | Octo-SPI interface (OCTOSPI) .....                                            | 41 |
| 3.22.1 | OCTOSPI TrustZone security .....                                              | 41 |
| 3.23   | Delay block (DLYB) .....                                                      | 42 |
| 3.24   | Analog-to-digital converters (ADC1 and ADC2) .....                            | 42 |
| 3.24.1 | Analog temperature sensor .....                                               | 42 |
| 3.24.2 | Internal voltage reference (VREFINT) .....                                    | 43 |
| 3.24.3 | VBAT battery voltage monitoring .....                                         | 43 |
| 3.25   | Digital temperature sensor (DTS) .....                                        | 43 |
| 3.26   | Digital to analog converter (DAC) .....                                       | 43 |
| 3.27   | Voltage reference buffer (VREFBUF) .....                                      | 44 |
| 3.28   | Digital camera interface (DCMI) .....                                         | 44 |
| 3.29   | Parallel synchronous slave interface (PSSI) .....                             | 45 |
| 3.30   | True random number generator (RNG) .....                                      | 45 |
| 3.31   | HASH hardware accelerator (HASH) .....                                        | 45 |
| 3.32   | Public key accelerator (PKA) .....                                            | 46 |
| 3.33   | Timers and watchdogs .....                                                    | 47 |
| 3.33.1 | Advanced-control timers (TIM1, TIM8) .....                                    | 47 |
| 3.33.2 | General-purpose timers<br>(TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17) ..... | 47 |
| 3.33.3 | Basic timers (TIM6, TIM7) .....                                               | 48 |
| 3.33.4 | Low-power timers<br>(LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5, LPTIM6) .....    | 48 |

|          |                                                                                                                                         |            |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------|------------|
| 3.33.5   | Independent watchdog (IWDG)                                                                                                             | 49         |
| 3.33.6   | Window watchdog (WWDG)                                                                                                                  | 49         |
| 3.33.7   | SysTick timer                                                                                                                           | 49         |
| 3.34     | Real-time clock (RTC), tamper and backup registers                                                                                      | 50         |
| 3.34.1   | Real-time clock (RTC)                                                                                                                   | 50         |
| 3.34.2   | Tamper and backup registers (TAMP)                                                                                                      | 50         |
| 3.35     | Inter-integrated circuit interface (I <sup>2</sup> C)                                                                                   | 51         |
| 3.36     | Improved inter-integrated circuit (I3C)                                                                                                 | 52         |
| 3.37     | Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART) | 53         |
| 3.37.1   | Universal synchronous/asynchronous receiver transmitter (USART/UART)                                                                    | 54         |
| 3.37.2   | Low-power universal asynchronous receiver transmitter (LPUART)                                                                          | 55         |
| 3.38     | Serial peripheral interface (SPI) / inter-integrated sound interface (I2S)                                                              | 57         |
| 3.39     | Serial audio interface (SAI)                                                                                                            | 58         |
| 3.40     | Secure digital input/output and MultiMediaCards interface (SDMMC)                                                                       | 60         |
| 3.41     | Controller area network (FDCAN)                                                                                                         | 61         |
| 3.42     | USB full speed (USB)                                                                                                                    | 61         |
| 3.43     | USB Type-C/USB Power Delivery controller (UCPD)                                                                                         | 62         |
| 3.44     | Ethernet MAC interface with dedicated DMA controller (ETH)                                                                              | 62         |
| 3.45     | High-definition multimedia interface (HDMI) - consumer electronics control (CEC)                                                        | 63         |
| 3.46     | Development support                                                                                                                     | 63         |
| 3.46.1   | Serial-wire/JTAG debug port (SWJ-DP)                                                                                                    | 63         |
| 3.46.2   | Embedded Trace Macrocell                                                                                                                | 63         |
| <b>4</b> | <b>Pinout, pin description, and alternate functions</b>                                                                                 | <b>64</b>  |
| 4.1      | Pinout/ballout schematics                                                                                                               | 64         |
| 4.2      | Pin description                                                                                                                         | 77         |
| 4.3      | Alternate functions                                                                                                                     | 106        |
| <b>5</b> | <b>Electrical characteristics</b>                                                                                                       | <b>124</b> |
| 5.1      | Parameter conditions                                                                                                                    | 124        |
| 5.1.1    | Minimum and maximum values                                                                                                              | 124        |
| 5.1.2    | Typical values                                                                                                                          | 124        |

|        |                                                                      |     |
|--------|----------------------------------------------------------------------|-----|
| 5.1.3  | Typical curves                                                       | 124 |
| 5.1.4  | Loading capacitor                                                    | 124 |
| 5.1.5  | Pin input voltage                                                    | 124 |
| 5.1.6  | Power supply scheme                                                  | 125 |
| 5.2    | Absolute maximum ratings                                             | 127 |
| 5.3    | Operating conditions                                                 | 128 |
| 5.3.1  | General operating conditions                                         | 128 |
| 5.3.2  | VCAP external capacitor                                              | 133 |
| 5.3.3  | SMPS step-down converter                                             | 133 |
| 5.3.4  | Operating conditions at power-up/down                                | 136 |
| 5.3.5  | Embedded reset and power control block characteristics               | 136 |
| 5.3.6  | Embedded reference voltage                                           | 138 |
| 5.3.7  | Supply current characteristics                                       | 138 |
| 5.3.8  | External clock source characteristics                                | 150 |
| 5.3.9  | Internal clock source characteristics                                | 155 |
| 5.3.10 | PLL characteristics                                                  | 157 |
| 5.3.11 | Memory characteristics                                               | 159 |
| 5.3.12 | EMC characteristics                                                  | 160 |
| 5.3.13 | Absolute maximum ratings (electrical sensitivity)                    | 162 |
| 5.3.14 | I/O current injection characteristics                                | 162 |
| 5.3.15 | I/O port characteristics                                             | 163 |
| 5.3.16 | NRST pin characteristics                                             | 177 |
| 5.3.17 | Extended interrupt and event controller input (EXTI) characteristics | 178 |
| 5.3.18 | FMC characteristics                                                  | 178 |
| 5.3.19 | Octo-SPI interface characteristics                                   | 198 |
| 5.3.20 | Delay block (DLYB) characteristics                                   | 202 |
| 5.3.21 | DCMI interface characteristics                                       | 202 |
| 5.3.22 | PSSI interface characteristics                                       | 203 |
| 5.3.23 | 12-bit ADC characteristics                                           | 206 |
| 5.3.24 | DAC characteristics                                                  | 213 |
| 5.3.25 | Analog temperature sensor characteristics                            | 217 |
| 5.3.26 | Digital temperature sensor characteristics                           | 218 |
| 5.3.27 | V <sub>CORE</sub> monitoring characteristics                         | 218 |
| 5.3.28 | Temperature and V <sub>BAT</sub> monitoring                          | 218 |
| 5.3.29 | Voltage booster for analog switch                                    | 219 |
| 5.3.30 | V <sub>REFBUF</sub> characteristics                                  | 219 |
| 5.3.31 | Timer characteristics                                                | 220 |

|          |                                          |            |
|----------|------------------------------------------|------------|
| 5.3.32   | Low-power timer characteristics          | 221        |
| 5.3.33   | Communication interfaces                 | 221        |
| <b>6</b> | <b>Package information</b>               | <b>242</b> |
| 6.1      | Device marking                           | 242        |
| 6.2      | LQFP64 package information (5W)          | 243        |
| 6.3      | VFQFPN68 package information (B029)      | 246        |
| 6.4      | WLCSP80 package information (B0D4)       | 248        |
| 6.5      | LQFP100 package information (1L)         | 251        |
| 6.6      | LQFP144 package information (1A)         | 254        |
| 6.7      | UFBGA169 package information (A0YV)      | 258        |
| 6.8      | LQFP176 package information (1T)         | 261        |
| 6.9      | UFBGA(176+25) package information (A0E7) | 265        |
| 6.10     | TFBGA225 package information (B04V)      | 267        |
| 6.11     | Package thermal characteristics          | 269        |
| 6.11.1   | Reference documents                      | 271        |
| <b>7</b> | <b>Ordering information</b>              | <b>272</b> |
| <b>8</b> | <b>Important security notice</b>         | <b>274</b> |
| <b>9</b> | <b>Revision history</b>                  | <b>275</b> |

## List of tables

|           |                                                                                                                                                                |     |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Table 1.  | Device summary . . . . .                                                                                                                                       | 2   |
| Table 2.  | STM32H56xxx features and peripheral counts. . . . .                                                                                                            | 16  |
| Table 3.  | STM32H562/H563 boot mode when TrustZone is disabled (TZEN = 0xC3) . . . . .                                                                                    | 25  |
| Table 4.  | STM32H562/H563 boot mode when TrustZone is enabled (TZEN = 0xB4). . . . .                                                                                      | 25  |
| Table 5.  | ADC features . . . . .                                                                                                                                         | 42  |
| Table 6.  | Timer features. . . . .                                                                                                                                        | 47  |
| Table 7.  | I2C implementation. . . . .                                                                                                                                    | 52  |
| Table 8.  | I3C peripheral controller/target features versus MIPI v1.1 . . . . .                                                                                           | 53  |
| Table 9.  | USART, UART and LPUART features . . . . .                                                                                                                      | 53  |
| Table 10. | SPI features . . . . .                                                                                                                                         | 58  |
| Table 11. | SAI implementation. . . . .                                                                                                                                    | 59  |
| Table 12. | SDMMC features . . . . .                                                                                                                                       | 60  |
| Table 13. | Legend/abbreviations used in the pinout table . . . . .                                                                                                        | 77  |
| Table 14. | STM32H562xx and STM32H563xx pin/ball definition . . . . .                                                                                                      | 78  |
| Table 15. | Alternate functions AF0 to AF7 . . . . .                                                                                                                       | 106 |
| Table 16. | Alternate functions AF8 to AF15. . . . .                                                                                                                       | 115 |
| Table 17. | Voltage characteristics . . . . .                                                                                                                              | 127 |
| Table 18. | Current characteristics . . . . .                                                                                                                              | 128 |
| Table 19. | Thermal characteristics. . . . .                                                                                                                               | 128 |
| Table 20. | General operating conditions . . . . .                                                                                                                         | 128 |
| Table 21. | Maximum allowed clock frequencies . . . . .                                                                                                                    | 132 |
| Table 22. | Supply voltage and maximum frequency configuration . . . . .                                                                                                   | 133 |
| Table 23. | Characteristics of SMPS step-down converter external components. . . . .                                                                                       | 133 |
| Table 24. | Operating conditions at power-up/down (regulator ON) . . . . .                                                                                                 | 136 |
| Table 25. | Embedded reset and power control block characteristics. . . . .                                                                                                | 136 |
| Table 26. | Embedded reference voltage . . . . .                                                                                                                           | 138 |
| Table 27. | Internal reference voltage calibration value . . . . .                                                                                                         | 138 |
| Table 28. | Typical and maximum current consumption in Run mode, code with data processing<br>running from flash memory, 2-way instruction cache ON, PREFETCH ON . . . . . | 139 |
| Table 29. | Typical and maximum current consumption in Run mode, code with data processing<br>running from flash memory, 1-way instruction cache ON, PREFETCH ON . . . . . | 140 |
| Table 30. | Typical and maximum current consumption in Run mode, code with data processing<br>running from SRAM with cache 1-way . . . . .                                 | 140 |
| Table 31. | Typical and maximum current consumption in Run mode, code with data processing<br>running from SRAM with cache 2-way . . . . .                                 | 141 |
| Table 32. | Typical consumption in Run mode with CoreMark running<br>from flash memory and SRAM . . . . .                                                                  | 142 |
| Table 33. | Typical consumption in Run mode with SecureMark running from<br>flash memory and SRAM . . . . .                                                                | 143 |
| Table 34. | Typical and maximum current consumption in Sleep mode . . . . .                                                                                                | 143 |
| Table 35. | Typical and maximum current consumption in Stop mode . . . . .                                                                                                 | 144 |
| Table 36. | Typical and maximum current consumption in Standby mode . . . . .                                                                                              | 144 |
| Table 37. | Typical and maximum current consumption in VBAT mode . . . . .                                                                                                 | 145 |
| Table 38. | Peripheral current consumption in Sleep mode . . . . .                                                                                                         | 146 |
| Table 39. | Low-power mode wake-up timings . . . . .                                                                                                                       | 150 |
| Table 40. | High-speed external user clock characteristics. . . . .                                                                                                        | 150 |
| Table 41. | Low-speed external user clock characteristics . . . . .                                                                                                        | 151 |
| Table 42. | 4 to 50 MHz HSE oscillator characteristics. . . . .                                                                                                            | 153 |

|           |                                                                                        |     |
|-----------|----------------------------------------------------------------------------------------|-----|
| Table 43. | Low-speed external user clock characteristics . . . . .                                | 154 |
| Table 44. | HSI48 oscillator characteristics . . . . .                                             | 155 |
| Table 45. | HSI oscillator characteristics . . . . .                                               | 155 |
| Table 46. | CSI oscillator characteristics . . . . .                                               | 156 |
| Table 47. | LSI oscillator characteristics . . . . .                                               | 157 |
| Table 48. | PLL characteristics (wide VCO frequency range) . . . . .                               | 157 |
| Table 49. | PLL characteristics (medium VCO frequency range) . . . . .                             | 158 |
| Table 50. | Flash memory characteristics . . . . .                                                 | 159 |
| Table 51. | Flash memory programming . . . . .                                                     | 159 |
| Table 52. | Flash memory endurance and data retention . . . . .                                    | 160 |
| Table 53. | EMS characteristics . . . . .                                                          | 160 |
| Table 54. | EMI characteristics . . . . .                                                          | 161 |
| Table 55. | ESD absolute maximum ratings . . . . .                                                 | 162 |
| Table 56. | Electrical sensitivities . . . . .                                                     | 162 |
| Table 57. | I/O current injection susceptibility . . . . .                                         | 163 |
| Table 58. | I/O static characteristics . . . . .                                                   | 163 |
| Table 59. | Output voltage characteristics for all I/Os except PC13, PC14, PC15, and PI8 . . . . . | 166 |
| Table 60. | Output voltage characteristics for FT_c I/Os . . . . .                                 | 167 |
| Table 61. | Output voltage characteristics for PC13 and PI8 . . . . .                              | 167 |
| Table 62. | Output voltage characteristics for PC14 and PC15 . . . . .                             | 168 |
| Table 63. | Output timing characteristics (HSLV OFF) . . . . .                                     | 169 |
| Table 64. | Output timing characteristics (HSLV ON) . . . . .                                      | 173 |
| Table 65. | Output timing characteristics VDDIO2 1.2 V range (HSLV OFF) . . . . .                  | 174 |
| Table 66. | Output timing characteristics VDDIO2 1.2 V (HSLV ON) . . . . .                         | 176 |
| Table 67. | Output timing characteristics for FT_c I/Os (PB13/PB14) . . . . .                      | 177 |
| Table 68. | NRST pin characteristics . . . . .                                                     | 178 |
| Table 69. | EXTI input characteristics . . . . .                                                   | 178 |
| Table 70. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . . .                     | 180 |
| Table 71. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings . . . . .               | 180 |
| Table 72. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . . .                    | 181 |
| Table 73. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings . . . . .              | 182 |
| Table 74. | Asynchronous multiplexed PSRAM/NOR read timings . . . . .                              | 183 |
| Table 75. | Asynchronous multiplexed PSRAM/NOR read-NWAIT timings . . . . .                        | 183 |
| Table 76. | Asynchronous multiplexed PSRAM/NOR write timings . . . . .                             | 185 |
| Table 77. | Asynchronous multiplexed PSRAM/NOR write-NWAIT timings . . . . .                       | 185 |
| Table 78. | Synchronous multiplexed NOR/PSRAM read timings . . . . .                               | 187 |
| Table 79. | Synchronous multiplexed PSRAM write timings . . . . .                                  | 189 |
| Table 80. | Synchronous non-multiplexed NOR/PSRAM read timings . . . . .                           | 190 |
| Table 81. | Synchronous non-multiplexed PSRAM write timings . . . . .                              | 191 |
| Table 82. | Switching characteristics for NAND flash read cycles . . . . .                         | 194 |
| Table 83. | Switching characteristics for NAND flash write cycles . . . . .                        | 194 |
| Table 84. | SDRAM read timings . . . . .                                                           | 195 |
| Table 85. | LPDDR SDRAM read timings . . . . .                                                     | 196 |
| Table 86. | SDRAM write timings . . . . .                                                          | 197 |
| Table 87. | LPDDR SDRAM write timings . . . . .                                                    | 197 |
| Table 88. | OCTOSPI characteristics in SDR mode . . . . .                                          | 198 |
| Table 89. | OCTOSPI characteristics in DTR mode (no DQS) . . . . .                                 | 199 |
| Table 90. | OCTOSPI characteristics in DTR mode (with DQS) / HyperBus . . . . .                    | 200 |
| Table 91. | Delay block characteristics . . . . .                                                  | 202 |
| Table 92. | DCMI characteristics . . . . .                                                         | 203 |
| Table 93. | PSSI transmit characteristics . . . . .                                                | 204 |
| Table 94. | PSSI receive characteristics . . . . .                                                 | 204 |

|            |                                                                 |     |
|------------|-----------------------------------------------------------------|-----|
| Table 95.  | 12-bit ADC characteristics                                      | 206 |
| Table 96.  | Minimum sampling time versus $R_{AIN}$                          | 208 |
| Table 97.  | ADC accuracy                                                    | 210 |
| Table 98.  | DAC characteristics                                             | 213 |
| Table 99.  | DAC accuracy                                                    | 215 |
| Table 100. | Analog temperature sensor characteristics                       | 217 |
| Table 101. | Temperature sensor calibration values                           | 217 |
| Table 102. | Digital temperature sensor characteristics                      | 218 |
| Table 103. | $V_{CORE}$ monitoring characteristics                           | 218 |
| Table 104. | $V_{BAT}$ monitoring characteristics                            | 218 |
| Table 105. | $V_{BAT}$ charging characteristics                              | 219 |
| Table 106. | Temperature monitoring characteristics                          | 219 |
| Table 107. | Voltage booster for analog switch characteristics               | 219 |
| Table 108. | $V_{REFBUF}$ characteristics                                    | 219 |
| Table 109. | TIMx characteristics                                            | 221 |
| Table 110. | LPTIMx characteristics                                          | 221 |
| Table 111. | I2C analog filter characteristics                               | 222 |
| Table 112. | USART characteristics                                           | 222 |
| Table 113. | I3C open-drain measured timings                                 | 224 |
| Table 114. | I3C push-pull measured timings                                  | 225 |
| Table 115. | SPI characteristics                                             | 226 |
| Table 116. | I <sup>2</sup> S dynamic characteristics                        | 229 |
| Table 117. | USB DC electrical characteristics                               | 231 |
| Table 118. | USB startup time                                                | 231 |
| Table 119. | USB electrical characteristics                                  | 231 |
| Table 120. | USB BCD DC electrical characteristics                           | 232 |
| Table 121. | SAI characteristics                                             | 233 |
| Table 122. | Dynamic characteristics: SD/MMC, VDD = 2.7 to 3.6 V             | 235 |
| Table 123. | Dynamic characteristics: eMMC, VDD = 1.71 to 1.9 V              | 235 |
| Table 124. | Dynamic characteristics: Ethernet MAC signals for SMI           | 237 |
| Table 125. | Dynamic characteristics: Ethernet MAC signals for RMII          | 237 |
| Table 126. | Dynamic characteristics: Ethernet MAC signals for MII           | 238 |
| Table 127. | Dynamic JTAG characteristics                                    | 240 |
| Table 128. | Dynamic SWD characteristics                                     | 240 |
| Table 129. | LQFP64 - Mechanical data                                        | 244 |
| Table 130. | VFQFPN68 - Mechanical data                                      | 247 |
| Table 131. | WLCSP80 - Mechanical data                                       | 249 |
| Table 132. | WLCSP80 - Example of PCB design rules                           | 250 |
| Table 133. | LQFP100 - Mechanical data                                       | 252 |
| Table 134. | LQFP144 - Mechanical data                                       | 255 |
| Table 135. | UFBGA169 - Mechanical data                                      | 259 |
| Table 136. | UFBGA169 - Example of PCB design rules (0.5 mm pitch BGA)       | 260 |
| Table 137. | LQFP176 - Mechanical data                                       | 262 |
| Table 138. | UFBGA(176+25) - Mechanical data                                 | 265 |
| Table 139. | UFBGA(176+25) - Example of PCB design rules (0.65 mm pitch BGA) | 266 |
| Table 140. | TFBGA225 - Mechanical data                                      | 268 |
| Table 141. | TFBGA225 - Recommended PCB design rules (0.8 mm pitch BGA)      | 269 |
| Table 142. | Package thermal characteristics                                 | 270 |
| Table 143. | Document revision history                                       | 275 |

## List of figures

|            |                                                                                                                             |     |
|------------|-----------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 1.  | STM32H562xx and STM32H563xx block diagram . . . . .                                                                         | 19  |
| Figure 2.  | STM32H562xx and STM32H563xx power supply overview (with SMPS) . . . . .                                                     | 30  |
| Figure 3.  | STM32H562xx and STM32H563xx power supply overview (with LDO) . . . . .                                                      | 31  |
| Figure 4.  | Power-up/down sequence . . . . .                                                                                            | 32  |
| Figure 5.  | LQFP64 pinout . . . . .                                                                                                     | 64  |
| Figure 6.  | VFQFPN68 pinout . . . . .                                                                                                   | 65  |
| Figure 7.  | WLCSP80 SMPS ballout . . . . .                                                                                              | 65  |
| Figure 8.  | LQFP100 pinout . . . . .                                                                                                    | 66  |
| Figure 9.  | LQFP100 SMPS pinout . . . . .                                                                                               | 67  |
| Figure 10. | LQFP144 pinout . . . . .                                                                                                    | 68  |
| Figure 11. | LQFP144 SMPS pinout . . . . .                                                                                               | 69  |
| Figure 12. | UFBGA169 ballout . . . . .                                                                                                  | 70  |
| Figure 13. | UFBGA169 SMPS ballout. . . . .                                                                                              | 71  |
| Figure 14. | LQFP176 pinout . . . . .                                                                                                    | 72  |
| Figure 15. | LQFP176 SMPS pinout . . . . .                                                                                               | 73  |
| Figure 16. | UFBGA176+25 ballout . . . . .                                                                                               | 74  |
| Figure 17. | UFBGA176+25 SMPS ballout. . . . .                                                                                           | 75  |
| Figure 18. | TFBGA225 ballout . . . . .                                                                                                  | 76  |
| Figure 19. | Pin loading conditions . . . . .                                                                                            | 124 |
| Figure 20. | Pin input voltage . . . . .                                                                                                 | 124 |
| Figure 21. | Power supply scheme with SMPS . . . . .                                                                                     | 125 |
| Figure 22. | Power supply scheme with LDO . . . . .                                                                                      | 126 |
| Figure 23. | External capacitor $C_{EXT}$ . . . . .                                                                                      | 133 |
| Figure 24. | SMPS efficiency versus load current in Run, Sleep, and Stop modes<br>with SVOS3 mode, $T_J = 30^{\circ}\text{C}$ . . . . .  | 134 |
| Figure 25. | SMPS efficiency versus load current in Run, Sleep, and Stop modes<br>with SVOS3 mode, $T_J = 130^{\circ}\text{C}$ . . . . . | 134 |
| Figure 26. | SMPS efficiency versus load current in stop SVOV4, SVOS5, $T_J = 30^{\circ}\text{C}$ . . . . .                              | 135 |
| Figure 27. | SMPS efficiency versus load current in stop SVOV4, SVOS5, $T_J = 130^{\circ}\text{C}$ . . . . .                             | 135 |
| Figure 28. | High-speed external clock source AC timing diagram . . . . .                                                                | 151 |
| Figure 29. | Low-speed external clock source AC timing diagram . . . . .                                                                 | 152 |
| Figure 30. | Typical application with an 8 MHz crystal . . . . .                                                                         | 153 |
| Figure 31. | Typical application with a 32.768 kHz crystal . . . . .                                                                     | 154 |
| Figure 32. | VIL/VIH for all I/Os except BOOT0 . . . . .                                                                                 | 165 |
| Figure 33. | Recommended NRST pin protection . . . . .                                                                                   | 178 |
| Figure 34. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . . .                                                        | 179 |
| Figure 35. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . . .                                                       | 181 |
| Figure 36. | Asynchronous multiplexed PSRAM/NOR read waveforms. . . . .                                                                  | 182 |
| Figure 37. | Asynchronous multiplexed PSRAM/NOR write waveforms . . . . .                                                                | 184 |
| Figure 38. | Synchronous multiplexed NOR/PSRAM read timings . . . . .                                                                    | 186 |
| Figure 39. | Synchronous multiplexed PSRAM write timings. . . . .                                                                        | 188 |
| Figure 40. | Synchronous non-multiplexed NOR/PSRAM read timings . . . . .                                                                | 190 |
| Figure 41. | Synchronous non-multiplexed PSRAM write timings . . . . .                                                                   | 191 |
| Figure 42. | NAND controller waveforms for read access . . . . .                                                                         | 192 |
| Figure 43. | NAND controller waveforms for write access . . . . .                                                                        | 193 |
| Figure 44. | NAND controller waveforms for common memory read access . . . . .                                                           | 193 |
| Figure 45. | NAND controller waveforms for common memory write access. . . . .                                                           | 194 |
| Figure 46. | SDRAM read access waveforms (CL = 1) . . . . .                                                                              | 195 |

|            |                                                                                                             |     |
|------------|-------------------------------------------------------------------------------------------------------------|-----|
| Figure 47. | SDRAM write access waveforms . . . . .                                                                      | 196 |
| Figure 48. | OCTOSPI SDR read/write timing diagram . . . . .                                                             | 198 |
| Figure 49. | OCTOSPI timing diagram - DTR mode. . . . .                                                                  | 201 |
| Figure 50. | OCTOSPI HyperBus clock . . . . .                                                                            | 201 |
| Figure 51. | OCTOSPI HyperBus read. . . . .                                                                              | 201 |
| Figure 52. | OCTOSPI HyperBus write . . . . .                                                                            | 202 |
| Figure 53. | DCMI timing diagrams . . . . .                                                                              | 203 |
| Figure 54. | PSSI transmit timing diagram . . . . .                                                                      | 205 |
| Figure 55. | PSSI receive timing diagram . . . . .                                                                       | 205 |
| Figure 56. | ADC conversion timing diagram . . . . .                                                                     | 210 |
| Figure 57. | ADC accuracy characteristics. . . . .                                                                       | 211 |
| Figure 58. | Typical connection diagram when using the ADC with FT/TT pins<br>featuring analog switch function . . . . . | 211 |
| Figure 59. | Power supply and reference decoupling ( $V_{REF+}$ not connected to $V_{DDA}$ ). . . . .                    | 212 |
| Figure 60. | Power supply and reference decoupling ( $V_{REF+}$ connected to $V_{DDA}$ ). . . . .                        | 213 |
| Figure 61. | 12-bit buffered/non-buffered DAC. . . . .                                                                   | 217 |
| Figure 62. | USART timing diagram in Master mode . . . . .                                                               | 223 |
| Figure 63. | USART timing diagram in Slave mode . . . . .                                                                | 224 |
| Figure 64. | SPI timing diagram - Master mode . . . . .                                                                  | 227 |
| Figure 65. | SPI timing diagram - Slave mode and CPHA = 0 . . . . .                                                      | 228 |
| Figure 66. | SPI timing diagram - Slave mode and CPHA = 1 . . . . .                                                      | 228 |
| Figure 67. | I <sup>2</sup> S slave timing diagram (Philips protocol) <sup>(1)</sup> . . . . .                           | 230 |
| Figure 68. | I <sup>2</sup> S master timing diagram (Philips protocol) <sup>(1)</sup> . . . . .                          | 230 |
| Figure 69. | USB timings - definition of data signal rise and fall time. . . . .                                         | 231 |
| Figure 70. | SAI master timing waveforms . . . . .                                                                       | 234 |
| Figure 71. | SAI slave timing waveforms . . . . .                                                                        | 234 |
| Figure 72. | SDIO high-speed/eMMC timing . . . . .                                                                       | 236 |
| Figure 73. | SD default speed timings . . . . .                                                                          | 236 |
| Figure 74. | DDR mode timings . . . . .                                                                                  | 237 |
| Figure 75. | Ethernet RMII timing diagram . . . . .                                                                      | 238 |
| Figure 76. | Ethernet MII timing diagram . . . . .                                                                       | 239 |
| Figure 77. | Ethernet SMI timing diagram . . . . .                                                                       | 239 |
| Figure 78. | JTAG timing diagram . . . . .                                                                               | 240 |
| Figure 79. | SWD timing diagram . . . . .                                                                                | 241 |
| Figure 80. | LQFP64 - Outline <sup>(15)</sup> . . . . .                                                                  | 243 |
| Figure 81. | LQFP64 - Footprint example . . . . .                                                                        | 245 |
| Figure 82. | VFQFPN68 - Outline. . . . .                                                                                 | 246 |
| Figure 83. | VFQFPN68 - Footprint example . . . . .                                                                      | 247 |
| Figure 84. | WLCSP80 - Outline . . . . .                                                                                 | 248 |
| Figure 85. | WLCSP80 - Footprint example . . . . .                                                                       | 250 |
| Figure 86. | WLCSP80 marking example (package top view) . . . . .                                                        | 250 |
| Figure 87. | LQFP100 - Outline <sup>(15)</sup> . . . . .                                                                 | 251 |
| Figure 88. | LQFP100 - Footprint example . . . . .                                                                       | 253 |
| Figure 89. | LQFP144 - Outline <sup>(15)</sup> . . . . .                                                                 | 254 |
| Figure 90. | LQFP144 - Footprint example . . . . .                                                                       | 257 |
| Figure 91. | UFBGA169 - Outline. . . . .                                                                                 | 258 |
| Figure 92. | UFBGA169 - Footprint example . . . . .                                                                      | 260 |
| Figure 93. | LQFP176 - Outline <sup>(15)</sup> . . . . .                                                                 | 261 |
| Figure 94. | LQFP176 - Footprint example . . . . .                                                                       | 264 |
| Figure 95. | UFBGA(176+25) - Outline . . . . .                                                                           | 265 |
| Figure 96. | UFBGA(176+25) - Footprint example. . . . .                                                                  | 266 |
| Figure 97. | TFBGA225 - Outline <sup>(13)</sup> . . . . .                                                                | 267 |

|                                               |     |
|-----------------------------------------------|-----|
| Figure 98. TFBGA225 - Footprint example ..... | 269 |
|-----------------------------------------------|-----|

# 1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32H562xx and STM32H563xx microcontrollers.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32H562xx and STM32H563xx errata sheet.

For information on the Arm<sup>®(a)</sup> Cortex<sup>®</sup>-M33 core, refer to the Cortex<sup>®</sup>-M33 Technical Reference Manual, available from the [www.arm.com](http://www.arm.com) website.

The logo for Arm, consisting of the word "arm" in a lowercase, bold, sans-serif font.

---

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

## 2 Description

The STM32H562xx and STM32H563xx devices are high-performance microcontrollers of the STM32H5 series, based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 250 MHz.

The Cortex®-M33 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types. This core implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (up to 2 Mbytes of dual bank flash memory and 640 Kbytes of SRAM), a flexible external memory controller (FMC) for devices with packages of 100 pins and more, one OCTOSPI memory interface (at least one Quad-SPI available on all packages), and an extensive range of enhanced I/Os and peripherals connected to three APB buses, three AHB buses, and a 32-bit multi-AHB bus matrix.

The devices offer security foundation compliant with the trusted-based security architecture (TBSA) requirements from Arm®. They embed the features to implement a secure firmware update. Besides these capabilities, the devices incorporate a secure firmware installation that allows the customer to secure the provisioning of the code during its production. A flexible life cycle is managed thanks to multiple levels of protection and secure debug authentication. Firmware hardware isolation is supported thanks to securable peripherals, memories, and I/Os, and to privilege configuration of peripherals and memories.

The devices feature several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, secure, and hide protection areas.

Dedicated peripherals reinforce security: an HASH hardware accelerator, and a true random number generator.

The devices offer active tamper detection and protection against transient and environmental perturbation attacks, thanks to several internal monitoring, generating secret data erase in case of attack. This helps to fit the PCI requirements for point of sales applications.

The devices offer two fast 12-bit ADCs, two DAC channels, an internal voltage reference buffer, a low-power RTC, two 32-bit general-purpose timers, two 16-bit PWM timers dedicated to motor control, eight 16-bit general-purpose timers, two 16-bit basic timers, and six 16-bit low-power timers.

The devices also feature standard and advanced communication interfaces, namely: four I<sup>2</sup>Cs, one I3C, six SPIs, three I2Ss, six USARTs, six UARTs and one low-power UART, two SAIs, one digital camera interface (DCMI), up to two SDMMCs, up to two FDCANs, one USB full-speed, one USB Type-C®/USB power delivery controller, an Ethernet interface (available only on STM32H563xx).

The devices operate in the -40 to +85°C (+130°C junction) and -40 to +125°C (+130°C junction) temperature ranges, with a 1.71 to 3.6 V power supply.

A comprehensive set of power-saving modes enables the design of low-power applications.

Independent power supplies are supported: an analog independent supply input for ADC, DACs, a 3.3 V dedicated supply input for USB, and a dedicated supply input for some GPIOs and SDMMC. A VBAT input is available to connect a backup battery, to preserve the RTC functionality, and to backup 32 32-bit registers and a 4-Kbyte SRAM.

The devices offer nine packages, from 64 to 225 pins.

All packages are available with LDO or SMPS supply options for the  $V_{CORE}$  (except for LQFP64 and VFQFPN68 packages, not available in SMPS, and WLCSP80 and TFBGA225, not available in LDO).

**Table 2. STM32H56xxx features and peripheral counts**

| Peripherals                                            |                                       | STM32H563RI/G               | STM32H562RI/G      | STM32H563MI        | STM32H563VI/G | STM32H562VI/G | STM32H563ZI/G | STM32H562ZI/G | STM32H563AI/G | STM32H562AI/G | STM32H563II/G | STM32H562II/G | STM32H563LI |
|--------------------------------------------------------|---------------------------------------|-----------------------------|--------------------|--------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|-------------|
| Flash memory                                           |                                       | Up to 2 Mbytes              |                    |                    |               |               |               |               |               |               |               |               |             |
| SRAM                                                   | System                                | 640 (256 + 64 + 320) Kbytes |                    |                    |               |               |               |               |               |               |               |               |             |
|                                                        | Backup                                | 4 Kbytes                    |                    |                    |               |               |               |               |               |               |               |               |             |
| Flexible memory controller for external memories (FMC) |                                       | No                          | Yes <sup>(1)</sup> | Yes <sup>(2)</sup> | Yes           |               |               |               |               |               |               |               |             |
| OCTOSPI                                                |                                       | 1                           |                    |                    |               |               |               |               |               |               |               |               |             |
| Timers                                                 | Advanced control                      | 2 (16 bits)                 |                    |                    |               |               |               |               |               |               |               |               |             |
|                                                        | General purpose                       | 2 (32 bits) and 8 (16 bits) |                    |                    |               |               |               |               |               |               |               |               |             |
|                                                        | Basic                                 | 2 (16 bits)                 |                    |                    |               |               |               |               |               |               |               |               |             |
|                                                        | Low power                             | 6 (16 bits)                 |                    |                    |               |               |               |               |               |               |               |               |             |
|                                                        | SysTick timer                         | 2                           |                    |                    |               |               |               |               |               |               |               |               |             |
|                                                        | Watchdog timers (independent, window) | 2                           |                    |                    |               |               |               |               |               |               |               |               |             |

Table 2. STM32H56xxx features and peripheral counts (continued)

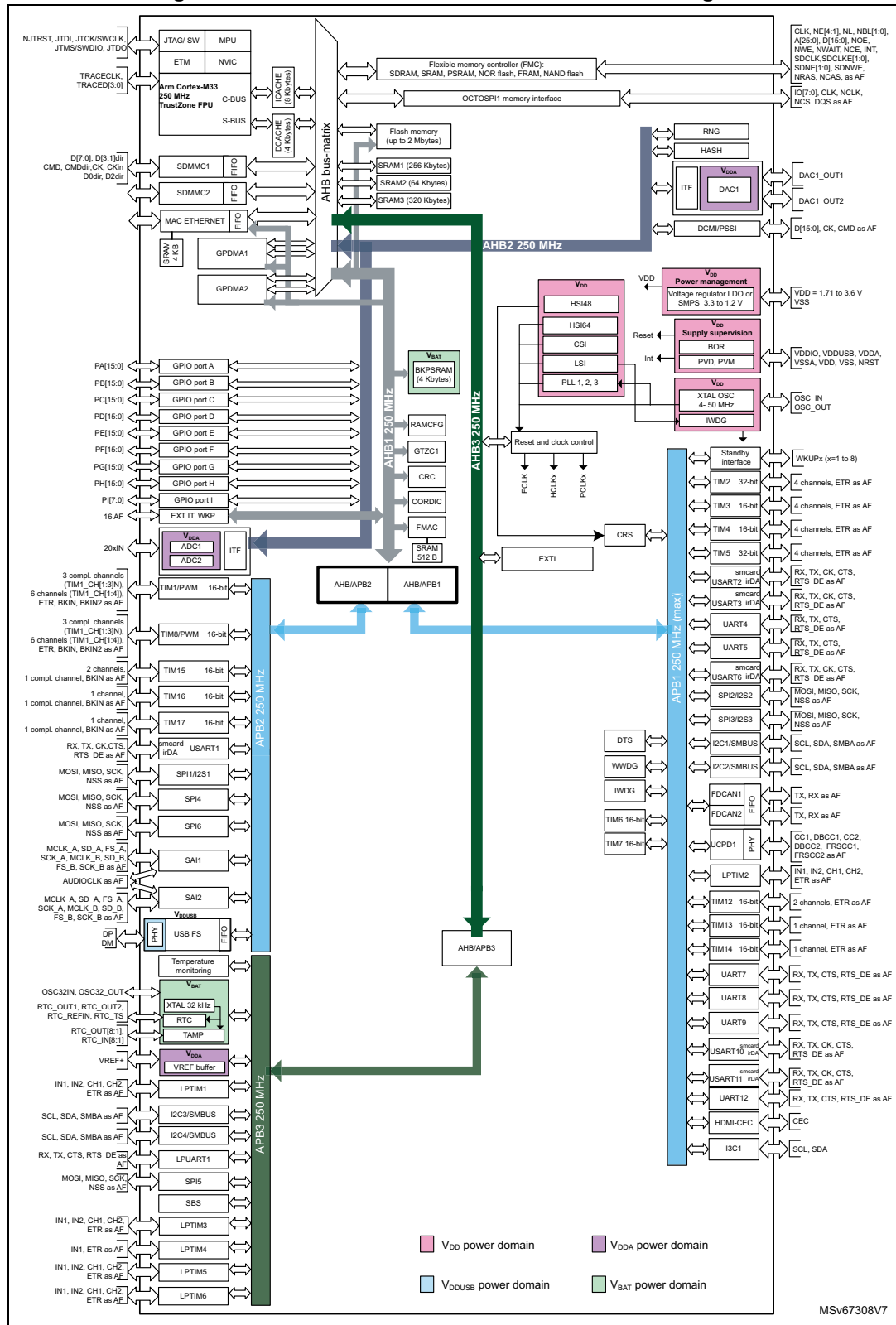
| Peripherals                            |                                                     | STM32H563RI/G     | STM32H562RI/G | STM32H563MI | STM32H563VI/G | STM32H562VI/G | STM32H563ZI/G | STM32H562ZI/G | STM32H563AI/G | STM32H562AI/G      | STM32H563II/G      | STM32H562II/G | STM32H563LI |
|----------------------------------------|-----------------------------------------------------|-------------------|---------------|-------------|---------------|---------------|---------------|---------------|---------------|--------------------|--------------------|---------------|-------------|
| Communication interfaces               | SPI / I2S                                           | 4/3               |               |             | 5/3           |               | 6/3           |               |               |                    |                    |               |             |
|                                        | I2C                                                 | 4                 |               |             |               |               |               |               |               |                    |                    |               |             |
|                                        | I3C                                                 | 1 <sup>(3)</sup>  |               |             |               |               |               |               |               |                    |                    |               |             |
|                                        | USART                                               | 5                 |               |             | 6             |               |               |               |               |                    |                    |               |             |
|                                        | UART                                                | 5                 |               |             | 6             |               |               |               |               |                    |                    |               |             |
|                                        | LPUART                                              | 1                 |               |             |               |               |               |               |               |                    |                    |               |             |
|                                        | SAI                                                 | 2                 |               |             |               |               |               |               |               |                    |                    |               |             |
|                                        | FDCAN                                               | 2                 | 1             | 2           | 1             | 2             | 1             | 2             | 1             | 2                  | 1                  | 2             |             |
|                                        | USB                                                 | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
|                                        | UCPD                                                | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
|                                        | SDMMC                                               | 1                 |               |             | 2             | 1             | 2             | 1             | 2             | 1                  | 2                  | 1             | 2           |
|                                        | Digital camera interface (DCMI)/PSSI <sup>(4)</sup> | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
|                                        | Ethernet (legacy/SMPS)                              | Yes/ No           | No            | No/Yes      | Yes/ No       | No            | Yes/ No       | No            | Yes/ Yes      | No                 | Yes/ Yes           | No            | No/Yes      |
|                                        | HDMI-CEC                                            | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
| CORDIC coprocessor                     |                                                     | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
| Filter mathematical accelerator (FMAC) |                                                     | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
| Real time clock (RTC)                  |                                                     | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
| Tamper pins                            | Legacy                                              | 5                 | NA            | 8           |               |               |               |               |               |                    |                    | NA            |             |
|                                        | SMPS                                                | NA                | 5             | 8           |               |               |               |               |               |                    |                    |               |             |
| Active tamperers <sup>(5)</sup>        | Legacy                                              | 4                 | NA            | 7           |               |               |               |               |               |                    |                    | NA            |             |
|                                        | SMPS                                                | NA                | 4             | 7           |               |               |               |               |               |                    |                    |               |             |
| True random number generator           |                                                     | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
| HASH (SHA-512)                         |                                                     | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
| PKA (ECDSA signature verification)     |                                                     | Yes               |               |             |               |               |               |               |               |                    |                    |               |             |
| GPIOs                                  | Legacy                                              | 53 <sup>(6)</sup> | NA            | 80          | 80            | 112           | 112           | 136           | 136           | 140 <sup>(7)</sup> | 140 <sup>(7)</sup> | NA            |             |
|                                        | SMPS                                                | NA                | 57            | 78          | NA            | 110           | NA            | 134           | NA            | 139                | NA                 | 140           |             |
| Wake-up pins                           | Legacy                                              | 6                 | NA            | 7           | 7             | 7             | 7             | 8             | 8             | 8                  | 8                  | NA            |             |
|                                        | SMPS                                                | NA <sup>(8)</sup> | 6             |             | NA            |               | NA            |               | 8             |                    | NA                 | 8             |             |
| Number of I/Os down to 1.08 V          | Legacy                                              | 0                 | NA            | 0           | 0             | 10            | 10            | 10            | 10            | 10                 | 10                 | NA            |             |
|                                        | SMPS                                                | NA                | 0             |             | NA            |               | NA            | 7             | NA            | 7                  | NA                 | 10            |             |

Table 2. STM32H56xxx features and peripheral counts (continued)

| Peripherals                       |                                    | STM32H563RI/G                                                                                          | STM32H562RI/G | STM32H563MI | STM32H563VI/G | STM32H562VI/G | STM32H563ZI/G | STM32H562ZI/G | STM32H563AI/G       | STM32H562AI/G | STM32H563II/G | STM32H562II/G | STM32H563LI |
|-----------------------------------|------------------------------------|--------------------------------------------------------------------------------------------------------|---------------|-------------|---------------|---------------|---------------|---------------|---------------------|---------------|---------------|---------------|-------------|
| ADC                               | 12-bit ADC                         | 2                                                                                                      |               |             |               |               |               |               |                     |               |               |               |             |
|                                   | Number of channels (legacy/SMPS)   | 16/NA                                                                                                  | NA/16         | 16 /14      | 16 /NA        | 20 /18        | 20 /NA        | 20 /20        | 20/ NA              | 20 /20        | 20/ NA        | NA/20         |             |
| DAC                               | 12-bit DAC controller              | 1                                                                                                      |               |             |               |               |               |               |                     |               |               |               |             |
|                                   | Number of 12-bit D to A converters | 2                                                                                                      |               |             |               |               |               |               |                     |               |               |               |             |
| Internal voltage reference buffer |                                    | No                                                                                                     |               |             | Yes           |               |               |               |                     |               |               |               |             |
| Maximum CPU frequency             |                                    | 250 MHz                                                                                                |               |             |               |               |               |               |                     |               |               |               |             |
| Operating voltage                 |                                    | 1.71 to 3.6 V                                                                                          |               |             |               |               |               |               |                     |               |               |               |             |
| Operating temperature             | Ambient                            | -40 to 85 or 105 °C / -40 to 125 °C                                                                    |               |             |               |               |               |               |                     |               |               |               |             |
|                                   | Junction                           | Voltage range VOS0 (up to 250 MHz): -40 to 105 °C<br>Voltage range VOS1 (up to 200 MHz): -40 to 130 °C |               |             |               |               |               |               |                     |               |               |               |             |
| Package                           |                                    | LQFP64<br>VFQFPN68                                                                                     | WLCSP80       | LQFP100     | LQFP144       |               | UFBGA169      |               | LQFP176<br>UFBGA176 |               | TFBGA225      |               |             |

1. 8-bit to interface LCD controller.
2. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
3. Shares the I/Os with I2C4.
4. DCMI and PSSI cannot be used at the same time, as they share the same circuitry.
5. Active tamper in output sharing mode (one output shared by all inputs).
6. 49 for LQFP64.
7. 136 for LQFP176.
8. 5 for VFQFPN68.

Figure 1. STM32H562xx and STM32H563xx block diagram



Note: PC[15:13] are in the  $V_{BAT}$  domain.

## 3 Functional overview

### 3.1 Arm Cortex-M33 core with TrustZone and FPU

The Cortex-M33 with TrustZone and FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security. This processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. It features:

- Arm TrustZone technology, using the Armv8-M main extension supporting secure and nonsecure states
- Memory protection units (MPUs), supporting up to 16 regions for secure and nonsecure applications
- Configurable secure attribute unit (SAU) supporting up to eight memory regions as secure or nonsecure
- Floating-point arithmetic functionality with support for single precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex-M33 processor supports the following bus interfaces:

- System AHB bus:  
The system AHB (S-AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, external RAM and external device, or Vendor\_SYS regions of the Armv8-M memory map.
- Code AHB bus:  
The code AHB (C-AHB) bus interface is used for any instruction fetch and data access to the code region of the Armv8-M memory map.

*Figure 1* shows the general block diagram of the STM32H562xx and STM32H563xx devices.

### 3.2 ART Accelerator (ICACHE and DCACHE)

#### 3.2.1 Instruction cache (ICACHE)

The instruction cache (ICACHE) is introduced on C-AHB code bus of Cortex-M33 processor to improve performance when fetching instruction (or data) from both internal and external memories.

ICACHE offers the following features:

- Multi-bus interface:
  - Slave port receiving the memory requests from the Cortex-M33 C-AHB code execution port
  - Master1 port performing refill requests to internal memories (flash memory and SRAMs)
  - Master2 port performing refill requests to external memories (external flash memory and RAMs through Octo-SPI and FMC interfaces)
  - Second slave port dedicated to ICACHE registers access

- Close to 0 wait-states instructions/data access performance:
  - 0 wait-states on cache hit
  - Hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - Critical-word-first refill policy, minimizing processor stalls on cache miss
  - Hit ratio improved by two-way set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - Dual master ports to decouple internal and external memory traffic, respectively, on fast and slow buses, minimizing impact on interrupt latency
  - Optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of a hit counter and a miss counter
- Extension of cacheable region beyond the code memory space, by means of address remapping logic that allows four cacheable external regions to be defined
- Power consumption reduced intrinsically (more accesses to cache memory rather than to bigger main memories); even improved by configuring ICACHE as direct mapped (rather than the default two-way set-associative mode)
- TrustZone security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

### 3.2.2 Data cache (DCACHE)

The data cache (DCACHE) is introduced on S-AHB system bus of Cortex-M33 processor to improve the performance of data traffic to/from external memories. DCACHE offers the following features:

- Multi-bus interface:
  - Slave port receiving the memory requests from the Cortex-M33 S-AHB system port
  - Master port performing refill requests to external memories (external flash memory and RAMs through Octo-SPI and FMC interfaces)
  - A second slave port dedicated to DCACHE registers access
- Close to 0 wait-states external data access performance:
  - 0 wait-states on cache hit
  - Hit-under-miss capability, allowing to serve new processor requests to cached data, while a line refill (due to a previous cache miss) is still ongoing
  - Critical-word-first refill policy for read transactions, minimizing processor stalls on cache miss
  - Hit ratio improved by two-way set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - Optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of two hit counters (for read and write) and two miss counters (for read and write)

- Supported cache accesses:
  - Supports both write-back and write-through policies (selectable with AHB bufferable attribute)
  - Read and write-back always allocated
  - Write-through always non-allocated (write-around)
  - Supports byte, half-word, and word writes
- TrustZone security support
- Maintenance operations for software management of cache coherency:
  - Full cache invalidation (non interruptible)
  - Address range clean and/or invalidate operations (background task, interruptible)
- Error management: detection of error for master port request initiated by DCACHE (line eviction or clean operation), with optional interrupt raising

### 3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by other active tasks. This memory area is organized into up to 20 protected areas (12 secure and 8 nonsecure). The MPU regions and registers are banked across secure and nonsecure states.

The MPU is especially helpful for applications where critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

If a program accesses a memory location prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area settings based on the process to be executed.

### 3.4 Embedded flash memory

The devices feature up to 2 Mbytes of embedded flash memory for storing programs and data. The flash memory supports a high-cycle data area of up to 100 K cycles.

The flash memory interface features dual-bank operating modes, and read-while-write (RWW). This allows a read operation to be performed on one bank while an erase or program operation is performed on the other bank. Each bank contains 128 8-Kbyte pages.

The flash memory embeds a 2-Kbyte OTP (one-time programmable) for user data, and up to 96 Kbytes supporting high cycling capability (100 K cycles), to use for data (EEPROM emulation).

Option bytes are available to set the flash memory protection mechanisms:

- Different product states for protecting memory content from debug access
- Write protection (WRP) to protect areas against erasing and programming. Two areas per bank can be selected with 8-Kbyte granularity.
- Sector group write-protection (WRPSG), protecting up to 32 groups of four sectors (32 Kbytes) per bank
- Two secure-only areas (one per user flash memory bank). When enabled, this area is accessible only if the device operates in Secure-access mode

- One HDP area per bank providing temporal isolation for startup code

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single-error detection and correction
- Double-error detection
- ECC fail address report

### 3.4.1 FLASH security and protections

Sensitive information is stored in the flash memory and it is important to protect the memory against unwanted operations such as reading confidential areas, illegal programming of immutable sectors, or malicious flash memory erasing.

For that purpose the following protection mechanisms are implemented:

- TrustZone backed watermark and block security protection
- Temporal isolation protection (HDP)
- Configuration protection
- User flash memory write protection
- Device non-volatile security life cycle and application boot state management
- OTP locking

Refer to the product reference manual for a detailed description of the security mechanisms.

### 3.4.2 FLASH privilege protection

Each flash memory sector can be programmed on the fly as privileged or unprivileged.

## 3.5 Embedded SRAMs

Four SRAMs are embedded in the STM32H562xx and STM32H563xx devices, each with specific features. SRAM1, SRAM2, and SRAM3 are the main ones.

These SRAMs are made of several blocks that can be powered down in Stop mode to reduce consumption:

- SRAM1: 256 Kbytes
- SRAM2: 64 Kbytes with ECC
- SRAM3: 320 Kbytes with optional ECC (when enabled, 64 Kbytes are reserved for it)
- BKPSRAM (backup SRAM): 4 Kbytes with optional ECC, can be retained in all low-power modes and when  $V_{DD}$  is off in VBAT mode

*Note:* The ECC is supported by SRAM2, SRAM3, and BKPSRAM when enabled with the SRAM2\_ECC, SRAM3\_ECC, and BKPSRAM\_ECC user option bits.

### 3.5.1 SRAMs TrustZone security

When the TrustZone security is enabled, all SRAMs are secure after reset. The SRAM1, SRAM2, SRAM3, can be programmed as secure or nonsecure by blocks, using the MPCBB (block-based memory protection controller).

The granularity of SRAM secure block based is a page of 512 bytes. Backup SRAM regions can be programmed as secure or nonsecure with watermark, using the TZSC (TrustZone security controller) in the GTZC (global TrustZone controller).

### 3.5.2 SRAMs privilege protection

SRAM1, SRAM2, and SRAM3, can be programmed as privileged or non-privileged by blocks, using the MPCBB. The granularity of SRAM privilege block based is a page of 512 bytes. Backup SRAM regions can be programmed as privileged or non-privileged with watermark, using the TZSC (TrustZone security controller) in the GTZC (global TrustZone controller).

## 3.6 Security overview

The STM32H562xx and STM32H563xx security enables the possibility to reopen the debug mode even if the product is in secure state.

The reopening of the debug mode is controlled with a debug authentication procedure which permits the authentication of the host.

Sensible assets (such as keys or secret codes) must be protected when opening the debug mode. The protection is made via code protection and hardware keys storage solutions where all *root of trust* can be protected thanks to hardware mechanisms.

In cases where sensitive information cannot be protected, a partial or a full regression can be launched to start a debug. Regressions are enabled by a debug authentication method.

Developers can introduce their own root of trust solution (OEM-iROT), including their installation in a non-trusted environment, thanks to a secure firmware install (SFI) solution.

The boot stages are isolated via a hardware mechanism called HDPL (temporal isolation level). The HDPL guarantees isolation of the different boot stages: ST assets, iROT (immutable root of trust), uROT (updatable root of trust), secure operating system and nonsecure applications.

The devices embed a hardware key storage solution with a dedicated flash memory area per boot stages with access-control based on HDPL, which can be secure or nonsecure.

STM32H562xx and STM32H563xx are powered by an Arm Cortex-M33 core, associated with all the TrustZone isolation infrastructure. This design permits to benefit from a run time isolation to run secure applications.

## 3.7 Boot modes

At startup, a BOOT0 pin and NSBOOTADD[31:8]/SECBOOTADD[31:8] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory
  - Bootloader
  - ST immutable root of trust (ST-iROT)
  - Root security service (RSS)
  - Debug authentication library (RSS-DA)

### Embedded bootloader

The embedded bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory by using USART, I2C, I3C, SPI, FDCAN, or USB\_FS in device mode through the DFU (device firmware upgrade).

Refer to AN2606 “STM32 microcontroller system memory boot mode”.

### Embedded root security services (RSS)

The embedded RSS are located in the secure information block, programmed by ST during production.

Refer to AN4992 “Introduction to secure firmware install (SFI) for STM32 MCUs”.

### Embedded immutable root of trust (ST-iROT)

The embedded ST-iROT in the system memory, programmed by ST during production. ST-iROT is the immutable root of trust managing the secure boot and secure install of the first updatable level to execute in a boot sequence.

### Embedded debug authentication (ST-DA)

The embedded ST-DA in the system memory is programmed by ST during production. ST-DA is the library that manages the debug authentication protocol, making it possible to securely reopen the debug or to launch regressions on secured products in the field.

## 3.7.1 STM32H562/H563xx boot modes

[Table 3](#) and [Table 4](#), respectively, provide the detail of the boot mode when TrustZone is disabled (TZEN = 0xC3) and enabled (TZEN = 0xB4).

**Table 3. STM32H562/H563 boot mode when TrustZone is disabled (TZEN = 0xC3)**

| PRODUCT_STATE               | BOOT0 pin | Boot address option byte selection | Boot area                                                | ST programmed default value |
|-----------------------------|-----------|------------------------------------|----------------------------------------------------------|-----------------------------|
| Open                        | 0         | NSBOOTADD[31:8]                    | Boot address defined by user option byte NSBOOTADD[31:8] | Flash: 0x0800 0000          |
| -                           | 1         | NA                                 | Bootloader                                               | Bootloader                  |
| Provisioning                | x         | NA                                 | RSS                                                      | RSS                         |
| Provisioned, Closed, Locked | x         | NSBOOTADD[31:8]                    | Boot address defined by user option byte NSBOOTADD[31:8] | Flash: 0x0800 0000          |

**Table 4. STM32H562/H563 boot mode when TrustZone is enabled (TZEN = 0xB4)**

| PRODUCT_STATE | BOOT0 pin | Boot address option-byte selection | Boot area                                                 | ST programmed default value |
|---------------|-----------|------------------------------------|-----------------------------------------------------------|-----------------------------|
| Open          | 0         | SECBOOTADD[31:8]                   | Boot address defined by user option byte SECBOOTADD[31:8] | Flash: 0x0C00 0000          |
| -             | 1         | NA                                 | Bootloader                                                | Bootloader                  |

Table 4. STM32H562/H563 boot mode when TrustZone is enabled (TZEN = 0xB4) (continued)

| PRODUCT_STATE                          | BOOT0 pin | Boot address option-byte selection | Boot area                                                 | ST programmed default value |
|----------------------------------------|-----------|------------------------------------|-----------------------------------------------------------|-----------------------------|
| Provisioning                           | x         | NA                                 | RSS                                                       | RSS                         |
| Provisioned, TZ_Closed, Closed, Locked | x         | SECBOOTADD[31:8]                   | Boot address defined by user option byte SECBOOTADD[31:8] | Flash: 0x0C00 0000          |

When TrustZone is enabled the boot space must be in secure area. SECBOOTADD0[24:0] option bytes are used to select the boot secure memory address. A unique boot entry option can be selected by setting the SECBOOT\_LOCK option bit.

### 3.8 Global TrustZone controller (GTZC)

GTZC is used to configure TrustZone and privileged attributes within the full system.

The GTZC includes three different sub-blocks:

- **TZSC: TrustZone security controller**  
This sub-block defines the secure/privilege state of slave/master peripherals. It also controls the nonsecure area size for the watermark memory peripheral controller (MPCWM). The TZSC block informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.
- **TZIC: TrustZone illegal access controller**  
This sub-block gathers all security illegal access events in the system and generates a secure interrupt towards NVIC.
- **MPCBB: MPCBB: block-based memory protection controller**  
This sub-block controls secure states of all memory blocks (512-byte pages) of the associated SRAM. This peripheral aims at configuring the internal RAM in a TrustZone system product having segmented SRAM with programmable-security and privileged attributes.

The GTZC main features are:

- Three independent 32-bit AHB interfaces for TZSC, TZIC and MPCBB
- MPCBB and TZIC accessible only with secure transactions
  - Enable illegal access events that may trigger a secure interrupt
- Secure and nonsecure access supported for privileged/non-privileged part of TZSC
- Set of registers to define product security settings:
  - Secure/privilege regions for external memories
  - Secure/privilege access mode for securable peripherals
  - Secure/privilege access mode for securable legacy masters

### 3.9 TrustZone security architecture

The security architecture is based on Arm TrustZone with the Armv8-M main extension.

The TrustZone security is activated by the TZEN option bit in the FLASH\_OTPR register.

When the TrustZone is enabled, the SAU (security attribution unit) and IDAU (implementation defined attribution unit) define the access permissions based on secure and nonsecure state.

- SAU: up to eight SAU configurable regions are available for security attribution.
- IDAU: It provides a first memory partition as nonsecure or nonsecure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on IDAU security attribution, the flash memory, system SRAMs and peripherals memory space is aliased twice for secure and nonsecure states. However, the external memories space is not aliased.

### 3.9.1 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be either securable or TrustZone-aware type as follows:

- securable: peripheral protected by an AHB/APB firewall gate controlled from TZSC to define security properties
- TrustZone-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone behavior such as a subset of registers being secure

### 3.9.2 Default TrustZone security state

The default system security state is detailed below:

- CPU:
  - Cortex-M33 is in secure state after reset. The boot address must be in secure address.
- Memory map:
  - SAU is fully secure after reset. Consequently, all memory map is fully secure. Up to eight SAU configurable regions are available for security attribution.
- Flash memory:
  - Flash memory security area is defined by watermark user options.
  - Flash memory block based area is nonsecure after reset.
- SRAMs:
  - All SRAMs are secure after reset. MPCBB (memory protection block based controller) is secure.
- External memories:
  - FMC, OCTOSPI banks are secure after reset. MPCWMx (memory protection watermark based controller) is secure.
- Peripherals
  - Securable peripherals are nonsecure after reset.
  - TrustZone-aware peripherals are nonsecure after reset. Their secure configuration registers are secure.
- All GPIOs are secure after reset.
- Interrupts:
  - NVIC: All interrupts are secure after reset. NVIC is banked for secure and nonsecure state.

- TZIC: All illegal access interrupts are disabled after reset.

## 3.10 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain ( $V_{\text{CORE}}$ )
  - $V_{\text{DD}}$  domain
  - Backup domain ( $V_{\text{BAT}}$ )
  - Analog domain ( $V_{\text{DDA}}$ )
  - SMPS power stage ( $V_{\text{DDSMPS}}$ , available only on SMPS packages)
  - $V_{\text{DDIO2}}$  domain
  - $V_{\text{DDUSB}}$  for USB transceiver
- System supply voltage regulation
  - SMPS step down converter
  - Voltage regulator (LDO)
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - PVD monitor
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- VBAT battery charging
- TrustZone security and privileged protection

### 3.10.1 Power supply schemes

The devices require a 1.71 to 3.6 V  $V_{\text{DD}}$  operating voltage supply. Several independent supplies can be provided for specific peripherals:

- $V_{\text{DD}} = 1.71 \text{ V to } 3.6 \text{ V}$   
 $V_{\text{DD}}$  is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- $V_{\text{DDA}} = 1.62 \text{ V (ADCs), } 1.8 \text{ V (DACs), or } 2.1 \text{ V (VREFBUF) to } 3.6 \text{ V}$   
 $V_{\text{DDA}}$  is the external analog power supply for ADCs, DACs and voltage reference buffer. This voltage level is independent from  $V_{\text{DD}}$ , and must preferably be connected to  $V_{\text{DD}}$  when these peripherals are not used.
- $V_{\text{DDSMPS}} = 1.71 \text{ V to } 3.6 \text{ V}$   
 $V_{\text{DDSMPS}}$  is the external power supply for the SMPS step down converter. It is provided externally through VDDSMPS supply pin and must be connected to the same supply than VDD.

- $V_{LXSMPS}$  is the switched SMPS step down converter output. The SMPS power supply pins are available only on packages with SMPS step down converter option.
- $V_{DDUSB} = 3.0\text{ V to }3.6\text{ V}$   
 $V_{DDUSB}$  is the external independent power supply for USB transceivers. It is independent from  $V_{DD}$ , and must preferably be connected to VDD when the USB is not used.
- $V_{DDIO2} = 1.08\text{ V to }3.6\text{ V}$   
 $V_{DDIO2}$  is the external power supply for ten I/Os (PD6, PD7, PG9:14, PB8, PB9). This voltage level is independent from  $V_{DD}$ , voltage and must preferably be connected to VDD when those pins are not used.
- $V_{BAT} = 1.2\text{ V to }3.6\text{ V}$   
 $V_{BAT}$  is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.
- $V_{REF-}$ ,  $V_{REF+}$   
 $V_{REF+}$  is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.  
 $V_{REF+}$  can be grounded when ADC and DAC are not active.  
 $V_{REF-}$  and  $V_{REF+}$  pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.  
When the  $V_{REF+}$  is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled.  
 $V_{REF-}$  must always be equal to  $V_{SSA}$ .

Depending upon the package, the devices embed an LDO and/or an SMPS regulator, to provide the  $V_{CORE}$  supply for digital peripherals, SRAM1, SRAM2, SRAM3, and embedded flash memory. The SMPS generates this voltage on VCAP (two pins), with a total external capacitor of 10  $\mu\text{F}$  (typical). The SMPS requires an external coil. The LDO generates this voltage on VCAP pin connected to an external capacitor of 2x 2.2  $\mu\text{F}$  (typical).

Both regulators can provide four different voltages (voltage scaling), and can operate in Stop modes.

Figure 2. STM32H562xx and STM32H563xx power supply overview (with SMPS)

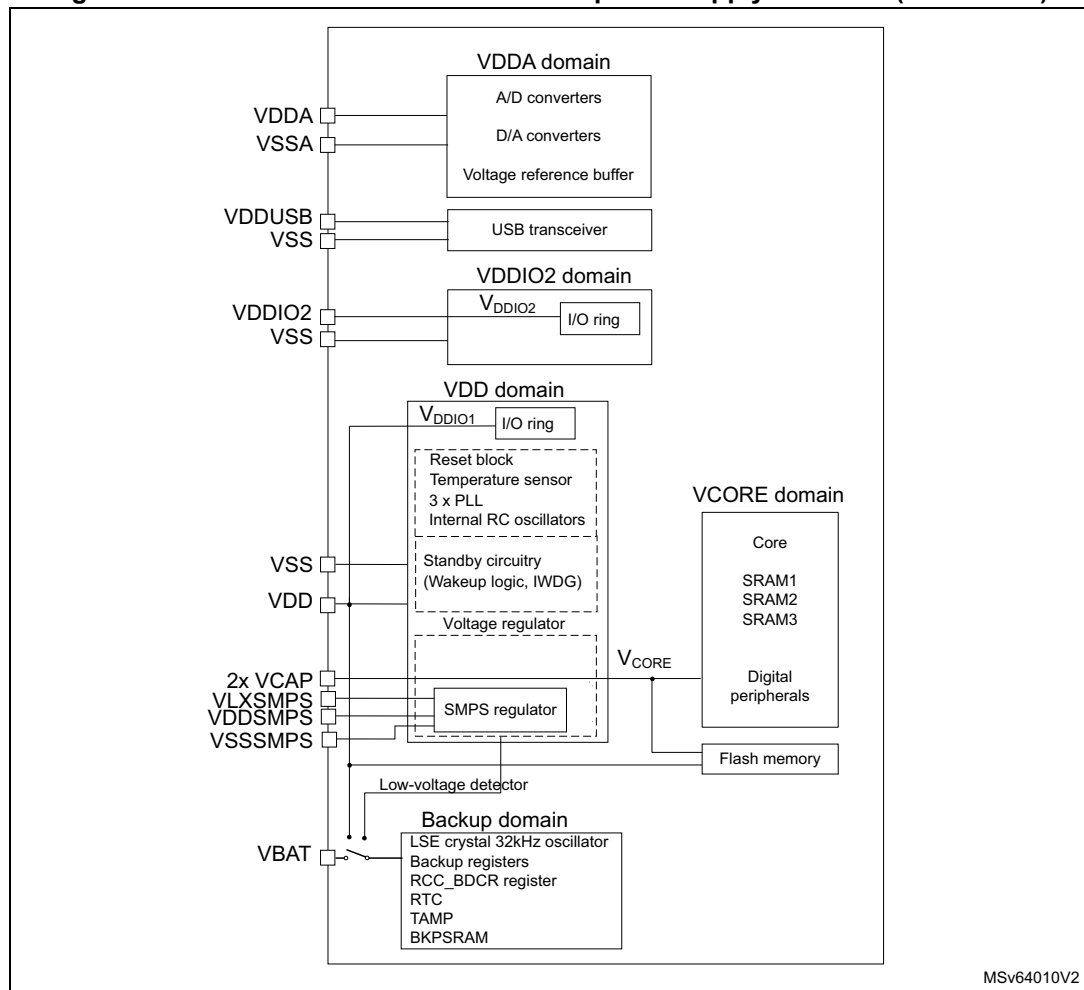
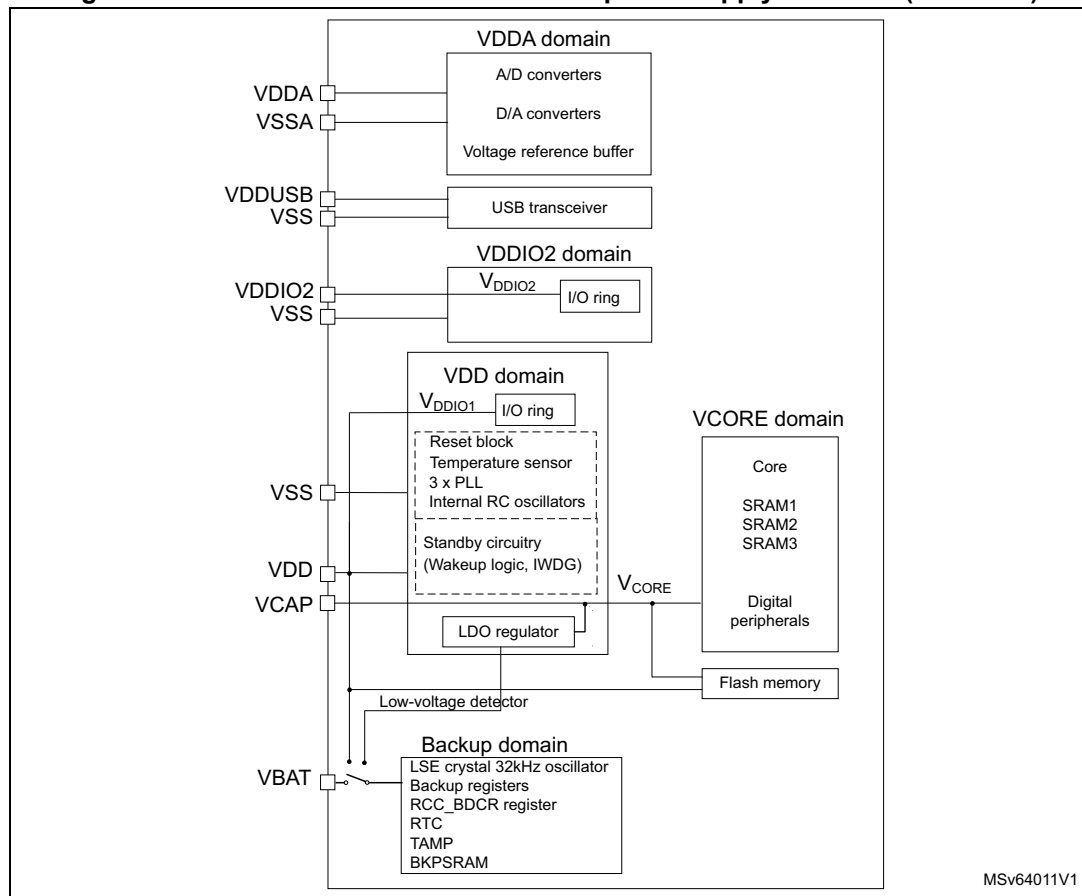


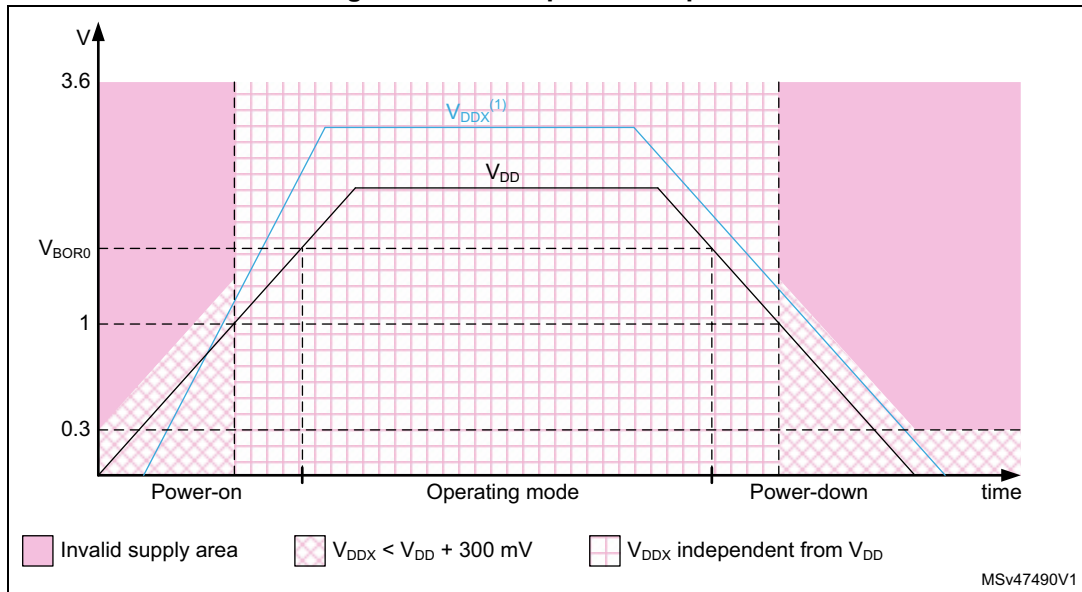
Figure 3. STM32H562xx and STM32H563xx power supply overview (with LDO)



During power-up and power-down phases, the following power sequence requirements must be respected:

- When  $V_{DD}$  is below 1 V, other power supplies ( $V_{DDA}$ ,  $V_{DDIO2}$ ,  $V_{DDUSB}$ ) must remain below  $V_{DD} + 300$  mV.
- When  $V_{DD}$  is above 1 V, all power supplies are independent.
- During the power-down phase,  $V_{DD}$  can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 4. Power-up/down sequence



1.  $V_{DDX}$  refers to any power supply among  $V_{DDA}$ ,  $V_{DDUSB}$ , and  $V_{DDIO2}$ .

### 3.10.2 Power supply supervisor

The devices have an integrated ultra-low-power brownout reset (BOR) active in all modes; The BOR ensures proper operation of the devices after power on and during power down. The devices remain in reset mode when the monitored supply voltage  $V_{DD}$  is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes. The devices feature an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}$  power supply and compares it to the  $V_{PVD}$  threshold.

An interrupt can be generated when  $V_{DD}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor that compares the independent supply voltages  $V_{DDA}$ ,  $V_{DDUSB}$  and  $V_{DDIO2}$  to ensure that the peripheral is in its functional supply range.

The devices support dynamic voltage scaling to optimize power consumption in Run mode. The voltage from the main regulator that supplies the logic ( $V_{CORE}$ ) can be adjusted according to the system maximum operating frequency.

The main regulator operates in the following ranges:

- VOS0 ( $V_{CORE} = 1.35$  V) with CPU and peripherals running at up to 250 MHz
- VOS1 ( $V_{CORE} = 1.2$  V) with CPU and peripherals running at up to 200 MHz
- VOS2 ( $V_{CORE} = 1.1$  V) with CPU and peripherals running at up to 150 MHz
- VOS3 ( $V_{CORE} = 1.0$  V) with CPU and peripherals running at up to 100 MHz

## Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**  
Only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**  
This mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the  $V_{CORE}$  domain are stopped, the PLL, the CSI, the HSI, the HSI48, and the HSE crystal oscillators are disabled. The LSE or LSI is still running.  
The RTC can remain active (Stop mode with RTC, Stop mode without RTC).  
The system clock when exiting from Stop mode can be either HSI up to 64 MHz, or CSI (4 MHz), depending on software configuration.
- **Standby mode**  
This mode is used to achieve the lowest power consumption with BOR. The PLL, the HSI, the CSI, the HSI48, and the HSE crystal oscillators are also switched off.  
The RTC can remain active (Standby mode with RTC, Standby mode without RTC).  
The BOR always remains active.  
The I/Os state during Standby mode can be retained.  
After entering Standby mode, SRAMs and register contents are lost, except for registers and backup SRAM in the Backup domain and Standby circuitry.  
The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a WKUP pin event (configurable rising or falling edge), an RTC event (alarm, periodic wake-up, timestamp), or a tamper detection occurs. The tamper detection can be due to external pins or to an internal failure detection.  
The system clock after wake-up is HSI at 32 MHz.

### 3.10.3 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled).

### 3.10.4 VBAT operation

The VBAT pin allows the device VBAT domain to be powered from an external battery or by an external super-capacitor.

The VBAT pin supplies the RTC with LSE, anti-tamper detection (TAMP), backup registers, and 4-Kbyte backup SRAM. Eight anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when  $V_{DD}$  is not present. An internal VBAT battery charging circuit is embedded and can be activated when  $V_{DD}$  is present.

*Note:* When the microcontroller is supplied from  $V_{BAT}$ , neither external interrupts nor RTC alarm/events exit it from the VBAT operation.

### 3.10.5 PWR TrustZone security

When the TrustZone security is activated by the TZEN option bit, the PWR is switched in TrustZone security mode.

The PWR TrustZone security secures the following configuration:

- Low-power mode
- Wake-up (WKUP) pins
- Voltage detection and monitoring
- VBAT mode

Some of the PWR configuration bits security are defined by the security of other peripherals:

- The voltage scaling (VOS) configuration is secure when the system clock selection is secure in RCC.
- The I/O pull-up/pull-down in Standby mode configuration is secure when the corresponding GPIO is secure.
- The backup domain write protection is secure when the RTC is secure.

## 3.11 Peripheral interconnect matrix

Several peripherals have direct connections between them, for autonomous communication, and to support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run and Sleep modes.

## 3.12 Reset and clock controller (RCC)

The clock controller distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Clock security system:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 50 MHz high-speed external crystal or ceramic resonator (HSE), can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 64 MHz high-speed internal RC oscillator (HSI), trimmable by software, can supply a PLL.
  - 4 MHz low-power internal oscillator (CSI), trimmable by software, can supply a PLL.
  - System PLL, which can be fed by HSE, HSI, or CSI, with a maximum frequency at 250 MHz.

- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48), can be used to drive the USB.
- **UCPD kernel clock,** derived from HSI clock. The HSI RC oscillator must be enabled prior to the UCPD kernel clock use.
- **Auxiliary clock source:** two ultra-low power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
- **Peripheral clock sources:** several peripherals have their own independent clock, whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, USB, SDMMC, RNG, FDCAN1, OCTOSPI, and the two SAI.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 32 MHz clock (HSI/2). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock automatically switches to HSI and a software interrupt is generated if enabled. LSE failure can also be detected and generates an interrupt.
- Clock-out capability:
  - **MCO (microcontroller clock output):** outputs one of the internal clocks for external use by the application.
  - **LSCO (low-speed clock output):** outputs LSI or LSE in all low-power modes (except VBAT mode).

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 250 MHz.

### 3.12.1 RCC TrustZone security

When the TrustZone security is activated by the TZEN option bit, the RCC is switched in TrustZone security mode.

The RCC TrustZone security secures some RCC system configuration and peripheral configuration clock from being read or modified by nonsecure accesses: when a peripheral is secure, the related peripheral clock, reset, clock source selection and clock enable during low-power modes control bits are secure.

A peripheral is in secure state:

- when its corresponding SEC security bit is set in the TZSC (TrustZone security controller), for securable peripherals.
- when a security feature of this peripheral is enabled through its dedicated bits, for TrustZone-aware peripherals.

## 3.13 Clock recovery system (CRS)

The devices embed a special block that allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. The trimming is based on the external synchronization signal, derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS\_SYNC pin, or generated

by user software. For faster lock-in during startup, automatic and manual trimming actions can be combined.

### 3.14 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

If needed, the I/Os alternate function configuration can be locked following a specific sequence, to avoid spurious writing to the I/Os registers.

Ten I/Os (PD6, PD7, PG9:14, PB8, PB9) can be independently supplied by a dedicated  $V_{DDIO}$  supply.

#### 3.14.1 GPIOs TrustZone security

Each I/O pin of GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a nonsecure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

### 3.15 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, GPDMA1, GPDMA2, SDMMC1, SDMMC2, Ethernet) and the slaves (flash memory, FMC, OCTOSPI, SRAMs, AHB and APB) peripherals. It ensures seamless and efficient operation, even when several high-speed peripherals work simultaneously.

### 3.16 General purpose direct memory access controller (GPDMA)

The GPDMA controller is a bus master and system peripheral. It used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU. The GPDMA main features are:

- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Sleep mode
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)

- Per channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension
- Per channel interrupt generation, with separately programmed interrupt enable per event
- Eight concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intra-channel and inter-channel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - 12 channels with linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Four channels with 2D source and destination addressing: programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level)
  - Support for scatter-gather (multi-buffer transfers), data interleaving and de-interleaving via 2D addressing
  - Programmable DMA request and trigger selection
  - Programmable DMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags
- TrustZone support:
  - Support for secure and nonsecure DMA transfers, independently at a first channel level, and independently at a source/destination and link sub-levels
  - Secure and nonsecure interrupts reporting, resulting from any of the respectively secure and nonsecure channels
  - TrustZone-aware AHB slave port, protecting any DMA secure resource (register, register field) from a nonsecure access
- Privileged/unprivileged support:
  - Support for privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port

## 3.17 Interrupts and events

### 3.17.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels and to handle up to 125 maskable interrupt channels plus the 16 interrupt lines of the Cortex-M33.

The NVIC benefits are the following:

- closely coupled NVIC giving low-latency interrupt processing
- interrupt entry vector table address passed directly to the core
- early processing of interrupts
- processing of late arriving higher priority interrupts
- support for tail chaining
- processor state automatically saved
- interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone support: NVIC registers banked across secure and nonsecure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

### 3.17.2 Extended interrupt/event controller (EXTI)

The extended interrupts and event controller (EXTI) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run modes. The EXTI also includes the EXTI multiplexer IO port selection.

The EXTI main features are the following:

- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt and event generation
  - Software trigger possibility
- TrustZone secure events
  - The access to control and configuration bits of secure input events can be made secure
- EXTI IO port selection

### 3.18 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and that can be stored at a given memory location.

### 3.19 CORDIC coprocessor (CORDIC)

The CORDIC coprocessor provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications. It speeds up the calculation of these functions compared to a software implementation, allowing a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

The CORDIC main features are:

- 24-bit CORDIC rotation engine
- Circular and hyperbolic modes
- Rotation and vectoring modes
- Functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm
- Programmable precision
- Low-latency AHB slave interface
- Results can be read as soon as ready without polling or interrupt
- DMA read and write channels
- Multiple register read/write by DMA

### 3.20 Filter math accelerator (FMAC)

The FMAC performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic that allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be done.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

The FMAC main features are:

- 16 x 16-bit multiplier
- 24 + 2-bit accumulator with addition and subtraction
- 16-bit input and output data

- 256 x 16-bit local memory
- Up to three areas can be defined in memory for data buffers (two input, one output), defined by programmable base address pointers and associated size registers
- Input and output buffers can be circular
- Filter functions: FIR, IIR (direct form 1)
- Vector functions: dot product, convolution, correlation
- AHB slave interface
- DMA read and write data channels

## 3.21 Flexible memory controller (FMC)

The FMC includes three memory controllers:

- NOR/PSRAM memory controller
- NAND memory controller
- SDRAM memory controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (four memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
  - Ferroelectric RAM (FRAM, FeRAM)
- Interface with synchronous DRAM (SDRAM/Mobile LPDDR SDRAM)
- 8-, 16- bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

### 3.21.1 LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel® 8080 and Motorola® 6800 modes, and is flexible enough to adapt to specific LCD interfaces.

This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

### 3.21.2 FMC TrustZone security

When the TrustZone security is enabled, the whole FMC banks are secure after reset. Nonsecure area can be configured using the TZSC MPCWMx controller.

- The FMC NOR/PSRAM bank:
  - Up to two nonsecure area can be configured through the TZSC MPCWM2 controller with a 64-Kbyte granularity
- The FMC NAND bank:

- Can be either configured as fully secure or fully nonsecure using the TZSC MPCWM3 controller

The FMC registers can be configured as secure through the TZSC controller.

## 3.22 Octo-SPI interface (OCTOSPI)

The OCTOSPI supports external memories such as serial PSRAMs, serial NAND/NOR flash memories, HyperRAMs™ and HyperFlash™ memories, with the following functional modes:

- Indirect mode: all the operations are performed using the OCTOSPI registers.
- Status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation.

The OCTOSPI supports the following protocols with associated frame formats:

- Standard frame format with the command, address, alternate byte, dummy cycles and data phase
- HyperBus™ frame format

The OCTOSPI offers the following features:

- Three functional modes: Indirect, Status-polling, and Memory-mapped
- Read and write support in Memory-mapped mode
- Supports for single, dual, quad and octal communication
- Dual-quad mode, where eight bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR (single-data rate) and DTR (double-transfer rate) support
- Data strobe support
- Fully programmable opcode
- Fully programmable frame format
- HyperBus support
- Integrated FIFO for reception and transmission
- 8-, 16-, and 32-bit data accesses allowed
- DMA channel for Indirect mode operations
- Interrupt generation on FIFO threshold, timeout, operation complete, and access error

### 3.22.1 OCTOSPI TrustZone security

When the TrustZone security is enabled, the whole OCTOSPI bank is secure after reset.

Up to two nonsecure area can be configured through the TZSC MPCWM1 controller with a granularity of 64 Kbytes.

The OCTOSPI registers can be configured as secure through the TZSC controller.

### 3.23 Delay block (DLYB)

The delay block (DLYB) is used to generate an output clock dephased from the input clock. The phase of the output clock must be programmed by the user application. The output clock is then used to clock the data received by another peripheral such as an SDMMC or Octo-SPI interface. The delay is voltage and temperature dependent, that may require the application to re-configure and recenter the output clock phase with the received data.

The delay block main features are:

- Input clock frequency ranging from 25 to 250 MHz
- Up to 12 oversampling phases

### 3.24 Analog-to-digital converters (ADC1 and ADC2)

The devices embed two successive approximation analog-to-digital converters.

**Table 5. ADC features**

| Mode/feature                   | ADC1                       | ADC2 |
|--------------------------------|----------------------------|------|
| Resolution                     | 12 bit                     |      |
| Maximum sampling speed         | 5 Msps (12-bit resolution) |      |
| Dual mode operation            | X                          |      |
| Hardware offset calibration    | X                          |      |
| Hardware linearity calibration | -                          |      |
| Single-end input               | X                          |      |
| Differential input             | X                          |      |
| Injected channel conversion    | X                          |      |
| Oversampling                   | Up to x256                 |      |
| Data register                  | 16 bits                    |      |
| Data register FIFO depth       | 3 stages                   |      |
| DMA support                    | X                          |      |
| Parallel data output to ADF    | -                          |      |
| Offset compensation            | X                          |      |
| Gain compensation              | -                          |      |
| Number of analog watchdogs     | 3                          |      |
| Option register                | -                          | X    |

#### 3.24.1 Analog temperature sensor

This sensor generates a voltage ( $V_{\text{SENSE}}$ ) that varies linearly with temperature. It is internally connected to an ADC input channel used to convert the output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset depends upon process variation, the uncalibrated internal temperature sensor is suitable for applications that detect only temperature changes.

To improve the measurement accuracy, each device is individually factory-calibrated by ST. The calibration data are stored in the system memory area, accessible in read-only mode.

### 3.24.2 Internal voltage reference ( $V_{\text{REFINT}}$ )

The internal voltage reference ( $V_{\text{REFINT}}$ ) provides a stable (bandgap) voltage output for the ADC. The  $V_{\text{REFINT}}$  is internally connected to ADC input channel.

The precise voltage of  $V_{\text{REFINT}}$  is individually measured for each part during manufacturing, and stored in the system memory area. It is accessible in read-only mode.

### 3.24.3 $V_{\text{BAT}}$ battery voltage monitoring

This embedded hardware enables the application to measure the  $V_{\text{BAT}}$  battery voltage using ADC or input channel. As the  $V_{\text{BAT}}$  voltage may be higher than the  $V_{\text{DDA}}$ , and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by four. As a consequence, the converted digital value is a quarter of the  $V_{\text{BAT}}$  voltage.

## 3.25 Digital temperature sensor (DTS)

The device embeds a sensor that converts the temperature into a square wave, whose frequency is proportional to the temperature. The PCLK or the LSE clock can be used as reference clock for the measurements. Use the formula given in the product reference manual to calculate the temperature according to the measured frequency stored in the DTS\_DR register.

## 3.26 Digital to analog converter (DAC)

The DAC module is a 12-bit voltage output digital-to-analog converter. The DAC can be configured in 8- or 12-bit mode, and can be used in conjunction with the DMA controller. In 12-bit mode, the data can be left- or right-aligned.

The DAC features two output channels, each with its own converter. In dual DAC channel mode, conversions can be done independently or simultaneously when both channels are grouped together for synchronous update operations. An input reference pin, VREF+ (shared with others analog peripherals), is available for better resolution. An internal reference can also be set on the same input.

The DAC\_OUTx pin can be used as general purpose input/output (GPIO) when the DAC output is disconnected from output pad and connected to on chip peripheral. The DAC output buffer can be optionally enabled to allow a high drive output current. An individual calibration can be applied on each DAC output channel. The DAC output channels support a low power mode, the Sample and hold mode.

The digital interface supports the following features:

- One DAC interface, maximum two output channels
- Left or right data alignment in 12-bit mode

- Synchronized update capability
- Noise-wave and triangular-wave generation
- Sawtooth wave generation
- Dual DAC channel for independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- Double data DMA capability to reduce the bus activity
- External triggers for conversion
- DAC output channel buffered/unbuffered modes
- Buffer offset calibration
- Each DAC output can be disconnected from the DAC\_OUTx output pin
- DAC output connection to on chip peripherals
- Sample and Hold mode for low-power operation in Stop mode. The DAC voltage can be changed autonomously with the DMA while the device is in Stop mode.
- Voltage reference input

### 3.27 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer that can be used as reference for ADCs and DACs, and also as reference for external components through the VREF+ pin.

The internal voltage reference buffer supports three voltages: 1.8, 2.048, and 2.5 V.

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDPA on some packages. In these packages the internal voltage reference buffer is not available.

### 3.28 Digital camera interface (DCMI)

The digital camera is a synchronous parallel interface able to receive a high-speed data flow from an external 8-, 10-, 12- or 14-bit CMOS camera module. It supports different data formats: YCbCr4:2:2/RGB565 progressive video and compressed data (JPEG). It can be used with black and white cameras, X24 and X5 cameras (it is assumed that all preprocessing such as resizing is performed in the camera module).

Main features:

- 8-, 10-, 12-, or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature
- Support of the following data formats:
  - 8/10/12/14-bit progressive video: monochrome or raw Bayer
  - YCbCr 4:2:2 progressive video
  - RGB 565 progressive video
  - Compressed data: JPEG

### 3.29 Parallel synchronous slave interface (PSSI)

The PSSI peripheral and the DCMI (digital camera interface) use the same circuitry. As a result, these two peripherals cannot be used at the same time: when using the PSSI, the DCMI registers cannot be accessed, and vice versa. In addition, the PSSI and the DCMI share the same alternate functions and the same interrupt vector.

The PSSI is a generic synchronous 8-/16-bit parallel data input/output slave interface. It enables the transmitter to send a data valid signal that indicates when the data is valid, and the receiver to output a flow control signal that indicates when it is ready to sample the data.

The PSSI peripheral main features are the following:

- Slave mode operation
- 8-bit or 16-bit parallel data input or output
- 4-word (16-byte) FIFO
- Data enable (PSSI\_DE) alternate function input and ready (PSSI\_RDY) alternate function output

When selected, these inputs can either enable the transmitter to indicate when the data is valid, or allow the receiver to indicate when it is ready to sample the data, or both.

### 3.30 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG).

The true random generator:

- delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage
- can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)
- produces four 32-bit random samples every 412 AHB clock cycles if  $f_{\text{AHB}} < 77 \text{ MHz}$  (256 RNG clock cycles otherwise)
- embeds start-up and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)
- has an AMBA AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored)

### 3.31 HASH hardware accelerator (HASH)

The HASH is a fully compliant implementation of the secure hash (SHA-1, SHA-224, SHA-256, SHA-512) and the HMAC (keyed-hash message authentication code) algorithms. HMAC is suitable for applications requiring message authentication.

The HASH computes FIPS (Federal information processing standards) approved digests of length of 160, 224, 256, 512 bits, for messages of up to  $(2^{64} - 1)$ .

The HASH main features are:

- Suitable for data authentication applications, compliant with:
  - FIPS PUB 180-4, *Secure Hash Standard* (SHA-1 and SHA-2 family)
  - FIPS PUB 186-4, *Digital Signature Standard* (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, *HMAC: Keyed-Hashing for Message Authentication* and Federal Information Processing Standards Publication FIPS PUB 198-1, *The Keyed-Hash Message Authentication Code* (HMAC)
- Fast computation of SHA-1, SHA-224, SHA-256, SHA-512
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
  - Word swapping supported: bits, bytes, half-words and 32-bit words
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits ( $16 \times 32$  bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size
- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- $8 \times 32$ -bit words (H0 to H7) for output message digest
- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of 4 supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Re-loadable digest registers
  - Hashing computation suspend/resume mechanism, including using DMA

### 3.32 Public key accelerator (PKA)

The PKA can verify ECDSA signatures, with all needed computation performed within the accelerator. The application CPU is needed only to manage the inputs and the outputs of the operation.

The PKA main features are:

- ECDSA signature verification
- Capability to handle operands up to 640 bits
- AMBA AHB slave peripheral, accessible through 32-bit word single accesses only (otherwise an AHB bus error is generated, and write accesses are ignored)

### 3.33 Timers and watchdogs

The devices include two advanced control timers, up to seven general-purpose timers, two basic timers, six low-power timers, two watchdog timers, and two SysTick timers.

[Table 6](#) compares the features of the advanced control, general-purpose, and basic timers.

**Table 6. Timer features**

| Type             | Timer                      | Counter resolution | Counter type      | Prescaler factor                | DMA request generation | Capture/compare channels | Complementary outputs |
|------------------|----------------------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|-----------------------|
| Advanced control | TIM1, TIM8                 | 16 bits            | Up, down, up/down | Any integer between 1 and 65536 | Yes                    | 4                        | 4                     |
| General purpose  | TIM2, TIM5                 | 32 bits            |                   |                                 |                        | 4                        | No                    |
|                  | TIM3, TIM4                 | 16 bits            |                   |                                 |                        | 4                        | No                    |
| General purpose  | TIM12, TIM15               | 16 bits            | Up                |                                 |                        | 2                        | 1                     |
|                  | TIM13, TIM14, TIM16, TIM17 |                    |                   |                                 |                        | 1                        | 1                     |
| Basic            | TIM6, TIM7                 | 16 bits            | Up                |                                 |                        | 0                        | No                    |

#### 3.33.1 Advanced-control timers (TIM1, TIM8)

These timers can be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 - 100 %)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the *Timer Link* feature for synchronization or event chaining.

#### 3.33.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

The devices embed up to seven synchronizable general-purpose timers (see [Table 6](#)), each of them can be used to generate PWM outputs, or act as a simple time base.

- TIM2 and TIM5  
Full-featured general-purpose timers with 32-bit auto-reload up/down counter and 32-bit prescaler.

These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counters can be frozen in Debug mode. All have independent DMA request generation and support quadrature encoders.

- TIM3 and TIM4

Full-featured general-purpose timers, with 16-bit auto-reload up/down counter and 16-bit prescaler.

These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output.

They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.

The counters can be frozen in Debug mode. All have independent DMA request generation and support quadrature encoders.

- TIM12, TIM13, TIM14, TIM15, TIM16, and TIM17

General-purpose timers with mid-range features, with 16-bit auto-reload up counter and 16-bit prescaler.

- TIM12 and TIM15 have two channels and one complementary channel
- TIM13, TIM14, TIM16, and TIM17 have one channel and one complementary channel

All channels can be used for input capture/output compare, PWM, or one-pulse mode output.

These timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in Debug mode.

### 3.33.3 Basic timers (TIM6, TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebase.

### 3.33.4 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5, LPTIM6)

The devices embed six low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wake up the system from Stop mode.

The low-power timers support the following features:

- 16-bit up counter with 16-bit autoreload register
- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by *Pulse Counter* application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode

- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode (except for LPTIM4)
- Repetition counter
- Up to two independent channels (except for LPTIM4) for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

### 3.33.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in Debug mode.

### 3.33.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

### 3.33.7 SysTick timer

The Cortex-M33 with TrustZone embeds two SysTick timers.

When TrustZone is activated, two SysTick timer are available:

- SysTick, secure instance
- SysTick, nonsecure instance

When TrustZone is disabled, only one SysTick timer is available. This timer (secure or nonsecure) is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.34 Real-time clock (RTC), tamper and backup registers

### 3.34.1 Real-time clock (RTC)

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in BCD (binary-coded decimal) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or nonsecure configuration
  - Alarm A, alarm B, wake-up timer and timestamp individual privileged protection

The RTC is supplied through a switch that takes power either from the  $V_{DD}$  supply when present or from the VBAT pin.

The RTC clock sources can be one of the following:

- 32.768 kHz external crystal (LSE)
- external resonator or oscillator (LSE)
- internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- high-speed external clock (HSE), divided by a prescaler in the RCC.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

### 3.34.2 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 32-bit backup registers are retained in all low-power modes and in VBAT mode. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with eight tamper pins and nine internal tampers. The external tamper pins can be configured for edge detection, or level detection with or without filtering, or active

tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, backup SRAM, SRAM2, caches and cryptographic peripherals.
- 32 32-bit backup registers:
  - The backup registers (TAMP\_BKPxR) are implemented in the Backup domain that remains powered-on by  $V_{BAT}$  when the  $V_{DD}$  power is switched off.
- Up to 8 tamper pins for 8 external tamper detection events:
  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks
  - Flexible active tamper I/O management: from 4 meshes (each input associated to its own exclusive output) to 7 meshes (single output shared for up to 7 tamper inputs)
  - Passive tampers: ultra-low power edge or level detection with internal pull-up hardware management
  - Configurable digital filter

*Note:* As input, only PC13, PI8, PA0, PA1, and PA2 are functional in Standby and VBAT modes. As output, only PC13 and PA1, and PI8 are functional in Standby and VBAT modes.

- Internal tamper events to protect against transient or environmental perturbation attacks
- Each tamper can be configured in two modes:
  - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate an RTC time stamp event.
- TrustZone support:
  - Tamper secure or nonsecure configuration.
  - Backup registers configuration in three configurable-size areas:
    - 1 read/write secure area
    - 1 write secure/read nonsecure area
    - 1 read/write nonsecure area
  - Secret key, stored in backup registers, protected against read and write access
- Tamper configuration and backup registers privilege protection
- Monotonic counter

### 3.35 Inter-integrated circuit interface (I2C)

The devices embed four I2Cs. Refer to [Table 7](#) for the implemented features.

The I<sup>2</sup>C bus interface handles communications between the microcontroller and the serial I<sup>2</sup>C bus. It controls all I<sup>2</sup>C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I<sup>2</sup>C-bus specification and user manual rev. 5 compatibility:

- Target and controller modes, multicontroller capability
- Standard-mode (Sm), with a bit rate up to 100 Kbit/s
- Fast-mode (Fm), with a bit rate up to 400 Kbit/s
- Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
- 7- and 10-bit addressing modes, multiple 7-bit target addresses
- Programmable setup and hold times
- Optional clock stretching
- System management bus (SMBus) specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources makes the I2C communication speed independent from the PCLK reprogramming
- Wake-up from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 7. I2C implementation

| Feature <sup>(1)</sup>                                       | I2C1 | I2C2 | I2C3 | I2C4 |
|--------------------------------------------------------------|------|------|------|------|
| Standard-mode (up to 100 Kbit/s)                             | X    | X    | X    | X    |
| Fast-mode (up to 400 Kbit/s)                                 | X    | X    | X    | X    |
| Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s) | X    | X    | X    | X    |
| Programmable analog and digital noise filters                | X    | X    | X    | X    |
| SMBus/PMBus hardware support                                 | X    | X    | X    | X    |
| Independent clock                                            | X    | X    | X    | X    |
| Wake-up capability                                           | X    | X    | X    | X    |

1. X: supported

### 3.36 Improved inter-integrated circuit (I3C)

The I3C interface handles communication between the MCU and others, like sensors and host processor(s), all connected on an I3C bus.

The peripheral implements the required features of the MIPI I3C specification v1.1. It can control I3C bus-specific sequencing, protocol, arbitration and timing, and can act as controller (formerly known as master) or as target (formerly known as slave). When acting as controller, the peripheral improves the features of the I2C interface, preserving some backward compatibility. It allows an I2C target to operate on an I3C bus in legacy I2C fast-mode (Fm) or legacy I2C fast-mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA to off-load the CPU.

Table 8. I3C peripheral controller/target features versus MIPI v1.1

| Feature                                  | MIPI v1.1 | When controller | When target | Comments                                                                                                                                     |
|------------------------------------------|-----------|-----------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| I3C SDR message                          | X         | X               | X           | -                                                                                                                                            |
| Legacy I <sup>2</sup> C message (Fm/Fm+) | X         | X               | -           | Mandatory when controller, and the I3C bus is mixed with (external) legacy I <sup>2</sup> C target(s).<br>Optional in MIPI v1.1 when target. |
| HDR DDR message                          | X         | -               | -           | Optional in MIPI v1.1                                                                                                                        |
| HDR-TSL/TSP, HDR-BT                      | X         | -               | -           |                                                                                                                                              |
| Dynamic address assignment               | X         | X               | X           | -                                                                                                                                            |
| Static address                           | X         | X               | -           | No (intended) support of I3C peripheral as a target on an I <sup>2</sup> C bus                                                               |
| Grouped addressing                       | X         | X               | -           | Optional in MIPI v1.1                                                                                                                        |
| CCCs                                     | X         | X               | X           | Mandatory and some optional CCCs supported                                                                                                   |
| Error detection and recovery             | X         | X               | X           | -                                                                                                                                            |
| In-band interrupt (with MDB)             | X         | X               | X           | -                                                                                                                                            |
| Secondary controller                     | X         | X               | X           | -                                                                                                                                            |
| Hot-join mechanism                       | X         | X               | X           | -                                                                                                                                            |
| Target reset                             | X         | X               | X           | -                                                                                                                                            |
| Synchronous timing control               | X         | X               | -           | Optional in MIPI v1.1                                                                                                                        |
| Asynchronous timing control 0            | X         | X               | -           |                                                                                                                                              |
| Asynchronous timing control 1, 2, 3      | X         | -               | -           | Optional in MIPI v1.1                                                                                                                        |
| Device to device tunneling               | X         | X               | -           | Optional in MIPI v1.1                                                                                                                        |
| Multi-lane data transfer                 | X         |                 | -           | Optional in MIPI v1.1                                                                                                                        |
| Monitoring device early termination      | X         | -               | -           | Optional in MIPI v1.1                                                                                                                        |

### 3.37 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices embed six universal synchronous receiver transmitters (USART1/USART2/USART3/USART6/USART10/USART11), six universal asynchronous receiver transmitters (UART4/UART5/UART7/UART8/UART9/UART12), one low-power universal asynchronous receiver transmitter (LPUART1).

Table 9. USART, UART and LPUART features

| Mode/feature <sup>(1)</sup>        | USART1/2/3/6 /10/11 | UART4/5/7/8/9/12 | LPUART1 |
|------------------------------------|---------------------|------------------|---------|
| Hardware flow control for modem    | X                   | X                | X       |
| Continuous communication using DMA | X                   | X                | X       |

Table 9. USART, UART and LPUART features (continued)

| Mode/feature <sup>(1)</sup>                  | USART1/2/3/6/10/11 | UART4/5/7/8/9/12 | LPUART1          |
|----------------------------------------------|--------------------|------------------|------------------|
| Multiprocessor communication                 | X                  | X                | X                |
| Synchronous mode (master/slave)              | X                  | -                | -                |
| Smartcard mode                               | X                  | -                | -                |
| Single-wire half-duplex communication        | X                  | X                | X                |
| IrDA SIR ENDEC block                         | X                  | X                | -                |
| LIN mode                                     | X                  | X                | -                |
| Dual-clock domain and wake-up from Stop mode | X <sup>(2)</sup>   | X <sup>(2)</sup> | X <sup>(2)</sup> |
| Receiver timeout interrupt                   | X                  | X                | -                |
| Modbus communication                         | X                  | X                | -                |
| Auto-baud rate detection                     | X                  | X                | -                |
| Driver enable                                | X                  | X                | X                |
| USART data length                            | 7, 8, and 9 bits   |                  |                  |
| Tx/Rx FIFO                                   | X                  | X                | X                |
| Tx/Rx FIFO size                              | 8 bytes            |                  |                  |

1. X = supported.

2. Wake-up supported from Stop mode.

### 3.37.1 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The USART offers a flexible means to perform full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communication (up to 20 Mbauds) is possible by using the DMA (direct memory access) for multibuffer configuration.

The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or by 8, to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data  
Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK

- Auto baud rate detection
- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous Master/Slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from stop capability
- LIN master synchronous break send capability and LIN slave break detection capability
  - 13-bit break generation and 10/11-bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16 bit duration for Normal mode
- Smartcard mode
  - Supports the T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

### 3.37.2 Low-power universal asynchronous receiver transmitter (LPUART)

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher-speed clock can be used to reach higher baud-rates.

The LPUART interface can be served by the DMA controller.

The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 to 9600 bauds using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data  
Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop capability

### 3.38 Serial peripheral interface (SPI) / inter-integrated sound interface (I2S)

The devices embed six serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave, and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to set up communication with concrete slave and to assure it handles the data flow properly. The Motorola data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 32-bit data size selection or fixed to 8-bit and 16-bit only
- Multi master or multi slave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency divided by 2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Wake-up from Stop capability
- Optional status pin RDY signaling the slave device ready to handle the data flow.

Three standard I2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in Master or Slave mode, in full-duplex communication modes, and can be configured to operate with configurable resolution as input or output channel.

I2S main features:

- Full duplex communication
- Simplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler
- Data length may be 16, 24 or 32 bits
- Channel length can be 16 or 32 in master, any value in slave
- Programmable clock polarity
- Error flags signaling for improved reliability: Underrun, Overrun, and Frame Error
- Embedded Rx and TxFIFOs
- Supported I2S protocols:
  - I2S Philips standard
  - MSB-Justified standard (left-justified)
  - LSB-Justified standard (right-justified)
  - PCM standard (with short and long frame synchronization)
- Data ordering programmable (LSb or MSb first)
- DMA capability for transmission and reception
- Master clock can be output to drive an external audio component. The ratio is fixed at 256 x FWS (where FWS is the audio sampling frequency)

**Table 10. SPI features**

| Feature                    | SPI1, SPI2, SPI3<br>(full feature set instances)        | SPI4, SPI5, SPI6<br>(full feature set instances)        |
|----------------------------|---------------------------------------------------------|---------------------------------------------------------|
| Data size                  | Configurable from 4- to 32-bit                          | Configurable from 4- to 16-bit                          |
| CRC computation            | CRC polynomial length<br>configurable from 5- to 33-bit | CRC polynomial length<br>configurable from 5- to 17-bit |
| Size of FIFOs              | 16x 8-bit                                               | 8x 8-bit                                                |
| Number of transferred data | Up to 65535                                             |                                                         |
| I2S feature                | Yes                                                     | No                                                      |

### 3.39 Serial audio interface (SAI)

The devices embed two SAIs. Refer to [Table 11](#) for the features implementation. The SAI bus interface handles communications between the MCU and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks that can be transmitters or receivers with their respective FIFO
- 8-word integrated FIFOs for each audio sub-block
- Synchronous or Asynchronous mode between the audio sub-blocks

- Master or slave configuration independent for both audio sub-blocks
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit
- Peripheral with large configurability and flexibility, allowing to target the following audio protocols: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF out
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame
- Number of bits by frame may be configurable
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/mono audio frame capability
- Communication clock strobing edge configurable (SCK)
- Error flags with associated interrupts if enabled respectively
  - Overrun and underrun detection
  - Anticipated frame synchronization signal detection in Slave mode
  - Late frame synchronization signal detection in Slave mode
  - Codec not ready for the AC'97 mode in reception
- Interruption sources when enabled:
  - Errors
  - FIFO requests
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

**Table 11. SAI implementation**

| Feature <sup>(1)</sup>                                 | SAI1        | SAI2        |
|--------------------------------------------------------|-------------|-------------|
| I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97         | X           | X           |
| Mute mode                                              | X           | X           |
| Stereo/mono audio frame capability.                    | X           | X           |
| 16 slots                                               | X           | X           |
| Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit | X           | X           |
| FIFO size                                              | X (8 words) | X (8 words) |
| SPDIF                                                  | X           | X           |
| PDM                                                    | X           | -           |

1. X: supported

### 3.40 Secure digital input/output and MultiMediaCards interface (SDMMC)

The SD/SDIO, embedded MultiMediaCard (eMMC™) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards, and eMMC devices.

The MultiMediaCard system specifications are available through the MultiMediaCard association website at [www.mmca.org](http://www.mmca.org), published by the MMCA technical committee.

SD memory card and SD I/O card system specifications are available through the SD card association website at [www.sdcard.org](http://www.sdcard.org).

The SDMMC features include the following:

- Compliance with Embedded MultiMediaCard System Specification Version 5.1  
Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit (HS200 SDMMC\_CLK speed limited to maximum allowed I/O speed, HS400 is not supported).
- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with SD memory card specifications version 6.0  
(SDR104 SDMMC\_CLK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Full compliance with SDIO card specification version 4.0  
Card support for two different databus modes: 1-bit (default) and 4-bit (SDR104 SDMMC\_CLK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Data transfer up to 208 Mbyte/s for the 8-bit mode, depending maximum allowed I/O speed.
- Data and command output enable signals to control external bidirectional drivers
- IDMA linked list support

The MultiMediaCard/SD bus connects cards to the host.

The current version of the SDMMC supports only one SD/SDIO/eMMC card at any one time and a stack of eMMC.

**Table 12. SDMMC features**

| Mode/feature <sup>(1)</sup>    | SDMMC1 | SDMMC2 |
|--------------------------------|--------|--------|
| Variable delay (SDR104, HS200) | X      | X      |
| SDMMC_CKIN                     | X      | X      |
| SDMMC_CDIN, SDMMC_D0DIR        | X      | -      |
| SDMMC_D123DIR                  | X      | -      |

1. X = supported.

When SDMMC peripherals are used simultaneously:

- Only one can be used in eMMC with 8-bit bus width.
- Usage of SDMMC1 SDIO voltage switch use is mutually exclusive with SDMMC2 eMMC with 8-bit bus width.
- If SDMMC1 must support SDIO UHS-I modes (SDR12, SDR25, SDR50, SDR104, or DDR50), SDMMC2 cannot support eMMC with 8-bit bus width.

- If SDMMC2 must support eMMC with 8-bit bus width, SDMMC1 can only support SDIO Default mode and High-speed mode.

### 3.41 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN module, a shared message RAM memory and a configuration block.

The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 0.8-Kbyte message RAM implements filters, receives FIFOs, transmits event FIFOs and transmits FIFOs.

The FDCAN main features are:

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015, -4
- CAN FD with maximum 64 data bytes supported
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- Two receive FIFOs of three payloads each (up to 64 bytes per payload)
- Separate signaling on reception of high priority messages
- Configurable transmit FIFO / queue of three payload (up to 64 bytes per payload)
- Configurable transmit Event FIFO
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

### 3.42 USB full speed (USB)

USB main features:

- USB specification version 2.0 full-speed compliant
- Host and device functions
- 2048 bytes of dedicated SRAM data buffer memory with 32-bit access
- USB clock recovery
- Configurable number of endpoints from 1 to 8
- Cyclic redundancy check (CRC) generation/checking, non-return-to-zero inverted (NRZI) encoding/decoding and bit-stuffing
- Isochronous transfers support
- Double-buffered bulk/isochronous endpoint support
- USB suspend/resume operations
- Frame-locked clock pulse generation
- USB 2.0 Link power management support
- Battery charging specification revision 1.2 support in device

### 3.43 USB Type-C/USB Power Delivery controller (UCPD)

The devices embed one controller (UCPD) compliant with USB Type-C Cable and Connector Specification release 2.0 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB power delivery requirements, featuring:

- USB Type-C pull-up ( $R_p$ , all values) and pull-down ( $R_d$ ) resistors
- “Dead battery” support
- USB power delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles:

- USB Type-C level detection with debounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB power delivery payload, generating interrupts (DMA compatible)
- USB power delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB power delivery messages and FRS signaling.

### 3.44 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for Ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Support of 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal 2-Kbyte FIFOs to buffer transmit and receive frames

- Support of hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Trigger of interrupt when system time becomes greater than target time

### 3.45 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed an HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake up the MCU from Stop mode on data reception.

### 3.46 Development support

#### 3.46.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

#### 3.46.2 Embedded Trace Macrocell

The Arm Embedded Trace Macrocell (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

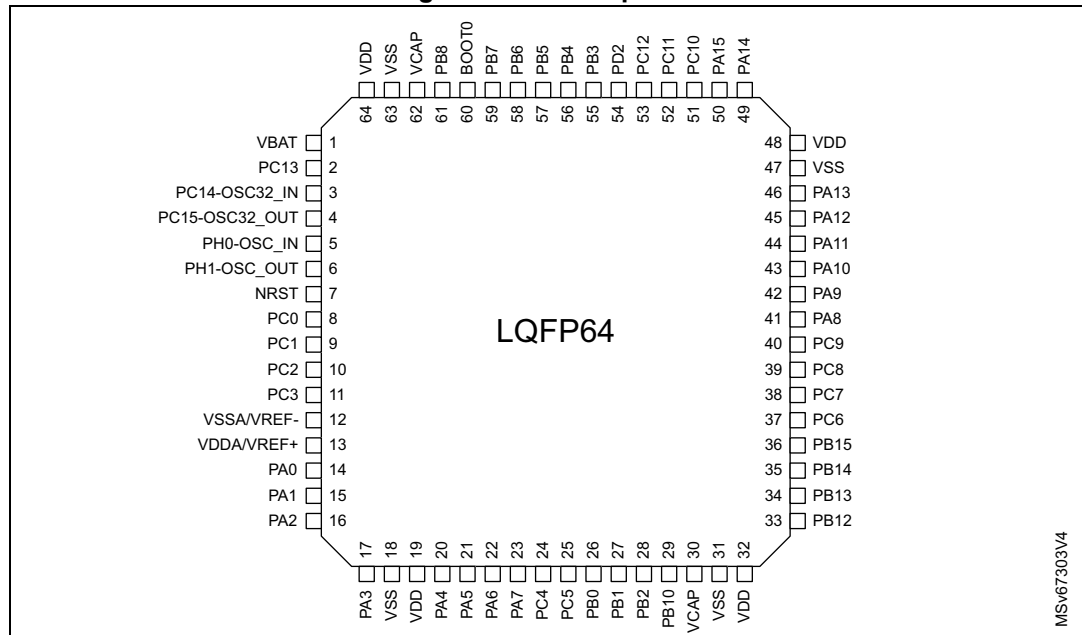
Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The ETM operates with third party debugger software tools.

## 4 Pinout, pin description, and alternate functions

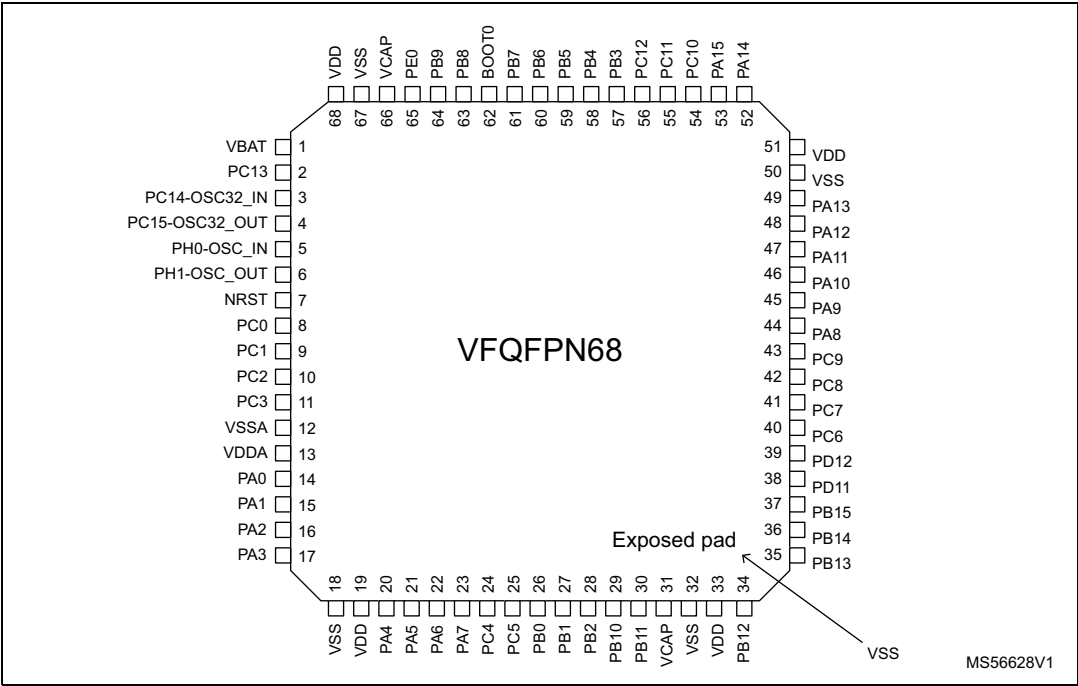
### 4.1 Pinout/ballout schematics

Figure 5. LQFP64 pinout



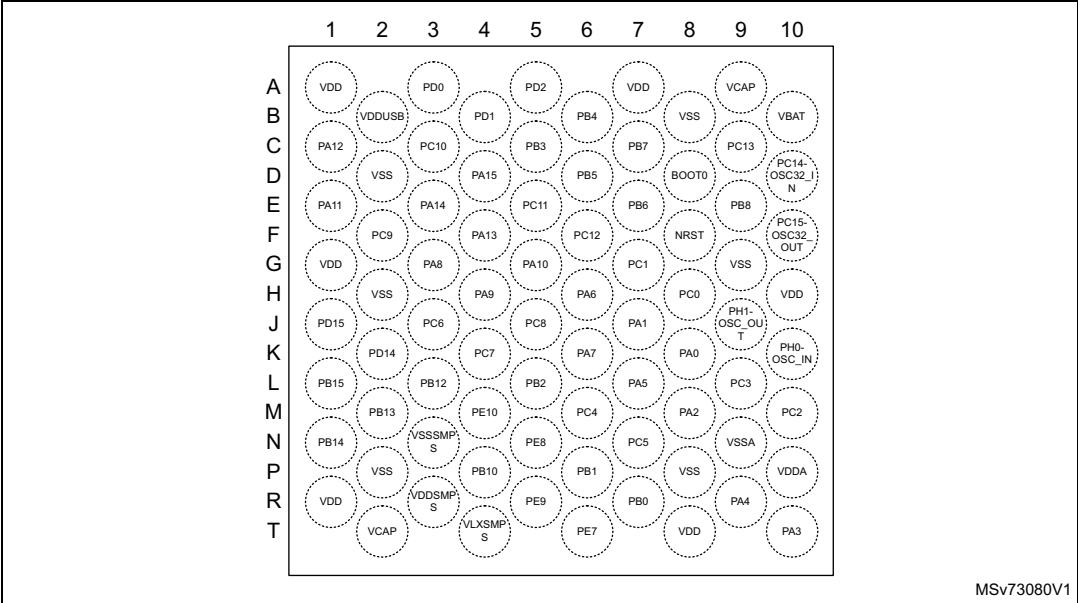
1. The above figure shows the package top view.

Figure 6. VFQFPN68 pinout



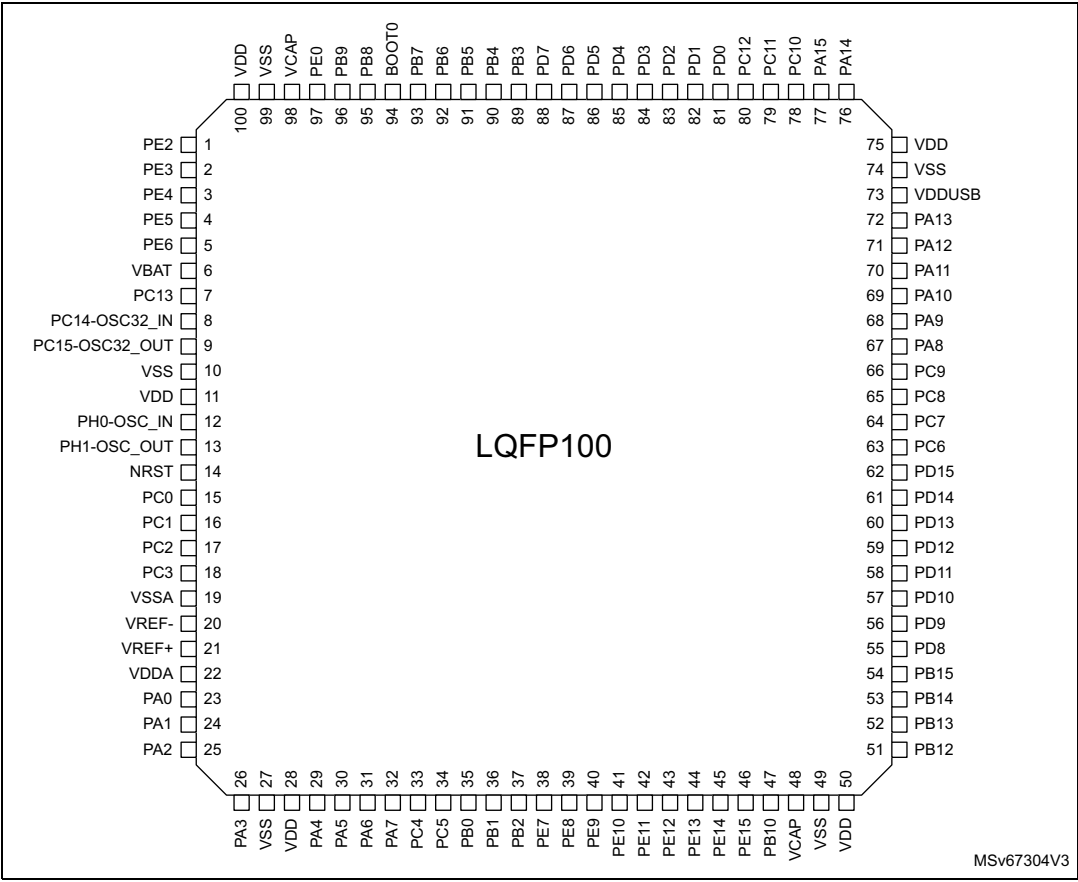
1. The above figure shows the package top view.
2. VSS pads are connected to the exposed pad.

Figure 7. WLCSP80 SMPS ballout



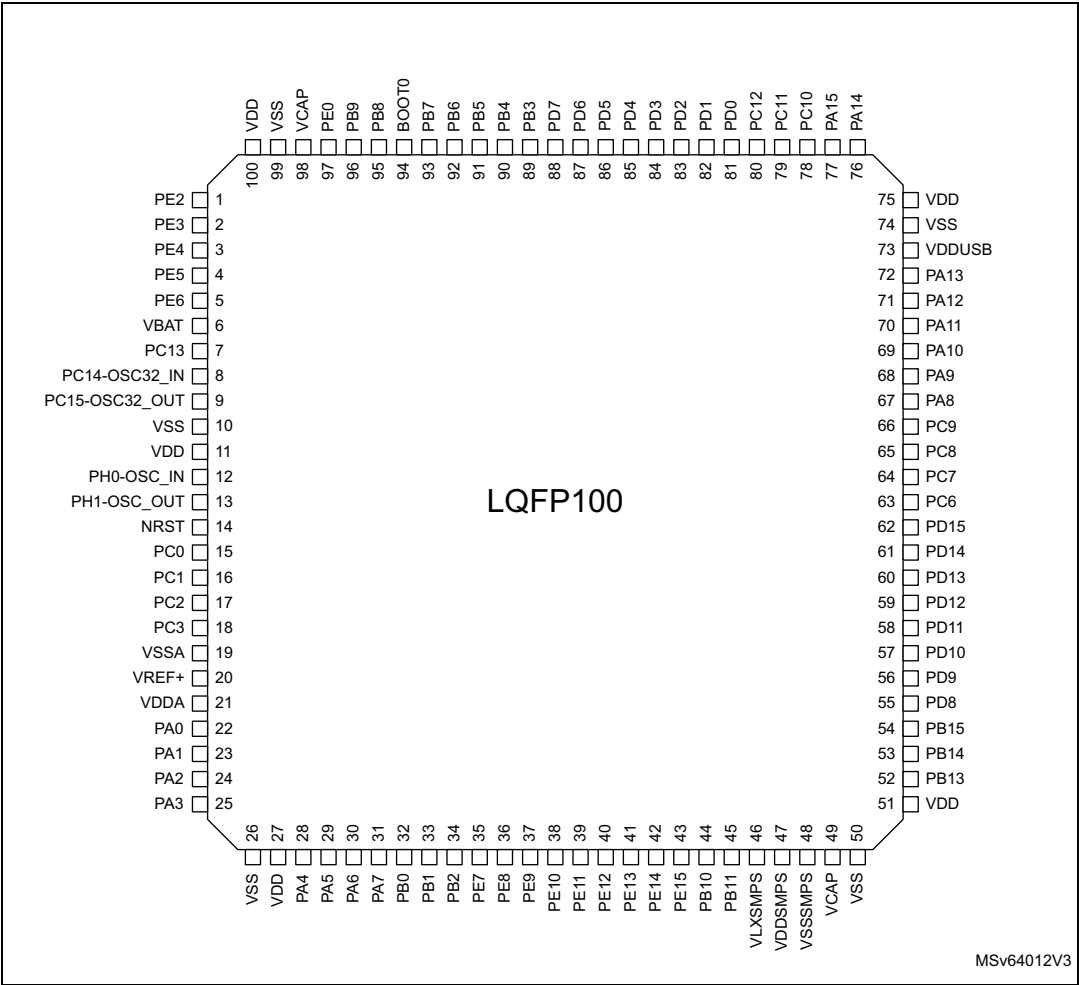
1. The above figure shows the package top view.

Figure 8. LQFP100 pinout



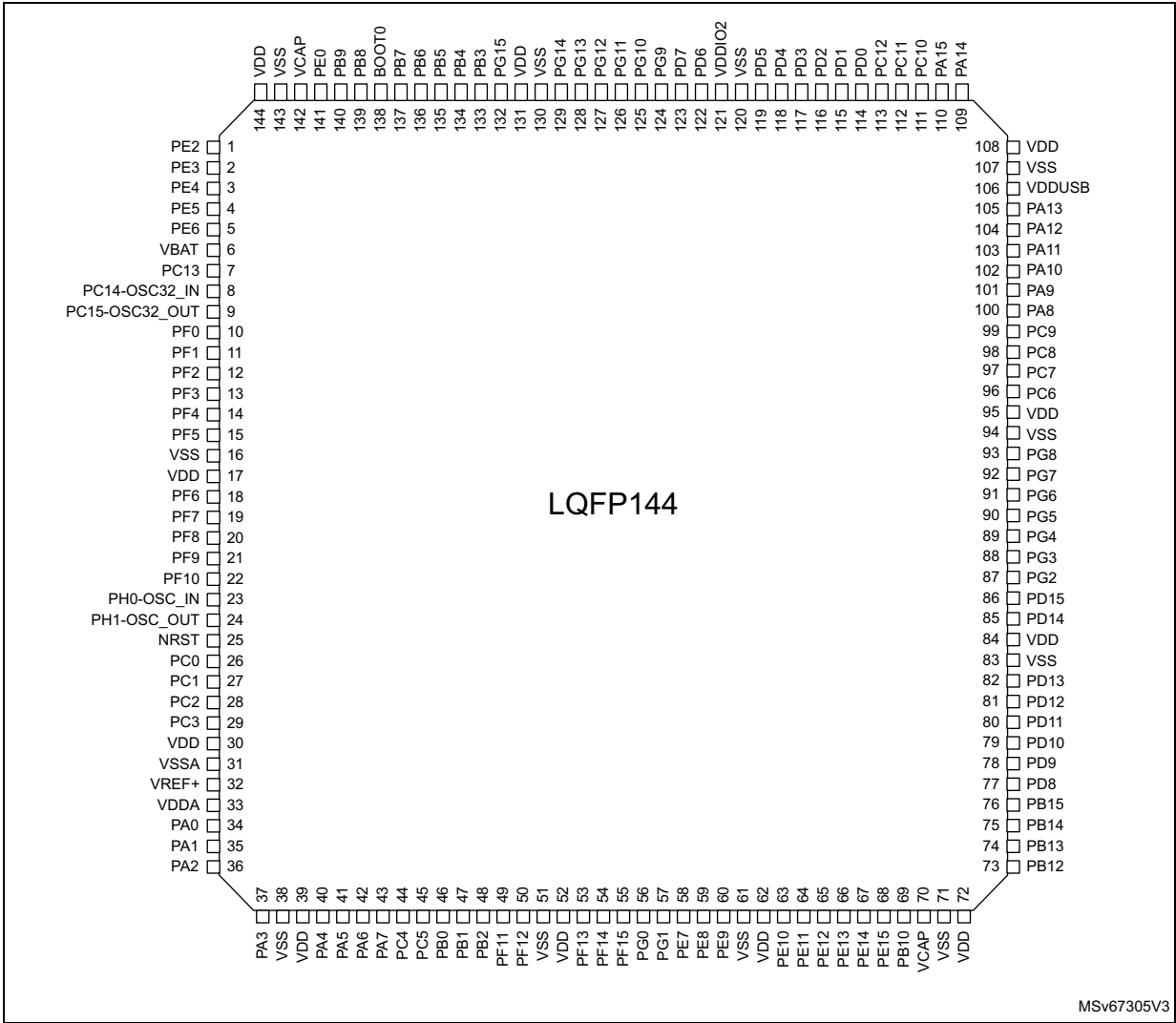
1. The above figure shows the package top view.

Figure 9. LQFP100 SMPS pinout



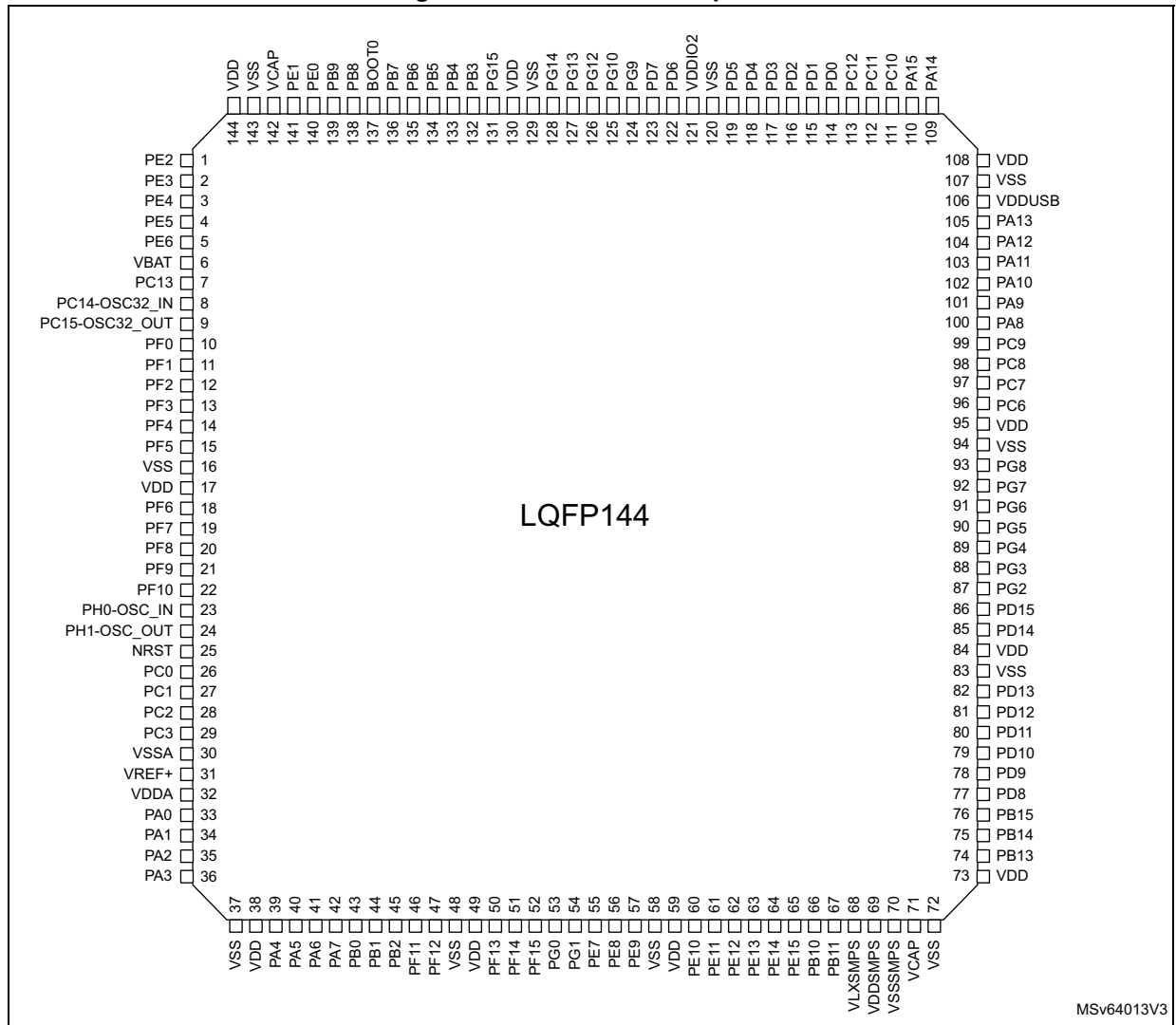
1. The above figure shows the package top view.

Figure 10. LQFP144 pinout



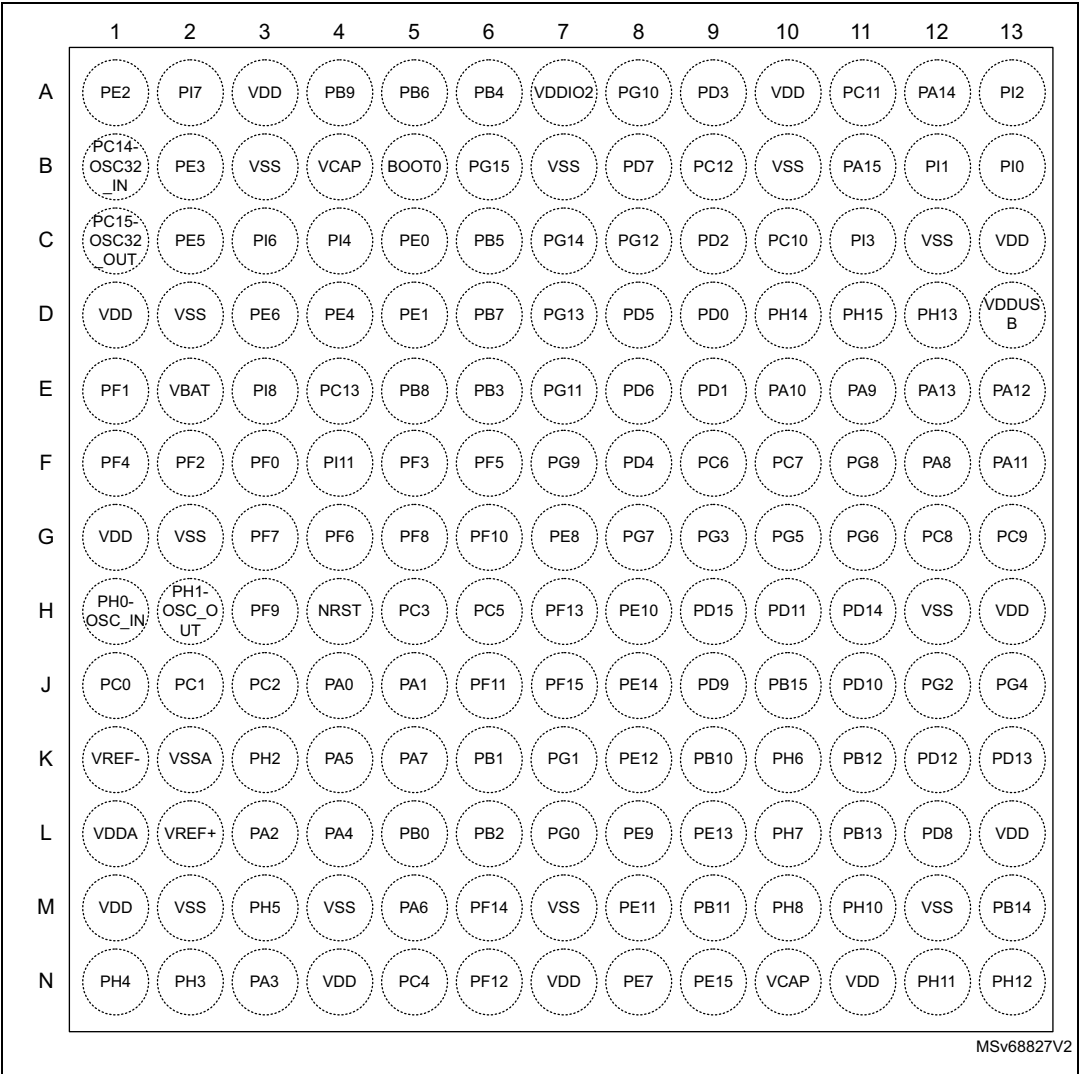
1. The above figure shows the package top view.

Figure 11. LQFP144 SMPS pinout



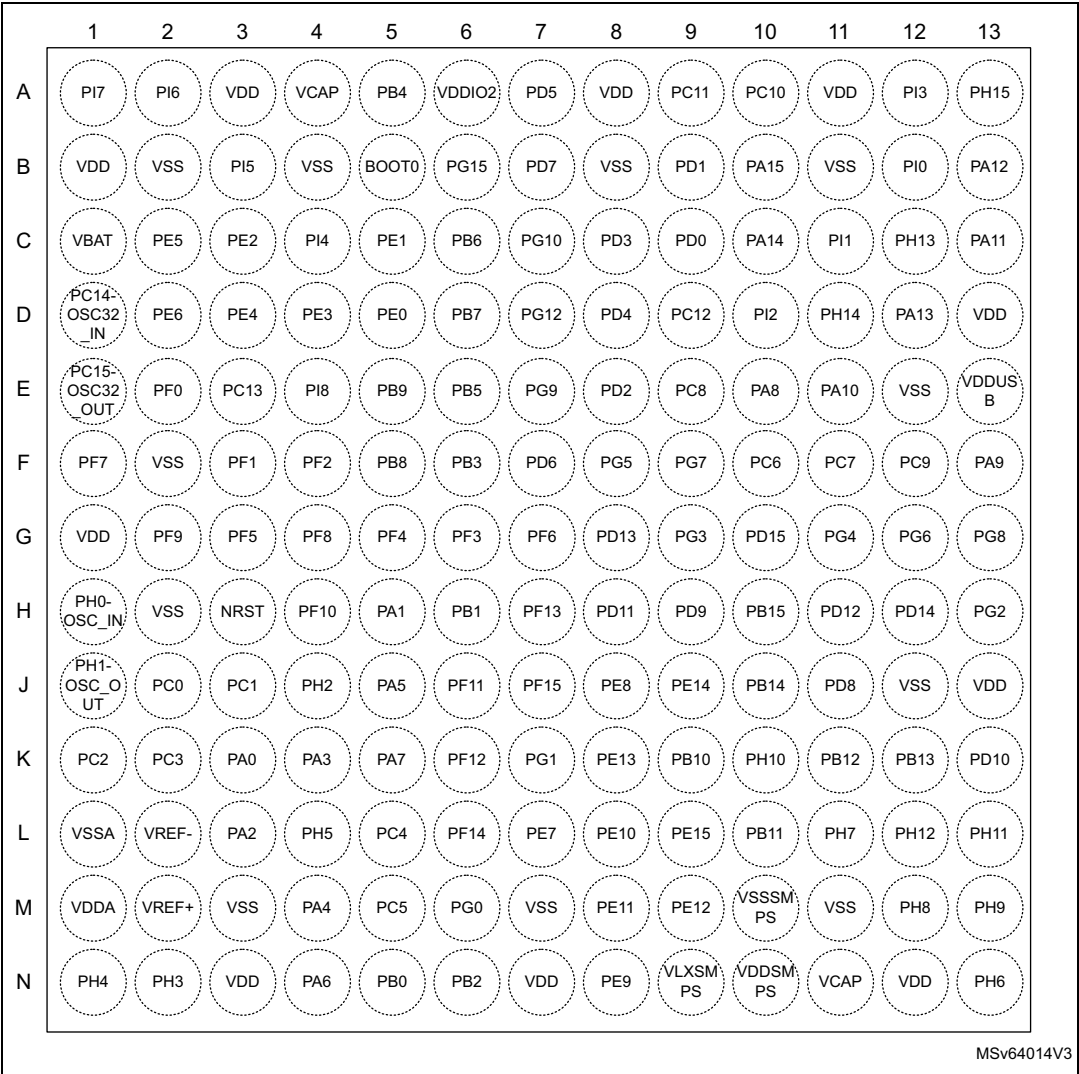
1. The above figure shows the package top view.

Figure 12. UFBGA169 ballout



1. The above figure shows the package top view.

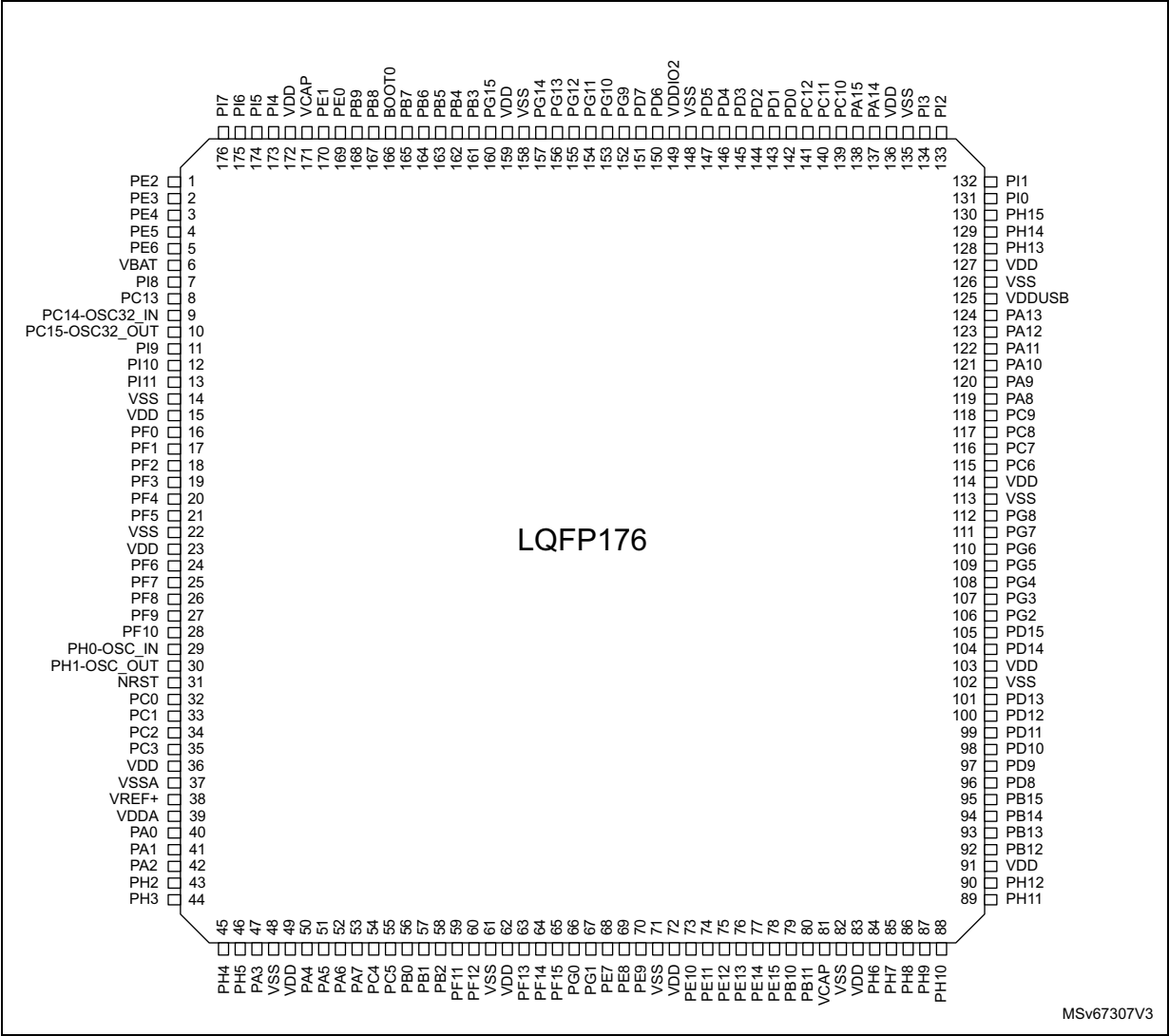
Figure 13. UFBGA169 SMPS ballout



MSv64014V3

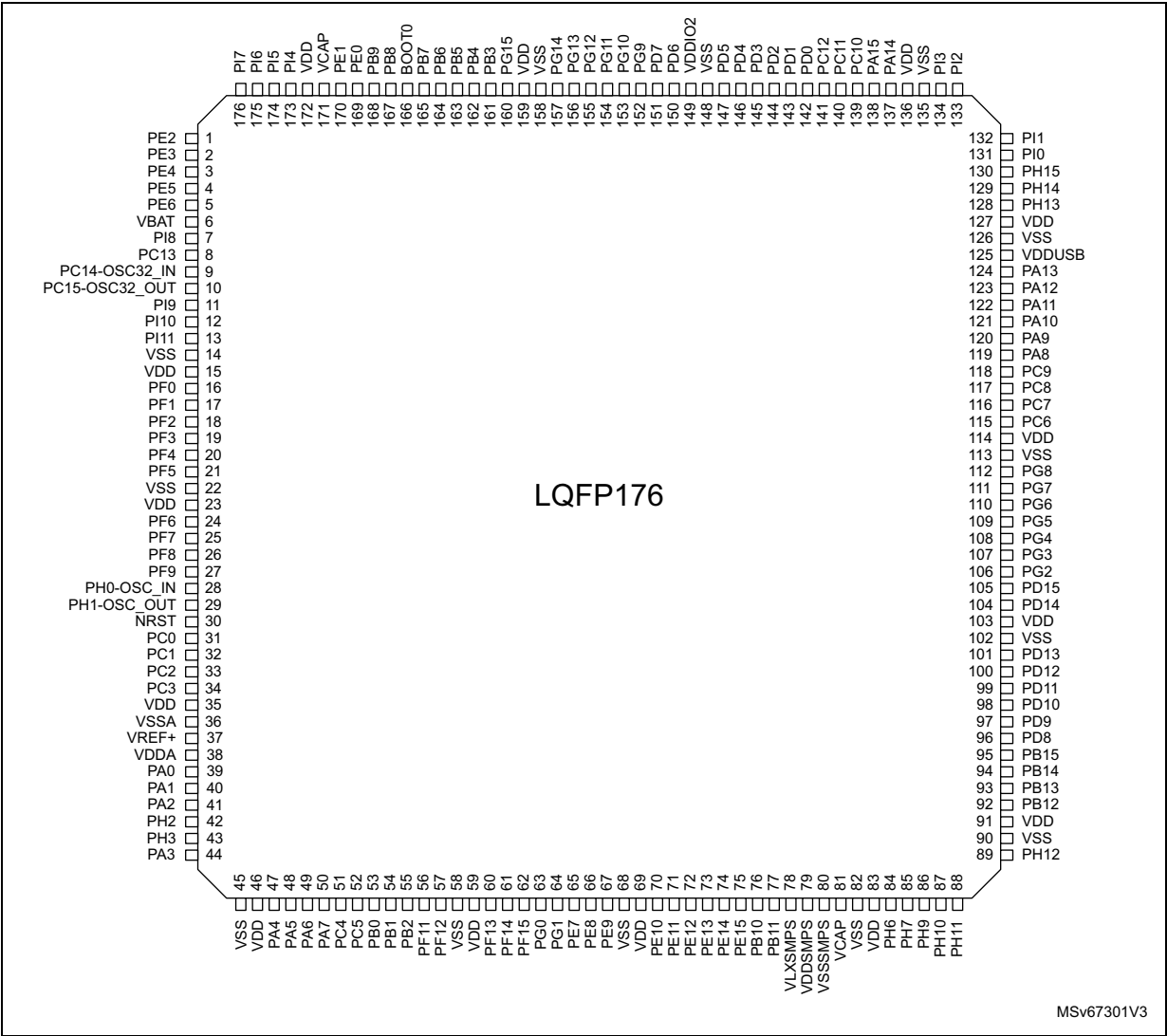
1. The above figure shows the package top view.

Figure 14. LQFP176 pinout



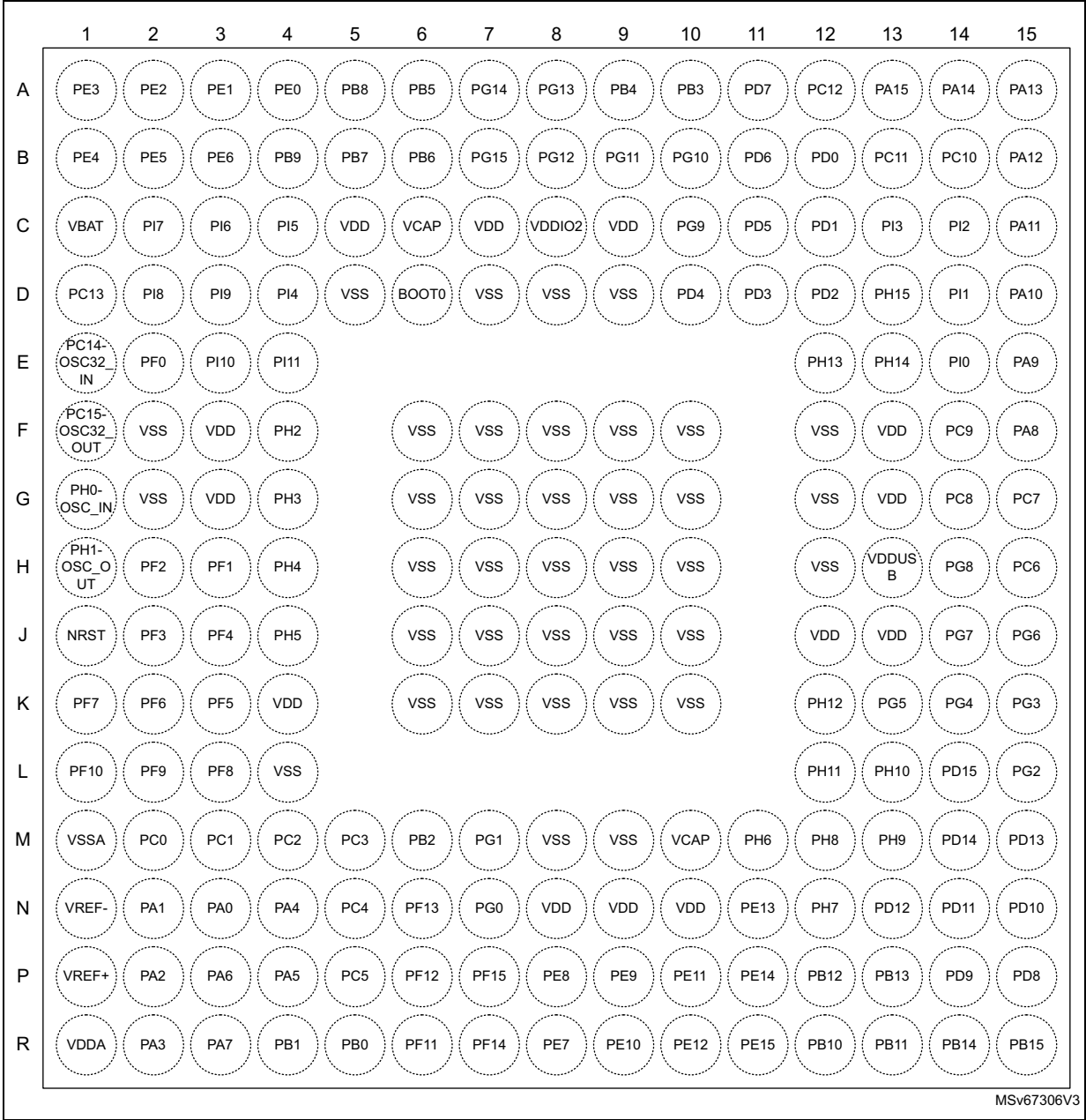
1. The above figure shows the package top view.

Figure 15. LQFP176 SMPS pinout



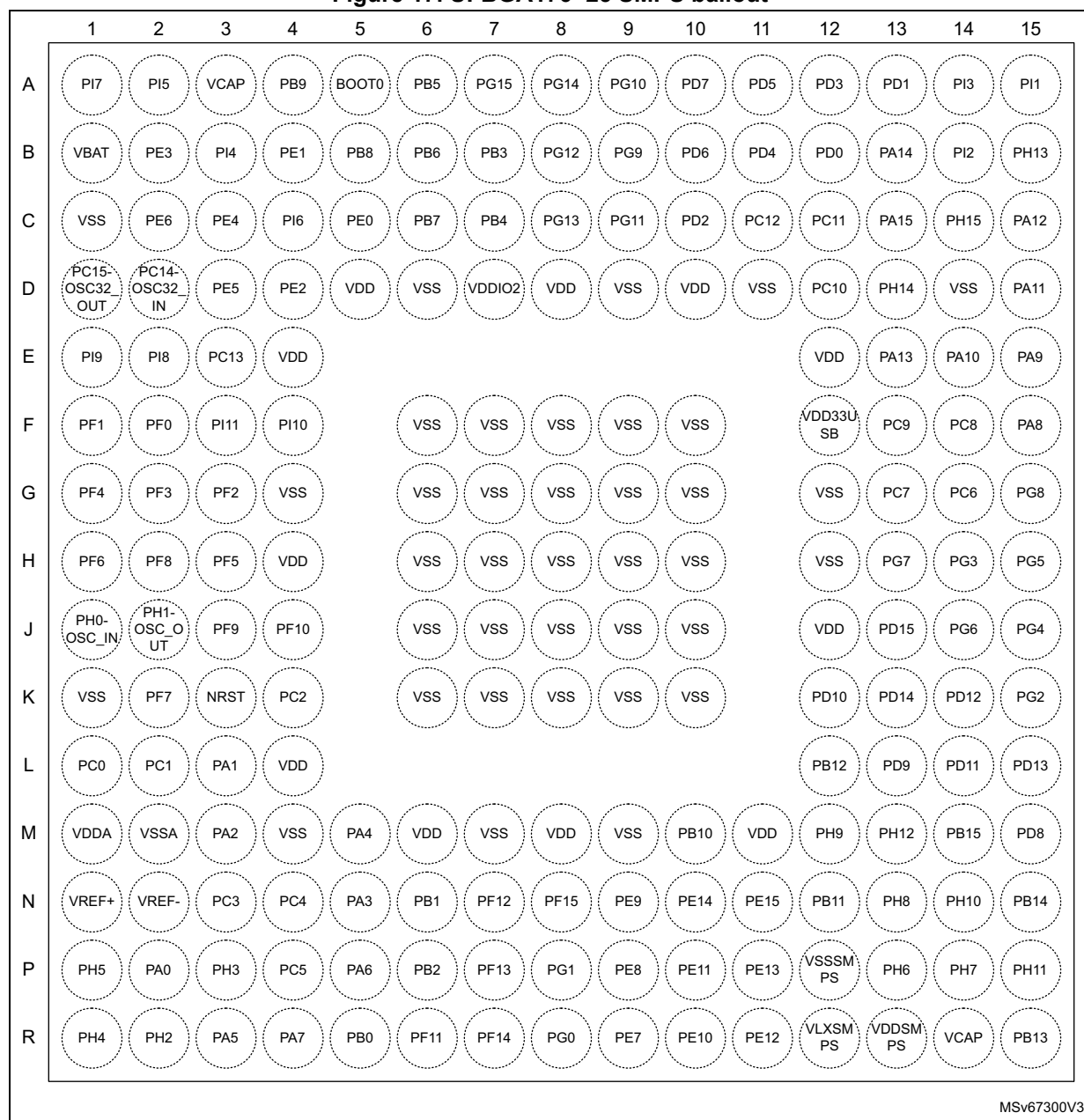
1. The above figure shows the package top view.

Figure 16. UFBGA176+25 ballout



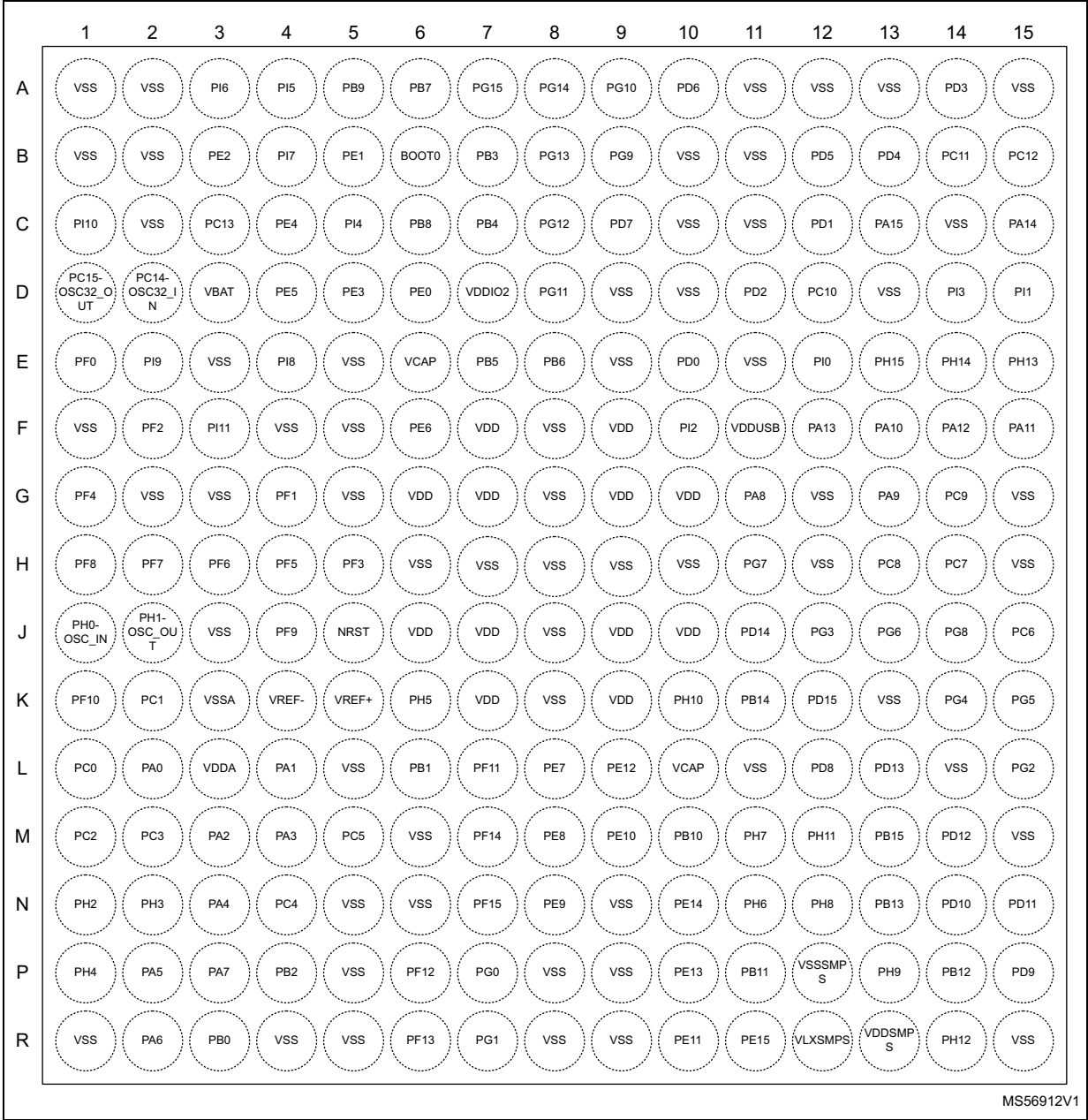
1. The above figure shows the package top view.

Figure 17. UFBGA176+25 SMPS ballout



1. The above figure shows the package top view.

Figure 18. TFBGA225 ballout



1. The above figure shows the package top view.

## 4.2 Pin description

**Table 13. Legend/abbreviations used in the pinout table**

| Name          |                      | Abbreviation                                                                                                                          | Definition                                                    |
|---------------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
| Pin name      |                      | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name |                                                               |
| Pin type      |                      | S                                                                                                                                     | Supply pin                                                    |
|               |                      | I                                                                                                                                     | Input only pin                                                |
|               |                      | I/O                                                                                                                                   | Input/output pin                                              |
| I/O structure |                      | FT                                                                                                                                    | 5 V-tolerant I/O                                              |
|               |                      | TT                                                                                                                                    | 3.6 V-tolerant I/O                                            |
|               |                      | RST                                                                                                                                   | Bidirectional reset pin with embedded weak pull-up resistor   |
|               |                      | Option for TT or FT I/Os <sup>(1)</sup>                                                                                               |                                                               |
|               |                      | _a                                                                                                                                    | I/O, with analog switch function supplied by V <sub>DDA</sub> |
|               |                      | _c                                                                                                                                    | I/O with USB Type-C power delivery function                   |
|               |                      | _d                                                                                                                                    | I/O with USB Type-C power delivery dead battery function      |
|               |                      | _f                                                                                                                                    | I/O, Fm+ capable                                              |
|               |                      | _h                                                                                                                                    | I/O with high-speed low-voltage mode                          |
|               |                      | _s                                                                                                                                    | I/O supplied only by V <sub>DDIO2</sub>                       |
|               |                      | _t                                                                                                                                    | I/O with tamper function functional in VBAT mode              |
|               |                      | _u                                                                                                                                    | I/O, with USB function supplied by V <sub>DDUSB</sub>         |
| Notes         |                      | Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset                                        |                                                               |
| Pin functions | Alternate functions  | Functions selected through GPIOx_AFR registers                                                                                        |                                                               |
|               | Additional functions | Functions directly selected/enabled through peripheral registers                                                                      |                                                               |

1. The related I/O structures in the following table are a concatenation of various options. Examples: FT\_hat, FT\_fs, FT\_u, TT\_a.



Table 14. STM32H562xx and STM32H563xx pin/ball definition

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                        | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                            |                      |
| -                            | 1            | 1            | C3            | 1            | D4               | B3            | -      | -        | 1       | 1       | A1       | 1       | A2          | PE2                                                        | I/O      | FT_h          | -     | TRACECLK, LPTIM1_IN2,<br>SAI1_CK1, SPI4_SCK,<br>SAI1_MCLK_A, USART10_RX,<br>UART8_TX, OCTOSPI1_IO2,<br>ETH_MII_TXD3, FMC_A23,<br>DCMI_D3/PSSI_D3, EVENTOUT | -                    |
| -                            | 2            | 2            | D4            | 2            | B2               | D5            | -      | -        | 2       | 2       | B2       | 2       | A1          | PE3                                                        | I/O      | FT_h          | -     | TRACED0, TIM15_BKIN,<br>SAI1_SD_B, USART10_TX,<br>FMC_A19, EVENTOUT                                                                                        | TAMP_IN6/TAMP_OUT3   |
| -                            | 3            | 3            | D3            | 3            | C3               | C4            | -      | -        | 3       | 3       | D4       | 3       | B1          | PE4                                                        | I/O      | FT_h          | -     | TRACED1, SAI1_D2,<br>TIM15_CH1N, SPI4_NSS,<br>SAI1_FS_A, FMC_A20,<br>DCMI_D4/PSSI_D4, EVENTOUT                                                             | TAMP_IN7/TAMP_OUT8   |
| -                            | 4            | 4            | C2            | 4            | D3               | D4            | -      | -        | 4       | 4       | C2       | 4       | B2          | PE5                                                        | I/O      | FT_h          | -     | TRACED2, SAI1_CK2,<br>TIM15_CH1, SPI4_MISO,<br>SAI1_SCK_A, FMC_A21,<br>DCMI_D6/PSSI_D6, EVENTOUT                                                           | TAMP_IN8/TAMP_OUT7   |
| -                            | 5            | 5            | D2            | 5            | C2               | F6            | -      | -        | 5       | 5       | D3       | 5       | B3          | PE6                                                        | I/O      | FT_h          | -     | TRACED3, TIM1_BKIN2,<br>SAI1_D1, TIM15_CH2,<br>SPI4_MOSI, SAI1_SD_A,<br>SAI2_MCLK_B, FMC_A22,<br>DCMI_D7/PSSI_D7, EVENTOUT                                 | TAMP_IN3/TAMP_OUT6   |
| A1                           | -            | -            | -             | -            | -                | F7            | -      | -        | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                                                                                                                                                          | -                    |
| B8                           | -            | -            | -             | -            | -                | A1            | -      | -        | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                                                                                                                                                          | -                    |
| B10                          | 6            | 6            | C1            | 6            | B1               | D3            | 1      | 1        | 6       | 6       | E2       | 6       | C1          | VBAT                                                       | S        | -             | -     | -                                                                                                                                                          | -                    |
| D2                           | -            | -            | -             | -            | -                | E3            | -      | -        | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                                                                                                                                                          | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                             | Additional functions                                         |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|-------------------------------------------------|--------------------------------------------------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                 |                                                              |
| -                            | -            | -            | E4            | 7            | E2               | E4            | -      | -       | -       | -       | E3       | 7       | D2          | PI8                                                        | I/O      | FT_t          | (5)   | EVENTOUT                                        | TAMP_IN2/TAMP_OUT3,<br>RTC_OUT2, WKUP3                       |
| C9                           | 7            | 7            | E3            | 8            | E3               | C3            | 2      | 2       | 7       | 7       | E4       | 8       | D1          | PC13                                                       | I/O      | FT_t          | (5)   | EVENTOUT                                        | TAMP_IN1/TAMP_OUT2/<br>TAMP_OUT3, RTC_OUT1/<br>RTC_TS, WKUP4 |
| G9                           | -            | -            | -             | -            | -                | E5            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                                               | -                                                            |
| D10                          | 8            | 8            | D1            | 9            | D2               | D2            | 3      | 3       | 8       | 8       | B1       | 9       | E1          | PC14-<br>OSC32_IN<br>(OSC32_IN)                            | I/O      | FT            | -     | EVENTOUT                                        | OSC32_IN                                                     |
| F10                          | 9            | 9            | E1            | 10           | D1               | D1            | 4      | 4       | 9       | 9       | C1       | 10      | F1          | PC15-<br>OSC32_OUT<br>(OSC32_OUT)                          | I/O      | FT            | -     | EVENTOUT                                        | OSC32_OUT                                                    |
| -                            | -            | -            | -             | 11           | E1               | E2            | -      | -       | -       | -       | -        | 11      | D3          | PI9                                                        | I/O      | FT_h          | -     | UART4_RX, FDCAN1_RX,<br>EVENTOUT                | -                                                            |
| -                            | -            | -            | -             | 12           | F4               | C1            | -      | -       | -       | -       | -        | 12      | E3          | PI10                                                       | I/O      | FT_h          | -     | FDCAN1_RX, ETH_MII_RX_ER,<br>PSSI_D14, EVENTOUT | -                                                            |
| -                            | -            | -            | -             | 13           | F3               | F3            | -      | -       | -       | -       | F4       | 13      | E4          | PI11                                                       | I/O      | FT            | -     | PSSI_D15, EVENTOUT                              | TAMP_IN4/TAMP_OUT5                                           |
| -                            | -            | -            | B2            | 14           | C1               | F8            | -      | -       | -       | -       | D2       | 14      | D5          | VSS                                                        | S        | -             | -     | -                                               | -                                                            |
| -                            | -            | -            | B1            | 15           | D5               | -             | -      | -       | -       | -       | D1       | 15      | C5          | VDD                                                        | S        | -             | -     | -                                               | -                                                            |
| -                            | -            | 10           | E2            | 16           | F2               | E1            | -      | -       | -       | 10      | F3       | 16      | E2          | PF0                                                        | I/O      | FT_f          | -     | I2C2_SDA, FMC_A0,<br>LPTIM5_CH1, EVENTOUT       | -                                                            |
| -                            | -            | 11           | F3            | 17           | F1               | G4            | -      | -       | -       | 11      | E1       | 17      | H3          | PF1                                                        | I/O      | FT_f          | -     | I2C2_SCL, FMC_A1,<br>LPTIM5_CH2, EVENTOUT       | -                                                            |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                              | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                  |                      |
| -                            | -            | 12           | F4            | 18           | G3               | F2            | -      | -       | -       | 12      | F2       | 18      | H2          | PF2                                                        | I/O      | FT_h          | -     | LPTIM3_CH2, LPTIM3_IN2,<br>I2C2_SMBA, UART12_TX,<br>USART11_CK, FMC_A2,<br>LPTIM5_IN1, EVENTOUT                  | -                    |
| -                            | -            | 13           | G6            | 19           | G2               | H5            | -      | -       | -       | 13      | F5       | 19      | J2          | PF3                                                        | I/O      | FT_h          | -     | LPTIM3_IN1, USART11_TX,<br>FMC_A3, LPTIM5_IN2,<br>EVENTOUT                                                       | -                    |
| -                            | -            | 14           | G5            | 20           | G1               | G1            | -      | -       | -       | 14      | F1       | 20      | J3          | PF4                                                        | I/O      | FT_h          | -     | LPTIM3_ETR, USART11_RX,<br>FMC_A4, EVENTOUT                                                                      | -                    |
| -                            | -            | 15           | G3            | 21           | H3               | H4            | -      | -       | -       | 15      | F6       | 21      | K3          | PF5                                                        | I/O      | FT_fh         | -     | LPTIM3_CH1, I2C4_SCL,<br>I3C1_SCL, UART12_RX,<br>USART11_CTS/USART11_NSS,<br>FMC_A5, LPTIM3_IN1,<br>EVENTOUT     | -                    |
| H2                           | 10           | 16           | F2            | 22           | G4               | -             | -      | -       | 10      | 16      | G2       | 22      | F2          | VSS                                                        | S        | -             | -     | -                                                                                                                | -                    |
| A7                           | 11           | 17           | G1            | 23           | E4               | -             | -      | -       | 11      | 17      | G1       | 23      | F3          | VDD                                                        | S        | -             | -     | -                                                                                                                | -                    |
| -                            | -            | 18           | G7            | 24           | H1               | H3            | -      | -       | -       | 18      | G4       | 24      | K2          | PF6                                                        | I/O      | FT_h          | -     | TIM16_CH1, SPI5_NSS,<br>SAI1_SD_B, UART7_RX,<br>OCTOSPI1_IO3, LPTIM5_CH1,<br>EVENTOUT                            | -                    |
| -                            | -            | 19           | F1            | 25           | K2               | H2            | -      | -       | -       | 19      | G3       | 25      | K1          | PF7                                                        | I/O      | FT_h          | -     | TIM17_CH1, SPI5_SCK,<br>SAI1_MCLK_B, UART7_TX,<br>OCTOSPI1_IO2, LPTIM5_CH2,<br>EVENTOUT                          | -                    |
| -                            | -            | 20           | G4            | 26           | H2               | H1            | -      | -       | -       | 20      | G5       | 26      | L3          | PF8                                                        | I/O      | FT_h          | -     | TIM16_CH1N, SPI5_MISO,<br>SAI1_SCK_B,<br>UART7_RTS/UART7_DE,<br>TIM13_CH1, OCTOSPI1_IO0,<br>LPTIM5_IN1, EVENTOUT | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                              | Additional functions                                         |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                  |                                                              |
| -                            | -            | 21           | G2            | 27           | J3               | J4            | -      | -        | -       | 21      | H3       | 27      | L2          | PF9                                                        | I/O      | FT_h          | -     | TIM17_CH1N, SPI5_MOSI,<br>SAI1_FS_B, UART7_CTS,<br>TIM14_CH1, OCTOSPI1_IO1,<br>LPTIM5_IN2, EVENTOUT                                              | -                                                            |
| -                            | -            | 22           | H4            | -            | J4               | K1            | -      | -        | -       | 22      | G6       | 28      | L1          | PF10                                                       | I/O      | FT_h          | -     | TIM16_BKIN, SAI1_D3,<br>PSSI_D15, OCTOSPI1_CLK,<br>DCMI_D11/PSSI_D11,<br>EVENTOUT                                                                | -                                                            |
| K10                          | 12           | 23           | H1            | 28           | J1               | J1            | 5      | 5        | 12      | 23      | H1       | 29      | G1          | PH0-<br>OSC_IN(PH0)                                        | I/O      | FT            | -     | EVENTOUT                                                                                                                                         | OSC_IN                                                       |
| J9                           | 13           | 24           | J1            | 29           | J2               | J2            | 6      | 6        | 13      | 24      | H2       | 30      | H1          | PH1-<br>OSC_OUT(PH1)                                       | I/O      | FT            | -     | EVENTOUT                                                                                                                                         | OSC_OUT                                                      |
| F8                           | 14           | 25           | H3            | 30           | K3               | J5            | 7      | 7        | 14      | 25      | H4       | 31      | J1          | NRST                                                       | I/O      | RST           | -     | -                                                                                                                                                | -                                                            |
| H8                           | 15           | 26           | J2            | 31           | L1               | L1            | 8      | 8        | 15      | 26      | J1       | 32      | M2          | PC0                                                        | I/O      | FT_a          | -     | TIM16_BKIN, SAI1_MCLK_A,<br>SPI2_RDY, SAI2_FS_B,<br>FMC_A25, OCTOSPI1_IO7,<br>FMC_SDNWE, EVENTOUT                                                | ADC12_INP10                                                  |
| G7                           | 16           | 27           | J3            | 32           | L2               | K2            | 9      | 9        | 16      | 27      | J2       | 33      | M3          | PC1                                                        | I/O      | FT_ah         | -     | TRACED0, SAI1_D1,<br>SPI2_MOSI/I2S2_SDO,<br>SAI1_SD_A,<br>USART11_RTS/USART11_DE,<br>SAI2_SD_A, SDMMC2_CK,<br>OCTOSPI1_IO4, ETH_MDC,<br>EVENTOUT | ADC12_INP11,<br>ADC12_INN10,<br>TAMP_IN3/TAMP_OUT5,<br>WKUP6 |
| M10                          | 17           | 28           | K1            | 33           | K4               | M1            | 10     | 10       | 17      | 28      | J3       | 34      | M4          | PC2                                                        | I/O      | FT_a          | -     | PWR_CSLEEP, TIM17_CH1,<br>TIM4_CH4, SPI2_MISO/I2S2_SDI,<br>OCTOSPI1_IO5, OCTOSPI1_IO2,<br>ETH_MII_TXD2, FMC_SDNE0,<br>EVENTOUT                   | ADC12_INP12,<br>ADC12_INN11                                  |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes          | Alternate functions                                                                                                                                                                  | Additional functions                                    |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |                |                                                                                                                                                                                      |                                                         |
| L9                           | 18           | 29           | K2            | 34           | N3               | M2            | 11     | 11      | 18      | 29      | H5       | 35      | M5          | PC3                                                        | I/O      | FT_a          | -              | PWR_CSTOP, SAI1_D3,<br>LPTIM3_CH1,<br>SPI2_MOSI/I2S2_SDO,<br>OCTOSPI1_IO6, OCTOSPI1_IO0,<br>ETH_MII_TX_CLK,<br>FMC_SDCKE0, EVENTOUT                                                  | ADC12_INP13,<br>ADC12_INN12                             |
| G1                           | -            | -            | -             | 35           | H4               | G10           | -      | -       | -       | 30      | M1       | 36      | G3          | VDD                                                        | S        | -             | -              | -                                                                                                                                                                                    | -                                                       |
| P2                           | -            | -            | H2            | -            | K1               | H6            | -      | -       | -       | -       | M2       | -       | G2          | VSS                                                        | S        | -             | -              | -                                                                                                                                                                                    | -                                                       |
| N9                           | 19           | 30           | L1            | 36           | M2               | K3            | 12     | 12      | 19      | 31      | K2       | 37      | M1          | VSSA                                                       | S        | -             | -              | -                                                                                                                                                                                    | -                                                       |
| -                            | -            | -            | L2            | -            | N2               | K4            | -      | -       | 20      | -       | K1       | -       | N1          | VREF-                                                      | S        | -             | -              | -                                                                                                                                                                                    | -                                                       |
| -                            | 20           | 31           | M2            | 37           | N1               | K5            | -      | -       | 21      | 32      | L2       | 38      | P1          | VREF+                                                      | S        | -             | -              | -                                                                                                                                                                                    | -                                                       |
| P10                          | 21           | 32           | M1            | 38           | M1               | L3            | 13     | 13      | 22      | 33      | L1       | 39      | R1          | VDDA                                                       | S        | -             | -              | -                                                                                                                                                                                    | -                                                       |
| K8                           | 22           | 33           | K3            | 39           | P2               | L2            | 14     | 14      | 23      | 34      | J4       | 40      | N3          | PA0                                                        | I/O      | FT_at         | <sup>(5)</sup> | TIM2_CH1, TIM5_CH1,<br>TIM8_ETR, TIM15_BKIN,<br>SPI6_NSS, SPI3_RDY,<br>USART2_CTS/USART2_NSS,<br>UART4_TX, SDMMC2_CMD,<br>SAI2_SD_B, ETH_MII_CRD,<br>TIM2_ETR, EVENTOUT              | ADC12_INP0, ADC12_INN1,<br>TAMP_IN2/TAMP_OUT1,<br>WKUP1 |
| J7                           | 23           | 34           | H5            | 40           | L3               | L4            | 15     | 15      | 24      | 35      | J5       | 41      | N2          | PA1                                                        | I/O      | FT_aht        | <sup>(5)</sup> | TIM2_CH2, TIM5_CH2,<br>TIM15_CH1N, LPTIM1_IN1,<br>OCTOSPI1_DQS,<br>USART2_RTS/USART2_DE,<br>UART4_RX, OCTOSPI1_IO3,<br>SAI2_MCLK_B,<br>ETH_MII_RX_CLK/ETH_RMII_RE<br>F_CLK, EVENTOUT | ADC12_INP1,<br>TAMP_IN5/TAMP_OUT4                       |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                    | Additional functions                         |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                        |                                              |
| M8                           | 24           | 35           | L3            | 41           | M3               | M3            | 16     | 16      | 25      | 36      | L3       | 42      | P2          | PA2                                                        | I/O      | FT_hat        | (5)   | TIM2_CH3, TIM5_CH3,<br>TIM15_CH1, LPTIM1_IN2,<br>USART2_TX, SAI2_SCK_B,<br>ETH_MDIO, EVENTOUT                          | ADC12_INP14,<br>TAMP_IN4/TAMP_OUT3,<br>WKUP2 |
| -                            | -            | -            | J4            | 42           | R2               | N1            | -      | -       | -       | -       | K3       | 43      | F4          | PH2                                                        | I/O      | FT_h          | -     | LPTIM1_IN2, OCTOSPI1_IO4,<br>SAI2_SCK_B, ETH_MII_CRS,<br>FMC_SDCKE0, EVENTOUT                                          | -                                            |
| H10                          | -            | -            | -             | -            | L4               | J6            | -      | -       | -       | -       | -        | -       | K4          | VDD                                                        | S        | -             | -     | -                                                                                                                      | -                                            |
| P8                           | -            | -            | -             | -            | M4               | -             | -      | -       | -       | -       | -        | -       | L4          | VSS                                                        | S        | -             | -     | -                                                                                                                      | -                                            |
| -                            | -            | -            | N2            | 43           | P3               | N2            | -      | -       | -       | -       | N2       | 44      | G4          | PH3                                                        | I/O      | FT_h          | -     | OCTOSPI1_IO5, SAI2_MCLK_B,<br>ETH_MII_COL, FMC_SDNE0,<br>EVENTOUT                                                      | -                                            |
| -                            | -            | -            | N1            | -            | R1               | P1            | -      | -       | -       | -       | N1       | 45      | H4          | PH4                                                        | I/O      | FT_fa         | -     | I2C2_SCL, SPI5_RDY, SPI6_RDY,<br>PSSI_D14, EVENTOUT                                                                    | -                                            |
| -                            | -            | -            | L4            | -            | P1               | K6            | -      | -       | -       | -       | M3       | 46      | J4          | PH5                                                        | I/O      | FT_fa         | -     | I2C2_SDA, SPI5_NSS,<br>SPI6_RDY, FMC_SDNWE,<br>EVENTOUT                                                                | -                                            |
| T10                          | 25           | 36           | K4            | 44           | N5               | M4            | 17     | 17      | 26      | 37      | N3       | 47      | R2          | PA3                                                        | I/O      | FT_ah         | -     | TIM2_CH4, TIM5_CH4,<br>OCTOSPI1_CLK, TIM15_CH2,<br>SPI2_NSS/I2S2_WS, SAI1_SD_B,<br>USART2_RX, ETH_MII_COL,<br>EVENTOUT | ADC12_INP15                                  |
| -                            | 26           | 37           | M3            | 45           | M7               | -             | 18     | 18      | 27      | 38      | M4       | 48      | M8          | VSS                                                        | S        | -             | -     | -                                                                                                                      | -                                            |
| R1                           | 27           | 38           | N3            | 46           | M6               | -             | 19     | 19      | 28      | 39      | N4       | 49      | N8          | VDD                                                        | S        | -             | -     | -                                                                                                                      | -                                            |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                                                   | Additional functions                      |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                                                       |                                           |
| R9                           | 28           | 39           | M4            | 47           | M5               | N3            | 20     | 20      | 29      | 40      | L4       | 50      | N4          | PA4                                                        | I/O      | TT_a          | -     | TIM5_ETR, LPTIM2_CH1,<br>SPI1_NSS/I2S1_WS,<br>SPI3_NSS/I2S3_WS,<br>USART2_CK, SPI6_NSS,<br>DCMI_HSYNC/PSSI_DE,<br>EVENTOUT                                                            | ADC12_INP18, DAC1_OUT1                    |
| L7                           | 29           | 40           | J5            | 48           | R3               | P2            | 21     | 21      | 30      | 41      | K4       | 51      | P4          | PA5                                                        | I/O      | TT_ah         | -     | TIM2_CH1, TIM8_CH1N,<br>SPI1_SCK/I2S1_CK, SPI6_SCK,<br>ETH_MII_TX_EN/ETH_RMII_TX_<br>EN, PSSI_D14, TIM2_ETR,<br>EVENTOUT                                                              | ADC12_INP19,<br>ADC12_INN18,<br>DAC1_OUT2 |
| H6                           | 30           | 41           | N4            | 49           | P5               | R2            | 22     | 22      | 31      | 42      | M5       | 52      | P3          | PA6                                                        | I/O      | FT_ah         | -     | TIM1_BKIN, TIM3_CH1,<br>TIM8_BKIN,<br>SPI1_MISO/I2S1_SDI,<br>OCTOSPI1_IO3, USART11_TX,<br>SPI6_MISO, TIM13_CH1,<br>DCMI_PIXCLK/PSSI_PDCK,<br>EVENTOUT                                 | ADC12_INP3                                |
| K6                           | 31           | 42           | K5            | 50           | R4               | P3            | 23     | 23      | 32      | 43      | K5       | 53      | R3          | PA7                                                        | I/O      | FT_ah         | -     | TIM1_CH1N, TIM3_CH2,<br>TIM8_CH1N,<br>SPI1_MOSI/I2S1_SDO,<br>USART11_RX, SPI6_MOSI,<br>TIM14_CH1, OCTOSPI1_IO2,<br>ETH_MII_RX_DV/ETH_RMII_CRS_<br>DV, FMC_SDNWE, FMC_NWE,<br>EVENTOUT | ADC12_INP7, ADC12_INN3                    |
| M6                           | -            | -            | L5            | 51           | N4               | N4            | 24     | 24      | 33      | 44      | N5       | 54      | N5          | PC4                                                        | I/O      | FT_a          | -     | TIM2_CH4, SAI1_CK1,<br>LPTIM2_ETR, I2S1_MCK,<br>USART3_RX,<br>ETH_MII_RXD0/ETH_RMII_RXD0<br>, FMC_SDNE0, EVENTOUT                                                                     | ADC12_INP4                                |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                                  | Additional functions   |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                                      |                        |
| N7                           | -            | -            | M5            | 52           | P4               | M5            | 25     | 25       | 34      | 45      | H6       | 55      | P5          | PC5                                                        | I/O      | FT_ah         | -     | TIM1_CH4N, SAI1_D3,<br>PSSI_D15, SAI1_FS_A,<br>UART12_RTS/UART12_DE,<br>OCTOSPI1_DQS,<br>ETH_MII_RXD1/ETH_RMII_RXD1<br>, FMC_SDCKE0, EVENTOUT                        | ADC12_INP8, ADC12_INN4 |
| T8                           | -            | -            | -             | -            | M8               | -             | -      | -        | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                                                                                                                                                                    | -                      |
| R7                           | 32           | 43           | N5            | 53           | R5               | R3            | 26     | 26       | 35      | 46      | L5       | 56      | R5          | PB0                                                        | I/O      | FT_ah         | -     | TIM1_CH2N, TIM3_CH3,<br>TIM8_CH2N, OCTOSPI1_IO1,<br>USART11_CK, UART4_CTS,<br>ETH_MII_RXD2, LPTIM3_CH1,<br>EVENTOUT                                                  | ADC12_INP9, ADC12_INN5 |
| P6                           | 33           | 44           | H6            | 54           | N6               | L6            | 27     | 27       | 36      | 47      | K6       | 57      | R4          | PB1                                                        | I/O      | FT_ah         | -     | TIM1_CH3N, TIM3_CH4,<br>TIM8_CH3N, OCTOSPI1_IO0,<br>ETH_MII_RXD3, LPTIM3_CH2,<br>EVENTOUT                                                                            | ADC12_INP5             |
| L5                           | 34           | 45           | N6            | 55           | P6               | P4            | 28     | 28       | 37      | 48      | L6       | 58      | M6          | PB2                                                        | I/O      | FT_h          | -     | RTC_OUT2, SAI1_D1,<br>TIM8_CH4N, SPI1_RDY,<br>LPTIM1_CH1, SAI1_SD_A,<br>SPI3_MOSI/I2S3_SDO,<br>OCTOSPI1_CLK,<br>OCTOSPI1_DQS,<br>SDMMC1_CMD, LPTIM5_ETR,<br>EVENTOUT | LSCO                   |
| -                            | -            | 46           | J6            | 56           | R6               | L7            | -      | -        | -       | 49      | J6       | 59      | R6          | PF11                                                       | I/O      | FT_ah         | -     | SPI5_MOSI, OCTOSPI1_NCLK,<br>SAI2_SD_B, FMC_NRAS,<br>DCMI_D12/PSSI_D12,<br>LPTIM6_CH1, EVENTOUT                                                                      | ADC1_INP2              |
| -                            | -            | 47           | K6            | 57           | N7               | P6            | -      | -        | -       | 50      | N6       | 60      | P6          | PF12                                                       | I/O      | FT_ah         | -     | FMC_A6, LPTIM6_CH2,<br>EVENTOUT                                                                                                                                      | ADC1_INP6, ADC1_INN2   |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                         | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|---------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                             |                      |
| -                            | -            | 48           | M7            | 58           | -                | J3            | -      | -        | -       | 51      | M7       | 61      | -           | VSS                                                        | S        | -             | -     | -                                                                                           | -                    |
| -                            | -            | 49           | N7            | 59           | -                | K7            | -      | -        | -       | 52      | N7       | 62      | N9          | VDD                                                        | S        | -             | -     | -                                                                                           | -                    |
| -                            | -            | 50           | H7            | 60           | P7               | R6            | -      | -        | -       | 53      | H7       | 63      | N6          | PF13                                                       | I/O      | FT_ah         | -     | I2C4_SMBA, FMC_A7,<br>LPTIM6_IN1, EVENTOUT                                                  | ADC2_INP2            |
| -                            | -            | 51           | L6            | 61           | R7               | M7            | -      | -        | -       | 54      | M6       | 64      | R7          | PF14                                                       | I/O      | FT_fah        | -     | FMC_A8, LPTIM6_IN2,<br>EVENTOUT                                                             | ADC2_INP6, ADC2_INN2 |
| -                            | -            | 52           | J7            | 62           | N8               | N7            | -      | -        | -       | 55      | J7       | 65      | P7          | PF15                                                       | I/O      | FT_fh         | -     | I2C4_SDA, I3C1_SDA, FMC_A9,<br>EVENTOUT                                                     | -                    |
| -                            | -            | 53           | M6            | 63           | R8               | P7            | -      | -        | -       | 56      | L7       | 66      | N7          | PG0                                                        | I/O      | FT_h          | -     | UART9_RX, FMC_A10,<br>LPTIM4_IN1, EVENTOUT                                                  | -                    |
| -                            | -            | -            | -             | -            | -                | K9            | -      | -        | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                                                                                           | -                    |
| -                            | -            | 54           | K7            | 64           | P8               | R7            | -      | -        | -       | 57      | K7       | 67      | M7          | PG1                                                        | I/O      | FT_h          | -     | SPI2_MOSI/I2S2_SDO,<br>UART9_TX, FMC_A11,<br>EVENTOUT                                       | -                    |
| T6                           | 35           | 55           | L7            | 65           | R9               | L8            | -      | -        | 38      | 58      | N8       | 68      | R8          | PE7                                                        | I/O      | FT_h          | -     | TIM1_ETR,<br>UART12_RTS/UART12_DE,<br>UART7_RX, OCTOSPI1_IO4,<br>FMC_D4/FMC_AD4, EVENTOUT   | -                    |
| N5                           | 36           | 56           | J8            | 66           | P9               | M8            | -      | -        | 39      | 59      | G7       | 69      | P8          | PE8                                                        | I/O      | FT_h          | -     | TIM1_CH1N,<br>UART12_CTS/UART12_NSS,<br>UART7_TX, OCTOSPI1_IO5,<br>FMC_D5/FMC_AD5, EVENTOUT | -                    |
| R5                           | 37           | 57           | N8            | 67           | N9               | N8            | -      | -        | 40      | 60      | L8       | 70      | P9          | PE9                                                        | I/O      | FT_h          | -     | TIM1_CH1, UART12_RX,<br>UART7_RTS/UART7_DE,<br>OCTOSPI1_IO6,<br>FMC_D6/FMC_AD6, EVENTOUT    | -                    |
| -                            | -            | 58           | -             | 68           | -                | K8            | -      | -        | -       | 61      | -        | 71      | -           | VSS                                                        | S        | -             | -     | -                                                                                           | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                        | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                            |                      |
| -                            | -            | 59           | -             | 69           | -                | -             | -      | -       | -       | 62      | -        | 72      | -           | VDD                                                        | S        | -             | -     | -                                                                                                                          | -                    |
| M4                           | 38           | 60           | L8            | 70           | R10              | M9            | -      | -       | 41      | 63      | H8       | 73      | R9          | PE10                                                       | I/O      | FT_h          | -     | TIM1_CH2N, UART12_TX,<br>UART7_CTS, OCTOSPI1_IO7,<br>FMC_D7/FMC_AD7, EVENTOUT                                              | -                    |
| -                            | 39           | 61           | M8            | 71           | P10              | R10           | -      | -       | 42      | 64      | M8       | 74      | P10         | PE11                                                       | I/O      | FT_h          | -     | TIM1_CH2, SPI1_RDY,<br>SPI4_NSS, OCTOSPI1_NCS,<br>SAI2_SD_B, FMC_D8/FMC_AD8,<br>EVENTOUT                                   | -                    |
| -                            | 40           | 62           | M9            | 72           | R11              | L9            | -      | -       | 43      | 65      | K8       | 75      | R10         | PE12                                                       | I/O      | FT_h          | -     | TIM1_CH3N, SPI4_SCK,<br>SAI2_SCK_B,<br>FMC_D9/FMC_AD9, EVENTOUT                                                            | -                    |
| -                            | 41           | 63           | K8            | 73           | P11              | P10           | -      | -       | 44      | 66      | L9       | 76      | N11         | PE13                                                       | I/O      | FT_h          | -     | TIM1_CH3, SPI4_MISO,<br>SAI2_FS_B,<br>FMC_D10/FMC_AD10,<br>EVENTOUT                                                        | -                    |
| -                            | 42           | 64           | J9            | 74           | N10              | N10           | -      | -       | 45      | 67      | J8       | 77      | P11         | PE14                                                       | I/O      | FT_h          | -     | TIM1_CH4, SPI4_MOSI,<br>SAI2_MCLK_B,<br>FMC_D11/FMC_AD11,<br>EVENTOUT                                                      | -                    |
| -                            | 43           | 65           | L9            | 75           | N11              | R11           | -      | -       | 46      | 68      | N9       | 78      | R11         | PE15                                                       | I/O      | FT_h          | -     | TIM1_BKIN, TIM1_CH4N,<br>USART10_CK,<br>FMC_D12/FMC_AD12,<br>EVENTOUT                                                      | -                    |
| P4                           | 44           | 66           | K9            | 76           | M10              | M10           | 29     | 29      | 47      | 69      | K9       | 79      | R12         | PB10                                                       | I/O      | FT_f          | -     | TIM2_CH3, LPTIM3_CH1,<br>LPTIM2_IN1, I2C2_SCL,<br>SPI2_SCK/I2S2_CK,<br>USART3_TX, OCTOSPI1_NCS,<br>ETH_MII_RX_ER, EVENTOUT | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                          | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                              |                      |
| -                            | 45           | 67           | L10           | 77           | N12              | P11           | -      | 30       | -       | -       | M9       | 80      | R13         | PB11                                                       | I/O      | FT_f          | -     | TIM2_CH4, LPTIM2_ETR,<br>I2C2_SDA, SPI2_RDY, SPI4_RDY,<br>USART3_RX,<br>ETH_MII_TX_EN/ETH_RMII_TX_<br>EN, FMC_NBL1, EVENTOUT | -                    |
| T4                           | 46           | 68           | N9            | 78           | R12              | R12           | -      | -        | -       | -       | -        | -       | -           | VLXSMPS                                                    | S        | -             | -     | -                                                                                                                            | -                    |
| R3                           | 47           | 69           | N10           | 79           | R13              | R13           | -      | -        | -       | -       | -        | -       | -           | VDDSMPS                                                    | S        | -             | -     | -                                                                                                                            | -                    |
| N3                           | 48           | 70           | M10           | 80           | P12              | P12           | -      | -        | -       | -       | -        | -       | -           | VSSSMPS                                                    | S        | -             | -     | -                                                                                                                            | -                    |
| T2                           | 49           | 71           | N11           | 81           | R14              | L10           | 30     | 31       | 48      | 70      | N10      | 81      | M10         | VCAP                                                       | S        | -             | -     | -                                                                                                                            | -                    |
| -                            | 50           | 72           | M11           | 82           | M9               | L5            | 31     | 32       | 49      | 71      | M12      | 82      | M9          | VSS                                                        | S        | -             | -     | -                                                                                                                            | -                    |
| -                            | 51           | 73           | N12           | 83           | M11              | -             | 32     | 33       | 50      | 72      | N11      | 83      | N10         | VDD                                                        | S        | -             | -     | -                                                                                                                            | -                    |
| -                            | -            | -            | N13           | 84           | P13              | N11           | -      | -        | -       | -       | K10      | 84      | M11         | PH6                                                        | I/O      | FT            | -     | TIM1_CH3N, TIM12_CH1,<br>TIM8_CH1, I2C2_SMBA,<br>SPI5_SCK, ETH_MII_RXD2,<br>FMC_SDNE1,<br>DCMI_D8/PSSI_D8, EVENTOUT          | -                    |
| -                            | -            | -            | L11           | 85           | P14              | M11           | -      | -        | -       | -       | L10      | 85      | N12         | PH7                                                        | I/O      | FT_f          | -     | TIM1_CH3, TIM8_CH1N,<br>I2C3_SCL, SPI5_MISO,<br>ETH_MII_RXD3, FMC_SDCKE1,<br>DCMI_D9/PSSI_D9, EVENTOUT                       | -                    |
| -                            | -            | -            | M12           | -            | N13              | N12           | -      | -        | -       | -       | M10      | 86      | M12         | PH8                                                        | I/O      | FT_fh         | -     | TIM1_CH2N, TIM5_ETR,<br>TIM8_CH2, I2C3_SDA,<br>SPI5_MOSI,<br>DCMI_HSYNC/PSSI_DE,<br>EVENTOUT                                 | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                    | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                        |                      |
| -                            | -            | -            | M13           | 86           | M12              | P13           | -      | -       | -       | -       | -        | 87      | M13         | PH9                                                        | I/O      | FT_h          | -     | TIM1_CH2, TIM12_CH2,<br>TIM8_CH2N, I2C3_SMBA,<br>SPI5_NSS, DCM1_D0/PSSI_D0,<br>EVENTOUT                                                                | -                    |
| -                            | -            | -            | K10           | 87           | N14              | K10           | -      | -       | -       | -       | M11      | 88      | L13         | PH10                                                       | I/O      | FT_h          | -     | TIM1_CH1N, TIM5_CH1,<br>TIM8_CH3, I2C4_SMBA,<br>SPI5_RDY, DCM1_D1/PSSI_D1,<br>EVENTOUT                                                                 | -                    |
| -                            | -            | -            | L13           | 88           | P15              | M12           | -      | -       | -       | -       | N12      | 89      | L12         | PH11                                                       | I/O      | FT_fh         | -     | TIM1_CH1, TIM5_CH2,<br>TIM8_CH3N, I2C4_SCL,<br>I3C1_SCL, DCM1_D2/PSSI_D2,<br>EVENTOUT                                                                  | -                    |
| -                            | -            | -            | L12           | 89           | M13              | R14           | -      | -       | -       | -       | N13      | 90      | K12         | PH12                                                       | I/O      | FT_fh         | -     | TIM1_BKIN, TIM5_CH3,<br>TIM8_BKIN, I2C4_SDA,<br>I3C1_SDA, TIM8_CH4N,<br>DCM1_D3/PSSI_D3, EVENTOUT                                                      | -                    |
| -                            | -            | -            | -             | 90           | H12              | R15           | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                                                                                                                                                      | -                    |
| -                            | -            | -            | -             | 91           | J12              | -             | -      | -       | -       | -       | L13      | 91      | J12         | VDD                                                        | S        | -             | -     | -                                                                                                                                                      | -                    |
| L3                           | -            | -            | K11           | 92           | L12              | P14           | 33     | 34      | 51      | 73      | K11      | 92      | P12         | PB12                                                       | I/O      | FT_fh         | -     | TIM1_BKIN, OCTOSPI1_NCLK,<br>I2C2_SDA, SPI2_NSS/I2S2_WS,<br>UCPD1_FRSTX, USART3_CK,<br>FDCAN2_RX,<br>ETH_MII_TXD0/ETH_RMII_TXD0,<br>UART5_RX, EVENTOUT | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes          | Alternate functions                                                                                                                                                                                                                | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |                |                                                                                                                                                                                                                                    |                      |
| M2                           | 52           | 74           | K12           | 93           | R15              | N13           | 34     | 35       | 52      | 74      | L11      | 93      | P13         | PB13                                                       | I/O      | FT_c          | <sup>(6)</sup> | TIM1_CH1N, LPTIM3_IN1,<br>LPTIM2_CH1, I2C2_SMBA,<br>SPI2_SCK/I2S2_CK,<br>USART3_CTS/USART3_NSS,<br>FDCAN2_TX, SDMMC1_D0,<br>UART5_TX, EVENTOUT                                                                                     | UCPD1_CC1            |
| N1                           | 53           | 75           | J10           | 94           | N15              | K11           | 35     | 36       | 53      | 75      | M13      | 94      | R14         | PB14                                                       | I/O      | FT_c          | <sup>(6)</sup> | TIM1_CH2N, TIM12_CH1,<br>TIM8_CH2N, USART1_TX,<br>SPI2_MISO/I2S2_SDI,<br>USART3_RTS/USART3_DE,<br>UART4_RTS/UART4_DE,<br>SDMMC2_D0, LPTIM3_ETR,<br>EVENTOUT                                                                        | UCPD1_CC2            |
| L1                           | 54           | 76           | H10           | 95           | M14              | M13           | 36     | 37       | 54      | 76      | J10      | 95      | R15         | PB15                                                       | I/O      | FT_h          | -              | RTC_REFIN, TIM1_CH3N,<br>TIM12_CH2, TIM8_CH3N,<br>USART1_RX,<br>SPI2_MOSI/I2S2_SDO,<br>USART11_CTS/USART11_NSS,<br>UART4_CTS, SDMMC2_D1,<br>OCTOSPI1_CLK,<br>ETH_MII_TXD1/ETH_RMII_TXD1,<br>DCMI_D2/PSSI_D2, UART5_RX,<br>EVENTOUT | PVD_IN               |
| -                            | 55           | 77           | J11           | 96           | M15              | L12           | -      | -        | 55      | 77      | L12      | 96      | P15         | PD8                                                        | I/O      | FT_h          | -              | USART3_TX,<br>FMC_D13/FMC_AD13,<br>EVENTOUT                                                                                                                                                                                        | -                    |
| -                            | -            | -            | -             | -            | G12              | -             | -      | -        | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -              | -                                                                                                                                                                                                                                  | -                    |
| -                            | 56           | 78           | H9            | 97           | L13              | P15           | -      | -        | 56      | 78      | J9       | 97      | P14         | PD9                                                        | I/O      | FT_h          | -              | USART3_RX, FDCAN2_RX,<br>FMC_D14/FMC_AD14,<br>EVENTOUT                                                                                                                                                                             | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                                                       | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                                                           |                      |
| -                            | 57           | 79           | K13           | 98           | K12              | N14           | -      | -       | 57      | 79      | J11      | 98      | N15         | PD10                                                       | I/O      | FT_h          | -     | LPTIM2_CH2, USART3_CK,<br>FMC_D15/FMC_AD15,<br>EVENTOUT                                                                                                                                   | -                    |
| -                            | 58           | 80           | H8            | 99           | L14              | N15           | -      | 38      | 58      | 80      | H10      | 99      | N14         | PD11                                                       | I/O      | FT_h          | -     | SAI1_CK1, LPTIM2_IN2,<br>I2C4_SMB, A,<br>USART3_CTS/USART3_NSS,<br>UART4_RX, OCTOSPI1_IO0,<br>SAI2_SD_A,<br>FMC_A16/FMC_CLE, EVENTOUT                                                     | -                    |
| -                            | 59           | 81           | H11           | 100          | K14              | M14           | -      | 39      | 59      | 81      | K12      | 100     | N13         | PD12                                                       | I/O      | FT_fh         | -     | LPTIM1_IN1, TIM4_CH1,<br>LPTIM2_IN1, I2C4_SCL,<br>I3C1_SCL, SAI1_D1,<br>USART3_RTS/USART3_DE,<br>UART4_TX, OCTOSPI1_IO1,<br>SAI2_FS_A, FMC_A17/FMC_ALE,<br>DCMI_D12/PSSI_D12,<br>EVENTOUT | -                    |
| -                            | 60           | 82           | G8            | 101          | L15              | L13           | -      | -       | 60      | 82      | K13      | 101     | M15         | PD13                                                       | I/O      | FT_fh         | -     | LPTIM1_CH1, TIM4_CH2,<br>LPTIM2_CH1, I2C4_SDA,<br>I3C1_SDA, OCTOSPI1_IO3,<br>SAI2_SCK_A,<br>UART9_RTS/UART9_DE,<br>FMC_A18, DCMI_D13/PSSI_D13,<br>LPTIM4_IN1, EVENTOUT                    | -                    |
| -                            | -            | 83           | J12           | 102          | -                | -             | -      | -       | -       | 83      | H12      | 102     | H12         | VSS                                                        | S        | -             | -     | -                                                                                                                                                                                         | -                    |
| -                            | -            | 84           | J13           | 103          | -                | -             | -      | -       | -       | 84      | H13      | 103     | J13         | VDD                                                        | S        | -             | -     | -                                                                                                                                                                                         | -                    |
| K2                           | 61           | 85           | H12           | 104          | K13              | J11           | -      | -       | 61      | 85      | H11      | 104     | M14         | PD14                                                       | I/O      | FT_h          | -     | TIM4_CH3, UART8_CTS,<br>UART9_RX, FMC_D0/FMC_AD0,<br>EVENTOUT                                                                                                                             | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                      | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                          |                      |
| J1                           | 62           | 86           | G10           | 105          | J13              | K12           | -      | -        | 62      | 86      | H9       | 105     | L14         | PD15                                                       | I/O      | FT_h          | -     | TIM4_CH4,<br>UART8_RTS/UART8_DE,<br>UART9_TX, FMC_D1/FMC_AD1,<br>EVENTOUT                                                | -                    |
| -                            | -            | -            | -             | -            | -                | -             | -      | -        | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                                                                                                                        | -                    |
| -                            | -            | -            | -             | -            | -                | -             | -      | -        | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                                                                                                                        | -                    |
| -                            | -            | 87           | H13           | 106          | K15              | L15           | -      | -        | -       | 87      | J12      | 106     | L15         | PG2                                                        | I/O      | FT_h          | -     | TIM8_BKIN, UART12_RX,<br>FMC_A12, LPTIM6_ETR,<br>EVENTOUT                                                                | -                    |
| -                            | -            | 88           | G9            | 107          | H14              | J12           | -      | -        | -       | 88      | G9       | 107     | K15         | PG3                                                        | I/O      | FT_h          | -     | TIM8_BKIN2, UART12_TX,<br>FMC_A13, LPTIM5_ETR,<br>EVENTOUT                                                               | -                    |
| -                            | -            | 89           | G11           | 108          | J15              | K14           | -      | -        | -       | 89      | J13      | 108     | K14         | PG4                                                        | I/O      | FT_h          | -     | TIM1_BKIN2,<br>FMC_A14/FMC_BA0,<br>LPTIM4_ETR, EVENTOUT                                                                  | -                    |
| -                            | -            | 90           | F8            | 109          | H15              | K15           | -      | -        | -       | 90      | G10      | 109     | K13         | PG5                                                        | I/O      | FT_h          | -     | TIM1_ETR, FMC_A15/FMC_BA1,<br>EVENTOUT                                                                                   | -                    |
| -                            | -            | 91           | G12           | 110          | J14              | J13           | -      | -        | -       | 91      | G11      | 110     | J15         | PG6                                                        | I/O      | FT_fh         | -     | TIM17_BKIN, I3C1_SDA,<br>I2C4_SDA, SPI1_RDY,<br>OCTOSPI1_NCS,<br>UCPD1_FRSTX, FMC_NE3,<br>DCMI_D12/PSSI_D12,<br>EVENTOUT | -                    |
| -                            | -            | 92           | F9            | 111          | H13              | H11           | -      | -        | -       | 92      | G8       | 111     | J14         | PG7                                                        | I/O      | FT_fh         | -     | SAI1_CK2, I3C1_SCL, I2C4_SCL,<br>SAI1_MCLK_A, USART6_CK,<br>UCPD1_FRSTX, FMC_INT,<br>DCMI_D13/PSSI_D13,<br>EVENTOUT      | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                        | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                            |                      |
| -                            | -            | 93           | G13           | 112          | G15              | J14           | -      | -       | -       | 93      | F11      | 112     | H14         | PG8                                                        | I/O      | FT_h          | -     | TIM8_ETR, SPI6_NSS,<br>USART6_RTS/USART6_DE,<br>ETH_PPS_OUT, FMC_SDCLK,<br>EVENTOUT                                                                        | -                    |
| -                            | -            | 94           | -             | 113          | -                | -             | -      | -       | -       | 94      | -        | 113     | -           | VSS                                                        | S        | -             | -     | -                                                                                                                                                          | -                    |
| -                            | -            | 95           | -             | 114          | -                | -             | -      | -       | -       | 95      | -        | 114     | -           | VDD                                                        | S        | -             | -     | -                                                                                                                                                          | -                    |
| J3                           | 63           | 96           | F10           | 115          | G14              | J15           | 37     | 40      | 63      | 96      | F9       | 115     | H15         | PC6                                                        | I/O      | FT_h          | -     | TIM3_CH1, TIM8_CH1,<br>I2S2_MCK, SAI1_SCK_A,<br>USART6_TX, SDMMC1_D0DIR,<br>FMC_NWAIT, SDMMC2_D6,<br>OCTOSPI1_IO5, SDMMC1_D6,<br>DCMI_D0/PSSI_D0, EVENTOUT | -                    |
| K4                           | 64           | 97           | F11           | 116          | G13              | H14           | 38     | 41      | 64      | 97      | F10      | 116     | G15         | PC7                                                        | I/O      | FT_h          | -     | TRGIO, TIM3_CH2, TIM8_CH2,<br>I2S3_MCK, USART6_RX,<br>SDMMC1_D123DIR, FMC_NE1,<br>SDMMC2_D7, OCTOSPI1_IO6,<br>SDMMC1_D7,<br>DCMI_D1/PSSI_D1, EVENTOUT      | -                    |
| J5                           | 65           | 98           | E9            | 117          | F14              | H13           | 39     | 42      | 65      | 98      | G12      | 117     | G14         | PC8                                                        | I/O      | FT_h          | -     | TRACED1, TIM3_CH3,<br>TIM8_CH3, USART6_CK,<br>UART5_RTS/UART5_DE,<br>FMC_NE2/FMC_NCE, FMC_INT,<br>FMC_ALE, SDMMC1_D0,<br>DCMI_D2/PSSI_D2, EVENTOUT         | -                    |
| F2                           | 66           | 99           | F12           | 118          | F13              | G14           | 40     | 43      | 66      | 99      | G13      | 118     | F14         | PC9                                                        | I/O      | FT_fh         | -     | MCO2, TIM3_CH4, TIM8_CH4,<br>I2C3_SDA, AUDIOCLK,<br>UART5_CTS, OCTOSPI1_IO0,<br>FMC_CLE, SDMMC1_D1,<br>DCMI_D3/PSSI_D3, EVENTOUT                           | UCPD1_DB2            |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                       | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                           |                      |
| -                            | -            | -            | -             | -            | -                | -             | -      | -        | -       | -       | -        | -       | G12         | VSS                                                        | S        | -             | -     | -                                                                                                                                         | -                    |
| -                            | -            | -            | -             | -            | -                | -             | -      | -        | -       | -       | -        | -       | G13         | VDD                                                        | S        | -             | -     | -                                                                                                                                         | -                    |
| G3                           | 67           | 100          | E10           | 119          | F15              | G11           | 41     | 44       | 67      | 100     | F12      | 119     | F15         | PA8                                                        | I/O      | FT_fh         | -     | MCO1, TIM1_CH1, TIM8_BKIN2,<br>I2C3_SCL, SPI1_RDY,<br>USART1_CK, USB_SOF,<br>UART7_RX, FMC_NOE,<br>DCMI_D3/PSSI_D3, EVENTOUT              | -                    |
| H4                           | 68           | 101          | F13           | 120          | E15              | G13           | 42     | 45       | 68      | 101     | E11      | 120     | E15         | PA9                                                        | I/O      | FT_d          | -     | TIM1_CH2, LPUART1_TX,<br>I2C3_SMBA, SPI2_SCK/I2S2_CK,<br>USART1_TX, ETH_MII_TX_ER,<br>FMC_NWE, DCMI_D0/PSSI_D0,<br>EVENTOUT               | UCPD1_DB1            |
| G5                           | 69           | 102          | E11           | 121          | E14              | F13           | 43     | 46       | 69      | 102     | E10      | 121     | D15         | PA10                                                       | I/O      | FT_h          | -     | TIM1_CH3, LPUART1_RX,<br>LPTIM2_IN2, UCPD1_FRSTX,<br>USART1_RX, FDCAN2_TX,<br>SDMMC1_D0,<br>DCMI_D1/PSSI_D1, EVENTOUT                     | -                    |
| E1                           | 70           | 103          | C13           | 122          | D15              | F15           | 44     | 47       | 70      | 103     | F13      | 122     | C15         | PA11                                                       | I/O      | FT_u          | -     | TIM1_CH4, LPUART1_CTS,<br>SPI2_NSS/I2S2_WS, UART4_RX,<br>USART1_CTS/USART1_NSS,<br>FDCAN1_RX, USB_DM,<br>EVENTOUT                         | -                    |
| C1                           | 71           | 104          | B13           | 123          | C15              | F14           | 45     | 48       | 71      | 104     | E13      | 123     | B15         | PA12                                                       | I/O      | FT_u          | -     | TIM1_ETR,<br>LPUART1_RTS/LPUART1_DE,<br>SPI2_SCK/I2S2_CK, UART4_TX,<br>USART1_RTS/USART1_DE,<br>SAI2_FS_B, FDCAN1_TX,<br>USB_DP, EVENTOUT | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                      | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                          |                      |
| F4                           | 72           | 105          | D12           | 124          | E13              | F12           | 46     | 49      | 72      | 105     | E12      | 124     | A15         | PA13<br>(JTMS/SWDIO)                                       | I/O      | FT            | (7)   | JTMS/SWDIO, EVENTOUT                                                                     | -                    |
| -                            | 74           | 107          | E12           | 126          | D14              | -             | 47     | 50      | 74      | 107     | C12      | 126     | F12         | VSS                                                        | S        | -             | -     | -                                                                                        | -                    |
| -                            | 75           | 108          | D13           | 127          | E12              | -             | 48     | 51      | 75      | 108     | C13      | 127     | F13         | VDD                                                        | S        | -             | -     | -                                                                                        | -                    |
| B2                           | 73           | 106          | E13           | 125          | F12              | F11           | -      | -       | 73      | 106     | D13      | 125     | H13         | VDDUSB                                                     | S        | -             | -     | -                                                                                        | -                    |
| -                            | -            | -            | C12           | 128          | B15              | E15           | -      | -       | -       | -       | D12      | 128     | E12         | PH13                                                       | I/O      | FT_h          | -     | LPTIM1_IN2, TIM8_CH1N,<br>UART8_TX, UART4_TX,<br>FDCAN1_TX, DCM1_D3/PSSI_D3,<br>EVENTOUT | -                    |
| -                            | -            | -            | D11           | 129          | D13              | E14           | -      | -       | -       | -       | D10      | 129     | E13         | PH14                                                       | I/O      | FT_h          | -     | TIM8_CH2N, UART4_RX,<br>FDCAN1_RX,<br>DCMI_D4/PSSI_D4, EVENTOUT                          | -                    |
| -                            | -            | -            | A13           | 130          | C14              | E13           | -      | -       | -       | -       | D11      | 130     | D13         | PH15                                                       | I/O      | FT_h          | -     | TIM8_CH3N,<br>DCMI_D11/PSSI_D11,<br>EVENTOUT                                             | -                    |
| -                            | -            | -            | B12           | 131          | -                | E12           | -      | -       | -       | -       | B13      | 131     | E14         | PI0                                                        | I/O      | FT_h          | -     | TIM5_CH4, SPI2_NSS/I2S2_WS,<br>DCMI_D13/PSSI_D13,<br>EVENTOUT                            | -                    |
| -                            | -            | -            | C11           | 132          | A15              | D15           | -      | -       | -       | -       | B12      | 132     | D14         | PI1                                                        | I/O      | FT_h          | -     | TIM8_BKIN2,<br>SPI2_SCK/I2S2_CK,<br>DCMI_D8/PSSI_D8, EVENTOUT                            | -                    |
| -                            | -            | -            | D10           | 133          | B14              | F10           | -      | -       | -       | -       | A13      | 133     | C14         | PI2                                                        | I/O      | FT_h          | -     | TIM8_CH4, SPI2_MISO/I2S2_SDI,<br>DCMI_D9/PSSI_D9, EVENTOUT                               | -                    |
| -                            | -            | -            | A12           | 134          | A14              | D14           | -      | -       | -       | -       | C11      | 134     | C13         | PI3                                                        | I/O      | FT_h          | -     | TIM8_ETR,<br>SPI2_MOSI/I2S2_SDO,<br>DCMI_D10/PSSI_D10,<br>EVENTOUT                       | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                                                 | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                                                     |                      |
| -                            | -            | -            | B8            | 135          | D9               | -             | -      | -        | -       | -       | B10      | 135     | D9          | VSS                                                        | S        | -             | -     | -                                                                                                                                                                                   | -                    |
| -                            | -            | -            | A8            | 136          | D8               | -             | -      | -        | -       | -       | A10      | 136     | C9          | VDD                                                        | S        | -             | -     | -                                                                                                                                                                                   | -                    |
| E3                           | 76           | 109          | C10           | 137          | B13              | C15           | 49     | 52       | 76      | 109     | A12      | 137     | A14         | PA14<br>(JTCK/SWCLK)                                       | I/O      | FT            | (7)   | JTCK/SWCLK, EVENTOUT                                                                                                                                                                | -                    |
| D4                           | 77           | 110          | B10           | 138          | C13              | C13           | 50     | 53       | 77      | 110     | B11      | 138     | A13         | PA15(JTDI)                                                 | I/O      | FT            | (7)   | JTDI, TIM2_CH1, LPTIM3_IN2,<br>HDMI_CEC, SPI1_NSS/I2S1_WS,<br>SPI3_NSS/I2S3_WS, SPI6_NSS,<br>UART4_RTS/UART4_DE,<br>UART7_TX, FMC_NBL1,<br>DCMI_D11/PSSI_D11, TIM2_ETR,<br>EVENTOUT | -                    |
| C3                           | 78           | 111          | A10           | 139          | D12              | D12           | 51     | 54       | 78      | 111     | C10      | 139     | B14         | PC10                                                       | I/O      | FT_h          | -     | LPTIM3_ETR,<br>SPI3_SCK/I2S3_CK,<br>USART3_TX, UART4_TX,<br>OCTOSPI1_IO1,<br>ETH_MII_TXD0/ETH_RMII_TXD0,<br>SDMMC1_D2,<br>DCMI_D8/PSSI_D8, EVENTOUT                                 | -                    |
| E5                           | 79           | 112          | A9            | 140          | C12              | B14           | 52     | 55       | 79      | 112     | A11      | 140     | B13         | PC11                                                       | I/O      | FT_h          | -     | LPTIM3_IN1,<br>SPI3_MISO/I2S3_SDI,<br>USART3_RX, UART4_RX,<br>OCTOSPI1_NCS, SDMMC1_D3,<br>DCMI_D4/PSSI_D4, EVENTOUT                                                                 | -                    |
| F6                           | 80           | 113          | D9            | 141          | C11              | B15           | 53     | 56       | 80      | 113     | B9       | 141     | A12         | PC12                                                       | I/O      | FT_h          | -     | TRACED3, TIM15_CH1,<br>SPI6_SCK,<br>SPI3_MOSI/I2S3_SDO,<br>USART3_CK, UART5_TX,<br>SDMMC1_CK,<br>DCMI_D9/PSSI_D9, EVENTOUT                                                          | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions | Additional functions                                                                                     |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|------------------------------------------------------------|----------|---------------|-------|---------------------|----------------------------------------------------------------------------------------------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFPFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25                                                |          |               |       |                     |                                                                                                          |
| -                            | -            | -            | B11           | -            | D11              | -             | -      | -        | -       | -       | -        | -       | -                                                          | VSS      | S             | -     | -                   | -                                                                                                        |
| -                            | -            | -            | A11           | -            | D10              | -             | -      | -        | -       | -       | -        | -       | -                                                          | VDD      | S             | -     | -                   | -                                                                                                        |
| A3                           | 81           | 114          | C9            | 142          | B12              | E10           | -      | -        | 81      | 114     | D9       | 142     | B12                                                        | PD0      | I/O           | FT_h  | -                   | TIM8_CH4N, UART4_RX,<br>FDCAN1_RX, UART9_CTS,<br>FMC_D2/FMC_AD2, EVENTOUT                                |
| B4                           | 82           | 115          | B9            | 143          | A13              | C12           | -      | -        | 82      | 115     | E9       | 143     | C12                                                        | PD1      | I/O           | FT_h  | -                   | UART4_TX, FDCAN1_TX,<br>FMC_D3/FMC_AD3, EVENTOUT                                                         |
| A5                           | 83           | 116          | E8            | 144          | C10              | D11           | 54     | -        | 83      | 116     | C9       | 144     | D12                                                        | PD2      | I/O           | FT_h  | -                   | TRACED2, TIM3_ETR,<br>TIM15_BKIN, UART5_RX,<br>SDMMC1_CMD,<br>DCMI_D11/PSSI_D11,<br>LPTIM4_ETR, EVENTOUT |
| -                            | 84           | 117          | C8            | 145          | A12              | A14           | -      | -        | 84      | 117     | A9       | 145     | D11                                                        | PD3      | I/O           | FT_h  | -                   | SPI2_SCK/I2S2_CK,<br>USART2_CTS/USART2_NSS,<br>FMC_CLK, DCMI_D5/PSSI_D5,<br>EVENTOUT                     |
| -                            | 85           | 118          | D8            | 146          | B11              | B13           | -      | -        | 85      | 118     | F8       | 146     | D10                                                        | PD4      | I/O           | FT_h  | -                   | USART2_RTS/USART2_DE,<br>OCTOSPI1_IO4, FMC_NOE,<br>EVENTOUT                                              |
| -                            | 86           | 119          | A7            | 147          | A11              | B12           | -      | -        | 86      | 119     | D8       | 147     | C11                                                        | PD5      | I/O           | FT_h  | -                   | TIM1_CH4N, SPI2_RDY,<br>USART2_TX, FDCAN1_TX,<br>OCTOSPI1_IO5, FMC_NWE,<br>EVENTOUT                      |
| -                            | -            | 120          | -             | 148          | -                | -             | -      | -        | -       | 120     | B7       | 148     | D8                                                         | VSS      | S             | -     | -                   | -                                                                                                        |
| -                            | -            | 121          | A6            | 149          | D7               | D7            | -      | -        | -       | 121     | A7       | 149     | C8                                                         | VDDIO2   | S             | -     | -                   | -                                                                                                        |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                     | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                         |                      |
| -                            | 87           | 122          | F7            | 150          | B10              | A10           | -      | -       | 87      | 122     | E8       | 150     | B11         | PD6                                                        | I/O      | FT_sh         | -     | SAI1_D1, SPI3_MOSI/I2S3_SDO,<br>SAI1_SD_A, USART2_RX,<br>OCTOSPI1_IO6, SDMMC2_CK,<br>FMC_NWAIT,<br>DCMI_D10/PSSI_D10,<br>EVENTOUT                       | -                    |
| -                            | 88           | 123          | B7            | 151          | A10              | C9            | -      | -       | 88      | 123     | B8       | 151     | A11         | PD7                                                        | I/O      | FT_sh         | -     | SPI1_MOSI/I2S1_SDO,<br>USART2_CK, OCTOSPI1_IO7,<br>SDMMC2_CMD,<br>FMC_NE1/FMC_NCE,<br>LPTIM4_OUT, EVENTOUT                                              | -                    |
| -                            | -            | -            | -             | -            | D6               | -             | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                                                                                                                                                       | -                    |
| -                            | -            | 124          | E7            | 152          | B9               | B9            | -      | -       | -       | 124     | F7       | 152     | C10         | PG9                                                        | I/O      | FT_sh         | -     | SPI1_MISO/I2S1_SDI,<br>USART6_RX, OCTOSPI1_IO6,<br>SAI2_FS_B, SDMMC2_D0,<br>FMC_NE2/FMC_NCE,<br>DCMI_VSYNC/PSSI_RDY,<br>EVENTOUT                        | -                    |
| -                            | -            | 125          | C7            | 153          | A9               | A9            | -      | -       | -       | 125     | A8       | 153     | B10         | PG10                                                       | I/O      | FT_sh         | -     | SPI1_NSS/I2S1_WS, SAI2_SD_B,<br>SDMMC2_D1, FMC_NE3,<br>DCMI_D2/PSSI_D2, EVENTOUT                                                                        | -                    |
| -                            | -            | -            | -             | 154          | C9               | D8            | -      | -       | -       | 126     | E7       | 154     | B9          | PG11                                                       | I/O      | FT_sh         | -     | LPTIM1_IN2, SPI1_SCK/I2S1_CK,<br>USART10_RX,<br>USART11_RTS/USART11_DE,<br>SDMMC2_D2,<br>ETH_MII_TX_EN/ETH_RMII_TX_<br>EN, DCMI_D3/PSSI_D3,<br>EVENTOUT | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                                                    | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                                                        |                      |
| -                            | -            | 126          | D7            | 155          | B8               | C8            | -      | -       | -       | 127     | C8       | 155     | B8          | PG12                                                       | I/O      | FT_sh         | -     | LPTIM1_IN1, PSSI_D15,<br>SPI6_MISO, USART10_TX,<br>USART6_RTS/USART6_DE,<br>SDMMC2_D3,<br>ETH_MII_TXD1/ETH_RMII_TXD1,<br>FMC_NE4, DCMI_D11/PSSI_D11,<br>LPTIM5_CH1, EVENTOUT           | -                    |
| -                            | -            | 127          | -             | 156          | C8               | B8            | -      | -       | -       | 128     | D7       | 156     | A8          | PG13                                                       | I/O      | FT_sh         | -     | TRACED0, LPTIM1_CH1,<br>SPI6_SCK,<br>USART10_CTS/USART10_NSS,<br>USART6_CTS/USART6_NSS,<br>SDMMC2_D6,<br>ETH_MII_TXD0/ETH_RMII_TXD0,<br>FMC_A24, LPTIM5_CH2,<br>EVENTOUT               | -                    |
| -                            | -            | 128          | -             | 157          | A8               | A8            | -      | -       | -       | 129     | C7       | 157     | A7          | PG14                                                       | I/O      | FT_sh         | -     | TRACED1, LPTIM1_ETR,<br>LPTIM1_CH2, SPI6_MOSI,<br>USART10_RTS/USART10_DE,<br>USART6_TX, OCTOSPI1_IO7,<br>SDMMC2_D7,<br>ETH_MII_TXD1/ETH_RMII_TXD1,<br>FMC_A25, LPTIM5_IN1,<br>EVENTOUT | -                    |
| -                            | -            | 129          | B4            | 158          | -                | -             | -      | -       | -       | 130     | -        | 158     | D7          | VSS                                                        | S        | -             | -     | -                                                                                                                                                                                      | -                    |
| -                            | -            | 130          | A3            | 159          | -                | -             | -      | -       | -       | 131     | -        | 159     | C7          | VDD                                                        | S        | -             | -     | -                                                                                                                                                                                      | -                    |
| -                            | -            | 131          | B6            | 160          | A7               | A7            | -      | -       | -       | 132     | B6       | 160     | B7          | PG15                                                       | I/O      | FT_h          | -     | SPI4_RDY, USART10_CK,<br>USART6_CTS/USART6_NSS,<br>FMC_NCAS,<br>DCMI_D13/PSSI_D13,<br>EVENTOUT                                                                                         | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                                                                             | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                                                                                 |                      |
| C5                           | 89           | 132          | F6            | 161          | B7               | B7            | 55     | 57      | 89      | 133     | E6       | 161     | A10         | PB3(JTDO/<br>TRACESWO)                                     | I/O      | FT_fh         | -     | JTDO/TRACESWO, TIM2_CH2,<br>I2C2_SDA, SPI1_SCK/I2S1_CK,<br>SPI3_SCK/I2S3_CK,<br>UART12_CTS/UART12_NSS,<br>SPI6_SCK, SDMMC2_D2,<br>CRS_SYNC, UART7_RX,<br>LPTIM6_ETR, EVENTOUT                                   | -                    |
| B6                           | 90           | 133          | A5            | 162          | C7               | C7            | 56     | 58      | 90      | 134     | A6       | 162     | A9          | PB4(NJTRST)                                                | I/O      | FT_h          | -     | NJTRST, TIM16_BKIN,<br>TIM3_CH1, OCTOSPI1_CLK,<br>LPTIM1_CH2,<br>SPI1_MISO/I2S1_SDI,<br>SPI3_MISO/I2S3_SDI,<br>SPI2_NSS/I2S2_WS, SPI6_MISO,<br>SDMMC2_D3, UART7_TX,<br>DCMI_D7/PSSI_D7, EVENTOUT                | -                    |
| D6                           | 91           | 134          | E6            | 163          | A6               | E7            | 57     | 59      | 91      | 135     | C6       | 163     | A6          | PB5                                                        | I/O      | FT_h          | -     | TIM17_BKIN, TIM3_CH2,<br>OCTOSPI1_NCLK, I2C1_SMBA,<br>SPI1_MOSI/I2S1_SDO,<br>I2C4_SMBA,<br>SPI3_MOSI/I2S3_SDO,<br>SPI6_MOSI, FDCAN2_RX,<br>ETH_PPS_OUT, FMC_SDCKE1,<br>DCMI_D10/PSSI_D10,<br>UART5_RX, EVENTOUT | -                    |
| E7                           | 92           | 135          | C6            | 164          | B6               | E8            | 58     | 60      | 92      | 136     | A5       | 164     | B6          | PB6                                                        | I/O      | FT_f          | -     | TIM16_CH1N, TIM4_CH1,<br>I3C1_SCL, I2C1_SCL,<br>HDMI_CEC, I2C4_SCL,<br>USART1_TX, LPUART1_TX,<br>FDCAN2_TX, OCTOSPI1_NCS,<br>FMC_SDNE1,<br>DCMI_D5/PSSI_D5, UART5_TX,<br>EVENTOUT                               | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |          |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                                                   | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|----------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VFQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                                                                                                                                       |                      |
| C7                           | 93           | 136          | D6            | 165          | C6               | A6            | 59     | 61       | 93      | 137     | D6       | 165     | B5          | PB7                                                        | I/O      | FT_fa         | -     | TIM17_CH1N, TIM4_CH2,<br>I3C1_SDA, I2C1_SDA,<br>I2C4_SDA, USART1_RX,<br>LPUART1_RX, FDCAN1_TX,<br>SDMMC2_D5, SDMMC2_CKIN,<br>FMC_NL,<br>DCMI_VSYNC/PSSI_RDY,<br>EVENTOUT              | WKUP5                |
| D8                           | 94           | 137          | B5            | 166          | A5               | B6            | 60     | 62       | 94      | 138     | B5       | 166     | D6          | BOOT0                                                      | I        | B             | -     | -                                                                                                                                                                                     | -                    |
| E9                           | 95           | 138          | F5            | 167          | B5               | C6            | 61     | 63       | 95      | 139     | E5       | 167     | A5          | PB8                                                        | I/O      | FT_fhs        | -     | TIM16_CH1, TIM4_CH3,<br>I3C1_SCL, I2C1_SCL, SPI4_RDY,<br>I2C4_SCL, SDMMC1_CKIN,<br>UART4_RX, FDCAN1_RX,<br>SDMMC2_D4, ETH_MII_TXD3,<br>SDMMC1_D4,<br>DCMI_D6/PSSI_D6, EVENTOUT        | -                    |
| -                            | 96           | 139          | E5            | 168          | A4               | A5            | -      | 64       | 96      | 140     | A4       | 168     | B4          | PB9                                                        | I/O      | FT_fhs        | -     | TIM17_CH1, TIM4_CH4,<br>I3C1_SDA, I2C1_SDA,<br>SPI2_NSS/I2S2_WS, I2C4_SDA,<br>SDMMC1_CDIR, UART4_TX,<br>FDCAN1_TX, SDMMC2_D5,<br>SDMMC2_CKIN, SDMMC1_D5,<br>DCMI_D7/PSSI_D7, EVENTOUT | -                    |
| -                            | 97           | 140          | D5            | 169          | C5               | D6            | -      | 65       | 97      | 141     | C5       | 169     | A4          | PE0                                                        | I/O      | FT_h          | -     | LPTIM1_ETR, TIM4_ETR,<br>LPTIM2_CH2, LPTIM2_ETR,<br>SPI3_RDY, UART8_RX,<br>FDCAN1_RX, SAI2_MCLK_A,<br>FMC_NBL0, DCMI_D2/PSSI_D2,<br>EVENTOUT                                          | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                        | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|----------------------------------------------------------------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                                                                            |                      |
| -                            | -            | 141          | C5            | 170          | B4               | B5            | -      | -       | -       | -       | D5       | 170     | A3          | PE1                                                        | I/O      | FT_h          | -     | LPTIM1_IN2, UART8_TX,<br>FDCAN1_TX, FMC_NBL1,<br>DCMI_D3/PSSI_D3, EVENTOUT | -                    |
| A9                           | 98           | 142          | A4            | 171          | A3               | E6            | 62     | 66      | 98      | 142     | B4       | 171     | C6          | VCAP                                                       | S        | -             | -     | -                                                                          | -                    |
| -                            | 99           | 143          | -             | -            | -                | -             | 63     | 67      | 99      | 143     | B3       | -       | -           | VSS                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | 100          | 144          | -             | 172          | -                | -             | 64     | 68      | 100     | 144     | A3       | 172     | -           | VDD                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | -            | -            | C4            | 173          | B3               | C5            | -      | -       | -       | -       | C4       | 173     | D4          | PI4                                                        | I/O      | FT_h          | -     | TIM8_BKIN, SPI2_RDY,<br>SAI2_MCLK_A,<br>DCMI_D5/PSSI_D5, EVENTOUT          | -                    |
| -                            | -            | -            | B3            | 174          | A2               | A4            | -      | -       | -       | -       | -        | 174     | C4          | PI5                                                        | I/O      | FT_h          | -     | TIM8_CH1, SAI2_SCK_A,<br>DCMI_VSYNC/PSSI_RDY,<br>EVENTOUT                  | -                    |
| -                            | -            | -            | A2            | 175          | C4               | A3            | -      | -       | -       | -       | C3       | 175     | C3          | PI6                                                        | I/O      | FT_h          | -     | TIM8_CH2, SAI2_SD_A,<br>DCMI_D6/PSSI_D6, EVENTOUT                          | -                    |
| -                            | -            | -            | A1            | 176          | A1               | B4            | -      | -       | -       | -       | A2       | 176     | C2          | PI7                                                        | I/O      | FT_h          | -     | TIM8_CH3, SAI2_FS_A,<br>DCMI_D7/PSSI_D7, EVENTOUT                          | -                    |
| -                            | -            | -            | -             | -            | F6               | L11           | -      | -       | -       | -       | -        | -       | F6          | VSS                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | -            | -            | -             | -            | F7               | R1            | -      | -       | -       | -       | -        | -       | F7          | VSS                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | -            | -            | -             | -            | F8               | A15           | -      | -       | -       | -       | -        | -       | F8          | VSS                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | -            | -            | -             | -            | F9               | E11           | -      | -       | -       | -       | -        | -       | F9          | VSS                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | -            | -            | -             | -            | F10              | G12           | -      | -       | -       | -       | -        | -       | F10         | VSS                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | -            | -            | -             | -            | G6               | H10           | -      | -       | -       | -       | -        | -       | G6          | VSS                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | -            | -            | -             | -            | G7               | G15           | -      | -       | -       | -       | -        | -       | G7          | VSS                                                        | S        | -             | -     | -                                                                          | -                    |
| -                            | -            | -            | -             | -            | G8               | A2            | -      | -       | -       | -       | -        | -       | G8          | VSS                                                        | S        | -             | -     | -                                                                          | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|---------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                     |                      |
| -                            | -            | -            | -             | -            | G9               | A11           | -      | -       | -       | -       | -        | -       | G9          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | G10              | A12           | -      | -       | -       | -       | -        | -       | G10         | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | H6               | A13           | -      | -       | -       | -       | -        | -       | H6          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | H7               | B1            | -      | -       | -       | -       | -        | -       | H7          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | H8               | B2            | -      | -       | -       | -       | -        | -       | H8          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | H9               | B10           | -      | -       | -       | -       | -        | -       | H9          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | H10              | B11           | -      | -       | -       | -       | -        | -       | H10         | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | J6               | C2            | -      | -       | -       | -       | -        | -       | J6          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | J7               | C10           | -      | -       | -       | -       | -        | -       | J7          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | J8               | C11           | -      | -       | -       | -       | -        | -       | J8          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | J9               | C14           | -      | -       | -       | -       | -        | -       | J9          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | J10              | D9            | -      | -       | -       | -       | -        | -       | J10         | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | K6               | D10           | -      | -       | -       | -       | -        | -       | K6          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | K7               | D13           | -      | -       | -       | -       | -        | -       | K7          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | K8               | E9            | -      | -       | -       | -       | -        | -       | K8          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | K9               | F1            | -      | -       | -       | -       | -        | -       | K9          | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | K10              | F4            | -      | -       | -       | -       | -        | -       | K10         | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | F5            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | G2            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | G3            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |



Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|---------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                     |                      |
| -                            | -            | -            | -             | -            | -                | G5            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | M6            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | M15           | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | H12           | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | H15           | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | K13           | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | L14           | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | N5            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | N6            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | N9            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | P5            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | P8            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | P9            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | R4            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | R5            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | R8            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | R9            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | G8            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | H7            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | H8            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | H9            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |

Table 14. STM32H562xx and STM32H563xx pin/ball definition (continued)

| Pin number <sup>(1)(2)</sup> |              |              |               |              |                  |               |        |         |         |         |          |         |             | Pin name<br>(function<br>after<br>reset) <sup>(3)(4)</sup> | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|------------------------------|--------------|--------------|---------------|--------------|------------------|---------------|--------|---------|---------|---------|----------|---------|-------------|------------------------------------------------------------|----------|---------------|-------|---------------------|----------------------|
| WLCSP80 SMPS                 | LQFP100 SMPS | LQFP144 SMPS | UFBGA169 SMPS | LQFP176 SMPS | UFBGA176+25 SMPS | TFBGA225 SMPS | LQFP64 | VQFPN68 | LQFP100 | LQFP144 | UFBGA169 | LQFP176 | UFBGA176+25 |                                                            |          |               |       |                     |                      |
| -                            | -            | -            | -             | -            | -                | J8            | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | R15           | -      | -       | -       | -       | -        | -       | -           | VSS                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | F9            | -      | -       | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | G6            | -      | -       | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | J10           | -      | -       | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | G7            | -      | -       | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | G9            | -      | -       | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | J7            | -      | -       | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                   | -                    |
| -                            | -            | -            | -             | -            | -                | J9            | -      | -       | -       | -       | -        | -       | -           | VDD                                                        | S        | -             | -     | -                   | -                    |

1. The devices with SMPS correspond to commercial codes STM32H563xlxxQ.
2. A non-connected I/O in a given package is configured as an output tied to VSS. When VREF+ pad is not available on a package, the internal voltage reference buffer (VREFBUF) is not available and must be kept disabled.
3. PC13, PC14, and PC15 are supplied through the power switch (by VSW). This switch sinks a limited amount of current, hence the use of PC13 to PC15 GPIOs in output mode is limited: The speed must not exceed 2 MHz with a maximum load of 30 pF. These GPIOs must not be used as current sources (for example to drive a LED).
4. After a Backup domain power-up, PC13, PC14, and PC15 operate as GPIOs. Their function depends upon the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the backup domain and RTC register descriptions in the product reference manual.
5. As a tamper input, only PC13, PI8, PA0, PA1, and PA2 are functional in Standby and VBAT mode. As a tamper output, only PC13, PA1, and PI8 are functional in Standby and VBAT mode.
6. For the output timing characteristics refer to [Table 67](#).
7. After reset, these pins are configured as JTAG/SW debug alternate functions. The internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated too.



## 4.3 Alternate functions

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup>

| Port |      | AF0        | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                            |
|------|------|------------|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------------------------------------------------------------|
|      |      | SYS        | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART11/2/3/6/<br>10/11 |
| A    | PA0  | -          | TIM2_CH1                | TIM5_CH1                               | TIM8_ETR                                     | TIM15_BKIN                                                          | SPI6_NSS                                                       | SPI3_RDY                                                                 | USART2_CTS/<br>USART2_NSS                                                      |
|      | PA1  | -          | TIM2_CH2                | TIM5_CH2                               | -                                            | TIM15_CH1N                                                          | LPTIM1_IN1                                                     | OCTOSPI1_DQS                                                             | USART2_RTS/<br>USART2_DE                                                       |
|      | PA2  | -          | TIM2_CH3                | TIM5_CH3                               | -                                            | TIM15_CH1                                                           | LPTIM1_IN2                                                     | -                                                                        | USART2_TX                                                                      |
|      | PA3  | -          | TIM2_CH4                | TIM5_CH4                               | OCTOSPI1_CLK                                 | TIM15_CH2                                                           | SPI2_NSS/I2S2_WS                                               | SAI1_SD_B                                                                | USART2_RX                                                                      |
|      | PA4  | -          | -                       | TIM5_ETR                               | LPTIM2_CH1                                   | -                                                                   | SPI1_NSS/I2S1_WS                                               | SPI3_NSS/<br>I2S3_WS                                                     | USART2_CK                                                                      |
|      | PA5  | -          | TIM2_CH1                | -                                      | TIM8_CH1N                                    | -                                                                   | SPI1_SCK/I2S1_CK                                               | -                                                                        | -                                                                              |
|      | PA6  | -          | TIM1_BKIN               | TIM3_CH1                               | TIM8_BKIN                                    | -                                                                   | SPI1_MISO/I2S1_SDI                                             | OCTOSPI1_IO3                                                             | USART11_TX                                                                     |
|      | PA7  | -          | TIM1_CH1N               | TIM3_CH2                               | TIM8_CH1N                                    | -                                                                   | SPI1_MOSI/I2S1_SDO                                             | -                                                                        | USART11_RX                                                                     |
|      | PA8  | MCO1       | TIM1_CH1                | -                                      | TIM8_BKIN2                                   | I2C3_SCL                                                            | SPI1_RDY                                                       | -                                                                        | USART1_CK                                                                      |
|      | PA9  | -          | TIM1_CH2                | -                                      | LPUART1_TX                                   | I2C3_SMBA                                                           | SPI2_SCK/I2S2_CK                                               | -                                                                        | USART1_TX                                                                      |
|      | PA10 | -          | TIM1_CH3                | -                                      | LPUART1_RX                                   | LPTIM2_IN2                                                          | -                                                              | UCPD1_FRSTX                                                              | USART1_RX                                                                      |
|      | PA11 | -          | TIM1_CH4                | -                                      | LPUART1_CTS                                  | -                                                                   | SPI2_NSS/I2S2_WS                                               | UART4_RX                                                                 | USART1_CTS/<br>USART1_NSS                                                      |
|      | PA12 | -          | TIM1_ETR                | -                                      | LPUART1_RTS/<br>LPUART1_DE                   | -                                                                   | SPI2_SCK/I2S2_CK                                               | UART4_TX                                                                 | USART1_RTS/<br>USART1_DE                                                       |
|      | PA13 | JTMS/SWDIO | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                              |
|      | PA14 | JTCK/SWCLK | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                              |
|      | PA15 | JTDI       | TIM2_CH1                | LPTIM3_IN2                             | -                                            | HDMI_CEC                                                            | SPI1_NSS/I2S1_WS                                               | SPI3_NSS/<br>I2S3_WS                                                     | SPI6_NSS                                                                       |

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup> (continued)

| Port |      | AF0               | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                            |
|------|------|-------------------|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------------------------------------------------------------|
|      |      | SYS               | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART11/2/3/6/<br>10/11 |
| B    | PB0  | -                 | TIM1_CH2N               | TIM3_CH3                               | TIM8_CH2N                                    | -                                                                   | -                                                              | OCTOSPI1_IO1                                                             | USART11_CK                                                                     |
|      | PB1  | -                 | TIM1_CH3N               | TIM3_CH4                               | TIM8_CH3N                                    | -                                                                   | -                                                              | OCTOSPI1_IO0                                                             | -                                                                              |
|      | PB2  | RTC_OUT2          | -                       | SAI1_D1                                | TIM8_CH4N                                    | SPI1_RDY                                                            | LPTIM1_CH1                                                     | SAI1_SD_A                                                                | SPI3_MOSI/<br>I2S3_SDO                                                         |
|      | PB3  | JTDO/<br>TRACESWO | TIM2_CH2                | -                                      | -                                            | I2C2_SDA                                                            | SPI1_SCK/I2S1_CK                                               | SPI3_SCK/<br>I2S3_CK                                                     | UART12_CTS/<br>UART12_NSS                                                      |
|      | PB4  | NJTRST            | TIM16_BKIN              | TIM3_CH1                               | OCTOSPI1_CLK                                 | LPTIM1_CH2                                                          | SPI1_MISO/I2S1_SDI                                             | SPI3_MISO/<br>I2S3_SDI                                                   | SPI2_NSS/<br>I2S2_WS                                                           |
|      | PB5  | -                 | TIM17_BKIN              | TIM3_CH2                               | OCTOSPI1_NCLK                                | I2C1_SMBA                                                           | SPI1_MOSI/I2S1_SDO                                             | I2C4_SMBA                                                                | SPI3_MOSI/<br>I2S3_SDO                                                         |
|      | PB6  | -                 | TIM16_CH1N              | TIM4_CH1                               | I3C1_SCL                                     | I2C1_SCL                                                            | HDMI_CEC                                                       | I2C4_SCL                                                                 | USART1_TX                                                                      |
|      | PB7  | -                 | TIM17_CH1N              | TIM4_CH2                               | I3C1_SDA                                     | I2C1_SDA                                                            | -                                                              | I2C4_SDA                                                                 | USART1_RX                                                                      |
|      | PB8  | -                 | TIM16_CH1               | TIM4_CH3                               | I3C1_SCL                                     | I2C1_SCL                                                            | SPI4_RDY                                                       | I2C4_SCL                                                                 | SDMMC1_CKIN                                                                    |
|      | PB9  | -                 | TIM17_CH1               | TIM4_CH4                               | I3C1_SDA                                     | I2C1_SDA                                                            | SPI2_NSS/I2S2_WS                                               | I2C4_SDA                                                                 | SDMMC1_CDIR                                                                    |
|      | PB10 | -                 | TIM2_CH3                | LPTIM3_CH1                             | LPTIM2_IN1                                   | I2C2_SCL                                                            | SPI2_SCK/I2S2_CK                                               | -                                                                        | USART3_TX                                                                      |
|      | PB11 | -                 | TIM2_CH4                | -                                      | LPTIM2_ETR                                   | I2C2_SDA                                                            | SPI2_RDY                                                       | SPI4_RDY                                                                 | USART3_RX                                                                      |
|      | PB12 | -                 | TIM1_BKIN               | -                                      | OCTOSPI1_NCLK                                | I2C2_SDA                                                            | SPI2_NSS/I2S2_WS                                               | UCPD1_FRSTX                                                              | USART3_CK                                                                      |
|      | PB13 | -                 | TIM1_CH1N               | LPTIM3_IN1                             | LPTIM2_CH1                                   | I2C2_SMBA                                                           | SPI2_SCK/I2S2_CK                                               | -                                                                        | USART3_CTS/<br>USART3_NSS                                                      |
|      | PB14 | -                 | TIM1_CH2N               | TIM12_CH1                              | TIM8_CH2N                                    | USART1_TX                                                           | SPI2_MISO/I2S2_SDI                                             | -                                                                        | USART3_RTS/<br>USART3_DE                                                       |
|      | PB15 | RTC_REFIN         | TIM1_CH3N               | TIM12_CH2                              | TIM8_CH3N                                    | USART1_RX                                                           | SPI2_MOSI/I2S2_SDO                                             | -                                                                        | USART11_CTS/<br>USART11_NSS                                                    |

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup> (continued)

| Port |      | AF0        | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                           |
|------|------|------------|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|      |      | SYS        | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART1/2/3/6/<br>10/11 |
| C    | PC0  | -          | TIM16_BKIN              | -                                      | -                                            | -                                                                   | -                                                              | SAI1_MCLK_A                                                              | SPI2_RDY                                                                      |
|      | PC1  | TRACED0    | -                       | SAI1_D1                                | -                                            | -                                                                   | SPI2_MOSI/I2S2_SDO                                             | SAI1_SD_A                                                                | USART11_RTS/<br>USART11_DE                                                    |
|      | PC2  | PWR_CSLEEP | TIM17_CH1               | TIM4_CH4                               | -                                            | -                                                                   | SPI2_MISO/I2S2_SDI                                             | OCTOSPI1_IO5                                                             | -                                                                             |
|      | PC3  | PWR_CSTOP  | -                       | SAI1_D3                                | LPTIM3_CH1                                   | -                                                                   | SPI2_MOSI/I2S2_SDO                                             | OCTOSPI1_IO6                                                             | -                                                                             |
|      | PC4  | -          | TIM2_CH4                | SAI1_CK1                               | LPTIM2_ETR                                   | -                                                                   | I2S1_MCK                                                       | -                                                                        | USART3_RX                                                                     |
|      | PC5  | -          | TIM1_CH4N               | SAI1_D3                                | -                                            | PSSI_D15                                                            | -                                                              | SAI1_FS_A                                                                | UART12_RTS/<br>UART12_DE                                                      |
|      | PC6  | -          | -                       | TIM3_CH1                               | TIM8_CH1                                     | -                                                                   | I2S2_MCK                                                       | SAI1_SCK_A                                                               | USART6_TX                                                                     |
|      | PC7  | TRGIO      | -                       | TIM3_CH2                               | TIM8_CH2                                     | -                                                                   | -                                                              | I2S3_MCK                                                                 | USART6_RX                                                                     |
|      | PC8  | TRACED1    | -                       | TIM3_CH3                               | TIM8_CH3                                     | -                                                                   | -                                                              | -                                                                        | USART6_CK                                                                     |
|      | PC9  | MCO2       | -                       | TIM3_CH4                               | TIM8_CH4                                     | I2C3_SDA                                                            | AUDIOCLK                                                       | -                                                                        | -                                                                             |
|      | PC10 | -          | -                       | LPTIM3_ETR                             | -                                            | -                                                                   | -                                                              | SPI3_SCK/<br>I2S3_CK                                                     | USART3_TX                                                                     |
|      | PC11 | -          | -                       | LPTIM3_IN1                             | -                                            | -                                                                   | -                                                              | SPI3_MISO/<br>I2S3_SDI                                                   | USART3_RX                                                                     |
|      | PC12 | TRACED3    | -                       | TIM15_CH1                              | -                                            | -                                                                   | SPI6_SCK                                                       | SPI3_MOSI/<br>I2S3_SDO                                                   | USART3_CK                                                                     |
|      | PC13 | -          | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PC14 | -          | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PC15 | -          | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup> (continued)

| Port |      | AF0     | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                           |
|------|------|---------|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|      |      | SYS     | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART1/2/3/6/<br>10/11 |
| D    | PD0  | -       | -                       | -                                      | TIM8_CH4N                                    | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PD1  | -       | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PD2  | TRACED2 | -                       | TIM3_ETR                               | -                                            | TIM15_BKIN                                                          | -                                                              | -                                                                        | -                                                                             |
|      | PD3  | -       | -                       | -                                      | -                                            | -                                                                   | SPI2_SCK/I2S2_CK                                               | -                                                                        | USART2_CTS/<br>USART2_NSS                                                     |
|      | PD4  | -       | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | USART2_RTS/<br>USART2_DE                                                      |
|      | PD5  | -       | TIM1_CH4N               | -                                      | -                                            | -                                                                   | SPI2_RDY                                                       | -                                                                        | USART2_TX                                                                     |
|      | PD6  | -       | -                       | SAI1_D1                                | -                                            | -                                                                   | SPI3_MOSI/I2S3_SDO                                             | SAI1_SD_A                                                                | USART2_RX                                                                     |
|      | PD7  | -       | -                       | -                                      | -                                            | -                                                                   | SPI1_MOSI/I2S1_SDO                                             | -                                                                        | USART2_CK                                                                     |
|      | PD8  | -       | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | USART3_TX                                                                     |
|      | PD9  | -       | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | USART3_RX                                                                     |
|      | PD10 | -       | -                       | -                                      | LPTIM2_CH2                                   | -                                                                   | -                                                              | -                                                                        | USART3_CK                                                                     |
|      | PD11 | -       | -                       | SAI1_CK1                               | LPTIM2_IN2                                   | I2C4_SMBA                                                           | -                                                              | -                                                                        | USART3_CTS/<br>USART3_NSS                                                     |
|      | PD12 | -       | LPTIM1_IN1              | TIM4_CH1                               | LPTIM2_IN1                                   | I2C4_SCL                                                            | I3C1_SCL                                                       | SAI1_D1                                                                  | USART3_RTS/<br>USART3_DE                                                      |
|      | PD13 | -       | LPTIM1_CH1              | TIM4_CH2                               | LPTIM2_CH1                                   | I2C4_SDA                                                            | I3C1_SDA                                                       | -                                                                        | -                                                                             |
|      | PD14 | -       | -                       | TIM4_CH3                               | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PD15 | -       | -                       | TIM4_CH4                               | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup> (continued)

| Port |      | AF0      | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                           |
|------|------|----------|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|      |      | SYS      | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART1/2/3/6/<br>10/11 |
| E    | PE0  | -        | LPTIM1_ETR              | TIM4_ETR                               | LPTIM2_CH2                                   | LPTIM2_ETR                                                          | -                                                              | SPI3_RDY                                                                 | -                                                                             |
|      | PE1  | -        | LPTIM1_IN2              | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PE2  | TRACECLK | LPTIM1_IN2              | SAI1_CK1                               | -                                            | -                                                                   | SPI4_SCK                                                       | SAI1_MCLK_A                                                              | USART10_RX                                                                    |
|      | PE3  | TRACED0  | -                       | -                                      | -                                            | TIM15_BKIN                                                          | -                                                              | SAI1_SD_B                                                                | USART10_TX                                                                    |
|      | PE4  | TRACED1  | -                       | SAI1_D2                                | -                                            | TIM15_CH1N                                                          | SPI4_NSS                                                       | SAI1_FS_A                                                                | -                                                                             |
|      | PE5  | TRACED2  | -                       | SAI1_CK2                               | -                                            | TIM15_CH1                                                           | SPI4_MISO                                                      | SAI1_SCK_A                                                               | -                                                                             |
|      | PE6  | TRACED3  | TIM1_BKIN2              | SAI1_D1                                | -                                            | TIM15_CH2                                                           | SPI4_MOSI                                                      | SAI1_SD_A                                                                | -                                                                             |
|      | PE7  | -        | TIM1_ETR                | -                                      | -                                            | -                                                                   | -                                                              | UART12_RTS/<br>UART12_DE                                                 | UART7_RX                                                                      |
|      | PE8  | -        | TIM1_CH1N               | -                                      | -                                            | -                                                                   | -                                                              | UART12_CTS/<br>UART12_NSS                                                | UART7_TX                                                                      |
|      | PE9  | -        | TIM1_CH1                | -                                      | -                                            | -                                                                   | -                                                              | UART12_RX                                                                | UART7_RTS/<br>UART7_DE                                                        |
|      | PE10 | -        | TIM1_CH2N               | -                                      | -                                            | -                                                                   | -                                                              | UART12_TX                                                                | UART7_CTS                                                                     |
|      | PE11 | -        | TIM1_CH2                | -                                      | -                                            | SPI1_RDY                                                            | SPI4_NSS                                                       | OCTOSPI1_NCS                                                             | -                                                                             |
|      | PE12 | -        | TIM1_CH3N               | -                                      | -                                            | -                                                                   | SPI4_SCK                                                       | -                                                                        | -                                                                             |
|      | PE13 | -        | TIM1_CH3                | -                                      | -                                            | -                                                                   | SPI4_MISO                                                      | -                                                                        | -                                                                             |
|      | PE14 | -        | TIM1_CH4                | -                                      | -                                            | -                                                                   | SPI4_MOSI                                                      | -                                                                        | -                                                                             |
|      | PE15 | -        | TIM1_BKIN               | -                                      | TIM1_CH4N                                    | -                                                                   | -                                                              | -                                                                        | USART10_CK                                                                    |

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup> (continued)

| Port |      | AF0 | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                           |
|------|------|-----|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|      |      | SYS | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART1/2/3/6/<br>10/11 |
| F    | PF0  | -   | -                       | -                                      | -                                            | I2C2_SDA                                                            | -                                                              | -                                                                        | -                                                                             |
|      | PF1  | -   | -                       | -                                      | -                                            | I2C2_SCL                                                            | -                                                              | -                                                                        | -                                                                             |
|      | PF2  | -   | -                       | LPTIM3_CH2                             | LPTIM3_IN2                                   | I2C2_SMBA                                                           | -                                                              | UART12_TX                                                                | USART11_CK                                                                    |
|      | PF3  | -   | -                       | LPTIM3_IN1                             | -                                            | -                                                                   | -                                                              | -                                                                        | USART11_TX                                                                    |
|      | PF4  | -   | -                       | LPTIM3_ETR                             | -                                            | -                                                                   | -                                                              | -                                                                        | USART11_RX                                                                    |
|      | PF5  | -   | -                       | LPTIM3_CH1                             | -                                            | I2C4_SCL                                                            | I3C1_SCL                                                       | UART12_RX                                                                | USART11_CTS/<br>USART11_NSS                                                   |
|      | PF6  | -   | TIM16_CH1               | -                                      | -                                            | -                                                                   | SPI5_NSS                                                       | SAI1_SD_B                                                                | UART7_RX                                                                      |
|      | PF7  | -   | TIM17_CH1               | -                                      | -                                            | -                                                                   | SPI5_SCK                                                       | SAI1_MCLK_B                                                              | UART7_TX                                                                      |
|      | PF8  | -   | TIM16_CH1N              | -                                      | -                                            | -                                                                   | SPI5_MISO                                                      | SAI1_SCK_B                                                               | UART7_RTS/<br>UART7_DE                                                        |
|      | PF9  | -   | TIM17_CH1N              | -                                      | -                                            | -                                                                   | SPI5_MOSI                                                      | SAI1_FS_B                                                                | UART7_CTS                                                                     |
|      | PF10 | -   | TIM16_BKIN              | SAI1_D3                                | -                                            | PSSI_D15                                                            | -                                                              | -                                                                        | -                                                                             |
|      | PF11 | -   | -                       | -                                      | -                                            | -                                                                   | SPI5_MOSI                                                      | -                                                                        | -                                                                             |
|      | PF12 | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PF13 | -   | -                       | -                                      | -                                            | I2C4_SMBA                                                           | -                                                              | -                                                                        | -                                                                             |
|      | PF14 | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PF15 | -   | -                       | -                                      | -                                            | I2C4_SDA                                                            | I3C1_SDA                                                       | -                                                                        | -                                                                             |

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup> (continued)

| Port |      | AF0     | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                           |
|------|------|---------|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|      |      | SYS     | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART1/2/3/6/<br>10/11 |
| G    | PG0  | -       | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PG1  | -       | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | SPI2_MOSI/<br>I2S2_SDO                                                        |
|      | PG2  | -       | -                       | -                                      | TIM8_BKIN                                    | -                                                                   | -                                                              | -                                                                        | UART12_RX                                                                     |
|      | PG3  | -       | -                       | -                                      | TIM8_BKIN2                                   | -                                                                   | -                                                              | -                                                                        | UART12_TX                                                                     |
|      | PG4  | -       | TIM1_BKIN2              | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PG5  | -       | TIM1_ETR                | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PG6  | -       | TIM17_BKIN              | -                                      | I3C1_SDA                                     | I2C4_SDA                                                            | SPI1_RDY                                                       | -                                                                        | -                                                                             |
|      | PG7  | -       | -                       | SAI1_CK2                               | I3C1_SCL                                     | I2C4_SCL                                                            | -                                                              | SAI1_MCLK_A                                                              | USART6_CK                                                                     |
|      | PG8  | -       | -                       | -                                      | TIM8_ETR                                     | -                                                                   | SPI6_NSS                                                       | -                                                                        | USART6_RTS/<br>USART6_DE                                                      |
|      | PG9  | -       | -                       | -                                      | -                                            | -                                                                   | SPI1_MISO/I2S1_SDI                                             | -                                                                        | USART6_RX                                                                     |
|      | PG10 | -       | -                       | -                                      | -                                            | -                                                                   | SPI1_NSS/I2S1_WS                                               | -                                                                        | -                                                                             |
|      | PG11 | -       | LPTIM1_IN2              | -                                      | -                                            | -                                                                   | SPI1_SCK/I2S1_CK                                               | USART10_RX                                                               | USART11_RTS/<br>USART11_DE                                                    |
|      | PG12 | -       | LPTIM1_IN1              | -                                      | -                                            | PSSI_D15                                                            | SPI6_MISO                                                      | USART10_TX                                                               | USART6_RTS/<br>USART6_DE                                                      |
|      | PG13 | TRACED0 | LPTIM1_CH1              | -                                      | -                                            | -                                                                   | SPI6_SCK                                                       | USART10_CTS/<br>USART10_NSS                                              | USART6_CTS/<br>USART6_NSS                                                     |
|      | PG14 | TRACED1 | LPTIM1_ETR              | -                                      | -                                            | LPTIM1_CH2                                                          | SPI6_MOSI                                                      | USART10_RTS/<br>USART10_DE                                               | USART6_TX                                                                     |
|      | PG15 | -       | -                       | -                                      | -                                            | -                                                                   | SPI4_RDY                                                       | USART10_CK                                                               | USART6_CTS/<br>USART6_NSS                                                     |

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup> (continued)

| Port |      | AF0 | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                           |
|------|------|-----|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|      |      | SYS | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART1/2/3/6/<br>10/11 |
| H    | PH0  | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PH1  | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PH2  | -   | LPTIM1_IN2              | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PH3  | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PH4  | -   | -                       | -                                      | -                                            | I2C2_SCL                                                            | SPI5_RDY                                                       | -                                                                        | SPI6_RDY                                                                      |
|      | PH5  | -   | -                       | -                                      | -                                            | I2C2_SDA                                                            | SPI5_NSS                                                       | -                                                                        | SPI6_RDY                                                                      |
|      | PH6  | -   | TIM1_CH3N               | TIM12_CH1                              | TIM8_CH1                                     | I2C2_SMBA                                                           | SPI5_SCK                                                       | -                                                                        | -                                                                             |
|      | PH7  | -   | TIM1_CH3                | -                                      | TIM8_CH1N                                    | I2C3_SCL                                                            | SPI5_MISO                                                      | -                                                                        | -                                                                             |
|      | PH8  | -   | TIM1_CH2N               | TIM5_ETR                               | TIM8_CH2                                     | I2C3_SDA                                                            | SPI5_MOSI                                                      | -                                                                        | -                                                                             |
|      | PH9  | -   | TIM1_CH2                | TIM12_CH2                              | TIM8_CH2N                                    | I2C3_SMBA                                                           | SPI5_NSS                                                       | -                                                                        | -                                                                             |
|      | PH10 | -   | TIM1_CH1N               | TIM5_CH1                               | TIM8_CH3                                     | I2C4_SMBA                                                           | SPI5_RDY                                                       | -                                                                        | -                                                                             |
|      | PH11 | -   | TIM1_CH1                | TIM5_CH2                               | TIM8_CH3N                                    | I2C4_SCL                                                            | I3C1_SCL                                                       | -                                                                        | -                                                                             |
|      | PH12 | -   | TIM1_BKIN               | TIM5_CH3                               | TIM8_BKIN                                    | I2C4_SDA                                                            | I3C1_SDA                                                       | -                                                                        | -                                                                             |
|      | PH13 | -   | LPTIM1_IN2              | -                                      | TIM8_CH1N                                    | -                                                                   | -                                                              | -                                                                        | UART8_TX                                                                      |
|      | PH14 | -   | -                       | -                                      | TIM8_CH2N                                    | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PH15 | -   | -                       | -                                      | TIM8_CH3N                                    | -                                                                   | -                                                              | -                                                                        | -                                                                             |

Table 15. Alternate functions AF0 to AF7<sup>(1)</sup> (continued)

| Port |      | AF0 | AF1                     | AF2                                    | AF3                                          | AF4                                                                 | AF5                                                            | AF6                                                                      | AF7                                                                           |
|------|------|-----|-------------------------|----------------------------------------|----------------------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|      |      | SYS | LPTIM1/<br>TIM1/2/16/17 | LPTIM3/<br>PDM_SAI1/<br>TIM3/4/5/12/15 | I3C1/LPTIM2/3/<br>LPUART1/<br>OCTOSPI/TIM1/8 | CEC/DCMI/<br>I2C1/2/3/4/<br>LPTIM1/2/SPI1/<br>I2S1/TIM15/<br>USART1 | CEC/I3C1/LPTIM1/<br>SPI1/I2S1/SPI2/I2S2/<br>SPI3/I2S3/SPI4/5/6 | I2C4/OCTOSPI/<br>SAI1/SPI3/I2S3/<br>SPI4/UART4/12/<br>USART10/<br>USB_PD | SDMMC1/SPI2/<br>I2S2/SPI3/I2S3/<br>SPI6/UART7/8/12<br>/USART1/2/3/6/<br>10/11 |
| I    | PI0  | -   | -                       | TIM5_CH4                               | -                                            | -                                                                   | SPI2_NSS/I2S2_WS                                               | -                                                                        | -                                                                             |
|      | PI1  | -   | -                       | -                                      | TIM8_BKIN2                                   | -                                                                   | SPI2_SCK/I2S2_CK                                               | -                                                                        | -                                                                             |
|      | PI2  | -   | -                       | -                                      | TIM8_CH4                                     | -                                                                   | SPI2_MISO/I2S2_SDI                                             | -                                                                        | -                                                                             |
|      | PI3  | -   | -                       | -                                      | TIM8_ETR                                     | -                                                                   | SPI2_MOSI/I2S2_SDO                                             | -                                                                        | -                                                                             |
|      | PI4  | -   | -                       | -                                      | TIM8_BKIN                                    | -                                                                   | -                                                              | -                                                                        | SPI2_RDY                                                                      |
|      | PI5  | -   | -                       | -                                      | TIM8_CH1                                     | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PI6  | -   | -                       | -                                      | TIM8_CH2                                     | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PI7  | -   | -                       | -                                      | TIM8_CH3                                     | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PI8  | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PI9  | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PI10 | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |
|      | PI11 | -   | -                       | -                                      | -                                            | -                                                                   | -                                                              | -                                                                        | -                                                                             |

1. Refer to the next table for AF8 to AF15.

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup>

| Port | AF8                                        |                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|--------------------------------------------|------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
|      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 |                        | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORmux]/FMC<br>[NOR_RAM]/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16]/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII]/<br>FMC[NAND16]/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>FMC[SDRAM_16bit]<br>/SDMMC1 | DCMI/FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| A    | PA0                                        | UART4_TX               | SDMMC2_CMD                                                                                | SAI2_SD_B                                                   | ETH_MII_CRS                                                             | -                                                                            | -                                                            | TIM2_ETR                    | EVENTOUT |
|      | PA1                                        | UART4_RX               | OCTOSPI1_IO3                                                                              | SAI2_MCLK_B                                                 | ETH_MII_RX_CLK/E<br>TH_RMII_REF_CLK                                     | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PA2                                        | SAI2_SCK_B             | -                                                                                         | -                                                           | ETH_MDIO                                                                | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PA3                                        | -                      | -                                                                                         | -                                                           | ETH_MII_COL                                                             | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PA4                                        | SPI6_NSS               | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_HSYNC/<br>PSSI_DE                                       | -                           | EVENTOUT |
|      | PA5                                        | SPI6_SCK               | -                                                                                         | -                                                           | ETH_MII_TX_EN/<br>ETH_RMII_TX_EN                                        | -                                                                            | PSSI_D14                                                     | TIM2_ETR                    | EVENTOUT |
|      | PA6                                        | SPI6_MISO              | TIM13_CH1                                                                                 | -                                                           | -                                                                       | -                                                                            | DCMI_PIXCLK/<br>PSSI_PDCK                                    | -                           | EVENTOUT |
|      | PA7                                        | SPI6_MOSI              | TIM14_CH1                                                                                 | OCTOSPI1_IO2                                                | ETH_MII_RX_DV/<br>ETH_RMII_CRS_DV                                       | FMC_SDNWE                                                                    | FMC_NWE                                                      | -                           | EVENTOUT |
|      | PA8                                        | -                      | -                                                                                         | USB_SOF                                                     | UART7_RX                                                                | FMC_NOE                                                                      | DCMI_D3/PSSI_D3                                              | -                           | EVENTOUT |
|      | PA9                                        | -                      | -                                                                                         | -                                                           | ETH_MII_TX_ER                                                           | FMC_NWE                                                                      | DCMI_D0/PSSI_D0                                              | -                           | EVENTOUT |
|      | PA10                                       | -                      | FDCAN2_TX                                                                                 | -                                                           | -                                                                       | SDMMC1_D0                                                                    | DCMI_D1/PSSI_D1                                              | -                           | EVENTOUT |
|      | PA11                                       | -                      | FDCAN1_RX                                                                                 | USB_DM                                                      | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PA12                                       | SAI2_FS_B              | FDCAN1_TX                                                                                 | USB_DP                                                      | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PA13                                       | -                      | -                                                                                         | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PA14                                       | -                      | -                                                                                         | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PA15                                       | UART4_RTS/<br>UART4_DE | -                                                                                         | -                                                           | UART7_TX                                                                | FMC_NBL1                                                                     | DCMI_D11/PSSI_D11                                            | TIM2_ETR                    | EVENTOUT |

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup> (continued)

|      |      | AF8                                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|------|--------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
| Port |      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORmux]/FMC<br>[NOR_RAM]/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16]/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII]/<br>FMC[NAND16]/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>FMC[SDRAM_16bit]<br>/SDMMC1 | DCMI/FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| B    | PB0  | UART4_CTS                                  | -                                                                                         | -                                                           | ETH_MII_RXD2                                                            | -                                                                            | -                                                            | LPTIM3_CH1                  | EVENTOUT |
|      | PB1  | -                                          | -                                                                                         | -                                                           | ETH_MII_RXD3                                                            | -                                                                            | -                                                            | LPTIM3_CH2                  | EVENTOUT |
|      | PB2  | -                                          | OCTOSPI1_CLK                                                                              | OCTOSPI1_DQS                                                | -                                                                       | SDMMC1_CMD                                                                   | LPTIM5_ETR                                                   | -                           | EVENTOUT |
|      | PB3  | SPI6_SCK                                   | SDMMC2_D2                                                                                 | CRS_SYNC                                                    | UART7_RX                                                                | -                                                                            | -                                                            | LPTIM6_ETR                  | EVENTOUT |
|      | PB4  | SPI6_MISO                                  | SDMMC2_D3                                                                                 | -                                                           | UART7_TX                                                                | -                                                                            | DCMI_D7/PSSI_D7                                              | -                           | EVENTOUT |
|      | PB5  | SPI6_MOSI                                  | FDCAN2_RX                                                                                 | -                                                           | ETH_PPS_OUT                                                             | FMC_SDCKE1                                                                   | DCMI_D10/PSSI_D10                                            | UART5_RX                    | EVENTOUT |
|      | PB6  | LPUART1_TX                                 | FDCAN2_TX                                                                                 | OCTOSPI1_NCS                                                | -                                                                       | FMC_SDNE1                                                                    | DCMI_D5/PSSI_D5                                              | UART5_TX                    | EVENTOUT |
|      | PB7  | LPUART1_RX                                 | FDCAN1_TX                                                                                 | SDMMC2_D5                                                   | SDMMC2_CKIN                                                             | FMC_NL                                                                       | DCMI_VSYNC/<br>PSSI_RDY                                      | -                           | EVENTOUT |
|      | PB8  | UART4_RX                                   | FDCAN1_RX                                                                                 | SDMMC2_D4                                                   | ETH_MII_TXD3                                                            | SDMMC1_D4                                                                    | DCMI_D6/PSSI_D6                                              | -                           | EVENTOUT |
|      | PB9  | UART4_TX                                   | FDCAN1_TX                                                                                 | SDMMC2_D5                                                   | SDMMC2_CKIN                                                             | SDMMC1_D5                                                                    | DCMI_D7/PSSI_D7                                              | -                           | EVENTOUT |
|      | PB10 | -                                          | OCTOSPI1_NCS                                                                              | -                                                           | ETH_MII_RX_ER                                                           | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PB11 | -                                          | -                                                                                         | -                                                           | ETH_MII_TX_EN/ET<br>H_RMII_TX_EN                                        | FMC_NBL1                                                                     | -                                                            | -                           | EVENTOUT |
|      | PB12 | -                                          | FDCAN2_RX                                                                                 | -                                                           | ETH_MII_TXD0/<br>ETH_RMII_TXD0                                          | -                                                                            | -                                                            | UART5_RX                    | EVENTOUT |
|      | PB13 | -                                          | FDCAN2_TX                                                                                 | -                                                           | -                                                                       | SDMMC1_D0                                                                    | -                                                            | UART5_TX                    | EVENTOUT |
|      | PB14 | UART4_RTS/<br>UART4_DE                     | SDMMC2_D0                                                                                 | -                                                           | -                                                                       | -                                                                            | -                                                            | LPTIM3_ETR                  | EVENTOUT |
|      | PB15 | UART4_CTS                                  | SDMMC2_D1                                                                                 | OCTOSPI1_CLK                                                | ETH_MII_TXD1/<br>ETH_RMII_TXD1                                          | -                                                                            | DCMI_D2/PSSI_D2                                              | UART5_RX                    | EVENTOUT |

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup> (continued)

| Port |      | AF8                                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|------|--------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
|      |      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORmux]/FMC<br>[NOR_RAM]/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16]/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII]/<br>FMC[NAND16]/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>FMC[SDRAM_16bit]<br>/SDMMC1 | DCMI/FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| C    | PC0  | SAI2_FS_B                                  | FMC_A25                                                                                   | OCTOSPI1_IO7                                                | -                                                                       | FMC_SDNWE                                                                    | -                                                            | -                           | EVENTOUT |
|      | PC1  | SAI2_SD_A                                  | SDMMC2_CK                                                                                 | OCTOSPI1_IO4                                                | ETH_MDC                                                                 | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PC2  | -                                          | OCTOSPI1_IO2                                                                              | -                                                           | ETH_MII_TXD2                                                            | FMC_SDNE0                                                                    | -                                                            | -                           | EVENTOUT |
|      | PC3  | -                                          | OCTOSPI1_IO0                                                                              | -                                                           | ETH_MII_TX_CLK                                                          | FMC_SDCKE0                                                                   | -                                                            | -                           | EVENTOUT |
|      | PC4  | -                                          | -                                                                                         | -                                                           | ETH_MII_RXD0/<br>ETH_RMII_RXD0                                          | FMC_SDNE0                                                                    | -                                                            | -                           | EVENTOUT |
|      | PC5  | -                                          | -                                                                                         | OCTOSPI1_DQS                                                | ETH_MII_RXD1/<br>ETH_RMII_RXD1                                          | FMC_SDCKE0                                                                   | -                                                            | -                           | EVENTOUT |
|      | PC6  | SDMMC1_D0D<br>IR                           | FMC_NWAIT                                                                                 | SDMMC2_D6                                                   | OCTOSPI1_IO5                                                            | SDMMC1_D6                                                                    | DCMI_D0/PSSI_D0                                              | -                           | EVENTOUT |
|      | PC7  | SDMMC1_D12<br>3DIR                         | FMC_NE1                                                                                   | SDMMC2_D7                                                   | OCTOSPI1_IO6                                                            | SDMMC1_D7                                                                    | DCMI_D1/PSSI_D1                                              | -                           | EVENTOUT |
|      | PC8  | UART5_RTS/<br>UART5_DE                     | FMC_NE2/<br>FMC_NCE                                                                       | FMC_INT                                                     | FMC_ALE                                                                 | SDMMC1_D0                                                                    | DCMI_D2/PSSI_D2                                              | -                           | EVENTOUT |
|      | PC9  | UART5_CTS                                  | OCTOSPI1_IO0                                                                              | -                                                           | FMC_CLE                                                                 | SDMMC1_D1                                                                    | DCMI_D3/PSSI_D3                                              | -                           | EVENTOUT |
|      | PC10 | UART4_TX                                   | OCTOSPI1_IO1                                                                              | -                                                           | ETH_MII_TXD0/<br>ETH_RMII_TXD0                                          | SDMMC1_D2                                                                    | DCMI_D8/PSSI_D8                                              | -                           | EVENTOUT |
|      | PC11 | UART4_RX                                   | OCTOSPI1_NCS                                                                              | -                                                           | -                                                                       | SDMMC1_D3                                                                    | DCMI_D4/PSSI_D4                                              | -                           | EVENTOUT |
|      | PC12 | UART5_TX                                   | -                                                                                         | -                                                           | -                                                                       | SDMMC1_CK                                                                    | DCMI_D9/PSSI_D9                                              | -                           | EVENTOUT |
|      | PC13 | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PC14 | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PC15 | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup> (continued)

|      |      | AF8                                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|------|--------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
| Port |      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORmux]/FMC<br>[NOR_RAM]/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16]/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII]/<br>FMC[NAND16]/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>FMC[SDRAM_16bit]<br>/SDMMC1 | DCMI/FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| D    | PD0  | UART4_RX                                   | FDCAN1_RX                                                                                 | -                                                           | UART9_CTS                                                               | FMC_D2/FMC_AD2                                                               | -                                                            | -                           | EVENTOUT |
|      | PD1  | UART4_TX                                   | FDCAN1_TX                                                                                 | -                                                           | -                                                                       | FMC_D3/FMC_AD3                                                               | -                                                            | -                           | EVENTOUT |
|      | PD2  | UART5_RX                                   | -                                                                                         | -                                                           | -                                                                       | SDMMC1_CMD                                                                   | DCMI_D11/PSSI_D11                                            | LPTIM4_ETR                  | EVENTOUT |
|      | PD3  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_CLK                                                                      | DCMI_D5/PSSI_D5                                              | -                           | EVENTOUT |
|      | PD4  | -                                          | -                                                                                         | OCTOSPI1_IO4                                                | -                                                                       | FMC_NOE                                                                      | -                                                            | -                           | EVENTOUT |
|      | PD5  | -                                          | FDCAN1_TX                                                                                 | OCTOSPI1_IO5                                                | -                                                                       | FMC_NWE                                                                      | -                                                            | -                           | EVENTOUT |
|      | PD6  | -                                          | -                                                                                         | OCTOSPI1_IO6                                                | SDMMC2_CK                                                               | FMC_NWAIT                                                                    | DCMI_D10/PSSI_D10                                            | -                           | EVENTOUT |
|      | PD7  | -                                          | -                                                                                         | OCTOSPI1_IO7                                                | SDMMC2_CMD                                                              | FMC_NE1/<br>FMC_NCE                                                          | -                                                            | LPTIM4_OUT                  | EVENTOUT |
|      | PD8  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_D13/<br>FMC_AD13                                                         | -                                                            | -                           | EVENTOUT |
|      | PD9  | -                                          | FDCAN2_RX                                                                                 | -                                                           | -                                                                       | FMC_D14/<br>FMC_AD14                                                         | -                                                            | -                           | EVENTOUT |
|      | PD10 | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_D15/<br>FMC_AD15                                                         | -                                                            | -                           | EVENTOUT |
|      | PD11 | UART4_RX                                   | OCTOSPI1_IO0                                                                              | SAI2_SD_A                                                   | -                                                                       | FMC_A16/FMC_CLE                                                              | -                                                            | -                           | EVENTOUT |
|      | PD12 | UART4_TX                                   | OCTOSPI1_IO1                                                                              | SAI2_FS_A                                                   | -                                                                       | FMC_A17/FMC_ALE                                                              | DCMI_D12/PSSI_D12                                            | -                           | EVENTOUT |
|      | PD13 | -                                          | OCTOSPI1_IO3                                                                              | SAI2_SCK_A                                                  | UART9_RTS/<br>UART9_DE                                                  | FMC_A18                                                                      | DCMI_D13/PSSI_D13                                            | LPTIM4_IN1                  | EVENTOUT |
|      | PD14 | UART8_CTS                                  | -                                                                                         | -                                                           | UART9_RX                                                                | FMC_D0/FMC_AD0                                                               | -                                                            | -                           | EVENTOUT |
|      | PD15 | UART8_RTS/<br>UART8_DE                     | -                                                                                         | -                                                           | UART9_TX                                                                | FMC_D1/FMC_AD1                                                               | -                                                            | -                           | EVENTOUT |

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup> (continued)

| Port |      | AF8                                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|------|--------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
|      |      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORmux]/FMC<br>[NOR_RAM]/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16]/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII]/<br>FMC[NAND16]/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>FMC[SDRAM_16bit]<br>/SDMMC1 | DCMI/FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| E    | PE0  | UART8_RX                                   | FDCAN1_RX                                                                                 | SAI2_MCLK_A                                                 | -                                                                       | FMC_NBL0                                                                     | DCMI_D2/PSSI_D2                                              | -                           | EVENTOUT |
|      | PE1  | UART8_TX                                   | FDCAN1_TX                                                                                 | -                                                           | -                                                                       | FMC_NBL1                                                                     | DCMI_D3/PSSI_D3                                              | -                           | EVENTOUT |
|      | PE2  | UART8_TX                                   | OCTOSPI1_IO2                                                                              | -                                                           | ETH_MII_TXD3                                                            | FMC_A23                                                                      | DCMI_D3/PSSI_D3                                              | -                           | EVENTOUT |
|      | PE3  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A19                                                                      | -                                                            | -                           | EVENTOUT |
|      | PE4  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A20                                                                      | DCMI_D4/PSSI_D4                                              | -                           | EVENTOUT |
|      | PE5  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A21                                                                      | DCMI_D6/PSSI_D6                                              | -                           | EVENTOUT |
|      | PE6  | -                                          | -                                                                                         | SAI2_MCLK_B                                                 | -                                                                       | FMC_A22                                                                      | DCMI_D7/PSSI_D7                                              | -                           | EVENTOUT |
|      | PE7  | -                                          | -                                                                                         | OCTOSPI1_IO4                                                | -                                                                       | FMC_D4/FMC_AD4                                                               | -                                                            | -                           | EVENTOUT |
|      | PE8  | -                                          | -                                                                                         | OCTOSPI1_IO5                                                | -                                                                       | FMC_D5/FMC_AD5                                                               | -                                                            | -                           | EVENTOUT |
|      | PE9  | -                                          | -                                                                                         | OCTOSPI1_IO6                                                | -                                                                       | FMC_D6/FMC_AD6                                                               | -                                                            | -                           | EVENTOUT |
|      | PE10 | -                                          | -                                                                                         | OCTOSPI1_IO7                                                | -                                                                       | FMC_D7/FMC_AD7                                                               | -                                                            | -                           | EVENTOUT |
|      | PE11 | -                                          | -                                                                                         | SAI2_SD_B                                                   | -                                                                       | FMC_D8/FMC_AD8                                                               | -                                                            | -                           | EVENTOUT |
|      | PE12 | -                                          | -                                                                                         | SAI2_SCK_B                                                  | -                                                                       | FMC_D9/FMC_AD9                                                               | -                                                            | -                           | EVENTOUT |
|      | PE13 | -                                          | -                                                                                         | SAI2_FS_B                                                   | -                                                                       | FMC_D10/<br>FMC_AD10                                                         | -                                                            | -                           | EVENTOUT |
|      | PE14 | -                                          | -                                                                                         | SAI2_MCLK_B                                                 | -                                                                       | FMC_D11/<br>FMC_AD11                                                         | -                                                            | -                           | EVENTOUT |
|      | PE15 | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_D12/<br>FMC_AD12                                                         | -                                                            | -                           | EVENTOUT |

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup> (continued)

| Port |      | AF8                                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|------|--------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
|      |      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORmux]/FMC<br>[NOR_RAM]/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16]/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII]/<br>FMC[NAND16]/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>FMC[SDRAM_16bit]<br>/SDMMC1 | DCMI/FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| F    | PF0  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A0                                                                       | LPTIM5_CH1                                                   | -                           | EVENTOUT |
|      | PF1  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A1                                                                       | LPTIM5_CH2                                                   | -                           | EVENTOUT |
|      | PF2  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A2                                                                       | LPTIM5_IN1                                                   | -                           | EVENTOUT |
|      | PF3  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A3                                                                       | LPTIM5_IN2                                                   | -                           | EVENTOUT |
|      | PF4  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A4                                                                       | -                                                            | -                           | EVENTOUT |
|      | PF5  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A5                                                                       | -                                                            | LPTIM3_IN1                  | EVENTOUT |
|      | PF6  | -                                          | -                                                                                         | OCTOSPI1_IO3                                                | -                                                                       | -                                                                            | LPTIM5_CH1                                                   | -                           | EVENTOUT |
|      | PF7  | -                                          | -                                                                                         | OCTOSPI1_IO2                                                | -                                                                       | -                                                                            | LPTIM5_CH2                                                   | -                           | EVENTOUT |
|      | PF8  | -                                          | TIM13_CH1                                                                                 | OCTOSPI1_IO0                                                | -                                                                       | -                                                                            | LPTIM5_IN1                                                   | -                           | EVENTOUT |
|      | PF9  | -                                          | TIM14_CH1                                                                                 | OCTOSPI1_IO1                                                | -                                                                       | -                                                                            | LPTIM5_IN2                                                   | -                           | EVENTOUT |
|      | PF10 | -                                          | OCTOSPI1_CLK                                                                              | -                                                           | -                                                                       | -                                                                            | DCMI_D11/PSSI_D11                                            | -                           | EVENTOUT |
|      | PF11 | -                                          | OCTOSPI1_NCLK                                                                             | SAI2_SD_B                                                   | -                                                                       | FMC_NRAS                                                                     | DCMI_D12/PSSI_D12                                            | LPTIM6_CH1                  | EVENTOUT |
|      | PF12 | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A6                                                                       | -                                                            | LPTIM6_CH2                  | EVENTOUT |
|      | PF13 | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A7                                                                       | -                                                            | LPTIM6_IN1                  | EVENTOUT |
|      | PF14 | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A8                                                                       | -                                                            | LPTIM6_IN2                  | EVENTOUT |
|      | PF15 | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A9                                                                       | -                                                            | -                           | EVENTOUT |

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup> (continued)

| Port |      | AF8                                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|------|--------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
|      |      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORmux]/FMC<br>[NOR_RAM]/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16]/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII]/<br>FMC[NAND16]/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>FMC[SDRAM_16bit]<br>/SDMMC1 | DCMI/FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| G    | PG0  | -                                          | -                                                                                         | -                                                           | UART9_RX                                                                | FMC_A10                                                                      | -                                                            | LPTIM4_IN1                  | EVENTOUT |
|      | PG1  | -                                          | -                                                                                         | -                                                           | UART9_TX                                                                | FMC_A11                                                                      | -                                                            | -                           | EVENTOUT |
|      | PG2  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A12                                                                      | -                                                            | LPTIM6_ETR                  | EVENTOUT |
|      | PG3  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A13                                                                      | LPTIM5_ETR                                                   | -                           | EVENTOUT |
|      | PG4  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A14/FMC_BA0                                                              | -                                                            | LPTIM4_ETR                  | EVENTOUT |
|      | PG5  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_A15/FMC_BA1                                                              | -                                                            | -                           | EVENTOUT |
|      | PG6  | -                                          | -                                                                                         | OCTOSPI1_NCS                                                | UCPD1_FRSTX                                                             | FMC_NE3                                                                      | DCMI_D12/PSSI_D12                                            | -                           | EVENTOUT |
|      | PG7  | -                                          | -                                                                                         | -                                                           | UCPD1_FRSTX                                                             | FMC_INT                                                                      | DCMI_D13/PSSI_D13                                            | -                           | EVENTOUT |
|      | PG8  | -                                          | -                                                                                         | -                                                           | ETH_PPS_OUT                                                             | FMC_SDCLK                                                                    | -                                                            | -                           | EVENTOUT |
|      | PG9  | -                                          | OCTOSPI1_IO6                                                                              | SAI2_FS_B                                                   | SDMMC2_D0                                                               | FMC_NE2/<br>FMC_NCE                                                          | DCMI_VSYNC/<br>PSSI_RDY                                      | -                           | EVENTOUT |
|      | PG10 | -                                          | -                                                                                         | SAI2_SD_B                                                   | SDMMC2_D1                                                               | FMC_NE3                                                                      | DCMI_D2/PSSI_D2                                              | -                           | EVENTOUT |
|      | PG11 | -                                          | -                                                                                         | SDMMC2_D2                                                   | ETH_MII_TX_EN/ET<br>H_RMII_TX_EN                                        | -                                                                            | DCMI_D3/PSSI_D3                                              | -                           | EVENTOUT |
|      | PG12 | -                                          | -                                                                                         | SDMMC2_D3                                                   | ETH_MII_TXD1/<br>ETH_RMII_TXD1                                          | FMC_NE4                                                                      | DCMI_D11/PSSI_D11                                            | LPTIM5_CH1                  | EVENTOUT |
|      | PG13 | -                                          | -                                                                                         | SDMMC2_D6                                                   | ETH_MII_TXD0/<br>ETH_RMII_TXD0                                          | FMC_A24                                                                      | LPTIM5_CH2                                                   | -                           | EVENTOUT |
|      | PG14 | -                                          | OCTOSPI1_IO7                                                                              | SDMMC2_D7                                                   | ETH_MII_TXD1/<br>ETH_RMII_TXD1                                          | FMC_A25                                                                      | LPTIM5_IN1                                                   | -                           | EVENTOUT |
|      | PG15 | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_NCAS                                                                     | DCMI_D13/PSSI_D13                                            | -                           | EVENTOUT |

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup> (continued)

| Port |      | AF8                                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|------|--------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
|      |      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORMux)/FMC<br>[NOR_RAM)/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16)/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII)/<br>FMC[NAND16)/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16)/<br>FMC[NORMux)/<br>FMC[NOR_RAM)/<br>FMC[SDRAM_16bit)<br>/SDMMC1 | DCMI/FMC[NAND16)/<br>FMC[NORMux)/<br>FMC[NOR_RAM)/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| H    | PH0  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PH1  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PH2  | -                                          | OCTOSPI1_IO4                                                                              | SAI2_SCK_B                                                  | ETH_MII_CRS                                                             | FMC_SDCKE0                                                                   | -                                                            | -                           | EVENTOUT |
|      | PH3  | -                                          | OCTOSPI1_IO5                                                                              | SAI2_MCLK_B                                                 | ETH_MII_COL                                                             | FMC_SDNE0                                                                    | -                                                            | -                           | EVENTOUT |
|      | PH4  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | PSSI_D14                                                     | -                           | EVENTOUT |
|      | PH5  | -                                          | -                                                                                         | -                                                           | -                                                                       | FMC_SDNWE                                                                    | -                                                            | -                           | EVENTOUT |
|      | PH6  | -                                          | -                                                                                         | -                                                           | ETH_MII_RXD2                                                            | FMC_SDNE1                                                                    | DCMI_D8/PSSI_D8                                              | -                           | EVENTOUT |
|      | PH7  | -                                          | -                                                                                         | -                                                           | ETH_MII_RXD3                                                            | FMC_SDCKE1                                                                   | DCMI_D9/PSSI_D9                                              | -                           | EVENTOUT |
|      | PH8  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_HSYNC/<br>PSSI_DE                                       | -                           | EVENTOUT |
|      | PH9  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_D0/PSSI_D0                                              | -                           | EVENTOUT |
|      | PH10 | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_D1/PSSI_D1                                              | -                           | EVENTOUT |
|      | PH11 | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_D2/PSSI_D2                                              | -                           | EVENTOUT |
|      | PH12 | -                                          | -                                                                                         | TIM8_CH4N                                                   | -                                                                       | -                                                                            | DCMI_D3/PSSI_D3                                              | -                           | EVENTOUT |
|      | PH13 | UART4_TX                                   | FDCAN1_TX                                                                                 | -                                                           | -                                                                       | -                                                                            | DCMI_D3/PSSI_D3                                              | -                           | EVENTOUT |
|      | PH14 | UART4_RX                                   | FDCAN1_RX                                                                                 | -                                                           | -                                                                       | -                                                                            | DCMI_D4/PSSI_D4                                              | -                           | EVENTOUT |
|      | PH15 | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_D11/PSSI_D11                                            | -                           | EVENTOUT |

Table 16. Alternate functions AF8 to AF15<sup>(1)</sup> (continued)

|      |      | AF8                                        | AF9                                                                                       | AF10                                                        | AF11                                                                    | AF12                                                                         | AF13                                                         | AF14                        | AF15     |
|------|------|--------------------------------------------|-------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------|----------|
| Port |      | LPUART1/SAI2<br>/SDMMC1/SPI6<br>/UART4/5/8 | FDCAN1/2/FMC<br>[NAND16]/FMC<br>[NORmux]/FMC<br>[NOR_RAM]/<br>OCTOSPI/<br>SDMMC2/TIM13/14 | CRS/FMC[NAND<br>16]/OCTOSPI/S<br>AI2/SDMMC2/<br>TIM8/USB_PD | ETH[MII/RMII]/<br>FMC[NAND16]/<br>OCTOSPI/<br>SDMMC2/<br>UART7/9/USB_PD | FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>FMC[SDRAM_16bit]<br>/SDMMC1 | DCMI/FMC[NAND16]/<br>FMC[NORmux]/<br>FMC[NOR_RAM]/<br>LPTIM5 | LPTIM3/4/5/6/<br>TIM2/UART5 | SYS      |
| I    | PI0  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_D13/PSSI_D13                                            | -                           | EVENTOUT |
|      | PI1  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_D8/PSSI_D8                                              | -                           | EVENTOUT |
|      | PI2  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_D9/PSSI_D9                                              | -                           | EVENTOUT |
|      | PI3  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | DCMI_D10/PSSI_D10                                            | -                           | EVENTOUT |
|      | PI4  | -                                          | -                                                                                         | SAI2_MCLK_A                                                 | -                                                                       | -                                                                            | DCMI_D5/PSSI_D5                                              | -                           | EVENTOUT |
|      | PI5  | -                                          | -                                                                                         | SAI2_SCK_A                                                  | -                                                                       | -                                                                            | DCMI_VSYNC/<br>PSSI_RDY                                      | -                           | EVENTOUT |
|      | PI6  | -                                          | -                                                                                         | SAI2_SD_A                                                   | -                                                                       | -                                                                            | DCMI_D6/PSSI_D6                                              | -                           | EVENTOUT |
|      | PI7  | -                                          | -                                                                                         | SAI2_FS_A                                                   | -                                                                       | -                                                                            | DCMI_D7/PSSI_D7                                              | -                           | EVENTOUT |
|      | PI8  | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PI9  | UART4_RX                                   | FDCAN1_RX                                                                                 | -                                                           | -                                                                       | -                                                                            | -                                                            | -                           | EVENTOUT |
|      | PI10 | -                                          | FDCAN1_RX                                                                                 | -                                                           | ETH_MII_RX_ER                                                           | -                                                                            | PSSI_D14                                                     | -                           | EVENTOUT |
|      | PI11 | -                                          | -                                                                                         | -                                                           | -                                                                       | -                                                                            | PSSI_D15                                                     | -                           | EVENTOUT |

1. Refer to the previous table for AF0 to AF7.

## 5 Electrical characteristics

### 5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_J = 25^\circ\text{C}$  and  $T_J = T_{J\text{max}}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes, and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean  $\pm 3\sigma$ ).

#### 5.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = V_{DDA} = 3.3\text{ V}$  (for the  $1.71 \leq V_{DD} \leq 3.6\text{ V}$  voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean  $\pm 2\sigma$ ).

#### 5.1.3 Typical curves

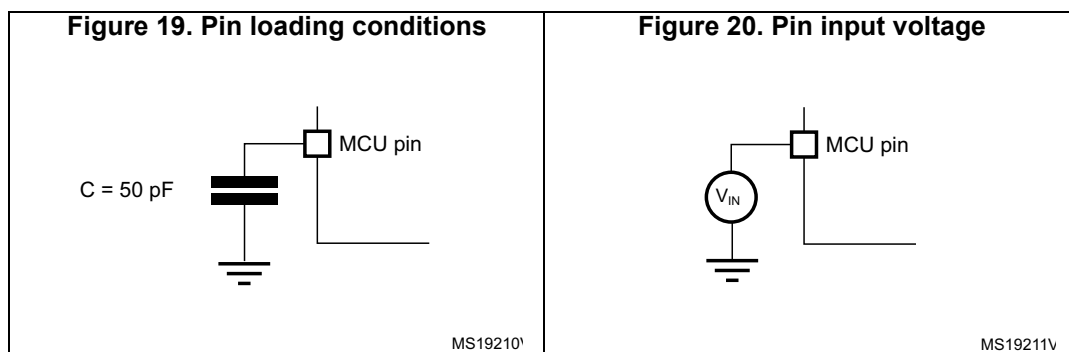
Unless otherwise specified, all typical curves are given only as design guidelines, and are not tested.

#### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 19](#).

#### 5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 20](#).



## 5.1.6 Power supply scheme

Figure 21. Power supply scheme with SMPS

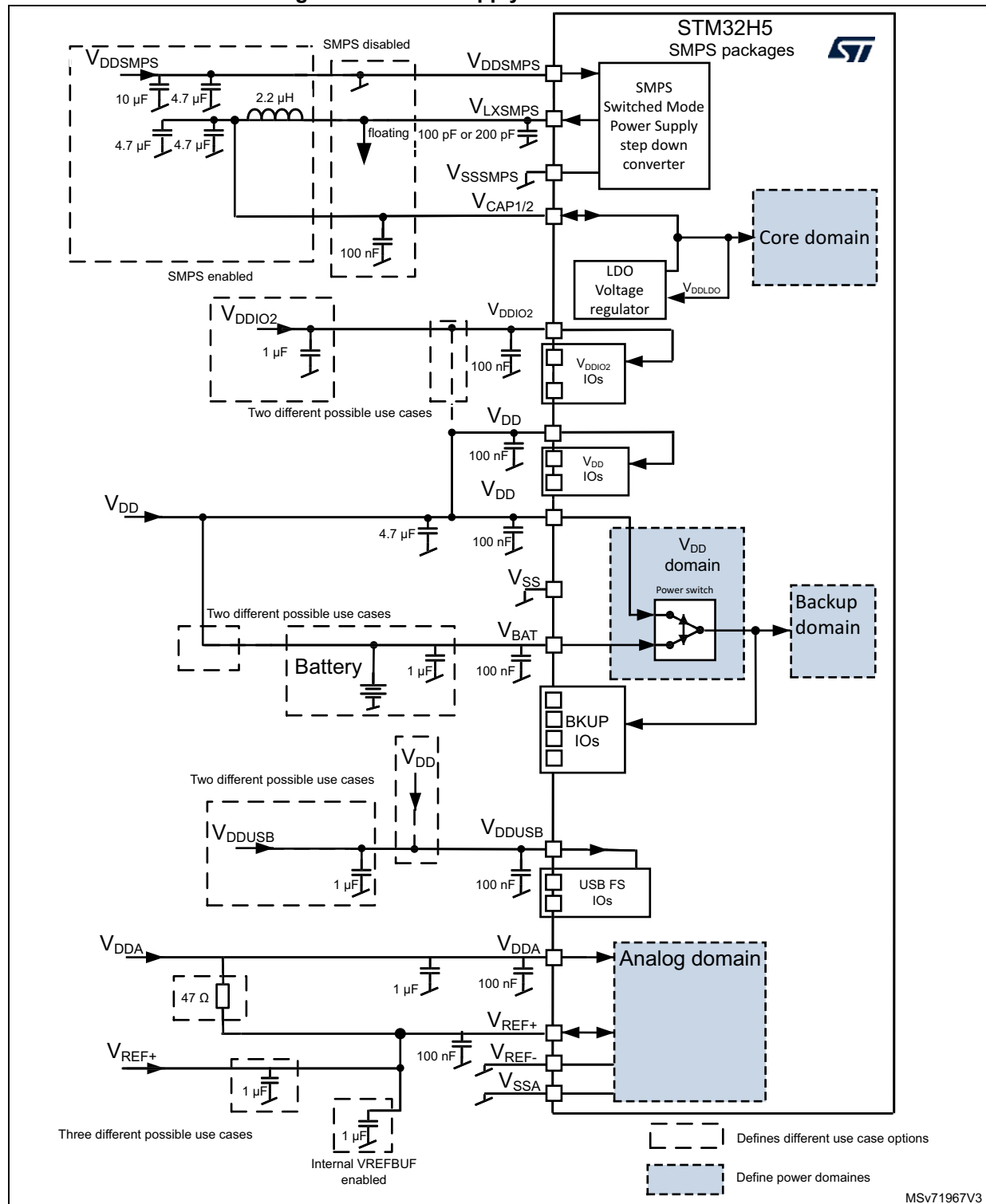
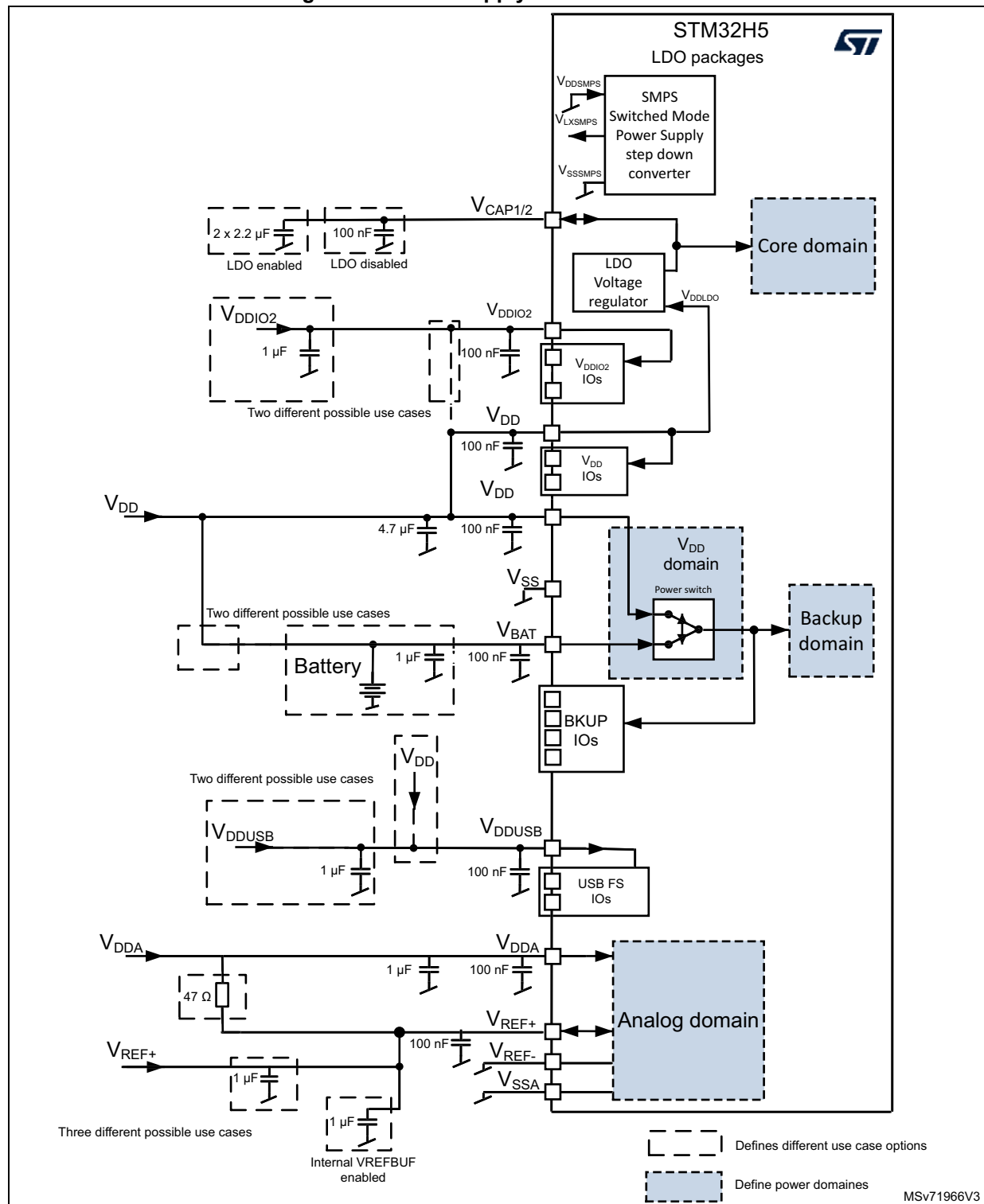


Figure 22. Power supply scheme with LDO



Note: Refer to “Getting started with STM32H5 Series hardware development” (AN5711) for more details.

**Caution:** Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 17](#), [Table 18](#), and [Table 19](#) may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

**Table 17. Voltage characteristics<sup>(1)</sup>**

| Symbol                     | Ratings                                                                                                                                       | Min            | Max                                                                                 | Unit |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|----------------|-------------------------------------------------------------------------------------|------|
| $V_{DDx} - V_{SS}$         | External main supply voltage (including $V_{DDSMPS}^{(2)}$ , $V_{DDA}$ , $V_{DDUSB}$ , $V_{DDIO2}^{(2)(3)(4)}$ , $V_{BAT}$ , and $V_{REF+}$ ) | -0.3           | 4.0                                                                                 | V    |
| $V_{DDIOx}^{(4)} - V_{SS}$ | I/O supply when HSLV <sup>(2)</sup> = 0                                                                                                       | -0.3           | 4.0                                                                                 | V    |
|                            | I/O supply when HSLV <sup>(2)</sup> = 1                                                                                                       | -0.3           | 2.75                                                                                |      |
| $V_{IN}^{(5)}$             | Input voltage on FT_xxx pins except FT_c pins                                                                                                 | $V_{SS} - 0.3$ | $\min(\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0, 6.0 \text{ V})^{(6)(7)}$   | V    |
|                            | Input voltage on FT_t in $V_{BAT}$ mode                                                                                                       | $V_{SS} - 0.3$ | $\min(\min(V_{BAT}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0 \text{ V}, 6.0 \text{ V})$ |      |
|                            | Input voltage on TT_xx pins                                                                                                                   | $V_{SS} - 0.3$ | 4.0                                                                                 |      |
|                            | Input voltage on BOOT0 pin                                                                                                                    | $V_{SS}$       | $\min(\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0, 6.0 \text{ V})^{(6)}$      |      |
|                            | Input voltage on FT_c pins                                                                                                                    | $V_{SS} - 0.3$ | 5.5                                                                                 |      |
|                            | Input voltage on any other pins                                                                                                               | $V_{SS} - 0.3$ | 4.0                                                                                 |      |
| $V_{REF+} - V_{DDA}$       | Allowed voltage difference for $V_{REF+} > V_{DDA}$                                                                                           | -              | 0.4                                                                                 |      |
| $ \Delta V_{DDx} $         | Variations between different $V_{DDx}$ power pins of the same domain                                                                          | -              | 50.0                                                                                | mV   |
| $ V_{SSx} - V_{SS} $       | Variations between all the different ground pins                                                                                              | -              | 50.0                                                                                |      |

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ,  $V_{DDUSB}$ ,  $V_{DDIO2}$ ,  $V_{REF+}$ ,  $V_{DDSMPS}$ ,  $V_{BAT}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2. HSLV = High-speed low-voltage mode. Refer to General purpose I/Os (GPIO) section of RM0481.
3. If HSLV = 0.
4.  $V_{DDIO1}$  or  $V_{DDIO2}$ .  $V_{DDIO1} = V_{DD}$ .
5.  $V_{IN}$  maximum must always be respected. Refer to the maximum allowed injected current values.
6. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
7. This formula must be applied on power supplies related to the I/O structure described by the pin definition table.

Table 18. Current characteristics

| Symbol                  | Ratings                                                                         | Max    | Unit |
|-------------------------|---------------------------------------------------------------------------------|--------|------|
| $\Sigma I_{V_{DD}}$     | Total current into sum of all $V_{DD}$ power lines (source) <sup>(1)</sup>      | 350    | mA   |
| $\Sigma I_{V_{SS}}$     | Total current out of sum of all $V_{SS}$ ground lines (sink) <sup>(1)</sup>     | 350    |      |
| $I_{V_{DD}}$            | Maximum current into each $V_{DD}$ power pin (source) <sup>(1)</sup>            | 100    |      |
| $I_{V_{SS}}$            | Maximum current out of each $V_{SS}$ ground pin (sink) <sup>(1)</sup>           | 100    |      |
| $I_{IO(PIN)}$           | Output current sunk/sourced by any I/O and control pin                          | 20     |      |
| $\Sigma I_{IO(PIN)}$    | Total output current sunk by sum of all I/Os and control pins <sup>(2)</sup>    | 140    |      |
|                         | Total output current sourced by sum of all I/Os and control pins <sup>(2)</sup> | 140    |      |
| $I_{INJ(PIN)}^{(3)(4)}$ | Injected current on FT_xxx, TT_xx, NRST pins                                    | -5 / 0 |      |
| $\Sigma  I_{INJ(PIN)} $ | Total injected current (sum of all I/Os and control pins) <sup>(5)</sup>        | ±25    |      |

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ,  $V_{DDIO2}$ , and  $V_{BAT}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supplies, in the allowed range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection (when  $V_{IN} > V_{DDIOx}$ ) is not possible on these I/Os, and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 17](#) for the minimum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum  $\Sigma |I_{INJ(PIN)}|$  is the absolute sum of the negative injected currents (instantaneous values).

Table 19. Thermal characteristics

| Symbol    | Ratings                      | Value              | Unit |
|-----------|------------------------------|--------------------|------|
| $T_{STG}$ | Storage temperature range    | -65 to +150        | °C   |
| $T_J$     | Maximum junction temperature | 130 <sup>(1)</sup> | °C   |

1. The junction temperature is limited to 105°C in the VOS0 voltage range.

## 5.3 Operating conditions

### 5.3.1 General operating conditions

Table 20. General operating conditions

| Symbol       | Parameter                                                | Operating conditions    | Min                 | Typ | Max      | Unit |
|--------------|----------------------------------------------------------|-------------------------|---------------------|-----|----------|------|
| $V_{DD}$     | Standard operating voltage                               | HSLV <sup>(1)</sup> = 0 | 1.71 <sup>(2)</sup> | -   | 3.6      | V    |
|              |                                                          | HSLV <sup>(1)</sup> = 1 | 1.71 <sup>(2)</sup> | -   | 2.7      |      |
| $V_{DDSMPS}$ | Supply voltage for the internal SMPS step-down converter | $V_{DD}$                | $V_{DD}$            | -   | $V_{DD}$ | V    |

Table 20. General operating conditions (continued)

| Symbol      | Parameter                                        | Operating conditions                                                              | Min  | Typ | Max                                                                                      | Unit |
|-------------|--------------------------------------------------|-----------------------------------------------------------------------------------|------|-----|------------------------------------------------------------------------------------------|------|
| $V_{DDIO2}$ | PB8, PB9, PD6, PD7, PG[9:14] I/Os supply voltage | At least one I/O in PB8, PB9, PD6, PD7, PG[9:14] is used, HSLV <sup>(1)</sup> = 0 | 1.08 | -   | 3.6                                                                                      | V    |
|             |                                                  | At least one I/O in PB8, PB9, PD6, PD7, PG[9:14] is used, HSLV <sup>(1)</sup> = 1 | 1.08 | -   | 2.7                                                                                      |      |
|             |                                                  | PB8, PB9, PD6, PD7, PG[9:14] are not used                                         | 0    |     | 3.6                                                                                      |      |
| $V_{DDUSB}$ | USB supply voltage                               | USB is used                                                                       | 3.0  | -   | 3.6                                                                                      | V    |
|             |                                                  | USB is not used                                                                   | 0    | -   | 3.6                                                                                      |      |
| $V_{DDA}$   | Analog supply voltage                            | ADC is used                                                                       | 1.62 | -   | 3.6                                                                                      | V    |
|             |                                                  | DAC is used                                                                       | 1.8  | -   |                                                                                          |      |
|             |                                                  | VREFBUF is used                                                                   | 2.1  | -   |                                                                                          |      |
|             |                                                  | ADC, DAC, and VREFBUF are not used                                                | 0    | -   |                                                                                          |      |
| $V_{BAT}$   | Backup domain supply voltage                     | -                                                                                 | 1.2  | -   | 3.6                                                                                      | V    |
| $V_{IN}$    | I/O input voltage                                | All I/Os except FT_c and TT_xx                                                    | -0.3 | -   | min (min ( $V_{DD}$ , $V_{DDA}$ , $V_{DDUSB}$ , $V_{DDIO2}$ ) + 3.6 V, 5.5 V)<br>(3)(4)  | V    |
|             |                                                  | Input voltage on FT_t in VBAT mode                                                | -0.3 | -   | min (min ( $V_{BAT}$ , $V_{DDA}$ , $V_{DDUSB}$ , $V_{DDIO2}$ ) + 3.6 V, 5.5 V)<br>(3)(4) |      |
|             |                                                  | FT_c I/O                                                                          | -0.3 | -   | 5.0                                                                                      |      |
|             |                                                  | TT_xx I/O                                                                         | -0.3 | -   | $V_{DDIOx} + 0.3$                                                                        |      |

Table 20. General operating conditions (continued)

| Symbol                   | Parameter                                                                                                    | Operating conditions                                            | Min                                                                                                                                                                                                                                                           | Typ  | Max  | Unit |
|--------------------------|--------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|
| $V_{CORE}$               | Internal regulator ON                                                                                        | VOS0 <sup>(5)</sup><br>(max frequency for AHB and APB: 250 MHz) | 1.30                                                                                                                                                                                                                                                          | 1.35 | 1.40 | V    |
|                          |                                                                                                              | VOS1<br>(max frequency for AHB and APB: 200 MHz)                | 1.15                                                                                                                                                                                                                                                          | 1.20 | 1.26 |      |
|                          |                                                                                                              | VOS2<br>(max frequency for AHB and APB: 150 MHz)                | 1.05                                                                                                                                                                                                                                                          | 1.10 | 1.15 |      |
|                          |                                                                                                              | VOS3<br>(max frequency for AHB and APB: 100 MHz)                | 0.95                                                                                                                                                                                                                                                          | 1.00 | 1.05 |      |
|                          | Regulator OFF:<br>external $V_{CORE}$ voltage<br>must be supplied from<br>external regulator on<br>VCAP pins | VOS0 <sup>(5)</sup>                                             | 1.32                                                                                                                                                                                                                                                          | 1.35 | 1.40 | V    |
|                          |                                                                                                              | VOS1                                                            | 1.17                                                                                                                                                                                                                                                          | 1.20 | 1.26 |      |
|                          |                                                                                                              | VOS2                                                            | 1.07                                                                                                                                                                                                                                                          | 1.10 | 1.15 |      |
|                          |                                                                                                              | VOS3                                                            | 0.97                                                                                                                                                                                                                                                          | 1.00 | 1.05 |      |
|                          | Stop mode                                                                                                    | SVOS3                                                           | -                                                                                                                                                                                                                                                             | 1.0  | -    | V    |
|                          |                                                                                                              | SVOS4                                                           | -                                                                                                                                                                                                                                                             | 0.9  | -    |      |
|                          |                                                                                                              | SVOS5                                                           | -                                                                                                                                                                                                                                                             | 0.74 | -    |      |
| $f_{HCLK}$               | AHB clock frequency                                                                                          | VOS0 <sup>(5)</sup>                                             | -                                                                                                                                                                                                                                                             | -    | 250  | MHz  |
|                          |                                                                                                              | VOS1                                                            | -                                                                                                                                                                                                                                                             | -    | 200  |      |
|                          |                                                                                                              | VOS2                                                            | -                                                                                                                                                                                                                                                             | -    | 150  |      |
|                          |                                                                                                              | VOS3                                                            | -                                                                                                                                                                                                                                                             | -    | 100  |      |
| $f_{PCLKx}$<br>(x=1,2,3) | APB1, APB2, APB3<br>clock frequency                                                                          | VOS0 <sup>(5)</sup>                                             | -                                                                                                                                                                                                                                                             | -    | 250  | MHz  |
|                          |                                                                                                              | VOS1                                                            | -                                                                                                                                                                                                                                                             | -    | 200  |      |
|                          |                                                                                                              | VOS2                                                            | -                                                                                                                                                                                                                                                             | -    | 150  |      |
|                          |                                                                                                              | VOS3                                                            | -                                                                                                                                                                                                                                                             | -    | 100  |      |
| $P_D$                    | Power dissipation at<br>$T_A = 85$ or $105$ °C<br>for suffix 6 or 7<br>versions <sup>(6)</sup>               | LQFP64                                                          | See <a href="#">Table 142</a> for<br>appropriate thermal<br>resistance and package.<br>Power dissipation is<br>calculated according to<br>ambient temperature<br>( $T_A$ ), maximum junction<br>temperature ( $T_J$ ), and<br>selected thermal<br>resistance. |      |      | mW   |
|                          |                                                                                                              | LQFP100                                                         |                                                                                                                                                                                                                                                               |      |      |      |
|                          |                                                                                                              | LQFP144                                                         |                                                                                                                                                                                                                                                               |      |      |      |
|                          |                                                                                                              | LQFP176                                                         |                                                                                                                                                                                                                                                               |      |      |      |
|                          |                                                                                                              | UFBGA169                                                        |                                                                                                                                                                                                                                                               |      |      |      |
|                          |                                                                                                              | UFBGA176                                                        |                                                                                                                                                                                                                                                               |      |      |      |
|                          |                                                                                                              | VFQFPN68                                                        |                                                                                                                                                                                                                                                               |      |      |      |
|                          |                                                                                                              | WLCSP80                                                         |                                                                                                                                                                                                                                                               |      |      |      |

Table 20. General operating conditions (continued)

| Symbol | Parameter                                                                                    | Operating conditions      | Min                                                                                                                                                                                                                                | Typ | Max | Unit               |
|--------|----------------------------------------------------------------------------------------------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|--------------------|
| $P_D$  | Power dissipation at $T_A = 125\text{ }^{\circ}\text{C}$ for suffix 3 version <sup>(6)</sup> | LQFP100                   | See <a href="#">Table 142</a> for appropriate thermal resistance and package. Power dissipation is calculated according to ambient temperature ( $T_A$ ), maximum junction temperature ( $T_J$ ), and selected thermal resistance. |     |     | mW                 |
|        |                                                                                              | LQFP144                   |                                                                                                                                                                                                                                    |     |     |                    |
|        |                                                                                              | LQFP176                   |                                                                                                                                                                                                                                    |     |     |                    |
|        |                                                                                              | UFBGA169                  |                                                                                                                                                                                                                                    |     |     |                    |
|        |                                                                                              | UFBGA176                  |                                                                                                                                                                                                                                    |     |     |                    |
|        |                                                                                              | TFBGA225                  |                                                                                                                                                                                                                                    |     |     |                    |
|        |                                                                                              | WLCSP80                   |                                                                                                                                                                                                                                    |     |     |                    |
| $T_A$  | Ambient temperature for the suffix 3 version                                                 | Maximum power dissipation | -40                                                                                                                                                                                                                                | -   | 125 | $^{\circ}\text{C}$ |
|        | Ambient temperature for the suffix 6 version                                                 | Maximum power dissipation | -40                                                                                                                                                                                                                                | -   | 85  |                    |
|        |                                                                                              | In LDO bypass mode        | -40                                                                                                                                                                                                                                | -   | 125 |                    |
|        | Ambient temperature for the suffix 7 version                                                 | Maximum power dissipation | -40                                                                                                                                                                                                                                | -   | 105 |                    |
|        |                                                                                              | In LDO bypass mode        | -40                                                                                                                                                                                                                                | -   | 125 |                    |
| $T_J$  | Junction temperature range                                                                   | VOS0                      | -40                                                                                                                                                                                                                                | -   | 105 | $^{\circ}\text{C}$ |
|        |                                                                                              | VOS1, VOS2, and VOS3      | -40                                                                                                                                                                                                                                | -   | 130 |                    |

1. HSLV = High-speed low-voltage mode. Refer to General-purpose I/Os (GPIO) section of RM0481.
2. When RESET is released functionality is guaranteed down to BOR level 0 minimum voltage.
3. This formula must be applied on power supplies related to the I/O structure described by the pin definition table. Maximum I/O input voltage is the smallest value between  $\min(V_{DD}, V_{DDA}, V_{DDIO2}) + 3.6\text{ V}$  and  $5.5\text{ V}$ .
4. For operation with voltages higher than  $\min(V_{DD}, V_{DDA}, V_{DDIO2}) + 0.3\text{ V}$ , the internal pull-up and pull-down resistors must be disabled.
5. In VOS0 mode the max  $T_J$  is  $105^{\circ}\text{C}$ .
6. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Table 19](#)).

Table 21. Maximum allowed clock frequencies

| Symbol <sup>(1)(2)</sup>               | Parameter            | VOS0 | VOS1 | VOS2 | VOS3 | Unit |
|----------------------------------------|----------------------|------|------|------|------|------|
| f <sub>CPU</sub>                       | CPU                  | 250  | 200  | 150  | 100  | MHz  |
| f <sub>HCLK</sub>                      | AHB                  | 250  | 200  | 150  | 100  |      |
| f <sub>PCLK</sub>                      | APB                  | 250  | 200  | 150  | 100  |      |
| -                                      | FMC                  | 250  | 200  | 150  | 100  |      |
| f <sub>octospi_ker_ck</sub>            | OCTOSPI[1:2]         | 250  | 200  | 150  | 100  |      |
| f <sub>sdmmc_ker_ck</sub>              | SDMMC[1:2]           | 250  | 200  | 150  | 100  |      |
| -                                      | HDMI_CEC             | 4    | 4    | 4    | 4    |      |
| f <sub>fdcan_ker_ck</sub>              | FDCAN                | 250  | 200  | 150  | 100  |      |
| f <sub>I2C_ker_ck</sub>                | I2C[1:4]             | 250  | 200  | 150  | 100  |      |
| f <sub>I3C_ker_ck</sub>                | I3C                  | 250  | 200  | 150  | 100  |      |
| f <sub>lptim_ker_ck</sub>              | LPTIM[1:6]           | 250  | 200  | 150  | 100  |      |
| f <sub>tim_ker_ck</sub>                | TIM[1:8], TIM[12:17] | 250  | 200  | 150  | 100  | MHz  |
|                                        | TIM6/17              | 64   | 64   | 64   | 64   |      |
| f <sub>rng_clk</sub>                   | RNG                  | 50   | 50   | 50   | 50   |      |
| f <sub>sai_a_ker_ck</sub>              | SAI1/2               | 250  | 200  | 150  | 100  |      |
| f <sub>sai_b_ker_ck</sub>              |                      |      |      |      |      |      |
| f <sub>spi_ker_ck</sub>                | SPI(I2S)1,2,3        | 125  | 100  | 75   | 50   |      |
|                                        | SPI4,5,6             | 125  | 100  | 75   | 50   |      |
| f <sub>lpuart_ker_ck</sub>             | LPUART1              | 250  | 200  | 150  | 100  |      |
| f <sub>usart_ker_ck</sub>              | USART/UART           | 250  | 200  | 150  | 100  |      |
| f <sub>usb_ker_ck</sub>                | USB FS               | 50   | 50   | 50   | 50   |      |
| f <sub>adc_ker_ck_input</sub>          | ADC                  | 250  | 200  | 150  | 100  |      |
| f <sub>adc_ker_ck</sub> <sup>(3)</sup> | ADC                  | 125  | 100  | 75   | 50   |      |
| f <sub>dac_ker_ck</sub>                | DAC                  | 250  | 200  | 150  | 100  |      |
| f <sub>ucpd_ker_ck</sub>               | USBPD                | 64   | 64   | 64   | 64   |      |
| f <sub>rtc_ker_ck</sub>                | RTC                  | 1    | 1    | 1    | 1    |      |
| -                                      | DCMI                 | 250  | 200  | 150  | 100  |      |

1. Specified by design - Not tested in production.
2. The maximum kernel clock frequencies can be limited by the maximum peripheral clock frequency (refer to each peripheral electrical characteristics).
3. This maximum kernel clock frequency does not consider the maximum ADC clock frequency (refer to [Table 95](#)).

### 5.3.2 VCAP external capacitor

The stabilization for the embedded LDO regulator is achieved by connecting an external capacitor  $C_{EXT}$  (whose value is specified in [Table 22](#)) to the VCAPx (one or two pins, depending upon the package). Two external capacitors must be connected to VCAP pins (refer to AN5711 “STM32H5 Series hardware development”).

Figure 23. External capacitor  $C_{EXT}$

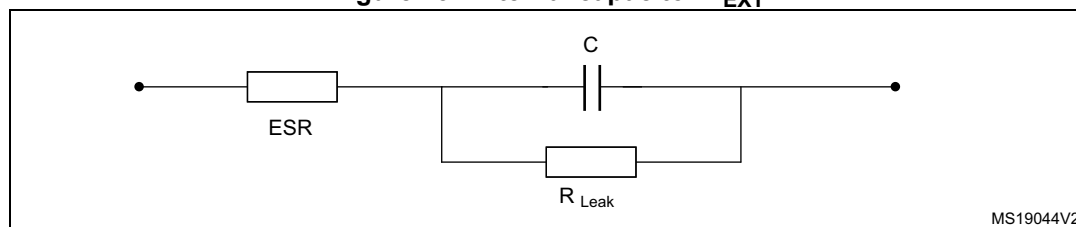


Table 22. Supply voltage and maximum frequency configuration

| Symbol    | Parameter                                              | Conditions        |
|-----------|--------------------------------------------------------|-------------------|
| $C_{EXT}$ | External capacitor for LDO enabled                     | 2.2 $\mu F^{(1)}$ |
| ESR       | Equivalent series resistance of the external capacitor | < 100 m $\Omega$  |

1. This value corresponds to  $C_{EXT}$  typical value. A variation of  $\pm 20\%$  is tolerated

### 5.3.3 SMPS step-down converter

The devices embed a high power efficiency SMPS step-down converter, that needs external components.

Table 23. Characteristics of SMPS step-down converter external components

| Symbol     | Parameter                                                                                  | Conditions                             | Min | Typ                | Max | Unit       |
|------------|--------------------------------------------------------------------------------------------|----------------------------------------|-----|--------------------|-----|------------|
| $C_{in}$   | Capacitance of external capacitor on VDDSMPS pins                                          | -                                      | -   | 4.7 <sup>(1)</sup> | -   | $\mu F$    |
|            | ESR of external capacitor                                                                  | 2.4 MHz                                | -   | -                  | 10  | m $\Omega$ |
| $C_{filt}$ | Capacitance of external capacitor on VLXSMPS pin                                           | -                                      | -   | 220                | -   | pF         |
| $C_{OUT}$  | Capacitance of external capacitor on VCAP pin                                              | -                                      | -   | 10 <sup>(1)</sup>  | -   | $\mu F$    |
|            | ESR of external capacitor                                                                  | 2.4 MHz                                | -   | -                  | 20  | m $\Omega$ |
| L          | Inductance of external inductor on VLXSMPS pin                                             | -                                      | -   | 2.2 <sup>(1)</sup> | -   | $\mu H$    |
|            | Series DC resistance                                                                       | All packages                           | -   | -                  | 150 | m $\Omega$ |
|            |                                                                                            | WLCSP80 package,<br>$V_{DDSMPS} > 3 V$ | -   | -                  | 300 |            |
| $I_{SAT}$  | DC current at which the inductance drops 30% from the value without current                | -                                      | 1   | -                  | -   | A          |
| $I_{RMS}$  | Average current for which the temperature of the inductor is raised 40°C by the DC current | -                                      | 1   | -                  | -   |            |

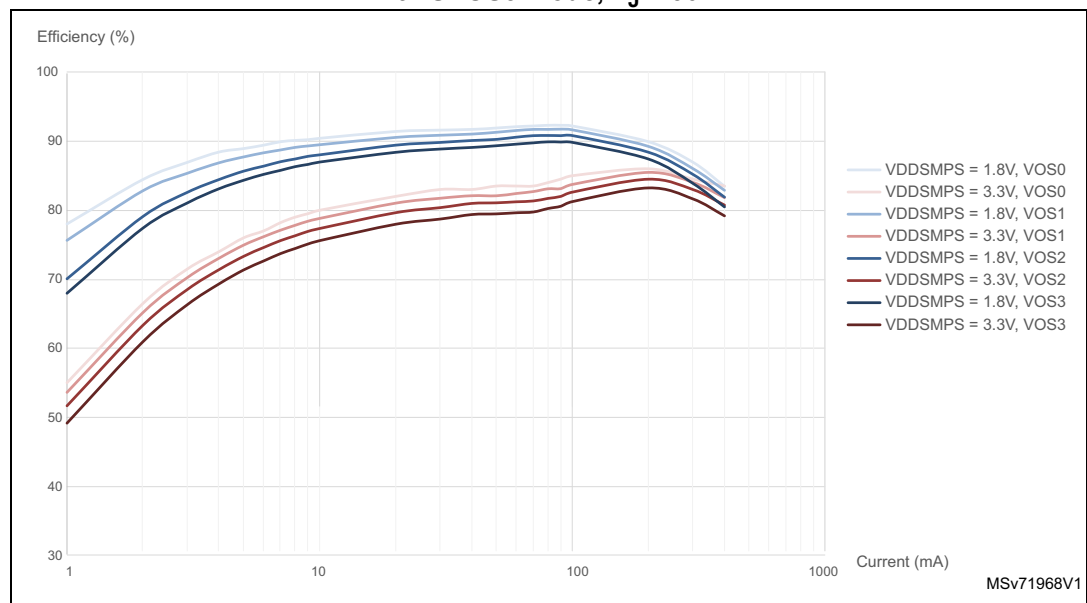
1. Tolerance: -50% and + 30% for all conditions.

The SMPS current consumption can be determined using the following formula based on the maximum LDO current consumption provided in [Section 5.3.7](#):

$$I_{DDSMPS} = I_{DDLDO} \times V_{CORE} / (V_{DD} \times \text{efficiency})$$

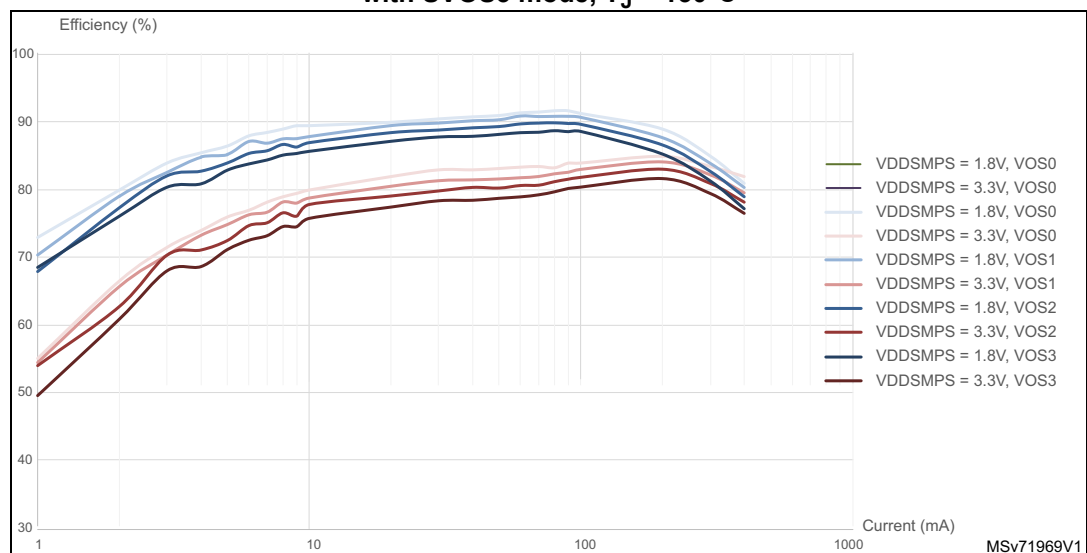
$I_{DDLDO}$  is the current in LDO configuration given in the following tables,  $V_{CORE}$  is the digital core supply (VCAP), and efficiency is defined in the following curves.

**Figure 24. SMPS efficiency versus load current in Run, Sleep, and Stop modes with SVOS3 mode,  $T_J = 30^\circ\text{C}$**

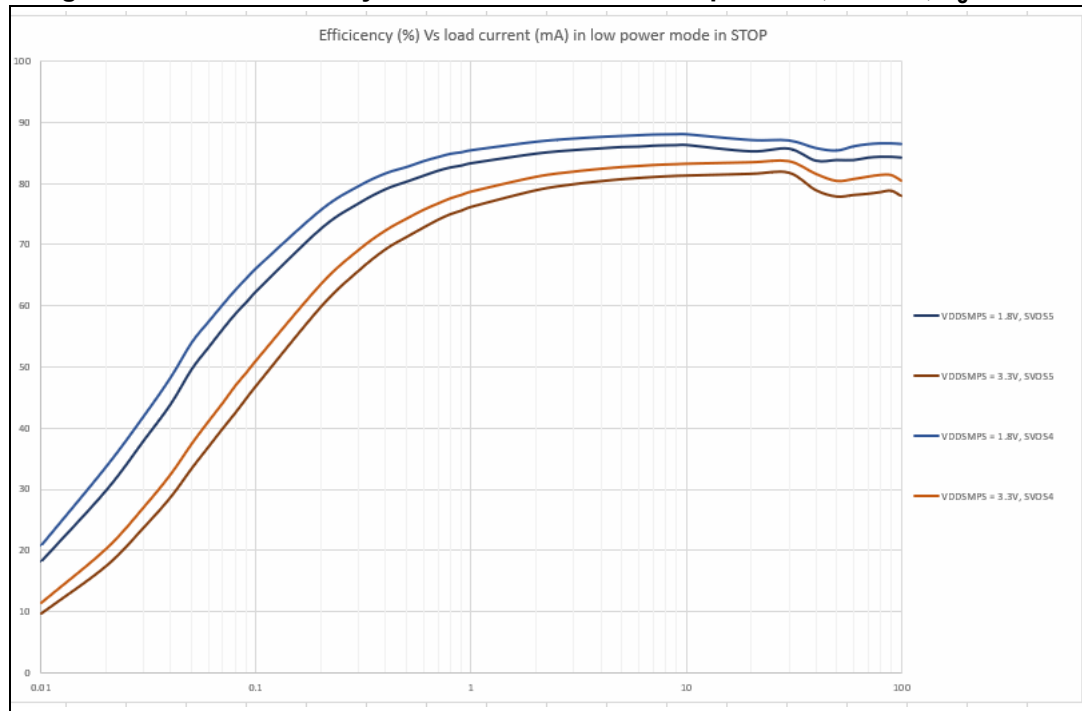
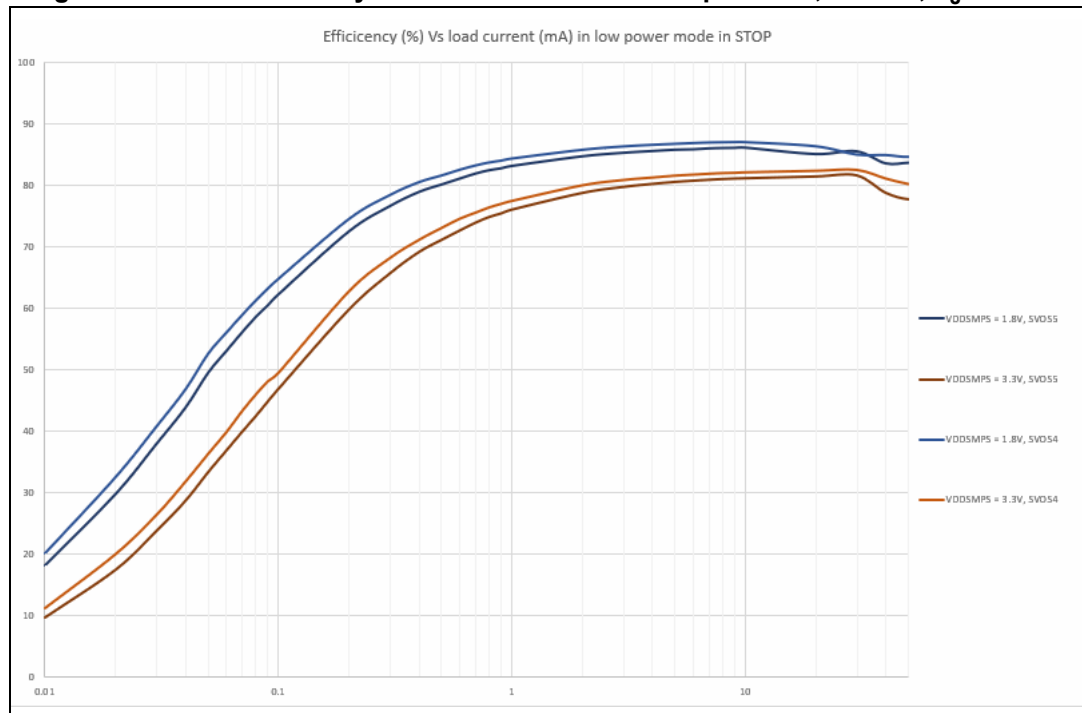


**Note:** SVOS3 is equivalent to VOS3 in Run and Sleep modes.

**Figure 25. SMPS efficiency versus load current in Run, Sleep, and Stop modes with SVOS3 mode,  $T_J = 130^\circ\text{C}$**



**Note:** SVOS3 is equivalent to VOS3 in Run and Sleep modes.

**Figure 26. SMPS efficiency versus load current in stop SVOV4, SVOS5,  $T_J = 30^\circ\text{C}$** **Figure 27. SMPS efficiency versus load current in stop SVOV4, SVOS5,  $T_J = 130^\circ\text{C}$** 

### 5.3.4 Operating conditions at power-up/down

Subject to general operating conditions for  $T_A$ .

**Table 24. Operating conditions at power-up/down (regulator ON)**

| Symbol       | Parameter                   | Min | Max      | Unit      |
|--------------|-----------------------------|-----|----------|-----------|
| $T_{VDD}$    | $V_{DD}$ rise time rate     | 0   | $\infty$ | $\mu s/V$ |
|              | $V_{DD}$ fall time rate     | 10  | $\infty$ |           |
| $T_{VDDA}$   | $V_{DDA}$ rise time rate    | 0   | $\infty$ |           |
|              | $V_{DDA}$ fall time rate    | 10  | $\infty$ |           |
| $T_{VDDUSB}$ | $T_{VDDUSB}$ rise time rate | 0   | $\infty$ |           |
|              | $T_{VDDUSB}$ fall time rate | 10  | $\infty$ |           |
| $T_{VDDIO2}$ | $T_{VDDIO2}$ rise time rate | 0   | $\infty$ |           |
|              | $T_{VDDIO2}$ fall time rate | 10  | $\infty$ |           |
| $T_{VBAT}$   | $T_{VBAT}$ rise time rate   | 0   | $\infty$ |           |
|              | $T_{VBAT}$ fall time rate   | 10  | $\infty$ |           |

### 5.3.5 Embedded reset and power control block characteristics

The parameters given in [Table 25](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 20](#).

**Table 25. Embedded reset and power control block characteristics<sup>(1)</sup>**

| Symbol               | Parameter                                   | Conditions      | Min  | Typ  | Max  | Unit    |
|----------------------|---------------------------------------------|-----------------|------|------|------|---------|
| $t_{RSTTEMPO}^{(2)}$ | Reset temporization after BOR0 detection    | $V_{DD}$ rising | -    | 377  | 550  | $\mu s$ |
| $V_{POR/PDR}$        | Power-on/down reset threshold (BORH_EN = 0) | Rising edge     | 1.62 | 1.67 | 1.71 | V       |
|                      |                                             | Falling edge    | 1.58 | 1.62 | 1.68 |         |
| $V_{BOR1}$           | Brownout reset threshold 1 (BORH_EN = 1)    | Rising edge     | 2.04 | 2.10 | 2.15 | V       |
|                      |                                             | Falling edge    | 1.95 | 2.00 | 2.06 |         |
| $V_{BOR2}$           | Brownout reset threshold 2 (BORH_EN = 1)    | Rising edge     | 2.34 | 2.41 | 2.47 |         |
|                      |                                             | Falling edge    | 2.25 | 2.31 | 2.37 |         |
| $V_{BOR3}$           | Brownout reset threshold 3 (BORH_EN = 1)    | Rising edge     | 2.63 | 2.70 | 2.78 |         |
|                      |                                             | Falling edge    | 2.54 | 2.61 | 2.68 |         |

Table 25. Embedded reset and power control block characteristics<sup>(1)</sup> (continued)

| Symbol                                   | Parameter                                                                   | Conditions             | Min  | Typ  | Max   | Unit |
|------------------------------------------|-----------------------------------------------------------------------------|------------------------|------|------|-------|------|
| V <sub>PVD0</sub>                        | PVD threshold 0                                                             | Rising edge            | 1.90 | 1.96 | 2.01  | V    |
|                                          |                                                                             | Falling edge           | 1.81 | 1.86 | 1.91  |      |
| V <sub>PVD1</sub>                        | PVD threshold 1                                                             | Rising edge            | 2.05 | 2.10 | 2.16  |      |
|                                          |                                                                             | Falling edge           | 1.96 | 2.01 | 2.06  |      |
| V <sub>PVD2</sub>                        | PVD threshold 2                                                             | Rising edge            | 2.19 | 2.26 | 2.32  |      |
|                                          |                                                                             | Falling edge           | 2.10 | 2.15 | 2.21  |      |
| V <sub>PVD3</sub>                        | PVD threshold 3                                                             | Rising edge            | 2.35 | 2.41 | 2.47  |      |
|                                          |                                                                             | Falling edge           | 2.25 | 2.31 | 2.37  |      |
| V <sub>PVD4</sub>                        | PVD threshold 4                                                             | Rising edge            | 2.49 | 2.56 | 2.62  |      |
|                                          |                                                                             | Falling edge           | 2.39 | 2.45 | 2.51  |      |
| V <sub>PVD5</sub>                        | PVD threshold 5                                                             | Rising edge            | 2.64 | 2.71 | 2.78  |      |
|                                          |                                                                             | Falling edge           | 2.55 | 2.61 | 2.68  |      |
| V <sub>PVD6</sub>                        | PVD threshold 6                                                             | Rising edge            | 2.78 | 2.86 | 2.94  |      |
|                                          |                                                                             | Falling edge           | 2.69 | 2.76 | 2.83  |      |
| V <sub>POR/PDR</sub>                     | Hysteresis for power-on/down reset                                          | Hysteresis in Run mode | -    | 43   | -     | mV   |
| V <sub>hyst_BOR_PVD</sub>                | Hysteresis voltage of BOR (unless BORH_EN = 0) and PVD                      | -                      | -    | 100  | -     |      |
| I <sub>DD_BOR_PVD</sub> <sup>(2)</sup>   | BOR and PVD consumption from V <sub>DD</sub>                                | -                      | -    | -    | 0.630 | μA   |
| I <sub>DD_POR_PDR</sub>                  | POR and PDR consumption from V <sub>DD</sub>                                | -                      | 0.8  | -    | 1.2   |      |
| V <sub>AVD0</sub>                        | V <sub>DDA</sub> voltage monitor 0 threshold                                | Rising edge            | 1.66 | 1.71 | 1.76  | V    |
|                                          |                                                                             | Falling edge           | 1.56 | 1.61 | 1.66  |      |
| V <sub>AVD1</sub>                        | V <sub>DDA</sub> voltage monitor 1 threshold                                | Rising edge            | 2.06 | 2.12 | 2.19  |      |
|                                          |                                                                             | Falling edge           | 1.96 | 2.02 | 2.08  |      |
| V <sub>AVD2</sub>                        | V <sub>DDA</sub> voltage monitor 2 threshold                                | Rising edge            | 2.42 | 2.50 | 2.58  |      |
|                                          |                                                                             | Falling edge           | 2.35 | 2.42 | 2.49  |      |
| V <sub>AVD3</sub>                        | V <sub>DDA</sub> voltage monitor 3 threshold                                | Rising edge            | 2.74 | 2.83 | 2.91  | V    |
|                                          |                                                                             | Falling edge           | 2.64 | 2.72 | 2.80  |      |
| V <sub>IO2VM</sub>                       | V <sub>DDIO2</sub> voltage monitor threshold                                | -                      | -    | 0.9  | -     | V    |
| V <sub>hyst_AVD</sub>                    | Hysteresis of V <sub>DDA</sub> voltage monitor                              | -                      | -    | 100  | -     | mV   |
| I <sub>DD_AVD_IO2VM</sub> <sup>(2)</sup> | Power voltage detector consumption from V <sub>DD</sub> (AVD, IO2VM)        | -                      | -    | -    | 0.25  | μA   |
| I <sub>DD_AVD_A</sub> <sup>(2)</sup>     | Analog voltage detector consumption from V <sub>DDA</sub> (resistor bridge) | -                      | -    | -    | 0.25  |      |

1. Evaluated by characterization and not tested in production, unless otherwise specified.

2. Specified by design - Not tested in production

### 5.3.6 Embedded reference voltage

The parameters given in [Table 26](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20](#).

**Table 26. Embedded reference voltage**

| Symbol                     | Parameter                                                      | Conditions                                         | Min   | Typ   | Max   | Unit                    |
|----------------------------|----------------------------------------------------------------|----------------------------------------------------|-------|-------|-------|-------------------------|
| $V_{REFINT}^{(1)}$         | Internal reference voltage                                     | $-40^{\circ}\text{C} < T_J < +130^{\circ}\text{C}$ | 1.180 | 1.216 | 1.255 | V                       |
| $t_{S\_vrefint}^{(2)(3)}$  | ADC sampling time when reading the internal reference voltage  | -                                                  | 4.3   | -     | -     | $\mu\text{s}$           |
| $t_{start\_vrefint}^{(3)}$ | Start time of reference voltage buffer when the ADC is enabled | -                                                  | -     | -     | 4.4   |                         |
| $I_{refbuf}^{(3)}$         | Reference buffer consumption for ADC                           | $V_{DD} = 3.3\text{ V}$                            | 9     | 13.5  | 23    | $\mu\text{A}$           |
| $\Delta V_{REFINT}^{(3)}$  | Internal reference voltage spread over the temperature range   | $-40^{\circ}\text{C} < T_J < +130^{\circ}\text{C}$ | -     | 5     | 15    | mV                      |
| $T_{Ccoeff}$               | Average temperature coefficient                                | Average temperature coefficient                    | -     | 20    | 70    | ppm/ $^{\circ}\text{C}$ |
| $V_{DDcoeff}$              | Average voltage coefficient                                    | $3.0\text{ V} < V_{DD} < 3.6\text{ V}$             | -     | 10    | 1370  | ppm/V                   |
| $V_{REFINT\_DIV1}^{(3)}$   | 1/4 reference voltage                                          | -                                                  | -     | 25    | -     | % $V_{REFINT}$          |
| $V_{REFINT\_DIV2}^{(3)}$   | 1/2 reference voltage                                          |                                                    | -     | 50    | -     |                         |
| $V_{REFINT\_DIV3}^{(3)}$   | 3/4 reference voltage                                          |                                                    | -     | 75    | -     |                         |

1.  $V_{REFINT}$  does not take into account package and soldering effects.
2. The shortest sampling time for the application can be determined by multiple iterations.
3. Specified by design - Not tested in production.

**Table 27. Internal reference voltage calibration value**

| Symbol            | Parameter                                                            | Memory address            |
|-------------------|----------------------------------------------------------------------|---------------------------|
| $V_{REFINT\_CAL}$ | Raw data acquired at $30^{\circ}\text{C}$ , $V_{DDA} = 3.3\text{ V}$ | 0x08FF F810 - 0x08FF F811 |

### 5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory, and executed binary code.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.

- The flash memory access time is adjusted with the minimum wait-state number, depending on the  $f_{HCLK}$  frequency (refer to the tables detailing recommended number of wait states and programming delay available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency, and the APB clock frequency is AHB frequency.

The parameters given in the following tables are derived from tests performed under supply voltage conditions summarized in [Table 20](#), and, unless otherwise specified, at ambient temperature.

The maximum current consumption is given for LDO regulator ON.

**Table 28. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 2-way instruction cache ON, PREFETCH ON**

| Symbol               | Parameter                     | Conditions                  |      | f <sub>HCLK</sub><br>(MHz) | Typ<br>LDO | Typ<br>SMPS | Max <sup>(1)(2)</sup>    |                          |                           |                           | Unit |
|----------------------|-------------------------------|-----------------------------|------|----------------------------|------------|-------------|--------------------------|--------------------------|---------------------------|---------------------------|------|
|                      |                               |                             |      |                            |            |             | T <sub>J</sub> =<br>25°C | T <sub>J</sub> =<br>85°C | T <sub>J</sub> =<br>105°C | T <sub>J</sub> =<br>130°C |      |
| I <sub>DD(Run)</sub> | Supply current<br>in Run mode | All peripherals<br>disabled | VOS0 | 250                        | 32.1       | 17.5        | 37                       | 65                       | 87                        | -                         | mA   |
|                      |                               |                             |      | 215                        | 27.9       | 15.0        | 32                       | 60                       | 82                        | -                         |      |
|                      |                               |                             |      | 200                        | 25.7       | 13.8        | 30                       | 59                       | 81                        | -                         |      |
|                      |                               |                             | VOS1 | 200                        | 22.1       | 11.0        | 25                       | 45                       | 62                        | 93                        |      |
|                      |                               |                             |      | 180                        | 20.3       | 10.1        | 23                       | 43                       | 59                        | 90                        |      |
|                      |                               |                             |      | 168                        | 18.8       | 9.3         | 21                       | 42                       | 58                        | 89                        |      |
|                      |                               |                             | VOS2 | 150                        | 16.9       | 8.5         | 20                       | 40                       | 56                        | 88                        |      |
|                      |                               |                             |      | 150                        | 15.4       | 7.4         | 17                       | 33                       | 47                        | 73                        |      |
|                      |                               |                             | VOS3 | 100                        | 10.8       | 5.2         | 13                       | 28                       | 41                        | 68                        |      |
|                      |                               |                             |      | 100                        | 9.8        | 4.5         | 11                       | 23                       | 34                        | 55                        |      |
|                      |                               |                             |      | 60                         | 6.4        | 3.0         | 8.0                      | 20                       | 30                        | 52                        |      |
|                      |                               |                             | 25   | 3.2                        | 1.7        | 5.0         | 17                       | 27                       | 49                        |                           |      |
|                      |                               | All peripherals<br>enabled  | VOS0 | 250                        | 86.8       | 49.8        | 90                       | 118                      | 140                       | -                         |      |
|                      |                               |                             |      | 215                        | 75.0       | 43.2        | 78                       | 107                      | 128                       | -                         |      |
|                      |                               |                             |      | 200                        | 69.5       | 40.1        | 72                       | 102                      | 123                       | -                         |      |
|                      |                               |                             | VOS1 | 200                        | 60.7       | 31.7        | 62                       | 82                       | 99                        | 130                       |      |
|                      |                               |                             |      | 180                        | 55.1       | 28.5        | 56                       | 76                       | 92                        | 124                       |      |
|                      |                               |                             |      | 150                        | 45.8       | 23.4        | 47                       | 68                       | 84                        | 116                       |      |
|                      |                               |                             | VOS2 | 150                        | 41.9       | 20.0        | 43                       | 59                       | 72                        | 98                        |      |
|                      |                               |                             |      | 100                        | 28.5       | 13.8        | 30                       | 45                       | 58                        | 85                        |      |
|                      |                               |                             | VOS3 | 100                        | 25.9       | 11.7        | 27                       | 39                       | 49                        | 71                        |      |
|                      |                               |                             |      | 60                         | 16.2       | 7.5         | 17                       | 29                       | 40                        | 61                        |      |
|                      |                               |                             |      | 25                         | 7.5        | 3.8         | 9.0                      | 21                       | 31                        | 53                        |      |

1. Evaluated by characterization - Not tested in production.

2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

**Table 29. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 1-way instruction cache ON, PREFETCH ON**

| Symbol                | Parameter                     | Conditions                  |      | f <sub>HCLK</sub><br>(MHz) | Typ<br>LDO | Typ<br>SMPS | Max <sup>(1)(2)</sup>    |                          |                           |                           | Unit |
|-----------------------|-------------------------------|-----------------------------|------|----------------------------|------------|-------------|--------------------------|--------------------------|---------------------------|---------------------------|------|
|                       |                               |                             |      |                            |            |             | T <sub>J</sub> =<br>25°C | T <sub>J</sub> =<br>85°C | T <sub>J</sub> =<br>105°C | T <sub>J</sub> =<br>130°C |      |
| I <sub>DD</sub> (Run) | Supply current<br>in Run mode | All peripherals<br>disabled | VOS0 | 250                        | 29.2       | 15.9        | 34                       | 62                       | 84                        | -                         | mA   |
|                       |                               |                             |      | 200                        | 23.3       | 12.5        | 28                       | 56                       | 78                        | -                         |      |
|                       |                               |                             | VOS1 | 200                        | 20.1       | 10.0        | 23                       | 43                       | 59                        | 91                        |      |
|                       |                               |                             |      | 180                        | 18.5       | 9.2         | 21                       | 41                       | 57                        | 89                        |      |
|                       |                               |                             |      | 150                        | 15.4       | 7.8         | 18                       | 38                       | 54                        | 86                        |      |
|                       |                               |                             | VOS2 | 150                        | 14.0       | 6.7         | 16                       | 32                       | 45                        | 71                        |      |
|                       |                               |                             |      | 100                        | 9.8        | 4.8         | 12                       | 27                       | 40                        | 67                        |      |
|                       |                               |                             | VOS3 | 100                        | 8.9        | 4.2         | 10                       | 22                       | 33                        | 54                        |      |
|                       |                               |                             |      | 25                         | 3.0        | 1.6         | 4.0                      | 17                       | 27                        | 49                        |      |

1. Evaluated by characterization - Not tested in production.

2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

**Table 30. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-way**

| Symbol                   | Parameter                     | Conditions                  |      | f <sub>HCLK</sub><br>(MHz) | Typ<br>LDO | Typ<br>SMPS | Max <sup>(1)(2)</sup>    |                          |                           |                           | Unit |
|--------------------------|-------------------------------|-----------------------------|------|----------------------------|------------|-------------|--------------------------|--------------------------|---------------------------|---------------------------|------|
|                          |                               |                             |      |                            |            |             | T <sub>J</sub> =<br>25°C | T <sub>J</sub> =<br>85°C | T <sub>J</sub> =<br>105°C | T <sub>J</sub> =<br>130°C |      |
| I <sub>DD</sub><br>(Run) | Supply current<br>in Run mode | All peripherals<br>disabled | VOS0 | 250                        | 27.8       | 15.5        | 32                       | 61                       | 82                        | -                         | mA   |
|                          |                               |                             |      | 215                        | 24.1       | 13.4        | 29                       | 57                       | 79                        | -                         |      |
|                          |                               |                             |      | 200                        | 22.1       | 12.3        | 27                       | 55                       | 77                        | -                         |      |
|                          |                               |                             | VOS1 | 200                        | 19.1       | 9.9         | 22                       | 42                       | 58                        | 90                        |      |
|                          |                               |                             |      | 180                        | 17.6       | 9.1         | 20                       | 40                       | 56                        | 88                        |      |
|                          |                               |                             |      | 150                        | 14.6       | 7.6         | 22                       | 42                       | 58                        | 90                        |      |
|                          |                               |                             | VOS2 | 150                        | 13.3       | 6.6         | 17                       | 37                       | 53                        | 85                        |      |
|                          |                               |                             |      | 100                        | 9.4        | 4.7         | 11                       | 27                       | 40                        | 66                        |      |
|                          |                               |                             | VOS3 | 100                        | 8.5        | 4.1         | 10                       | 22                       | 33                        | 54                        |      |
|                          |                               |                             |      | 60                         | 5.6        | 2.8         | 7                        | 19                       | 30                        | 51                        |      |
|                          |                               |                             |      | 25                         | 2.9        | 1.6         | 4                        | 16                       | 27                        | 48                        |      |
|                          |                               |                             |      |                            |            |             |                          |                          |                           |                           |      |

1. Evaluated by characterization - Not tested in production.

2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 31. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 2-way

| Symbol               | Parameter                     | Conditions                  |      | f <sub>HCLK</sub><br>(MHz) | Typ<br>LDO | Typ<br>SMPS | Max <sup>(1)(2)</sup>    |                          |                           |                           | Unit |
|----------------------|-------------------------------|-----------------------------|------|----------------------------|------------|-------------|--------------------------|--------------------------|---------------------------|---------------------------|------|
|                      |                               |                             |      |                            |            |             | T <sub>J</sub> =<br>25°C | T <sub>J</sub> =<br>85°C | T <sub>J</sub> =<br>105°C | T <sub>J</sub> =<br>130°C |      |
| I <sub>DD(Run)</sub> | Supply current<br>in Run mode | All peripherals<br>disabled | VOS0 | 250                        | 30.8       | 17.2        | 35                       | 64                       | 86                        | -                         | mA   |
|                      |                               |                             |      | 215                        | 26.7       | 14.4        | 31                       | 60                       | 81                        | -                         |      |
|                      |                               |                             |      | 200                        | 24.6       | 13.3        | 29                       | 58                       | 80                        | -                         |      |
|                      |                               |                             | VOS1 | 200                        | 21.2       | 10.5        | 24                       | 44                       | 61                        | 93                        |      |
|                      |                               |                             |      | 180                        | 19.5       | 9.7         | 22                       | 42                       | 58                        | 90                        |      |
|                      |                               |                             |      | 168                        | 18.0       | 9.0         | 21                       | 41                       | 57                        | 89                        |      |
|                      |                               |                             | VOS2 | 150                        | 16.2       | 8.4         | 19                       | 39                       | 55                        | 87                        |      |
|                      |                               |                             |      | 150                        | 14.8       | 7.2         | 17                       | 33                       | 46                        | 72                        |      |
|                      |                               |                             | VOS3 | 100                        | 10.3       | 5.1         | 12                       | 28                       | 41                        | 67                        |      |
|                      |                               |                             |      | 100                        | 9.4        | 4.5         | 11                       | 23                       | 33                        | 55                        |      |
|                      |                               |                             |      | 60                         | 6.1        | 2.9         | 8.0                      | 20                       | 30                        | 52                        |      |
|                      |                               |                             | 25   | 3.2                        | 1.7        | 5.0         | 17                       | 27                       | 49                        |                           |      |

1. Evaluated by characterization - Not tested in production.

2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

**Table 32. Typical consumption in Run mode with CoreMark running from flash memory and SRAM<sup>(1)</sup>**

| Symbol               | Parameter                  | Conditions                                                     |       | f <sub>HCLK</sub><br>(MHz) | Typ<br>LDO | Typ<br>SMPS | Unit | Typ<br>LDO | Typ<br>SMPS | Unit   |
|----------------------|----------------------------|----------------------------------------------------------------|-------|----------------------------|------------|-------------|------|------------|-------------|--------|
|                      |                            | Peripheral                                                     | Code  |                            |            |             |      |            |             |        |
| I <sub>DD(Run)</sub> | Supply current in Run mode | All peripherals disabled, instruction cache 2-way, prefetch ON | FLASH | 250                        | 32.1       | 17.5        | mA   | 128.6      | 70.1        | μA/MHz |
|                      |                            |                                                                |       | 200                        | 22.1       | 10.97       |      | 110.7      | 54.8        |        |
|                      |                            |                                                                |       | 168                        | 18.8       | 9.3         |      | 111.8      | 55.6        |        |
|                      |                            |                                                                |       | 150                        | 15.4       | 8.5         |      | 102.7      | 56.9        |        |
|                      |                            |                                                                |       | 100                        | 9.8        | 4.5         |      | 97.9       | 45.3        |        |
|                      |                            | All peripherals disabled, instruction cache 1-way, prefetch ON | FLASH | 250                        | 29.2       | 15.9        |      | 116.6      | 63.8        |        |
|                      |                            |                                                                |       | 200                        | 20.1       | 12.5        |      | 100.4      | 62.7        |        |
|                      |                            |                                                                |       | 150                        | 14.0       | 10.0        |      | 93.3       | 66.4        |        |
|                      |                            |                                                                |       | 100                        | 8.9        | 4.2         |      | 88.9       | 41.7        |        |
|                      |                            | All peripherals disabled, instruction cache 2-way              | SRAM  | 250                        | 30.8       | 17.2        |      | 123.3      | 68.7        |        |
|                      |                            |                                                                |       | 200                        | 21.2       | 10.5        |      | 106.2      | 52.6        |        |
|                      |                            |                                                                |       | 168                        | 18.0       | 9.0         |      | 107.3      | 53.4        |        |
|                      |                            |                                                                |       | 150                        | 14.8       | 7.2         |      | 98.5       | 48.2        |        |
|                      |                            |                                                                |       | 100                        | 9.4        | 4.5         |      | 94.1       | 44.6        |        |
|                      |                            | All peripherals disabled, instruction cache 1-way              | SRAM  | 250                        | 27.8       | 15.5        |      | 111.1      | 61.9        |        |
|                      |                            |                                                                |       | 200                        | 19.1       | 9.9         |      | 95.4       | 49.3        |        |
|                      |                            |                                                                |       | 150                        | 13.3       | 6.6         |      | 88.9       | 43.8        |        |
|                      |                            |                                                                |       | 100                        | 8.5        | 4.1         |      | 84.9       | 40.7        |        |

1. Evaluated by characterization - Not tested in production.

**Table 33. Typical consumption in Run mode with SecureMark running from flash memory and SRAM<sup>(1)</sup>**

| Symbol               | Parameter                  | Conditions                                                     |       | f <sub>HCLK</sub><br>(MHz) | Typ<br>LDO | Typ<br>SMPS | Unit | Typ<br>LDO | Typ<br>SMPS | Unit   |
|----------------------|----------------------------|----------------------------------------------------------------|-------|----------------------------|------------|-------------|------|------------|-------------|--------|
|                      |                            | Peripheral                                                     | Code  |                            |            |             |      |            |             |        |
| I <sub>DD(Run)</sub> | Supply current in Run mode | All peripherals disabled, instruction cache 2-way, prefetch ON | FLASH | 250                        | 34.1       | 17.9        | mA   | 136.3      | 71.8        | μA/MHz |
|                      |                            |                                                                |       | 180                        | 21.8       | 10.6        |      | 120.9      | 58.8        |        |
|                      |                            |                                                                |       | 168                        | 20.1       | 9.8         |      | 119.7      | 58.5        |        |
|                      |                            |                                                                |       | 150                        | 24.9       | 7.7         |      | 166.2      | 51.2        |        |
|                      |                            |                                                                |       | 100                        | 10.6       | 4.8         |      | 106.0      | 47.6        |        |
|                      |                            | All peripherals disabled, instruction cache 1-way, prefetch ON | FLASH | 250                        | 31.3       | 16.6        |      | 125.2      | 66.3        |        |
|                      |                            |                                                                |       | 180                        | 20.1       | 9.8         |      | 111.6      | 54.5        |        |
|                      |                            |                                                                |       | 168                        | 18.5       | 9.1         |      | 110.4      | 54.2        |        |
|                      |                            |                                                                |       | 150                        | 18.8       | 7.2         |      | 125.1      | 47.7        |        |
|                      |                            |                                                                |       | 100                        | 9.8        | 4.5         |      | 98.3       | 44.5        |        |

1. Evaluated by characterization - Not tested in production.

**Table 34. Typical and maximum current consumption in Sleep mode**

| Symbol                 | Parameter                       | Conditions                  |      | f <sub>HCLK</sub><br>(MHz) | Typ<br>LDO | Typ<br>SMPS | Max <sup>(1) (2)</sup>   |                          |                           |                           | Unit |
|------------------------|---------------------------------|-----------------------------|------|----------------------------|------------|-------------|--------------------------|--------------------------|---------------------------|---------------------------|------|
|                        |                                 |                             |      |                            |            |             | T <sub>J</sub> =<br>25°C | T <sub>J</sub> =<br>85°C | T <sub>J</sub> =<br>105°C | T <sub>J</sub> =<br>130°C |      |
| I <sub>DD(sleep)</sub> | Supply current<br>in sleep mode | All peripherals<br>disabled | VOS0 | 250                        | 7.3        | 4.2         | 12                       | 40                       | 61                        | -                         | mA   |
|                        |                                 |                             |      | 200                        | 5.8        | 3.3         | 10                       | 38                       | 60                        | -                         |      |
|                        |                                 |                             | VOS1 | 200                        | 4.8        | 2.6         | 8                        | 27                       | 43                        | 75                        |      |
|                        |                                 |                             |      | 180                        | 4.8        | 2.6         | 8                        | 27                       | 43                        | 75                        |      |
|                        |                                 |                             |      | 168                        | 4.3        | 2.3         | 7                        | 26                       | 42                        | 74                        |      |
|                        |                                 |                             |      | 150                        | 3.9        | 2.2         | 7                        | 26                       | 42                        | 74                        |      |
|                        |                                 |                             | VOS2 | 150                        | 3.5        | 1.9         | 6                        | 21                       | 34                        | 60                        |      |
|                        |                                 |                             |      | 100                        | 2.8        | 1.6         | 5                        | 20                       | 33                        | 59                        |      |
|                        |                                 |                             | VOS3 | 100                        | 2.5        | 1.4         | 4                        | 16                       | 26                        | 48                        |      |
|                        |                                 |                             |      | 60                         | 2.0        | 1.2         | 4                        | 15                       | 26                        | 47                        |      |

1. Evaluated by characterization - Not tested in production.

2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 35. Typical and maximum current consumption in Stop mode

| Symbol                | Parameter              | Conditions                                                          |       | Typ LDO | Typ SMPS | Max <sup>(1) (2)</sup> |                       |                        |                        | Unit |
|-----------------------|------------------------|---------------------------------------------------------------------|-------|---------|----------|------------------------|-----------------------|------------------------|------------------------|------|
|                       |                        |                                                                     |       |         |          | T <sub>J</sub> = 25°C  | T <sub>J</sub> = 85°C | T <sub>J</sub> = 105°C | T <sub>J</sub> = 130°C |      |
| I <sub>DD(stop)</sub> | Supply current in Stop | Flash memory in low power mode, SRAMs ON                            | SVOS3 | 0.37    | 0.09     | 2.00                   | 13.98                 | 24.00                  | 44.39                  | mA   |
|                       |                        |                                                                     | SVOS4 | 0.27    | 0.07     | 1.40                   | 10.48                 | 18.37                  | 34.76                  |      |
|                       |                        |                                                                     | SVOS5 | 0.19    | 0.06     | 0.86                   | 7.08                  | 12.88                  | 25.31                  |      |
|                       |                        | Flash memory in normal mode, SRAMs ON                               | SVOS3 | 0.38    | 0.10     | 2.02                   | 14.01                 | 24.06                  | 44.55                  |      |
|                       |                        |                                                                     | SVOS4 | 0.29    | 0.09     | 1.42                   | 10.52                 | 18.46                  | 34.88                  |      |
|                       |                        | Flash memory in low power mode, SRAMs OFF except SRAM2 16 Kbytes ON | SVOS3 | 0.34    | 0.09     | 1.93                   | 13.28                 | 22.75                  | 41.99                  |      |
|                       |                        |                                                                     | SVOS4 | 0.25    | 0.07     | 1.35                   | 9.87                  | 17.33                  | 32.65                  |      |
|                       |                        |                                                                     | SVOS5 | 0.17    | 0.05     | 0.81                   | 6.46                  | 11.68                  | 22.86                  |      |
|                       |                        | Flash memory in low power mode, SRAMs OFF except SRAM2 ON           | SVOS3 | 0.35    | 0.10     | 1.95                   | 13.45                 | 23.02                  | 42.52                  |      |
|                       |                        |                                                                     | SVOS4 | 0.26    | 0.08     | 1.36                   | 10.01                 | 17.52                  | 33.10                  |      |
|                       |                        |                                                                     | SVOS5 | 0.17    | 0.08     | 0.82                   | 6.59                  | 11.92                  | 23.37                  |      |

1. Evaluated by characterization - Not tested in production.

2. The maximum values are given for LDO regulator ON. Refer to [Section 5.3.3](#) for the SMPS maximum current consumption.

Table 36. Typical and maximum current consumption in Standby mode

| Symbol                   | Parameter                                | Conditions |                            | Typ <sup>(1)</sup> |       |      |       | Max <sup>(1)</sup>    |                       |                        |                        | Unit |
|--------------------------|------------------------------------------|------------|----------------------------|--------------------|-------|------|-------|-----------------------|-----------------------|------------------------|------------------------|------|
|                          |                                          | Backup RAM | RTC and LSE <sup>(2)</sup> | 1.8 V              | 2.4 V | 3 V  | 3.3 V | T <sub>J</sub> = 25°C | T <sub>J</sub> = 85°C | T <sub>J</sub> = 105°C | T <sub>J</sub> = 130°C |      |
| I <sub>DD(standby)</sub> | Supply current in standby mode, IWDG OFF | OFF        | OFF                        | 2.58               | 2.78  | 3.01 | 3.19  | 5.9                   | 11.7                  | 21.2                   | 53                     | μA   |
|                          |                                          | ON         | OFF                        | 3.79               | 4.05  | 4.38 | 4.63  | 8.2                   | 21.0                  | 37.0                   | 90                     |      |
|                          |                                          | OFF        | ON                         | 2.91               | 3.15  | 3.47 | 3.67  | 6.9                   | 12.9                  | 22.5                   | 55                     |      |
|                          |                                          | ON         | ON                         | 4.16               | 4.46  | 4.85 | 5.12  | 9.2                   | 22.2                  | 38.3                   | 92                     |      |

1. Evaluated by characterization - Not tested in production.

2. LSE is in medium-low drive mode.

Table 37. Typical and maximum current consumption in V<sub>BAT</sub> mode<sup>(1)</sup>

| Symbol                | Parameter                               | Conditions |                            | Typ   |       |      |       | Max                    |                        |                         |                         | Unit |
|-----------------------|-----------------------------------------|------------|----------------------------|-------|-------|------|-------|------------------------|------------------------|-------------------------|-------------------------|------|
|                       |                                         | Backup RAM | RTC and LSE <sup>(2)</sup> | 1.8 V | 2.4 V | 3 V  | 3.3 V | T <sub>J</sub> = 25 °C | T <sub>J</sub> = 85 °C | T <sub>J</sub> = 105 °C | T <sub>J</sub> = 130 °C |      |
| I <sub>DD(VBAT)</sub> | Supply current in V <sub>BAT</sub> mode | OFF        | OFF                        | 0.01  | 0.01  | 0.02 | 0.02  | 0.2                    | 2.45                   | 6.2                     | 19.0                    | μA   |
|                       |                                         | ON         | OFF                        | 1.11  | 1.14  | 1.17 | 1.29  | 4.5                    | 16.05                  | 30.0                    | 72.2                    |      |
|                       |                                         | OFF        | ON                         | 0.45  | 0.46  | 0.48 | 0.59  | 1.2                    | 3.65                   | 7.5                     | 21.0                    |      |
|                       |                                         | ON         | ON                         | 1.56  | 1.57  | 1.62 | 1.84  | 5.5                    | 17.25                  | 31.3                    | 74.2                    |      |

1. Evaluated by characterization - Not tested in production.

2. LSE is in medium-low drive mode.

### I/O system current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 58](#).

To estimate the current consumption for the output pins, consider also external pull-downs or loads.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this current consumption can be avoided by configuring the I/Os in analog mode. This is notably the case of ADC input pins, to be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.

In addition to the internal peripheral current consumption, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I<sub>SW</sub> is the current sunk by a switching I/O to charge/discharge the capacitive load

V<sub>DDx</sub> is the MCU supply voltage

f<sub>SW</sub> is the I/O switching frequency

C<sub>L</sub> is the total capacitance seen by the I/O pin: C = C<sub>INT</sub> + C<sub>EXT</sub> + C<sub>S</sub>

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**On-chip peripheral current consumption**

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration
- All peripherals are disabled unless otherwise mentioned
- The I/O compensation cell is enabled
- $f_{HCLK}$  is the CPU clock,  $f_{PCLK} = f_{rcc\_cpu\_ck}$ , and  $f_{HCLK} = f_{rcc\_cpu\_ck}$ .

The given value is calculated by measuring the difference of current consumption:

- with all peripherals clocked off
- with only one peripheral clocked on
- $f_{rcc\_cpu\_ck} = 250$  MHz (Scale 0),  $f_{rcc\_cpu\_ck} = 200$  MHz (Scale 1),  $f_{rcc\_cpu\_ck} = 150$  MHz (Scale 2),  $f_{rcc\_cpu\_ck} = 100$  MHz (Scale 3)
- the ambient operating temperature is 25°C and  $V_{DD} = 3.0$  V

**Table 38. Peripheral current consumption in Sleep mode**

| Bus  | Peripheral | $I_{DD}$ (typ) |      |      |      | Unit        |
|------|------------|----------------|------|------|------|-------------|
|      |            | VOS0           | VOS1 | VOS2 | VOS3 |             |
| AHB1 | SRAM1      | 0.9            | 0.85 | 0.78 | 0.7  | $\mu A/MHz$ |
|      | BKPRAM     | 0.95           | 0.89 | 0.82 | 0.74 |             |
|      | CORDIC     | 0.5            | 0.45 | 0.42 | 0.4  |             |
|      | CRC        | 0.22           | 0.21 | 0.18 | 0.18 |             |
|      | DCACHE     | 0.66           | 0.59 | 0.55 | 0.51 |             |
|      | ETH        | 11.33          | 10   | 9.13 | 8.32 |             |
|      | FLASH      | 10.19          | 8.87 | 8.09 | 7.35 |             |
|      | FMAC       | 2.07           | 1.84 | 1.68 | 1.56 |             |
|      | GPDMA1     | 0.62           | 0.55 | 0.51 | 0.45 |             |
|      | GPDMA2     | 0.45           | 0.43 | 0.38 | 0.35 |             |
|      | GTZC1      | 1.19           | 1.05 | 0.97 | 0.9  |             |
|      | ICACHE     | 0.86           | 0.81 | 0.75 | 0.67 |             |
|      | RAMCFG     | 0.88           | 0.79 | 0.71 | 0.67 |             |
|      | AHB1       | 1.09           | 0.94 | 0.86 | 0.79 |             |

Table 38. Peripheral current consumption in Sleep mode (continued)

| Bus  | Peripheral | I <sub>DD</sub> (typ) |      |      |      | Unit   |
|------|------------|-----------------------|------|------|------|--------|
|      |            | VOS0                  | VOS1 | VOS2 | VOS3 |        |
| AHB2 | ADC12      | 2.35                  | 2.1  | 1.9  | 1.74 | μA/MHz |
|      | DAC1       | 1.35                  | 1.19 | 1.07 | 0.98 |        |
|      | DCMI       | 3.49                  | 3.09 | 2.83 | 2.55 |        |
|      | GPIOA      | 0.1                   | 0.08 | 0.07 | 0.08 |        |
|      | GPIOB      | 0.07                  | 0.06 | 0.05 | 0.05 |        |
|      | GPIOC      | 0.08                  | 0.05 | 0.04 | 0.04 |        |
|      | GIOD       | 0.09                  | 0.06 | 0.05 | 0.04 |        |
|      | GPIOE      | 0.09                  | 0.09 | 0.08 | 0.05 |        |
|      | GPIOF      | 0.06                  | 0.08 | 0.08 | 0.05 |        |
|      | GPIOG      | 0.07                  | 0.07 | 0.06 | 0.04 |        |
|      | GPIOH      | 0.07                  | 0.07 | 0.05 | 0.06 |        |
|      | GPIOI      | 0.07                  | 0.07 | 0.06 | 0.04 |        |
|      | HASH1      | 1.37                  | 1.2  | 1.1  | 1    |        |
|      | PKA        | 5.43                  | 4.78 | 4.37 | 3.98 |        |
|      | RNG1       | 1.12                  | 0.99 | 0.9  | 0.82 |        |
|      | SRAM2      | 1.33                  | 1.18 | 1.06 | 0.96 |        |
|      | SRAM3      | 1.5                   | 1.33 | 1.22 | 1.1  |        |
|      | AHB2       | 1.59                  | 1.39 | 1.29 | 1.16 |        |
| AHB4 | FMC        | 9.73                  | 8.48 | 7.69 | 6.95 | μA/MHz |
|      | OSPI1      | 2.88                  | 2.54 | 2.29 | 2.08 |        |
|      | SDMMC1     | 8.71                  | 7.64 | 6.98 | 6.36 |        |
|      | SDMMC2     | 8.46                  | 7.45 | 6.82 | 6.2  |        |
|      | AHB4       | 0.36                  | 0.32 | 0.32 | 0.28 |        |

Table 38. Peripheral current consumption in Sleep mode (continued)

| Bus  | Peripheral | I <sub>DD</sub> (typ) |      |      |      | Unit   |
|------|------------|-----------------------|------|------|------|--------|
|      |            | VOS0                  | VOS1 | VOS2 | VOS3 |        |
| APB1 | CEC        | 0.15                  | 0.15 | 0.14 | 0.11 | μA/MHz |
|      | CRS        | 0.22                  | 0.23 | 0.20 | 0.19 |        |
|      | FDCAN1     | 6.37                  | 5.63 | 5.14 | 4.70 |        |
|      | I2C1       | 0.57                  | 0.5  | 0.49 | 0.42 |        |
|      | I2C2       | 0.57                  | 0.52 | 0.5  | 0.46 |        |
|      | I3C1       | 0.28                  | 0.27 | 0.28 | 0.25 |        |
|      | LPTIM2     | 0.91                  | 0.81 | 0.75 | 0.69 |        |
|      | SPI2       | 1.04                  | 0.93 | 0.89 | 0.78 |        |
|      | SPI3       | 1.00                  | 0.92 | 0.85 | 0.76 |        |
|      | TIM12      | 1.41                  | 1.26 | 1.18 | 1.06 |        |
|      | TIM13      | 0.92                  | 0.82 | 0.77 | 0.70 |        |
|      | TIM14      | 0.89                  | 0.78 | 0.75 | 0.66 |        |
|      | TIM2       | 2.86                  | 2.51 | 2.30 | 2.11 |        |
|      | TIM3       | 2.52                  | 2.21 | 2.03 | 1.87 |        |
|      | TIM4       | 2.43                  | 2.15 | 1.96 | 1.79 |        |
|      | TIM5       | 2.79                  | 2.48 | 2.26 | 2.06 |        |
|      | TIM6       | 0.54                  | 0.49 | 0.45 | 0.42 |        |
|      | TIM7       | 0.56                  | 0.5  | 0.48 | 0.43 |        |
|      | UART12     | 1.17                  | 1.06 | 0.95 | 0.88 |        |
|      | UART4      | 1.12                  | 0.98 | 0.93 | 0.83 |        |
|      | UART5      | 1.09                  | 0.99 | 0.93 | 0.84 |        |
|      | UART7      | 1.28                  | 1.14 | 1.05 | 0.93 |        |
|      | UART8      | 1.17                  | 1.06 | 0.94 | 0.86 |        |
|      | UART9      | 1.12                  | 1.00 | 0.90 | 0.84 |        |
|      | UCPD1      | 1.1                   | 1.00 | 0.90 | 0.84 |        |
|      | USART10    | 1.35                  | 1.22 | 1.14 | 1.02 |        |
|      | USART11    | 1.24                  | 1.11 | 1.04 | 0.94 |        |
|      | USART2     | 1.42                  | 1.29 | 1.19 | 1.07 |        |
|      | USART3     | 1.35                  | 1.24 | 1.14 | 1.02 |        |
|      | USART6     | 1.19                  | 1.08 | 1.02 | 0.92 |        |
|      | WWDG1      | 0.39                  | 0.35 | 0.35 | 0.30 |        |
|      | APB1       | 1.85                  | 1.61 | 1.49 | 1.34 |        |

Table 38. Peripheral current consumption in Sleep mode (continued)

| Bus  | Peripheral | I <sub>DD</sub> (typ) |      |      |      | Unit   |
|------|------------|-----------------------|------|------|------|--------|
|      |            | VOS0                  | VOS1 | VOS2 | VOS3 |        |
| APB2 | SAI1       | 1.13                  | 0.99 | 0.93 | 0.82 | μA/MHz |
|      | SAI2       | 1.06                  | 0.9  | 0.85 | 0.75 |        |
|      | SPI1       | 1.03                  | 0.91 | 0.85 | 0.75 |        |
|      | SPI4       | 1.03                  | 0.89 | 0.83 | 0.73 |        |
|      | SPI6       | 1.03                  | 0.9  | 0.85 | 0.74 |        |
|      | TIM1       | 4.35                  | 3.86 | 3.52 | 3.2  |        |
|      | TIM15      | 2.08                  | 1.84 | 1.69 | 1.54 |        |
|      | TIM16      | 1.43                  | 1.26 | 1.16 | 1.05 |        |
|      | TIM17      | 1.44                  | 1.25 | 1.17 | 1.05 |        |
|      | TIM8       | 4.33                  | 3.82 | 3.5  | 3.18 |        |
|      | USART1     | 1.24                  | 1.11 | 1.02 | 0.91 |        |
|      | USBFS      | 2.53                  | 2.22 | 2.04 | 1.84 |        |
|      | APB2       | 1.04                  | 0.92 | 0.84 | 0.77 |        |
|      |            |                       |      |      |      |        |
| APB3 | I2C3       | 2.43                  | 2.14 | 1.93 | 1.76 | μA/MHz |
|      | I2C4       | 2.37                  | 2.08 | 1.89 | 1.73 |        |
|      | LPTIM1     | 0.92                  | 0.82 | 0.75 | 0.67 |        |
|      | LPTIM3     | 0.88                  | 0.77 | 0.71 | 0.65 |        |
|      | LPTIM4     | 0.49                  | 0.45 | 0.41 | 0.37 |        |
|      | LPTIM5     | 0.84                  | 0.76 | 0.69 | 0.63 |        |
|      | LPTIM6     | 0.93                  | 0.82 | 0.76 | 0.70 |        |
|      | LPUART1    | 0.84                  | 0.74 | 0.66 | 0.63 |        |
|      | RTCAPB     | 1.93                  | 1.70 | 1.54 | 1.38 |        |
|      | SBS        | 0.45                  | 0.41 | 0.38 | 0.34 |        |
|      | SPI5       | 1.05                  | 0.93 | 0.84 | 0.75 |        |
|      | VREFBUF    | 0.08                  | 0.08 | 0.07 | 0.05 |        |
|      | APB3       | 0.64                  | 0.57 | 0.53 | 0.48 |        |
|      |            |                       |      |      |      |        |

### Wake-up time from low-power modes

The times given in [Table 39](#) are measured starting from the wake-up event trigger up to the first instruction executed by the CPU:

- for Stop or Sleep modes: the wake-up event is WFE.
- WKUP (PA0) pin is used to wake-up from Standby, Stop, and Sleep modes.

All timings are derived from tests performed under ambient temperature and V<sub>DD</sub> = 3.0 V.

Table 39. Low-power mode wake-up timings<sup>(1)</sup>

| Symbol        | Parameter                      | Conditions                                        | Typ   | Max   | Unit             |
|---------------|--------------------------------|---------------------------------------------------|-------|-------|------------------|
| $t_{WUSLEEP}$ | Wake-up time from Sleep mode   | Instruction cache enabled                         | 15    | 16    | CPU clock cycles |
|               |                                | Instruction cache disabled                        | 15    | 16    |                  |
| $t_{WUSTOP}$  | Wake-up time from Stop mode    | SVOS3, HSI 64 MHz, flash memory in normal mode    | 4.0   | 4.8   | $\mu s$          |
|               |                                | SVOS3, HSI 64 MHz, flash memory in low-power mode | 7.9   | 11.5  |                  |
|               |                                | SVOS4, HSI 64 MHz, flash memory in normal mode    | 13.8  | 16.0  |                  |
|               |                                | SVOS4, HSI 64 MHz, flash memory in low-power mode | 17.7  | 21.9  |                  |
|               |                                | SVOS5, HSI 64 MHz, flash memory in low-power mode | 31.4  | 36.8  |                  |
|               |                                | SVOS3, CSI 4 MHz, flash memory in normal mode     | 25.5  | 31.0  |                  |
|               |                                | SVOS3, CSI 4 MHz, flash memory in low power mode  | 27.7  | 34.2  |                  |
|               |                                | SVOS4, CSI 4 MHz, flash memory in normal mode     | 35.3  | 40.8  |                  |
|               |                                | SVOS4, CSI 4 MHz, flash memory in low-power mode  | 37.5  | 44.0  |                  |
|               |                                | SVOS5, CSI 4 MHz, flash memory in low-power mode  | 51.2  | 58.9  |                  |
| $t_{WUSTBY}$  | Wake-up time from Standby mode | VCAP capacitors discharged                        | 506.0 | 653.6 |                  |

1. Evaluated by characterization - Not tested in production.

### 5.3.8 External clock source characteristics

#### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the [Table 40](#) in addition to [Table 58](#). The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0481).

Table 40. High-speed external user clock characteristics<sup>(1)</sup>

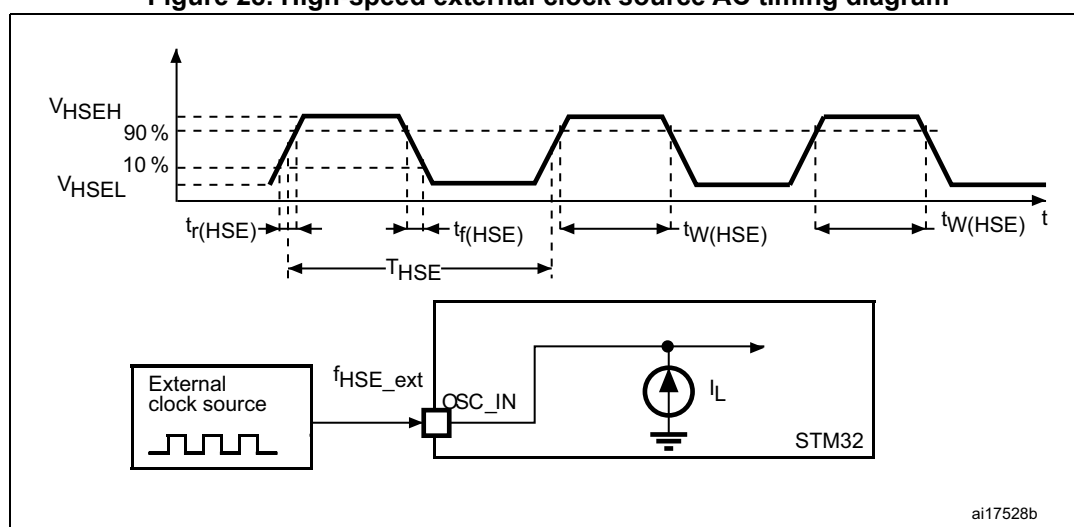
| Symbol                                     | Parameter                               | Conditions                    | Min          | Typ | Max          | Unit |
|--------------------------------------------|-----------------------------------------|-------------------------------|--------------|-----|--------------|------|
| $f_{HSE\_ext}$                             | User external clock source frequency    | External digital/analog clock | 4            | 25  | 50           | MHz  |
| $V_{HSEH}$                                 | Digital OSC_IN input high-level voltage | External digital clock        | $0.7 V_{DD}$ | -   | $V_{DD}$     | V    |
| $V_{HSEL}$                                 | Digital OSC_IN input low-level voltage  |                               | $V_{SS}$     | -   | $0.3 V_{DD}$ |      |
| $t_{w(HSEH)} / t_{w(HSEL)}$ <sup>(2)</sup> | Digital OSC_IN input high or low time   | External digital clock        | 7            | -   | -            | ns   |

Table 40. High-speed external user clock characteristics<sup>(1)</sup> (continued)

| Symbol                                                      | Parameter                                            | Conditions                                     | Min                   | Typ | Max                  | Unit |
|-------------------------------------------------------------|------------------------------------------------------|------------------------------------------------|-----------------------|-----|----------------------|------|
| $V_{isw(HSEH)}$<br>( $V_{HSEH} - V_{HSEL}$ ) <sup>(3)</sup> | Analog low-swing<br>OSC_IN peak-to-peak<br>amplitude | External analog low<br>swing clock             | 0.2                   | -   | $2/3 V_{DD}$         | V    |
| $DuCy_{HSE}$                                                | Analog low-swing<br>OSC_IN duty cycle                |                                                | 45                    | 50  | 55                   | %    |
| $t_{r(HSE)} / t_{f(HSE)}$                                   | Analog low-swing<br>OSC_IN rise and fall<br>times    | External analog low<br>swing clock, 10% to 90% | $0.05 / f_{HSE\_ext}$ | -   | $0.3 / f_{HSE\_ext}$ | ns   |

1. Specified by design - Not tested in production..
2. The rise and fall times for a digital input signal are not specified, but the  $V_{HSEH}$  and  $V_{HSEL}$  conditions must be fulfilled anyway.
3. The DC component of the signal must ensure that the signal peaks are located between  $V_{DD}$  and  $V_{SS}$ .

Figure 28. High-speed external clock source AC timing diagram



### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the [Table 41](#) in addition to [Table 58](#). The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0481).

Table 41. Low-speed external user clock characteristics<sup>(1)</sup>

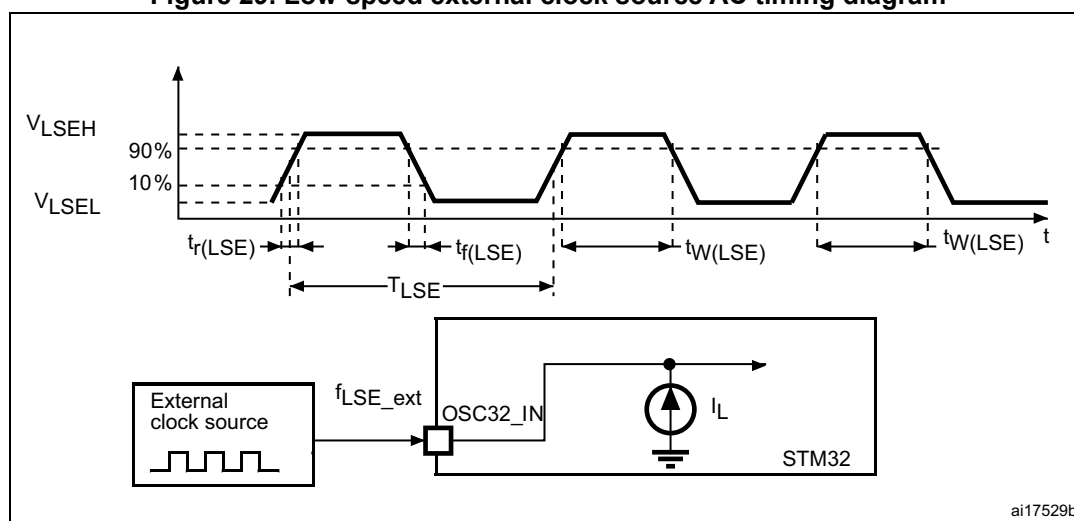
| Symbol         | Parameter                                    | Conditions                    | Min          | Typ    | Max          | Unit |
|----------------|----------------------------------------------|-------------------------------|--------------|--------|--------------|------|
| $f_{LSE\_ext}$ | User external clock source<br>frequency      | External digital/analog clock | -            | 32.768 | 1000         | kHz  |
| $V_{LSEH}$     | Digital OSC32_IN input<br>high-level voltage | External digital clock        | $0.7 V_{DD}$ | -      | $V_{DD}$     | V    |
| $V_{LSEL}$     | Digital OSC32_IN input<br>low-level voltage  |                               | $V_{SS}$     | -      | $0.3 V_{DD}$ |      |

**Table 41. Low-speed external user clock characteristics<sup>(1)</sup> (continued)**

| Symbol                                    | Parameter                                      | Conditions                                  | Min  | Typ | Max   | Unit |
|-------------------------------------------|------------------------------------------------|---------------------------------------------|------|-----|-------|------|
| $t_{w(LSEH)}/t_{w(LSEL)}$                 | Digital OSC_IN input high or low time          | External digital clock                      | 250  | -   | -     | ns   |
| $V_{isw\_H}$                              | Analog low-swing OSC_IN high-level voltage     | External analog low swing clock             | 0.6  | -   | 1.225 | V    |
| $V_{isw\_L}$                              | Analog low-swing OSC_IN low-level voltage      |                                             | 0.35 | -   | 0.8   |      |
| $V_{iswLSE}$<br>( $V_{LSEH} - V_{LSEL}$ ) | Analog low-swing OSC_IN peak-to-peak amplitude |                                             | 0.5  | -   | 0.875 |      |
| $DuCy_{LSE}$                              | Analog low-swing OSC_IN duty cycle             |                                             | 45   | 50  | 55    | %    |
| $t_{r(LSE)}/t_{f(LSE)}$                   | Analog low-swing OSC_IN rise and fall times    | External analog low swing clock, 10% to 90% | -    | 100 | 200   | ns   |

1. Specified by design - Not tested in production.

**Note:** For information on selecting the crystal, refer to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs" available from [www.st.com](http://www.st.com).

**Figure 29. Low-speed external clock source AC timing diagram**

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator.

All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 42](#). In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

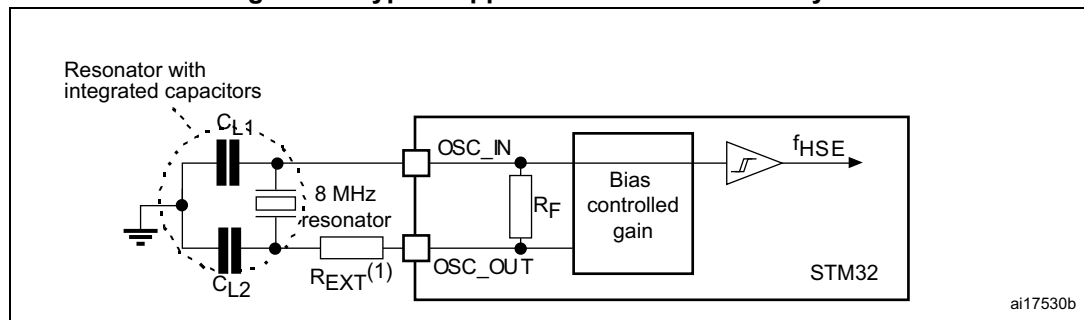
Table 42. 4 to 50 MHz HSE oscillator characteristics<sup>(1)</sup>

| Symbol                              | Parameter                   | Operating conditions <sup>(2)</sup>                                            | Min | Typ  | Max | Unit |
|-------------------------------------|-----------------------------|--------------------------------------------------------------------------------|-----|------|-----|------|
| F                                   | Oscillator frequency        | -                                                                              | 4   | -    | 50  | MHz  |
| R <sub>F</sub>                      | Feedback resistor           | -                                                                              | -   | 200  | -   | kΩ   |
| I <sub>DD(HSE)</sub>                | HSE current consumption     | During startup <sup>(3)</sup>                                                  | -   | -    | 10  | mA   |
|                                     |                             | V <sub>DD</sub> = 3 V, R <sub>m</sub> = 20 Ω, C <sub>L</sub> = 10 pF at 4 MHz  | -   | 0.44 | -   |      |
|                                     |                             | V <sub>DD</sub> = 3 V, R <sub>m</sub> = 20 Ω, C <sub>L</sub> = 10 pF at 8 MHz  | -   | 0.44 | -   |      |
|                                     |                             | V <sub>DD</sub> = 3 V, R <sub>m</sub> = 20 Ω, C <sub>L</sub> = 10 pF at 16 MHz | -   | 0.55 | -   |      |
|                                     |                             | V <sub>DD</sub> = 3 V, R <sub>m</sub> = 20 Ω, C <sub>L</sub> = 10 pF at 32 MHz | -   | 0.67 | -   |      |
|                                     |                             | V <sub>DD</sub> = 3 V, R <sub>m</sub> = 20 Ω, C <sub>L</sub> = 10 pF at 48 MHz | -   | 1.17 | -   |      |
| G <sub>m<sub>crit</sub>max</sub>    | Maximum critical crystal gm | Startup                                                                        | -   | -    | 1.5 | mA/V |
| t <sub>SU(HSE)</sub> <sup>(4)</sup> | Startup time                | V <sub>DD</sub> is stabilized                                                  | -   | 2    | -   | ms   |

1. Evaluated by design - Not tested in production.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the t<sub>SU(HSE)</sub> startup time
4. t<sub>SU(HSE)</sub> is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator, it can vary significantly with the crystal manufacturer

**Note:** For information on selecting the crystal, refer to AN2867 “Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs”, available from [www.st.com](http://www.st.com).

Figure 30. Typical application with an 8 MHz crystal



1. R<sub>EXT</sub> value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph is based on design simulation results obtained with typical external components specified in [Table 43](#). In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator

manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

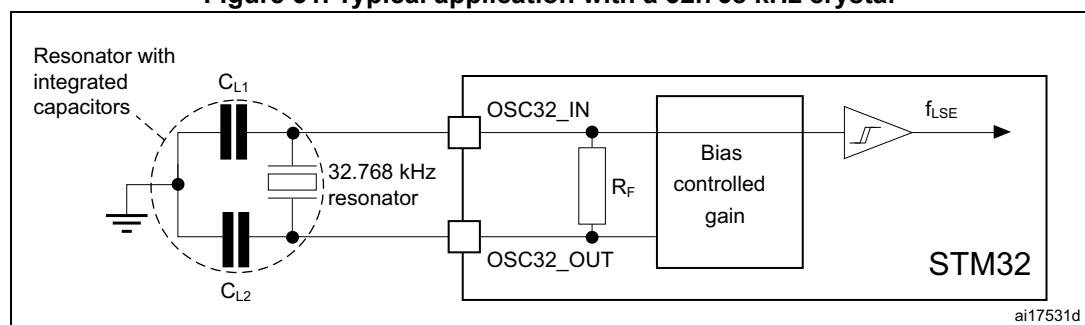
**Table 43. Low-speed external user clock characteristics<sup>(1)</sup>**

| Symbol                              | Parameter                   | Conditions <sup>(2)</sup>                        | Min | Typ    | Max  | Unit |
|-------------------------------------|-----------------------------|--------------------------------------------------|-----|--------|------|------|
| F                                   | Oscillator frequency        | -                                                | -   | 32.768 | -    | kHz  |
| I <sub>DD</sub>                     | LSE current consumption     | LSEDRV[1:0] = 00<br>Low drive capability         | -   | 246    | -    | nA   |
|                                     |                             | LSEDRV[1:0] = 01<br>Medium low drive capability  | -   | 333    | -    |      |
|                                     |                             | LSEDRV[1:0] = 10<br>Medium high drive capability | -   | 462    | -    |      |
|                                     |                             | LSEDRV[1:0] = 11<br>High drive capability        | -   | 747    | -    |      |
| G <sub>m</sub> <sub>critmax</sub>   | Maximum critical crystal gm | LSEDRV[1:0] = 00<br>Low drive capability         | -   | -      | 0.5  | μA/V |
|                                     |                             | LSEDRV[1:0] = 01<br>Medium low drive capability  | -   | -      | 0.75 |      |
|                                     |                             | LSEDRV[1:0] = 10<br>Medium high drive capability | -   | -      | 1.7  |      |
|                                     |                             | LSEDRV[1:0] = 11<br>High drive capability        | -   | -      | 2.7  |      |
| t <sub>SU(LSE)</sub> <sup>(3)</sup> | Startup time                | V <sub>DD</sub> is stabilized                    | -   | 2      | -    | s    |

1. Specified by design - Not tested in production.
2. Refer to the note and caution paragraphs below the table, and to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs".
3. t<sub>SU(LSE)</sub> is the startup time measured from the moment it is enabled (by software) to when a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal, it can vary significantly with the crystal manufacturer

**Note:** For information on selecting the crystal, refer to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs", available from [www.st.com](http://www.st.com).

**Figure 31. Typical application with a 32.768 kHz crystal**



**Note:** An external resistor is not required between OSC32\_IN and OSC32\_OUT, and it is forbidden to add one.

### 5.3.9 Internal clock source characteristics

The parameters given in [Table 44](#) to [Table 47](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 20](#).

#### 48 MHz high-speed internal RC oscillator (HSI48)

**Table 44. HSI48 oscillator characteristics**

| Symbol                                       | Parameter                                                                            | Conditions                                          | Min                 | Typ        | Max                 | Unit          |
|----------------------------------------------|--------------------------------------------------------------------------------------|-----------------------------------------------------|---------------------|------------|---------------------|---------------|
| $f_{\text{HSI48}}$                           | HSI48 frequency                                                                      | $V_{DD} = 3.3 \text{ V}$ , $T_J = 30^\circ\text{C}$ | 47.5 <sup>(1)</sup> | 48         | 48.5 <sup>(1)</sup> | MHz           |
| TRIM <sup>(3)</sup>                          | User trimming step                                                                   | -                                                   | -                   | 0.175      | 0.250               | %             |
| USER TRIM COVERAGE <sup>(2)</sup>            | User trimming coverage                                                               | $\pm 32$ steps                                      | $\pm 4.70$          | $\pm 5.6$  | -                   |               |
| DuCy(HSI48) <sup>(3)</sup>                   | Duty cycle                                                                           | -                                                   | 45                  | -          | 55                  | %             |
| ACC_HSI48_REL <sup>(3)</sup>                 | Accuracy of the HSI48 oscillator over temperature (reference is $30^\circ\text{C}$ ) | $T_J = -40$ to $130^\circ\text{C}$                  | -4.5                | -          | 4                   | %             |
| $\Delta V_{DD}(\text{HSI48})$                | HSI48 oscillator frequency drift with $V_{DD}$ (reference is 3.3 V)                  | $V_{DD} = 3.0$ to $3.6 \text{ V}$                   | -                   | 0.025      | 0.05                | %             |
|                                              |                                                                                      | $V_{DD} = 1.71$ to $3.6 \text{ V}$                  | -                   | 0.05       | 0.1                 |               |
| $t_{\text{su}}(\text{HSI48})$ <sup>(3)</sup> | HSI48 oscillator start-up time                                                       | -                                                   | -                   | 2.1        | 4.0                 | $\mu\text{s}$ |
| $I_{DD}(\text{HSI48})$ <sup>(3)</sup>        | HSI48 oscillator power consumption                                                   | -                                                   | -                   | 350        | 400                 | $\mu\text{A}$ |
| $N_T \text{ jitter}^{(3)}$                   | Next transition jitter accumulated jitter on 28 cycles                               | -                                                   | -                   | $\pm 0.15$ | -                   | ns            |
| $P_T \text{ jitter}^{(3)}$                   | Paired transition jitter accumulated jitter on 56 cycles <sup>(4)</sup>              | -                                                   | -                   | $\pm 0.25$ | -                   |               |

1. Calibrated during manufacturing tests.

2. Evaluated by characterization - Not tested in production.

3. Specified by design - Not tested in production.

4. Jitter measurements are performed without clock sources activated in parallel.

#### 64 MHz high-speed internal RC oscillator (HSI)

**Table 45. HSI oscillator characteristics<sup>(1)</sup>**

| Symbol           | Parameter          | Conditions                                                                                 | Min                 | Typ                 | Max                 | Unit |
|------------------|--------------------|--------------------------------------------------------------------------------------------|---------------------|---------------------|---------------------|------|
| $f_{\text{HSI}}$ | Frequency          | $V_{DD} = 3.3 \text{ V}$ , $T_J = 30^\circ\text{C}$                                        | 63.7 <sup>(2)</sup> | 64.0 <sup>(2)</sup> | 64.3 <sup>(2)</sup> | MHz  |
| TRIM             | User trimming step | Trimming is not a multiple of 32 <sup>(3)</sup>                                            | -                   | 0.24                | 0.32                | %    |
|                  |                    | Trimming is 128, 256, and 384 <sup>(3)</sup>                                               | -5.2                | -1.8                | -                   |      |
|                  |                    | Trimming is 64, 192, 320, and 488 <sup>(3)</sup>                                           | -1.4                | -0.8                | -                   |      |
|                  |                    | Other trimmings are multiples of 32 (not including multiples of 64 and 128) <sup>(3)</sup> | -0.6                | -0.25               | -                   |      |
| DuCy(HSI)        | Duty cycle         | -                                                                                          | 45                  | -                   | 55                  | %    |

Table 45. HSI oscillator characteristics<sup>(1)</sup> (continued)

| Symbol                              | Parameter                                              | Conditions                         | Min               | Typ | Max              | Unit          |
|-------------------------------------|--------------------------------------------------------|------------------------------------|-------------------|-----|------------------|---------------|
| $\Delta V_{DD}(\text{HSI})$         | Frequency drift with $V_{DD}$<br>(reference is 3.3 V)  | $V_{DD} = 1.71$ to $3.6$ V         | -0.12             | -   | 0.03             | %             |
| $\Delta T_{\text{EMP}}(\text{HSI})$ | Frequency drift with $V_{DD}$<br>(reference is 64 MHz) | $T_J = -20$ to $105^\circ\text{C}$ | -1 <sup>(4)</sup> | -   | 1 <sup>(4)</sup> |               |
|                                     |                                                        | $T_J = -40$ to $130^\circ\text{C}$ | -2 <sup>(4)</sup> | -   | 1 <sup>(4)</sup> |               |
| $t_{\text{su}}(\text{HSI})$         | Start-up time                                          | -                                  | -                 | 1.4 | 2.0              | $\mu\text{s}$ |
| $t_{\text{stab}}(\text{HSI})$       | Stabilization time                                     | At 1% of target frequency          | -                 | 4   | 8                | $\mu\text{s}$ |
|                                     |                                                        | At 1% of target frequency          | -                 | -   | 4                |               |
| $I_{DD}(\text{HSI})$                | Power consumption                                      | -                                  | -                 | 300 | 450              | $\mu\text{A}$ |

1. Specified by design - Not tested in production, unless otherwise specified.

2. Calibrated during manufacturing tests.

3. Trimming value of HSICAL[8:0].

4. Guaranteed by characterization - Not tested in production.

#### 4 MHz low-power internal RC oscillator (CSI)

Table 46. CSI oscillator characteristics<sup>(1)</sup>

| Symbol                              | Parameter                                                       | Conditions                                                                      | Min                 | Typ   | Max                 | Unit          |
|-------------------------------------|-----------------------------------------------------------------|---------------------------------------------------------------------------------|---------------------|-------|---------------------|---------------|
| $f_{\text{CSI}}$                    | Frequency                                                       | $V_{DD} = 3.3$ V, $T_J = 30^\circ\text{C}$                                      | 3.96 <sup>(2)</sup> | 4     | 4.04 <sup>(2)</sup> | MHz           |
| TRIM                                | User trimming step                                              | Trimming is not a multiple of 16                                                | -                   | 0.40  | 0.75                | %             |
|                                     |                                                                 | Trimming is not a multiple of 32                                                | -4.75               | -2.75 | 0.75                |               |
|                                     |                                                                 | Other trimmings are a multiple of 32<br>(not including multiples of 64 and 128) | -0.43               | 0.00  | 0.75                |               |
| $\text{DuCy}(\text{CSI})$           | Duty cycle                                                      | -                                                                               | 45                  | -     | 55                  | %             |
| $\Delta T_{\text{EMP}}(\text{CSI})$ | Frequency drift over temperature                                | $T_J = 0$ to $85^\circ\text{C}$                                                 | -3.7 <sup>(3)</sup> | -     | 4.5 <sup>(3)</sup>  | %             |
|                                     |                                                                 | $T_J = -40$ to $T_J = 130^\circ\text{C}$                                        | -11 <sup>(3)</sup>  | -     | 7.5 <sup>(3)</sup>  | %             |
| $\Delta V_{DD}(\text{CSI})$         | Frequency drift over $V_{DD}$                                   | $V_{DD} = 1.71$ to $3.6$ V                                                      | -0.06               | -     | 0.06                | %             |
| $t_{\text{su}}(\text{CSI})$         | Start-up time                                                   | -                                                                               | -                   | 1     | 2                   | $\mu\text{s}$ |
| $t_{\text{stab}}(\text{CSI})$       | Stabilization time<br>(to reach $\pm 3\%$ of $f_{\text{CSI}}$ ) | -                                                                               | -                   | -     | 4                   | cycle         |
| $I_{DD}(\text{CSI})$                | Power consumption                                               | -                                                                               | -                   | 23    | 30                  | $\mu\text{A}$ |

1. Specified by design - Not tested in production, unless otherwise specified.

2. Calibrated during manufacturing tests.

3. Evaluated by characterization - Not tested in production.

## Low-speed internal (LSI) RC oscillator

Table 47. LSI oscillator characteristics

| Symbol                              | Parameter                                 | Conditions                                                                                              | Min                  | Typ | Max                 | Unit          |
|-------------------------------------|-------------------------------------------|---------------------------------------------------------------------------------------------------------|----------------------|-----|---------------------|---------------|
| $f_{\text{LSI}}$                    | Frequency                                 | $V_{\text{DD}} = 3.3 \text{ V}$ , $T_{\text{J}} = 25^{\circ}\text{C}$                                   | 31.4 <sup>(1)</sup>  | 32  | 32.6 <sup>(1)</sup> | kHz           |
|                                     |                                           | $T_{\text{J}} = -40 \text{ to } 110^{\circ}\text{C}$ , $V_{\text{DD}} = 1.71 \text{ to } 3.6 \text{ V}$ | 29.76 <sup>(2)</sup> | -   | 33.6 <sup>(2)</sup> |               |
|                                     |                                           | $T_{\text{J}} = -40 \text{ to } 130^{\circ}\text{C}$ , $V_{\text{DD}} = 1.71 \text{ to } 3.6 \text{ V}$ | 29.4 <sup>(2)</sup>  | -   | 33.6 <sup>(2)</sup> |               |
| $t_{\text{su}}(\text{LSI})^{(3)}$   | Start-up time                             | -                                                                                                       | -                    | 80  | 130                 | $\mu\text{s}$ |
| $t_{\text{stab}}(\text{LSI})^{(3)}$ | Stabilization time<br>(5% of final value) | -                                                                                                       | -                    | 120 | 170                 |               |
| $I_{\text{DD}}(\text{LSI})^{(3)}$   | Power consumption                         | -                                                                                                       | -                    | 130 | 280                 | nA            |

1. Calibrated during manufacturing tests.

2. Evaluated by characterization - Not tested in production.

3. Specified by design - Not tested in production.

## 5.3.10 PLL characteristics

The parameters given in [Table 48](#) are derived from tests performed under temperature and  $V_{\text{DD}}$  supply voltage conditions summarized in [Table 20](#).

Table 48. PLL characteristics (wide VCO frequency range)<sup>(1)</sup>

| Symbol                   | Parameter                              | Conditions                                                   | Min | Typ | Max                | Unit          |
|--------------------------|----------------------------------------|--------------------------------------------------------------|-----|-----|--------------------|---------------|
| $f_{\text{PLL\_IN}}$     | PLL input clock                        | -                                                            | 2   | -   | 16                 | MHz           |
|                          | PLL input clock duty cycle             | -                                                            | 10  | -   | 90                 | %             |
| $f_{\text{PLL\_P\_OUT}}$ | PLL multiplier output clock<br>P, Q, R | VOS0                                                         | 1   | -   | 250 <sup>(2)</sup> | MHz           |
|                          |                                        | VOS1                                                         | 1   | -   | 200 <sup>(2)</sup> |               |
|                          |                                        | VOS2                                                         | 1   | -   | 150 <sup>(2)</sup> |               |
|                          |                                        | VOS3                                                         | 1   | -   | 100 <sup>(2)</sup> |               |
| $f_{\text{VCO\_OUT}}$    | PLL VCO output                         | -                                                            | 128 | -   | 560 <sup>(2)</sup> |               |
| $t_{\text{LOCK}}$        | PLL lock time                          | Normal mode                                                  | -   | 45  | 100 <sup>(3)</sup> | $\mu\text{s}$ |
|                          |                                        | Sigma-delta mode ( $f_{\text{PLL\_IN}} \geq 8 \text{ MHz}$ ) | -   | 60  | 120 <sup>(3)</sup> |               |

Table 48. PLL characteristics (wide VCO frequency range)<sup>(1)</sup> (continued)

| Symbol                | Parameter                                   | Conditions                                                                         |                   | Min | Typ  | Max | Unit |
|-----------------------|---------------------------------------------|------------------------------------------------------------------------------------|-------------------|-----|------|-----|------|
| Jitter                | Cycle-to-cycle jitter                       | f <sub>VCO_OUT</sub> = 128 MHz                                                     |                   | -   | 60   | -   | ±ps  |
|                       |                                             | f <sub>VCO_OUT</sub> = 200 MHz                                                     |                   | -   | 50   | -   |      |
|                       |                                             | f <sub>VCO_OUT</sub> = 400 MHz                                                     |                   | -   | 20   | -   |      |
|                       |                                             | f <sub>VCO_OUT</sub> = 560 MHz                                                     |                   | -   | 15   | -   |      |
|                       | Long term jitter <sup>(4)</sup>             | Normal mode (f <sub>PLL_IN</sub> = 2 MHz),<br>f <sub>VCO_OUT</sub> = 560 MHz       |                   | -   | ±0.2 | -   | %    |
|                       |                                             | Normal mode (f <sub>PLL_IN</sub> = 16 MHz),<br>f <sub>VCO_OUT</sub> = 560 MHz      |                   | -   | ±0.8 | -   |      |
|                       |                                             | Sigma-delta mode (f <sub>PLL_IN</sub> = 2 MHz),<br>f <sub>VCO_OUT</sub> = 560 MHz  |                   | -   | ±0.2 | -   |      |
|                       |                                             | Sigma-delta mode (f <sub>PLL_IN</sub> = 16 MHz),<br>f <sub>VCO_OUT</sub> = 560 MHz |                   | -   | ±0.8 | -   |      |
| I <sub>DD</sub> (PLL) | PLL power consumption on<br>V <sub>DD</sub> | f <sub>VCO_OUT</sub> = 560 MHz                                                     | V <sub>DD</sub>   | -   | 330  | 420 | µA   |
|                       |                                             |                                                                                    | V <sub>CORE</sub> | -   | 630  | -   |      |
|                       |                                             | f <sub>VCO_OUT</sub> = 128 MHz                                                     | V <sub>DD</sub>   | -   | 155  | 230 |      |
|                       |                                             |                                                                                    | V <sub>CORE</sub> | -   | 170  | -   |      |

1. Specified by design - Not tested in production, unless otherwise specified.

2. This value must be limited to the maximum frequency due to the product limitation.

3. Evaluated by characterization - Not tested in production.

4. Given as percentage of the input clock period.

Table 49. PLL characteristics (medium VCO frequency range)

| Symbol               | Parameter                              | Conditions       | Min <sup>(1)</sup> | Typ <sup>(1)</sup> | Max <sup>(1)</sup> | Unit |
|----------------------|----------------------------------------|------------------|--------------------|--------------------|--------------------|------|
| f <sub>PLL_IN</sub>  | PLL input clock                        | -                | 1                  | -                  | 2                  | MHz  |
|                      | PLL input clock duty cycle             | -                | 10                 | -                  | 90                 | %    |
| f <sub>PLL_OUT</sub> | PLL multiplier output clock<br>P, Q, R | VOS0             | 1.17               | -                  | 210                | MHz  |
|                      |                                        | VOS1             | 1.17               | -                  | 210                |      |
|                      |                                        | VOS2             | 1.17               | -                  | 160 <sup>(2)</sup> |      |
|                      |                                        | VOS3             | 1.17               | -                  | 88 <sup>(2)</sup>  |      |
| f <sub>VCO_OUT</sub> | PLL VCO output                         | -                | 150                | -                  | 420                |      |
| t <sub>LOCK</sub>    | PLL lock time                          | Normal mode      | -                  | 45                 | 80 <sup>(3)</sup>  | µs   |
|                      |                                        | Sigma-delta mode | Forbidden          |                    |                    |      |

Table 49. PLL characteristics (medium VCO frequency range) (continued)

| Symbol                | Parameter                                | Conditions                                 |                               | Min <sup>(1)</sup> | Typ <sup>(1)</sup> | Max <sup>(1)</sup> | Unit |
|-----------------------|------------------------------------------|--------------------------------------------|-------------------------------|--------------------|--------------------|--------------------|------|
| Jitter                | Cycle-to-cycle jitter                    | f <sub>VCO_OUT</sub> = 150 MHz             | -                             | -                  | 60                 | -                  | ±ps  |
|                       |                                          | f <sub>VCO_OUT</sub> = 200 MHz             | -                             | -                  | 40                 | -                  |      |
|                       |                                          | f <sub>VCO_OUT</sub> = 400 MHz             | -                             | -                  | 18                 | -                  |      |
|                       |                                          | f <sub>VCO_OUT</sub> = 420 MHz             | -                             | -                  | 15                 | -                  |      |
|                       | Period jitter                            | f <sub>VCO_OUT</sub> = 150 MHz             | f <sub>PLL_OUT</sub> = 50 MHz | -                  | 75                 | -                  |      |
|                       |                                          | f <sub>VCO_OUT</sub> = 400 MHz             |                               | -                  | 25                 | -                  |      |
|                       | Long term jitter <sup>(4)</sup>          | Normal mode f <sub>VCO_OUT</sub> = 400 MHz |                               | -                  | ±0.2               | -                  | %    |
| I <sub>DD</sub> (PLL) | PLL power consumption on V <sub>DD</sub> | f <sub>VCO_OUT</sub> = 420 MHz             | V <sub>DD</sub>               | -                  | 275                | 360                | µA   |
|                       |                                          |                                            | V <sub>CORE</sub>             | -                  | 450                | -                  |      |
|                       |                                          | f <sub>VCO_OUT</sub> = 150 MHz             | V <sub>DD</sub>               | -                  | 160                | 240                |      |
|                       |                                          |                                            | V <sub>CORE</sub>             | -                  | 165                | -                  |      |

1. Specified by design - Not tested in production, unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Evaluated by characterization - Not tested in production.
4. Given as percentage of the input clock period.

### 5.3.11 Memory characteristics

#### Flash memory

The characteristics are given at  $T_J = -40$  to  $130^\circ\text{C}$  unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

Table 50. Flash memory characteristics

| Symbol   | Parameter      | Conditions                  | Min | Typ | Max <sup>(1)</sup> | Unit |
|----------|----------------|-----------------------------|-----|-----|--------------------|------|
| $I_{DD}$ | Supply current | Word program <sup>(2)</sup> | -   | 2.5 | 3.6                | mA   |
|          |                | Sector erase                | -   | 1.8 | 4                  |      |
|          |                | Mass erase                  | -   | 2.0 | 4                  |      |

1. Specified by design - Not tested in production
2. Data are evaluated with a write of 50% of the programmed bits equal to 0.

Table 51. Flash memory programming<sup>(1)</sup>

| Symbol      | Parameter                    | Conditions           | Min <sup>(2)</sup> | Typ   | Max <sup>(1)</sup> | Unit          |
|-------------|------------------------------|----------------------|--------------------|-------|--------------------|---------------|
| $t_{prog}$  | Word program time            | 128 bits (user area) | -                  | 31    | 100                | $\mu\text{s}$ |
|             |                              | 16 bits (OTP area)   | -                  | 31    | 100                |               |
| $t_{ERASE}$ | Sector erase time (8 Kbytes) |                      | -                  | 2     | 10                 | ms            |
| $t_{ME}$    | Mass erase time              |                      | -                  | 0.512 | 2.6                | s             |
| $t_{BE}$    | Bank erase time              |                      | -                  | 0.256 | 1.3                | s             |

**Table 51. Flash memory programming<sup>(1)</sup> (continued)**

| Symbol            | Parameter           | Conditions | Min <sup>(2)</sup> | Typ | Max <sup>(1)</sup> | Unit |
|-------------------|---------------------|------------|--------------------|-----|--------------------|------|
| V <sub>prog</sub> | Programming voltage |            | 1.71               | -   | 3.6                | V    |

1. Data are valid for program memory and high-cycling data memory.

2. Specified by design - Not tested in production.

**Table 52. Flash memory endurance and data retention**

| Symbol            | Parameter                      | Conditions                           | Min <sup>(1)</sup> | Unit    |
|-------------------|--------------------------------|--------------------------------------|--------------------|---------|
| N <sub>PEND</sub> | Endurance program memory       | T <sub>J</sub> = -40 to +130°C       | 10                 | kcycles |
| N <sub>DEND</sub> | Endurance data memory          | T <sub>J</sub> = -40 to +130°C       | 100                |         |
| t <sub>PRET</sub> | Program memory, data retention | 1 kcycle at T <sub>A</sub> = 125°C   | 10                 | Years   |
|                   |                                | 1 kcycles at T <sub>A</sub> = 85°C   | 30                 |         |
|                   |                                | 10 kcycles at T <sub>A</sub> = 55°C  | 30                 |         |
| t <sub>DRET</sub> | Data retention for data memory | 100 kcycle at T <sub>A</sub> = 125°C | 1                  |         |
|                   |                                | 100 kcycles at T <sub>A</sub> = 85°C | 10                 |         |
|                   |                                | 100 kcycles at T <sub>A</sub> = 55°C | 10                 |         |

1. Evaluated by characterization - Not tested in production, unless otherwise specified.

### 5.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)**, positive and negative, is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V<sub>DD</sub> and V<sub>SS</sub> through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows to resume normal operation.

The test results are given in [Table 53](#). They are based on the EMS levels and classes defined in AN1709 “*EMC design guide for STM8, STM32 and legacy MCUs*”.

**Table 53. EMS characteristics**

| Symbol            | Parameter                                                                                                          | Conditions                                                                                                                         | Level/Class |
|-------------------|--------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|-------------|
| V <sub>FESD</sub> | Voltage limits to apply on any I/O pin to induce a functional disturbance                                          | V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25°C,<br>LQFP176-SMPS,<br>f <sub>rcu_cpu_ck</sub> = 250 MHz,<br>conform to IEC 61000-4-2 | 2B          |
| V <sub>FTB</sub>  | Fast transient voltage burst limits to apply through 100 pF on VDD and VSS pins to induce a functional disturbance |                                                                                                                                    | 5A          |

As a consequence, it is recommended to add a serial resistor (1 k $\Omega$ ), located as close as possible to the MCU, to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. Good EMC performance is highly dependent upon the user application, and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for its application.

### Software recommendations

The software flow must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (such as control registers)

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or on the oscillator pins for 1 s.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 “*Software techniques for improving microcontrollers EMC performance*”).

### Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard, which specifies the test board and the pin loading.

**Table 54. EMI characteristics**

| Symbol           | Parameter                 | Conditions                                                                                     | Monitored frequency band | Max vs. [f <sub>HSE</sub> /f <sub>CPU</sub> ] | Unit       |
|------------------|---------------------------|------------------------------------------------------------------------------------------------|--------------------------|-----------------------------------------------|------------|
|                  |                           |                                                                                                |                          | 25/250 MHz                                    |            |
| S <sub>EMI</sub> | Peak level <sup>(1)</sup> | V <sub>DD</sub> = 3.6 V, T <sub>A</sub> = 25°C, LQFP176-SMPS package, conforming to IEC61967-2 | 0.1 to 30 MHz            | 21                                            | dB $\mu$ V |
|                  |                           |                                                                                                | 30 to 130 MHz            | 22                                            |            |
|                  |                           |                                                                                                | 130 MHz to 1 GHz         | 29                                            |            |
|                  |                           |                                                                                                | 1 GHz to 2 GHz           | 21                                            |            |
|                  |                           |                                                                                                | EMI level                | 4                                             | -          |

1. Refer to the EMI radiated test chapter of application note AN1709 “*EMC design guide for STM8, STM32 and legacy MCUs*” available from the ST website [www.st.com](http://www.st.com).

### 5.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges (a positive pulse followed by a negative one) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

**Table 55. ESD absolute maximum ratings**

| Symbol                | Ratings                                               | Conditions                                                      | Packages              | Class | Maximum value <sup>(1)</sup> | Unit |
|-----------------------|-------------------------------------------------------|-----------------------------------------------------------------|-----------------------|-------|------------------------------|------|
| $V_{\text{ESD(HBM)}}$ | Electrostatic discharge voltage (human body model)    | $T_A = 25^\circ\text{C}$ , conforming to ANSI/ESDA/JEDEC JS-001 | Packages with SMPS    | 1C    | 1000 <sup>(2)</sup>          | V    |
|                       |                                                       |                                                                 | Packages without SMPS | 2     | 2000                         |      |
| $V_{\text{ESD(CDM)}}$ | Electrostatic discharge voltage (charge device model) | $T_A = 25^\circ\text{C}$ , conforming to ANSI/ESDA/JEDEC JS-002 | All packages          | C2a   | 500                          | V    |

1. Evaluated by characterization - Not tested in production.

2. The electrostatic discharge is 2000 V for all pins, except  $V_{\text{FBSMPS}}$ , for which the test fails at 2000 V and passes at 1600 V.

#### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output, and configurable I/O pin

These tests are compliant with the JESD78 IC latch-up standard.

**Table 56. Electrical sensitivities**

| Symbol | Parameter             | Conditions                                       | Class      |
|--------|-----------------------|--------------------------------------------------|------------|
| LU     | Static latch-up class | $T_J = 130^\circ\text{C}$ , conforming to JESD78 | II level A |

### 5.3.14 I/O current injection characteristics

As a general rule, avoid current injection to the I/O pins, due to external voltage below  $V_{\text{SS}}$  or above  $V_{\text{DD}}$  (for standard, 3.3 V-capable I/O pins) during the normal product operation. To give an indication of the device robustness when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed, the device is stressed by injecting current into the I/O pins (one at the time) programmed in floating input mode, and checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits ( $-5 / +0 \mu\text{A}$  range) of induced leakage current on adjacent pins, or other functional failures (such as reset, oscillator

frequency deviation).

The following table shows I/Os current injection susceptibility data. Negative/positive induced leakage currents are caused, respectively, by negative/positive injection.

**Table 57. I/O current injection susceptibility<sup>(1)</sup>**

| Symbol           | Description                                                            | Functional susceptibility |                    | Unit |
|------------------|------------------------------------------------------------------------|---------------------------|--------------------|------|
|                  |                                                                        | Negative injection        | Positive injection |      |
| I <sub>INJ</sub> | Injected current on pins PA4, PA5, PB2, PB12, PC14, PC15, PD8, and PH2 | 0                         | 0                  | mA   |
|                  | Injected current on all other pins                                     | 5                         | N/A                |      |

1. Evaluated by characterization - Not tested in production.

### 5.3.15 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 58](#) are derived from tests performed under the conditions summarized in [Table 20](#). All I/Os are CMOS and TTL compliant (except for BOOT0).

**Note:** For information on GPIO configuration, refer to AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption”, available on [www.st.com](http://www.st.com).

**Table 58. I/O static characteristics<sup>(1)</sup>**

| Symbol                          | Parameter                                   | Conditions                       | Min                                           | Typ | Max                                          | Unit |
|---------------------------------|---------------------------------------------|----------------------------------|-----------------------------------------------|-----|----------------------------------------------|------|
| V <sub>IL</sub>                 | I/O input low level voltage except BOOT0    | 1.08 V < V <sub>DD</sub> < 3.6 V | -                                             | -   | 0.3 V <sub>DDIOx</sub> <sup>(2)</sup>        | V    |
|                                 | I/O input low level voltage except BOOT0    |                                  | -                                             | -   | 0.4 V <sub>DDIOx</sub> - 0.1 <sup>(3)</sup>  |      |
|                                 | BOOT0 I/O input low level voltage           |                                  | -                                             | -   | 0.19 V <sub>DDIOx</sub> + 0.1 <sup>(3)</sup> |      |
| V <sub>IH</sub>                 | I/O input high level voltage except BOOT0   | 1.08 V < V <sub>DD</sub> < 3.6 V | 0.7 V <sub>DDIOx</sub> <sup>(2)</sup>         | -   | -                                            | V    |
|                                 | I/O input high level voltage except BOOT0   |                                  | 0.52 V <sub>DDIOx</sub> + 0.18 <sup>(3)</sup> | -   | -                                            |      |
|                                 | BOOT0 I/O input high level voltage          |                                  | 0.17 V <sub>DDIOx</sub> + 0.6 <sup>(3)</sup>  | -   | -                                            |      |
| V <sub>HYS</sub> <sup>(3)</sup> | TT_xx, FT_xxx and NRST I/O input hysteresis | 1.08 V < V <sub>DD</sub> < 3.6 V | -                                             | 250 | -                                            | mV   |
|                                 | BOOT0 I/O input hysteresis                  | 1.71 V < V <sub>DD</sub> < 3.6 V | -                                             | 200 | -                                            |      |

Table 58. I/O static characteristics<sup>(1)</sup> (continued)

| Symbol           | Parameter                                         | Conditions                                                                         | Min | Typ | Max       | Unit |
|------------------|---------------------------------------------------|------------------------------------------------------------------------------------|-----|-----|-----------|------|
| $I_{leak}^{(4)}$ | FT_xx input leakage current <sup>(3)</sup>        | $0 < V_{IN} \leq \text{Max}(V_{DDXXX})^{(7)}$                                      | -   | -   | $\pm 200$ | nA   |
|                  |                                                   | $\text{Max}(V_{DDXXX}) < V_{IN} \leq \text{Max}(V_{DDXXX}) + 1 \text{ V}^{(5)(7)}$ | -   | -   | 2500      |      |
|                  |                                                   | $\text{Max}(V_{DDXXX}) < V_{IN} \leq 5.5 \text{ V}^{(5)(7)}$                       | -   | -   | 750       |      |
|                  | TT_xx input leakage current                       | $0 < V_{IN} \leq \text{Max}(V_{DDXXX})^{(7)}$                                      | -   | -   | $\pm 200$ |      |
|                  | BOOT0                                             | $0 < V_{IN} \leq V_{DDOX}$                                                         | -   | -   | 15        |      |
| $R_{PU}$         | Weak pull-up equivalent resistor <sup>(6)</sup>   | $V_{IN} = V_{SS}$                                                                  | 30  | 40  | 50        | kΩ   |
| $R_{PD}$         | Weak pull-down equivalent resistor <sup>(6)</sup> | $V_{IN} = V_{DD}^{(7)}$                                                            | 30  | 40  | 50        |      |
| $C_{IO}$         | I/O pin capacitance                               | -                                                                                  | -   | 5   | -         | pF   |

1.  $V_{DDIOx}$  represents  $V_{DD}$  or  $V_{DDIO2}$ .

2. Compliant with CMOS requirements.

3. Specified by design - Not tested in production.

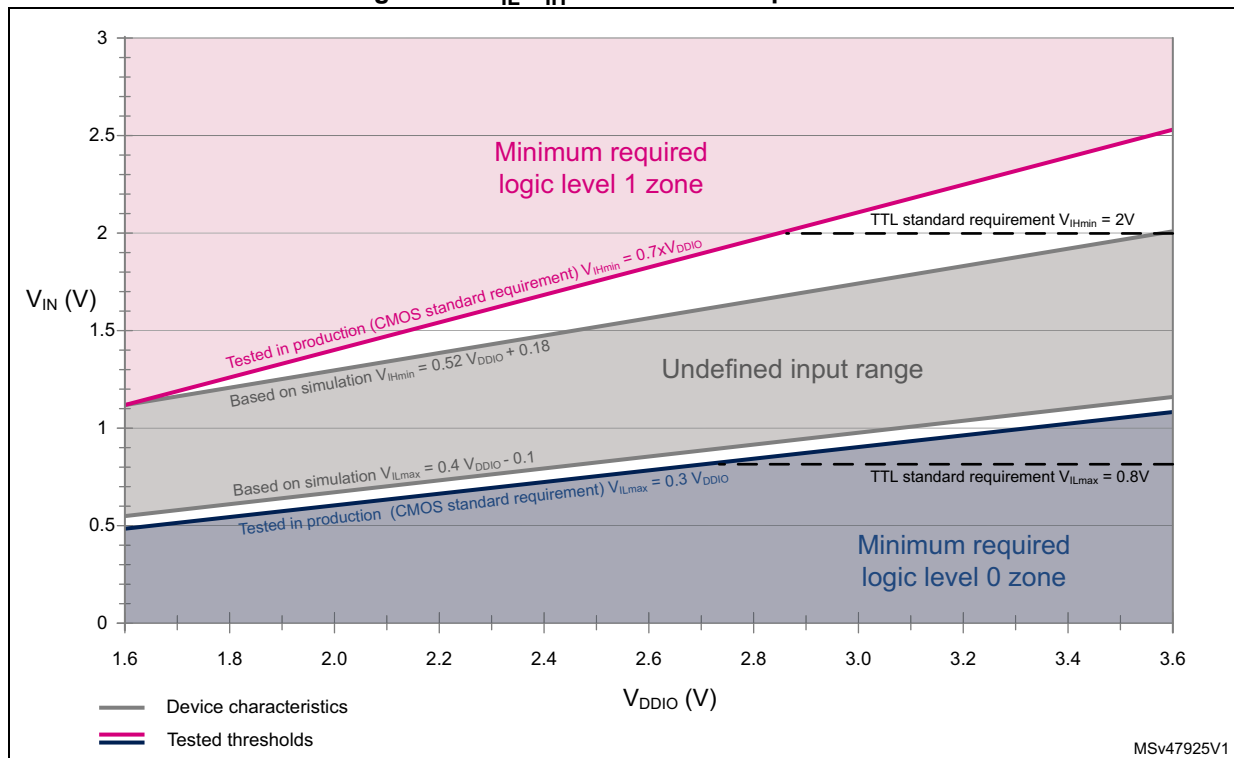
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula:  $I_{Total\_leak\_max} = 10 \mu A + [\text{number of I/Os where } V_{IN} \text{ is applied on the pad}] \times I_{lkg(Max)}$ .

5.  $V_{IN}$  must be lower than  $\text{Max}(V_{DDXXX}) + 3.6 \text{ V}$ .

6. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).

7.  $\text{Max}(V_{DDXXX})$  is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in the following figure.

Figure 32.  $V_{IL}/V_{IH}$  for all I/Os except BOOT0

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL}/V_{OH}$ ).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#). In particular:

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table 18](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table 18](#)).

### Output voltage levels

Unless otherwise specified, the parameters given in [Table 59](#) and [Table 61](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 20](#). All I/Os are CMOS and TTL compliant.

Table 59. Output voltage characteristics for all I/Os except PC13, PC14, PC15, and PI8

| Symbol            | Parameter                                                               | Conditions <sup>(1)</sup>                                                                          | Min             | Max             | Unit |
|-------------------|-------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|-----------------|-----------------|------|
| $V_{OL}$          | Output low level voltage                                                | CMOS port <sup>(2)</sup> , $I_{IO} = 8\text{ mA}$<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  | -               | 0.4             | V    |
| $V_{OH}$          | Output high level voltage                                               | CMOS port <sup>(2)</sup> , $I_{IO} = -8\text{ mA}$<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | $V_{DD} - 0.4$  | -               |      |
| $V_{OL}^{(3)}$    | Output low level voltage                                                | TTL port <sup>(2)</sup> , $I_{IO} = 8\text{ mA}$<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$   | -               | 0.4             |      |
| $V_{OH}^{(3)}$    | Output high level voltage                                               | TTL port <sup>(2)</sup> , $I_{IO} = -8\text{ mA}$<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  | 2.4             | -               |      |
| $V_{OL}^{(3)}$    | Output low level voltage                                                | $I_{IO} = 20\text{ mA}$<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                            | -               | 1.3             |      |
| $V_{OH}^{(3)}$    | Output high level voltage                                               | $I_{IO} = -20\text{ mA}$<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                           | $V_{DD} - 1.3$  | -               |      |
| $V_{OL}^{(3)}$    | Output low level voltage                                                | $I_{IO} = 4\text{ mA}$<br>$1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                            | -               | 0.4             |      |
| $V_{OH}^{(3)}$    | Output high level voltage                                               | $I_{IO} = -4\text{ mA}$<br>$1.71\text{ V} \leq V_{DD} < 3.6\text{ V}$                              | $V_{DD} - 0.4$  | -               |      |
| $V_{OL}^{(3)}$    | Output low level voltage                                                | $I_{IO} = 2\text{ mA}$<br>$1.08\text{ V} \leq V_{DD} \leq 1.32\text{ V}$                           | -               | $0.3 V_{DDIO2}$ |      |
| $V_{OH}^{(3)}$    | Output high level voltage                                               | $I_{IO} = -2\text{ mA}$<br>$1.71\text{ V} \leq V_{DD} < 1.32\text{ V}$                             | $0.7 V_{DDIO2}$ | -               |      |
| $V_{OLFM+}^{(3)}$ | Output low level voltage for an FTf I/O pin in (FT I/O with "f" option) | $I_{IO} = 20\text{ mA}$<br>$2.3\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                            | -               | 0.4             |      |
|                   |                                                                         | $I_{IO} = 10\text{ mA}$<br>$1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                           | -               | 0.4             |      |
|                   |                                                                         | $I_{IO} = 4.5\text{ mA}$<br>$1.08\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                          | -               | 0.4             |      |

1. The  $I_{IO}$  current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings  $\Sigma I_{IO}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 60. Output voltage characteristics for FT\_c I/Os

| Symbol         | Parameter                 | Conditions <sup>(1)</sup>                                                                             | Min            | Max | Unit |
|----------------|---------------------------|-------------------------------------------------------------------------------------------------------|----------------|-----|------|
| $V_{OL}$       | Output low level voltage  | CMOS port <sup>(2)</sup> , $I_{IO} = 2 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$  | -              | 0.4 | V    |
| $V_{OH}$       | Output high level voltage | CMOS port <sup>(2)</sup> , $I_{IO} = -2 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ | $V_{DD} - 0.4$ | -   |      |
| $V_{OL}^{(3)}$ | Output low level voltage  | TTL port <sup>(2)</sup> , $I_{IO} = 2 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$   | -              | 0.4 |      |
| $V_{OH}^{(3)}$ | Output high level voltage | TTL port <sup>(2)</sup> , $I_{IO} = -2 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$  | 2.4            | -   |      |
| $V_{OL}^{(3)}$ | Output low level voltage  | $I_{IO} = 1 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$                             | -              | 0.4 |      |
| $V_{OH}^{(3)}$ | Output high level voltage | $I_{IO} = -1 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$                            | $V_{DD} - 0.4$ | -   |      |
| $V_{OL}^{(3)}$ | Output low level voltage  | $I_{IO} = 0.1 \text{ mA}$<br>$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$                          | -              | 0.4 |      |
| $V_{OH}^{(3)}$ | Output high level voltage | $I_{IO} = -0.1 \text{ mA}$<br>$1.71 \text{ V} \leq V_{DD} < 3.6 \text{ V}$                            | $V_{DD} - 0.4$ | -   |      |

1. The  $I_{IO}$  current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings  $\Sigma I_{IO}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 61. Output voltage characteristics for PC13 and PI8<sup>(1)</sup>

| Symbol         | Parameter                 | Conditions <sup>(3)</sup>                                                                             | Min            | Max | Unit |
|----------------|---------------------------|-------------------------------------------------------------------------------------------------------|----------------|-----|------|
| $V_{OL}$       | Output low level voltage  | CMOS port <sup>(2)</sup> , $I_{IO} = 3 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$  | -              | 0.4 | V    |
| $V_{OH}$       | Output high level voltage | CMOS port <sup>(2)</sup> , $I_{IO} = -3 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ | $V_{DD} - 0.4$ | -   |      |
| $V_{OL}^{(3)}$ | Output low level voltage  | TTL port <sup>(2)</sup> , $I_{IO} = 3 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$   | -              | 0.4 |      |
| $V_{OH}^{(3)}$ | Output high level voltage | TTL port <sup>(2)</sup> , $I_{IO} = -3 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$  | 2.4            | -   |      |
| $V_{OL}^{(3)}$ | Output low level voltage  | $I_{IO} = 1.5 \text{ mA}$<br>$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$                          | -              | 0.4 |      |
| $V_{OH}^{(3)}$ | Output high level voltage | $I_{IO} = -1.5 \text{ mA}$<br>$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$                         | $V_{DD} - 0.4$ | -   |      |

1. The  $I_{IO}$  current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings  $\Sigma I_{IO}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

**Table 62. Output voltage characteristics for PC14 and PC15<sup>(1)</sup>**

| Symbol         | Parameter                 | Conditions <sup>(3)</sup>                                                                               | Min            | Max | Unit |
|----------------|---------------------------|---------------------------------------------------------------------------------------------------------|----------------|-----|------|
| $V_{OL}$       | Output low level voltage  | CMOS port <sup>(2)</sup> , $I_{IO} = 0.5 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$  | -              | 0.4 | V    |
| $V_{OH}$       | Output high level voltage | CMOS port <sup>(2)</sup> , $I_{IO} = -0.5 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ | $V_{DD} - 0.4$ | -   |      |
| $V_{OL}^{(3)}$ | Output low level voltage  | TTL port <sup>(2)</sup> , $I_{IO} = 0.5 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$   | -              | 0.4 |      |
| $V_{OH}^{(3)}$ | Output high level voltage | TTL port <sup>(2)</sup> , $I_{IO} = -0.5 \text{ mA}$<br>$2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$  | 2.4            | -   |      |
| $V_{OL}^{(3)}$ | Output low level voltage  | $I_{IO} = 0.25 \text{ mA}$<br>$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$                           | -              | 0.4 |      |
| $V_{OH}^{(3)}$ | Output high level voltage | $I_{IO} = -0.25 \text{ mA}$<br>$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$                          | $V_{DD} - 0.4$ | -   |      |

1. The  $I_{IO}$  current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings  $\Sigma I_{IO}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

### Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of GPIOx\_HSLVR register can be used to optimize the I/O speed when the voltage is below 2.7 V.

Table 63. Output timing characteristics (HSLV OFF)<sup>(1)</sup>

| Speed | Symbol              | Parameter                                                                 | Conditions                                                               | Min | Max  | Unit |
|-------|---------------------|---------------------------------------------------------------------------|--------------------------------------------------------------------------|-----|------|------|
| 00    | $F_{\max}^{(2)(3)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 8    | MHz  |
|       |                     |                                                                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 5    |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 10   |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 5    |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 12   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 5    |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 14   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 5    |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 16   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 5    |      |
|       | $t_r/t_f^{(4)(5)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 18.0 | ns   |
|       |                     |                                                                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 36.0 |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 17.0 |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 34.0 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 15.5 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 32.0 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 14.2 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 30.0 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 12.2 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 27   |      |

Table 63. Output timing characteristics (HSLV OFF)<sup>(1)</sup> (continued)

| Speed | Symbol              | Parameter                                                                 | Conditions                                                               | Min | Max  | Unit |
|-------|---------------------|---------------------------------------------------------------------------|--------------------------------------------------------------------------|-----|------|------|
| 01    | $F_{\max}^{(2)(3)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ |     | 40   | MHz  |
|       |                     |                                                                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 12   |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 45   |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 14   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 50   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 16   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 55   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 18   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 60   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 20   |      |
|       | $t_r/t_f^{(4)(5)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 6.2  | ns   |
|       |                     |                                                                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 11.4 |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 5.7  |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 10.5 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 5.1  |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 9.5  |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 4.5  |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  |     | 8.4  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ |     | 3.7  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  |     | 7.0  |      |

Table 63. Output timing characteristics (HSLV OFF)<sup>(1)</sup> (continued)

| Speed | Symbol              | Parameter                                                                 | Conditions                                                               | Min | Max | Unit |
|-------|---------------------|---------------------------------------------------------------------------|--------------------------------------------------------------------------|-----|-----|------|
| 10    | $F_{\max}^{(2)(3)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 80  | MHz  |
|       |                     |                                                                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 30  |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 90  |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 35  |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 100 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 40  |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 110 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 45  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 133 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 50  |      |
|       | $t_r/t_f^{(4)(5)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 3.8 | ns   |
|       |                     |                                                                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 7.5 |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 3.4 |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 6.6 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 2.9 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 5.7 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 2.5 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 4.7 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 1.9 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 3.7 |      |

Table 63. Output timing characteristics (HSLV OFF)<sup>(1)</sup> (continued)

| Speed | Symbol              | Parameter                                                                 | Conditions                                                               | Min | Max | Unit |
|-------|---------------------|---------------------------------------------------------------------------|--------------------------------------------------------------------------|-----|-----|------|
| 11    | $F_{\max}^{(2)(3)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 100 | MHz  |
|       |                     |                                                                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 40  |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 120 |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 50  |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 140 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 60  |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 166 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 70  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 200 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 80  |      |
|       | $t_r/t_f^{(4)(5)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 3.3 | ns   |
|       |                     |                                                                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 6.3 |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 2.8 |      |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 5.5 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 2.3 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 4.6 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 1.9 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 3.7 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | -   | 1.4 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$  | -   | 3   |      |

1. Specified by design - Not tested in production.

2. The maximum frequency is defined with the conditions  $(t_r + t_f) \leq 2/3 T$ ,  $\text{Skew} \leq 1/20 T$ , and  $45\% < \text{Duty cycle} < 55\%$ .

3. When  $2 \text{ V} < V_{\text{DD}} < 2.7 \text{ V}$  the maximum frequency is between values given for  $V_{\text{DD}} = 1.98 \text{ V}$  and  $V_{\text{DD}} = 2.7 \text{ V}$ .

4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

5. When  $2 \text{ V} < V_{\text{DD}} < 2.7 \text{ V}$  the maximum  $t_{\text{rise}}/t_{\text{fall}}$  is between values given for  $V_{\text{DD}} = 1.98 \text{ V}$  and  $V_{\text{DD}} = 2.7 \text{ V}$ .

## Output buffer timing characteristics (HSLV option enabled)

Table 64. Output timing characteristics (HSLV ON)<sup>(1)</sup>

| Speed | Symbol              | Parameter                                                                 | Conditions                                                              | Min | Max  | Unit |
|-------|---------------------|---------------------------------------------------------------------------|-------------------------------------------------------------------------|-----|------|------|
| 00    | $F_{\max}^{(2)}$    | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 8    | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 10   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 12   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 14   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 16   |      |
|       | $t_r/t_f^{(3)}$     | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 17.8 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 15.8 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 14.4 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 13.1 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 11.4 |      |
| 01    | $F_{\max}^{(2)}$    | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 40   | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 45   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 50   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 55   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 60   |      |
|       | $t_r/t_f^{(3)(4)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 7.2  | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 6.5  |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 5.6  |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 4.8  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 3.8  |      |
| 10    | $F_{\max}^{(2)(4)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 60   | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 70   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 90   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 110  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 140  |      |
|       | $t_r/t_f^{(3)(4)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 5.3  | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 4.6  |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 3.8  |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 3.0  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 2.2  |      |

Table 64. Output timing characteristics (HSLV ON)<sup>(1)</sup> (continued)

| Speed | Symbol              | Parameter                                                                 | Conditions                                                              | Min | Max | Unit |
|-------|---------------------|---------------------------------------------------------------------------|-------------------------------------------------------------------------|-----|-----|------|
| 11    | $F_{\max}^{(2)(4)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 67  | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 100 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 120 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 155 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 200 |      |
|       | $t_r/t_f^{(3)(4)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 5.0 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 4.1 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 3.3 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 2.5 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.71 \text{ V} \leq V_{\text{DD}} \leq 2 \text{ V}$ | -   | 1.8 |      |

1. Specified by design - Not tested in production.

2. The maximum frequency is defined with the conditions:  $(t_r+t_f) \leq 2/3 T$ ,  $\text{Skew} \leq 1/20 T$ ,  $45\% < \text{Duty cycle} < 55\%$ .

3. The fall and rise times are defined, respectively, between 90 and 10% and between 10 and 90% of the output waveform.

4. Compensation system enabled.

Table 65. Output timing characteristics  $V_{\text{DDIO2}} 1.2 \text{ V range}$  (HSLV OFF)<sup>(1)</sup>

| Speed | Symbol           | Parameter                                                                 | Conditions                                                                    | Min | Max  | Unit |
|-------|------------------|---------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----|------|------|
| 00    | $F_{\max}^{(2)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 1    | MHz  |
|       |                  |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 1    |      |
|       |                  |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 1    |      |
|       |                  |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 1    |      |
|       |                  |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 1    |      |
|       | $t_r/t_f^{(3)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 83.0 | ns   |
|       |                  |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 79.0 |      |
|       |                  |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 46.0 |      |
|       |                  |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 72.0 |      |
|       |                  |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{\text{DDIO2}} \leq 1.32 \text{ V}$ | -   | 68.0 |      |

Table 65. Output timing characteristics  $V_{DDIO2}$  1.2 V range (HSLV OFF)<sup>(1)</sup> (continued)

| Speed | Symbol              | Parameter                                                                 | Conditions                                                             | Min | Max  | Unit |
|-------|---------------------|---------------------------------------------------------------------------|------------------------------------------------------------------------|-----|------|------|
| 01    | $F_{\max}^{(2)}$    | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    |      |
|       | $t_r/t_f^{(3)}$     | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 24.5 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 22.2 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 20.0 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 17.8 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 15.0 |      |
| 10    | $F_{\max}^{(2)}$    | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 10   | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 10   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 10   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 10   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 10   |      |
|       | $t_r/t_f^{(3)}$     | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 16.2 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 14.3 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 12.2 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 10.0 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 7.9  |      |
| 11    | $F_{\max}^{(2)(4)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 20   | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 23   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 25   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 28   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 30   |      |
|       | $t_r/t_f^{(3)(4)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 14.0 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 12.0 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 10.0 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 8.0  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 6.0  |      |

1. Specified by design - Not tested in production.

2. The maximum frequency is defined with the conditions  $(t_r + t_f) \leq 2/3 T$ , Skew  $\leq 1/20 T$ , 45% < Duty cycle < 55%.

3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

4. Compensation system enabled.

Table 66. Output timing characteristics  $V_{DDIO2}$  1.2 V (HSLV ON)<sup>(1)</sup>

| Speed | Symbol              | Parameter                                                                 | Conditions                                                             | Min | Max  | Unit |
|-------|---------------------|---------------------------------------------------------------------------|------------------------------------------------------------------------|-----|------|------|
| 00    | $F_{\max}^{(2)}$    | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5    |      |
|       | $t_r/t_f^{(3)}$     | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 32.5 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 30.0 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 27.5 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 25.0 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 22.5 |      |
| 01    | $F_{\max}^{(2)}$    | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 15.0 | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 17.5 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 20.0 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 22.5 |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 25.0 |      |
|       | $t_r/t_f^{(3)}$     | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 14.6 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 12.9 |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 11.2 |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 9.3  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 7.3  |      |
| 10    | $F_{\max}^{(2)(4)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 25   | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 30   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 33   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 44   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 55   |      |
|       | $t_r/t_f^{(3)(4)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 11.6 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 9.7  |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 7.8  |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 6.1  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 4.3  |      |

Table 66. Output timing characteristics  $V_{DDIO2}$  1.2 V (HSLV ON)<sup>(1)</sup> (continued)

| Speed | Symbol              | Parameter                                                                 | Conditions                                                             | Min | Max  | Unit |
|-------|---------------------|---------------------------------------------------------------------------|------------------------------------------------------------------------|-----|------|------|
| 11    | $F_{\max}^{(2)(4)}$ | Maximum frequency                                                         | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 30   | MHz  |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 35   |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 44   |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 55   |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 77   |      |
|       | $t_r/t_f^{(3)(4)}$  | Output high to low level fall time and output low to high level rise time | $C = 50 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 11.1 | ns   |
|       |                     |                                                                           | $C = 40 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 9.2  |      |
|       |                     |                                                                           | $C = 30 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 7.2  |      |
|       |                     |                                                                           | $C = 20 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 5.4  |      |
|       |                     |                                                                           | $C = 10 \text{ pF}, 1.08 \text{ V} \leq V_{DDIO2} \leq 1.32 \text{ V}$ | -   | 3.6  |      |

1. Specified by design - Not tested in production.

2. The maximum frequency is defined with the conditions  $(t_r + t_f) \leq 2/3 T$ ,  $\text{Skew} \leq 1/20 T$ ,  $45\% < \text{Duty cycle} < 55\%$ .

3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

4. Compensation system enabled.

Table 67. Output timing characteristics for FT\_c I/Os (PB13/PB14)<sup>(1)(2)</sup>

| Speed | Symbol     | Parameter                 | Conditions                                                          | Min | Max | Unit |
|-------|------------|---------------------------|---------------------------------------------------------------------|-----|-----|------|
| 00    | $F_{\max}$ | Maximum frequency         | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{DDIO} \leq 3.6 \text{ V}$ | -   | 2   | MHz  |
|       |            |                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{DDIO} < 2.7 \text{ V}$   | -   | 1   |      |
|       | $t_r/t_f$  | Output rise and fall time | $C = 50 \text{ pF}, 2.7 \text{ V} \leq V_{DDIO} < 3.6 \text{ V}$    | -   | 166 | ns   |
|       |            |                           | $C = 50 \text{ pF}, 1.71 \text{ V} \leq V_{DDIO} < 2.7 \text{ V}$   | -   | 330 |      |
| 01    | $F_{\max}$ | Maximum frequency         | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{DDIO} < 3.6 \text{ V}$    | -   | 10  | MHz  |
|       |            |                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{DDIO} < 2.7 \text{ V}$   | -   | 4   |      |
|       | $t_r/t_f$  | Output rise and fall time | $C = 30 \text{ pF}, 2.7 \text{ V} \leq V_{DDIO} < 3.6 \text{ V}$    | -   | 33  | ns   |
|       |            |                           | $C = 30 \text{ pF}, 1.71 \text{ V} \leq V_{DDIO} < 2.7 \text{ V}$   | -   | 65  |      |

1. Specified by design - Not tested in production.

2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the product reference manual for a description of GPIO port configuration register.

### 5.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 58](#)).

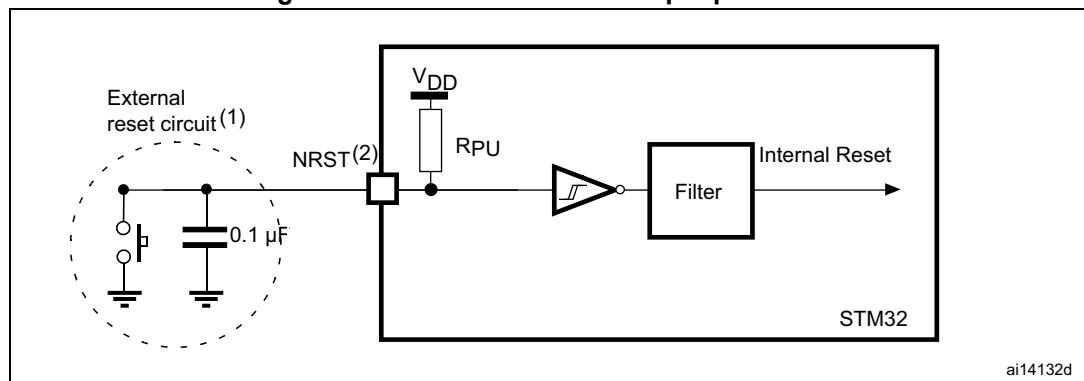
Unless otherwise specified, the parameters in [Table 68](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 20](#).

Table 68. NRST pin characteristics

| Symbol               | Parameter                                       | Conditions                              | Min | Typ | Max | Unit       |
|----------------------|-------------------------------------------------|-----------------------------------------|-----|-----|-----|------------|
| $R_{PU}^{(2)}$       | Weak pull-up equivalent resistor <sup>(1)</sup> | $V_{IN} = V_{SS}$                       | 30  | 40  | 50  | k $\Omega$ |
| $V_{F(NRST)}^{(2)}$  | NRST input filtered pulse                       | $1.71\text{ V} < V_{DD} < 3.6\text{ V}$ | -   | -   | 50  | ns         |
| $V_{NF(NRST)}^{(2)}$ | NRST input not filtered pulse                   | $1.71\text{ V} < V_{DD} < 3.6\text{ V}$ | 350 | -   | -   |            |

1. The pull-up is designed with a true resistance in series with a switchable PMOS. The PMOS contribution to the series resistance is minimum (~10 % order).
2. Specified by design - Not tested in production.

Figure 33. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 58](#), otherwise the reset is not taken into account by the device.

### 5.3.17 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length to ensure its detection by the event controller.

Table 69. EXTI input characteristics<sup>(1)</sup>

| Symbol | Parameter                        | Conditions | Min | Typ | Max | Unit |
|--------|----------------------------------|------------|-----|-----|-----|------|
| PLEC   | Pulse length to event controller | -          | 20  | -   | -   | ns   |

1. Specified by design - Not tested in production.

### 5.3.18 FMC characteristics

Unless otherwise specified, the parameters given in tables [70](#) to [83](#) are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency, and  $V_{DD}$  supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to  $OSPEEDRy[1:0] = 11$
- Measurement points are done at CMOS levels:  $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when  $V_{DD} \leq 2.7\text{ V}$
- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics.

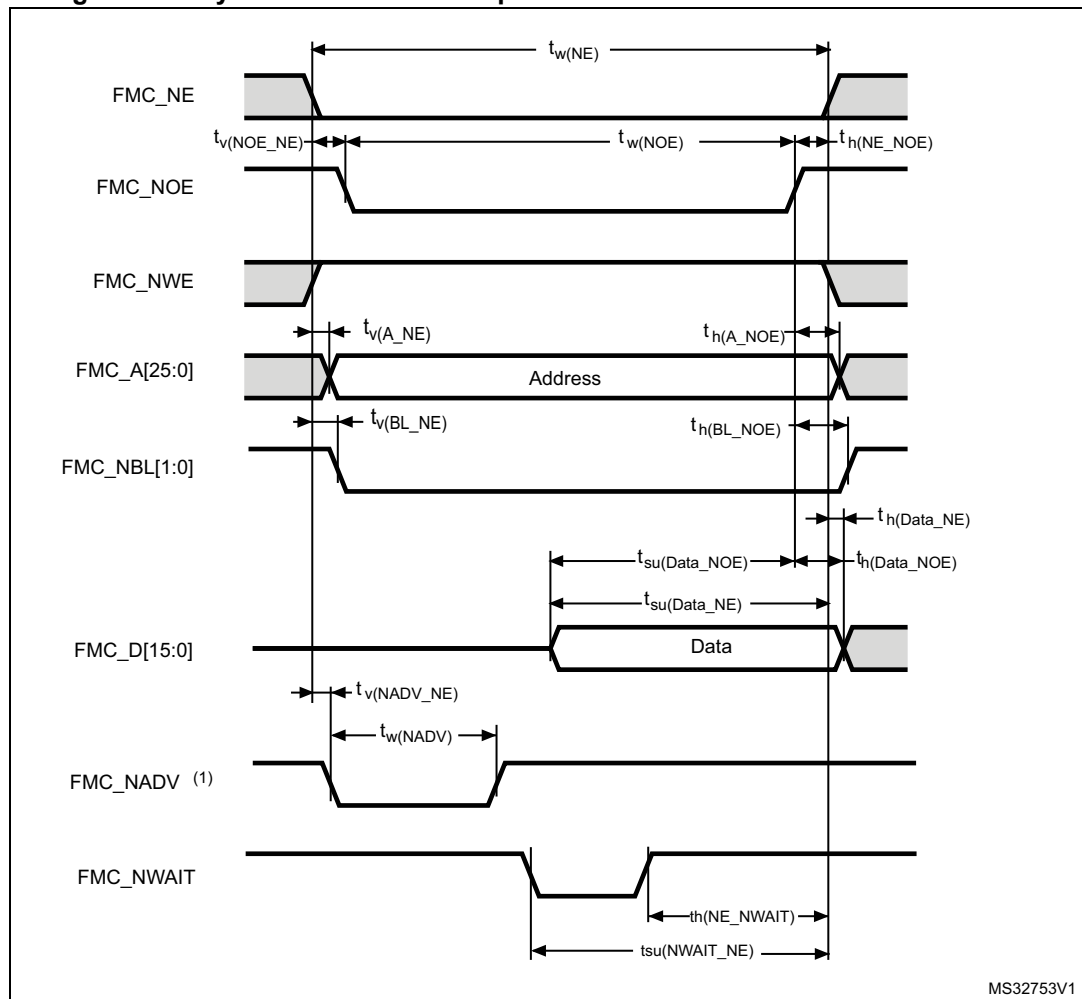
### Asynchronous waveforms and timings

Figures 34 through 36 represent asynchronous waveforms, tables 70 through 77 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load  $C_L = 30$  pF

In all timing tables, the  $T_{fmc\_ker\_ck}$  is the  $f_{HCLK}$  clock period.

**Figure 34. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**



1. Mode 2/B, C and D only. In Mode 1, FMC\_NADV is not used.

**Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings<sup>(1)</sup>**

| Symbol              | Parameter                             | Min                        | Max                      | Unit |
|---------------------|---------------------------------------|----------------------------|--------------------------|------|
| $t_{w(NE)}$         | FMC_NE low time                       | $3 T_{fmc\_ker\_ck} - 1$   | $3 T_{fmc\_ker\_ck} + 1$ | ns   |
| $t_{v(NOE\_NE)}$    | FMC_NEx low to FMC_NOE low            | 0                          | 0.5                      |      |
| $t_{w(NOE)}$        | FMC_NOE low time                      | $2 T_{fmc\_ker\_ck} - 1$   | $2 T_{fmc\_ker\_ck} + 1$ |      |
| $t_{h(NE\_NOE)}$    | FMC_NOE high to FMC_NE high hold time | $T_{fmc\_ker\_ck} - 0.5$   | -                        |      |
| $t_{v(A\_NE)}$      | FMC_NEx low to FMC_A valid            | -                          | 1                        |      |
| $t_{h(A\_NOE)}$     | Address hold time after FMC_NOE high  | $2 T_{fmc\_ker\_ck} - 1.5$ | -                        |      |
| $t_{su(Data\_NE)}$  | Data to FMC_NEx high setup time       | $T_{fmc\_ker\_ck} + 10$    | -                        |      |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOEx high setup time      | 9                          | -                        |      |
| $t_{h(Data\_NOE)}$  | Data hold time after FMC_NOE high     | 0                          | -                        |      |
| $t_{h(Data\_NE)}$   | Data hold time after FMC_NEx high     | 0                          | -                        |      |
| $t_{v(NADV\_NE)}$   | FMC_NEx low to FMC_NADV low           | -                          | 0.5                      |      |
| $t_{w(NADV)}$       | FMC_NADV low time                     | -                          | $T_{fmc\_ker\_ck} + 1$   |      |

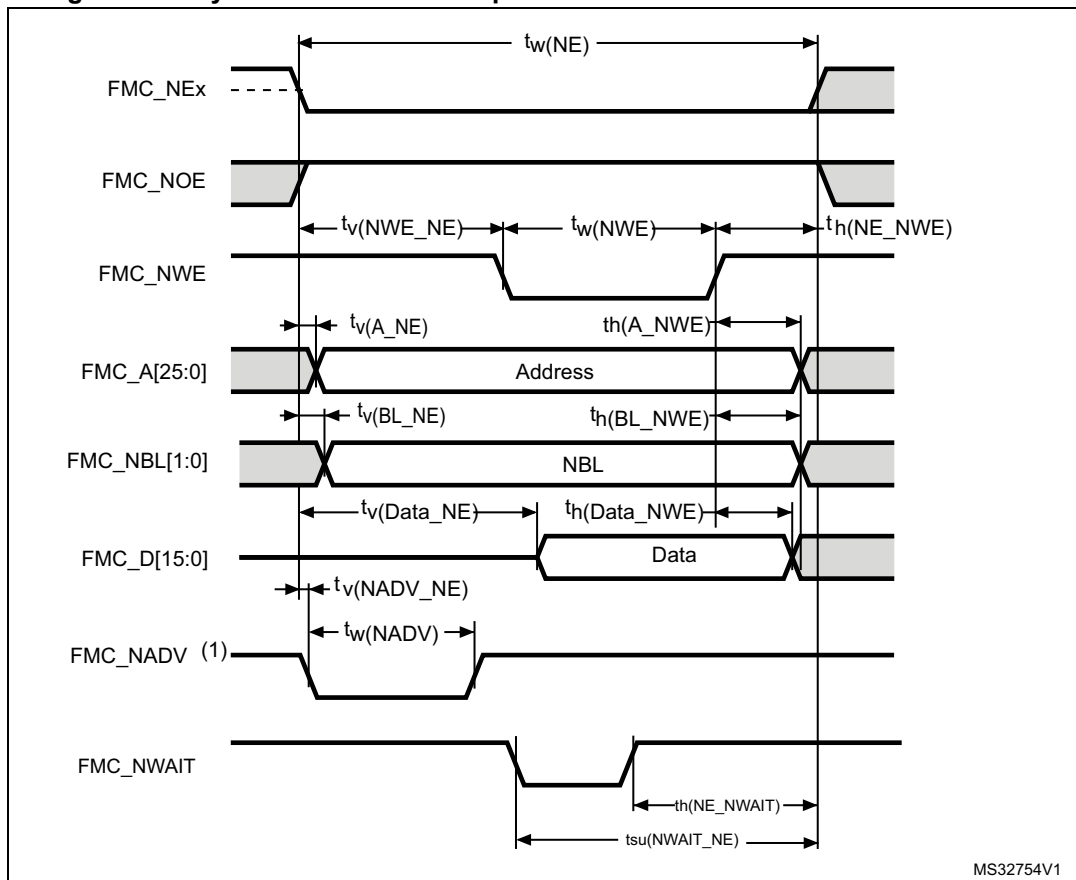
1. Evaluated by characterization - Not tested in production.

**Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings<sup>(1)(2)</sup>**

| Symbol              | Parameter                                 | Min                       | Max                      | Unit |
|---------------------|-------------------------------------------|---------------------------|--------------------------|------|
| $t_{w(NE)}$         | FMC_NE low time                           | $8 T_{fmc\_ker\_ck} - 1$  | $8 T_{fmc\_ker\_ck} + 1$ | ns   |
| $t_{w(NOE)}$        | FMC_NOE low time                          | $7 T_{fmc\_ker\_ck} - 1$  | $7 T_{fmc\_ker\_ck} + 1$ |      |
| $t_{w(NWAIT)}$      | FMC_NWAIT low time                        | $T_{fmc\_ker\_ck} - 0.5$  | -                        |      |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high       | $5 T_{fmc\_ker\_ck} + 10$ | -                        |      |
| $t_{h(NE\_NWAIT)}$  | FMC_NEx hold time after FMC_NWAIT invalid | $4 T_{fmc\_ker\_ck} + 10$ | -                        |      |

1. Evaluated by characterization - Not tested in production.

2.  $N_{WAIT}$  pulse width is equal to one  $fmc\_ker\_ck$  cycle.

**Figure 35. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**

1. Mode 2/B, C and D only. In Mode 1, FMC\_NADV is not used.

**Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings<sup>(1)</sup>**

| Symbol             | Parameter                             | Min                      | Max                      | Unit |
|--------------------|---------------------------------------|--------------------------|--------------------------|------|
| $t_{w(NE)}$        | FMC_NE low time                       | $3 T_{fmc\_ker\_ck} - 1$ | $3 T_{fmc\_ker\_ck} + 1$ | ns   |
| $t_{v(NWE\_NE)}$   | FMC_NEx low to FMC_NWE low            | $T_{fmc\_ker\_ck} - 1$   | $T_{fmc\_ker\_ck} + 0.5$ |      |
| $t_{w(NWE)}$       | FMC_NWE low time                      | $T_{fmc\_ker\_ck} - 1$   | $T_{fmc\_ker\_ck} + 1$   |      |
| $t_{h(NE\_NWE)}$   | FMC_NWE high to FMC_NE high hold time | $T_{fmc\_ker\_ck} - 1$   | -                        |      |
| $t_{v(A\_NE)}$     | FMC_NEx low to FMC_A valid            | -                        | 0.5                      |      |
| $t_{h(A\_NWE)}$    | Address hold time after FMC_NWE high  | $T_{fmc\_ker\_ck} - 1$   | -                        |      |
| $t_{v(BL\_NE)}$    | FMC_NEx low to FMC_BL valid           | -                        | 0.5                      |      |
| $t_{h(BL\_NWE)}$   | FMC_BL hold time after FMC_NWE high   | $T_{fmc\_ker\_ck} - 1$   | -                        |      |
| $t_{v(Data\_NE)}$  | Data to FMC_NEx low to Data valid     | -                        | $T_{fmc\_ker\_ck} + 1$   |      |
| $t_{h(Data\_NWE)}$ | Data hold time after FMC_NWE high     | $T_{fmc\_ker\_ck}$       | -                        |      |
| $t_{v(NADV\_NE)}$  | FMC_NEx low to FMC_NADV low           | -                        | 0.5                      |      |
| $t_{w(NADV)}$      | FMC_NADV low time                     | -                        | $T_{fmc\_ker\_ck} + 1$   |      |

1. Evaluated by characterization - Not tested in production.

**Table 73. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings<sup>(1)(2)</sup>**

| Symbol              | Parameter                                 | Min                       | Max                      | Unit |
|---------------------|-------------------------------------------|---------------------------|--------------------------|------|
| $t_{w(NE)}$         | FMC_NE low time                           | $8 T_{fmc\_ker\_ck} - 1$  | $8 T_{fmc\_ker\_ck} + 1$ | ns   |
| $t_{w(NWE)}$        | FMC_NWE low time                          | $6 T_{fmc\_ker\_ck} - 1$  | $6 T_{fmc\_ker\_ck} + 1$ |      |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high       | $5 T_{fmc\_ker\_ck} + 10$ | -                        |      |
| $t_{h(NE\_NWAIT)}$  | FMC_NEx hold time after FMC_NWAIT invalid | $4 T_{fmc\_ker\_ck} + 10$ | -                        |      |

1. Evaluated by characterization - Not tested in production.

2.  $N_{WAIT}$  pulse width is equal to one  $fmc\_ker\_ck$  cycle.

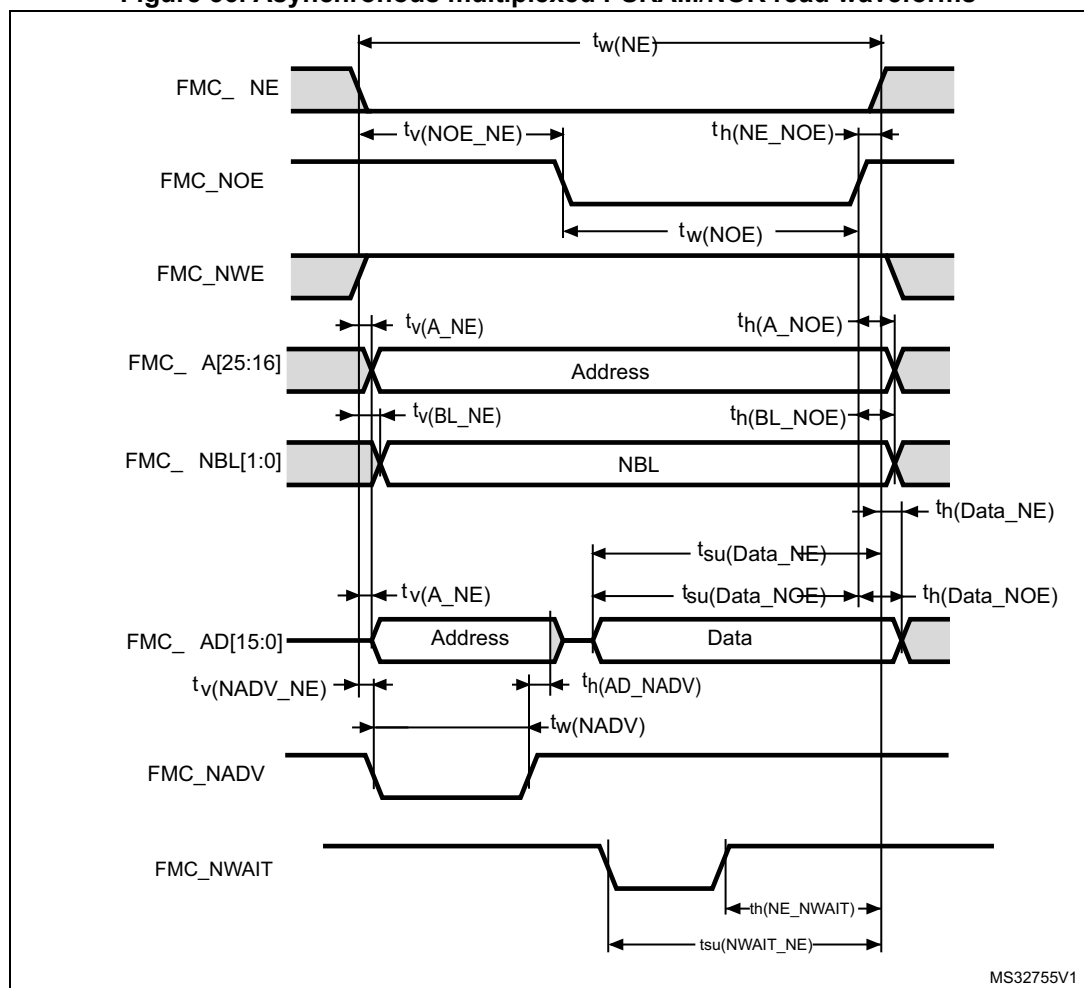
**Figure 36. Asynchronous multiplexed PSRAM/NOR read waveforms**

Table 74. Asynchronous multiplexed PSRAM/NOR read timings<sup>(1)</sup>

| Symbol              | Parameter                                           | Min                        | Max                        | Unit |
|---------------------|-----------------------------------------------------|----------------------------|----------------------------|------|
| $t_{w(NE)}$         | FMC_NE low time                                     | $4 T_{fmc\_ker\_ck} - 1$   | $4 T_{fmc\_ker\_ck} + 1$   | ns   |
| $t_{v(NOE\_NE)}$    | FMC_NEx low to FMC_NOE low                          | $2 T_{fmc\_ker\_ck} - 1$   | $2 T_{fmc\_ker\_ck} + 0.5$ |      |
| $t_{tw(NOE)}$       | FMC_NOE low time                                    | $T_{fmc\_ker\_ck} - 1$     | $T_{fmc\_ker\_ck} + 1$     |      |
| $t_{h(NE\_NOE)}$    | FMC_NOE high to FMC_NE high hold time               | $T_{fmc\_ker\_ck} - 0.5$   | -                          |      |
| $t_{v(A\_NE)}$      | FMC_NEx low to FMC_A valid                          | -                          | 1                          |      |
| $t_{v(NADV\_NE)}$   | FMC_NEx low to FMC_NADV low                         | 0                          | 1                          |      |
| $t_{w(NADV)}$       | FMC_NADV low time                                   | $T_{fmc\_ker\_ck} - 0.5$   | $T_{fmc\_ker\_ck} + 1$     |      |
| $t_{h(AD\_NADV)}$   | FMC_AD(address) valid hold time after FMC_NADV high | $T_{fmc\_ker\_ck} + 0.5$   | -                          |      |
| $t_{h(A\_NOE)}$     | Address hold time after FMC_NOE high                | $2 T_{fmc\_ker\_ck} - 0.5$ | -                          |      |
| $t_{su(Data\_NE)}$  | Data to FMC_NEx high setup time                     | $T_{fmc\_ker\_ck} + 10$    | -                          |      |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOE high setup time                     | 9                          | -                          |      |
| $t_{h(Data\_NE)}$   | Data hold time after FMC_NEx high                   | 0                          | -                          |      |
| $t_{h(Data\_NOE)}$  | Data hold time after FMC_NOE high                   | 0                          | -                          |      |

1. Evaluated by characterization - Not tested in production.

Table 75. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings<sup>(1) (2)</sup>

| Symbol              | Parameter                                 | Min                       | Max                      | Unit |
|---------------------|-------------------------------------------|---------------------------|--------------------------|------|
| $t_{w(NE)}$         | FMC_NE low time                           | $9 T_{fmc\_ker\_ck} - 1$  | $9 T_{fmc\_ker\_ck} + 1$ | ns   |
| $t_{w(NOE)}$        | FMC_NOE low time                          | $7 T_{fmc\_ker\_ck} - 1$  | $7 T_{fmc\_ker\_ck} + 1$ |      |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high       | $4 T_{fmc\_ker\_ck} + 10$ | -                        |      |
| $t_{h(NE\_NWAIT)}$  | FMC_NEx hold time after FMC_NWAIT invalid | $3 T_{fmc\_ker\_ck} + 10$ | -                        |      |

1. Evaluated by characterization - Not tested in production.

2. NWAIT pulse width is equal to one fmc\_ker\_ck cycle.

Figure 37. Asynchronous multiplexed PSRAM/NOR write waveforms

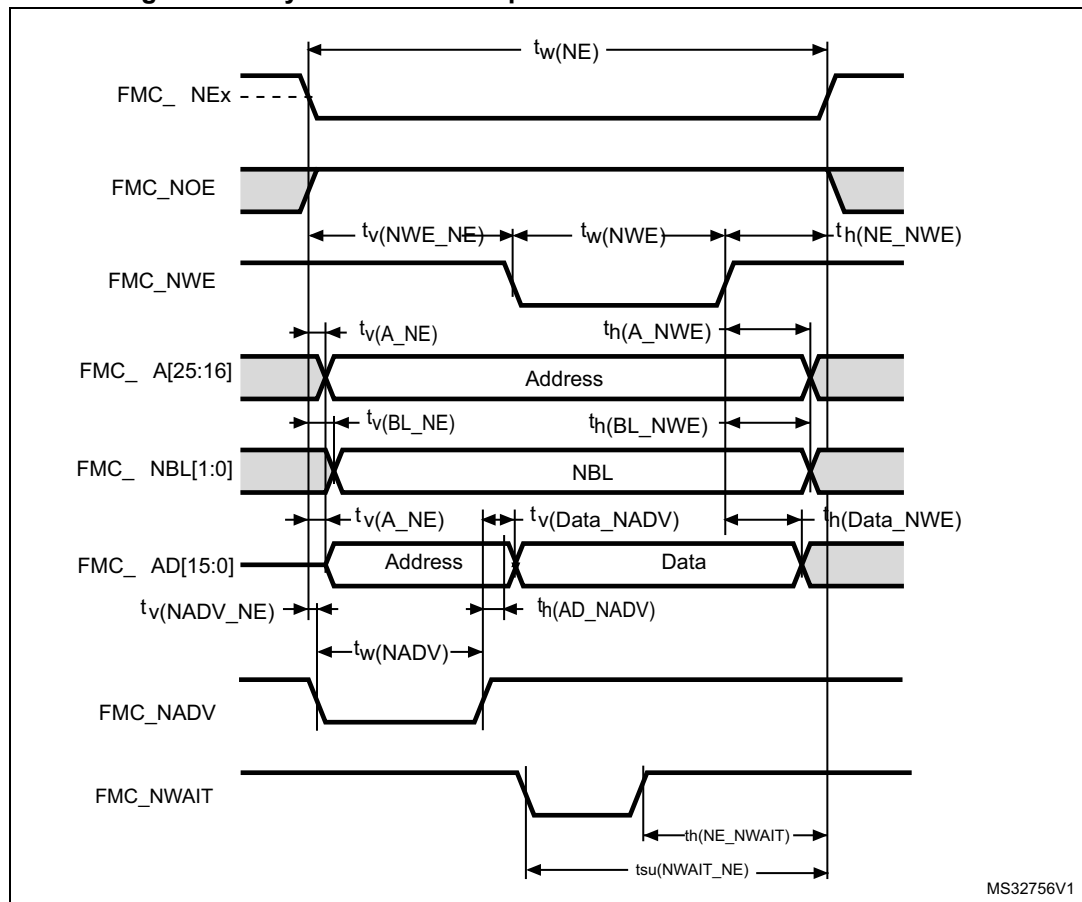


Table 76. Asynchronous multiplexed PSRAM/NOR write timings<sup>(1)</sup>

| Symbol              | Parameter                                           | Min                      | Max                      | Unit |
|---------------------|-----------------------------------------------------|--------------------------|--------------------------|------|
| $t_{w(NE)}$         | FMC_NE low time                                     | $4 T_{fmc\_ker\_ck} - 1$ | $4 T_{fmc\_ker\_ck} + 1$ | ns   |
| $t_{v(NWE\_NE)}$    | FMC_NEx low to FMC_NWE low                          | $T_{fmc\_ker\_ck} - 1$   | $T_{fmc\_ker\_ck} + 0.5$ |      |
| $t_{w(NWE)}$        | FMC_NWE low time                                    | $2 T_{fmc\_ker\_ck} - 1$ | $2 T_{fmc\_ker\_ck} + 1$ |      |
| $t_{h(NE\_NWE)}$    | FMC_NWE high to FMC_NE high hold time               | $T_{fmc\_ker\_ck} - 0.5$ | -                        |      |
| $t_{v(A\_NE)}$      | FMC_NEx low to FMC_A valid                          | -                        | 0.5                      |      |
| $t_{v(NADV\_NE)}$   | FMC_NEx low to FMC_NADV low                         | 0                        | 1                        |      |
| $t_{w(NADV)}$       | FMC_NADV low time                                   | $T_{fmc\_ker\_ck} - 1$   | $T_{fmc\_ker\_ck} + 1$   |      |
| $t_{h(AD\_NADV)}$   | FMC_AD(address) valid hold time after FMC_NADV high | $T_{fmc\_ker\_ck} - 1$   | -                        |      |
| $t_{h(A\_NWE)}$     | Address hold time after FMC_NWE high                | $T_{fmc\_ker\_ck} - 1$   | -                        |      |
| $t_{h(BL\_NWE)}$    | FMC_BL hold time after FMC_NWE high                 | $T_{fmc\_ker\_ck} - 1$   | -                        |      |
| $t_{v(BL\_NE)}$     | FMC_NEx low to FMC_BL valid                         | -                        | 0.5                      |      |
| $t_{v(Data\_NADV)}$ | FMC_NADV high to Data valid                         | -                        | $T_{fmc\_ker\_ck} + 0.5$ |      |
| $t_{h(Data\_NWE)}$  | Data hold time after FMC_NWE high                   | $T_{fmc\_ker\_ck} - 0.5$ | -                        |      |

1. Evaluated by characterization - Not tested in production.

Table 77. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings<sup>(1)(2)</sup>

| Symbol              | Parameter                                 | Min                       | Max                      | Unit |
|---------------------|-------------------------------------------|---------------------------|--------------------------|------|
| $t_{w(NE)}$         | FMC_NE low time                           | $9 T_{fmc\_ker\_ck} - 1$  | $9 T_{fmc\_ker\_ck} + 1$ | ns   |
| $t_{w(NWE)}$        | FMC_NWE low time                          | $7 T_{fmc\_ker\_ck} - 1$  | $7 T_{fmc\_ker\_ck} + 1$ |      |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high       | $5 T_{fmc\_ker\_ck} + 10$ | -                        |      |
| $t_{h(NE\_NWAIT)}$  | FMC_NEx hold time after FMC_NWAIT invalid | $4 T_{fmc\_ker\_ck} + 10$ | -                        |      |

1. Evaluated by characterization - Not tested in production.

2.  $N_{WAIT}$  pulse width is equal to one  $fmc\_ker\_ck$  cycle.

Figures 38 through 41 represent synchronous waveforms, tables 78 through 81 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC\_BurstAccessMode\_Enable
- MemoryType = FMC\_MemoryType\_CRAM
- WriteBurst = FMC\_WriteBurst\_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash, DataLatency = 0 for PSRAM.
- With capacity load  $C_L = 30 \text{ pF}$

- For  $2.7\text{ V} < V_{DD} < 3.6\text{ V}$ : maximum FMC\_CLK = 100 MHz at  $C_L = 20\text{ pF}$
- For  $1.71\text{ V} < V_{DD} < 1.8\text{ V}$ : maximum FMC\_CLK = 95 MHz at  $C_L = 20\text{ pF}$
- For  $1.71\text{ V} < V_{DD} < 1.8\text{ V}$ : maximum FMC\_CLK = 100 MHz at  $C_L = 15\text{ pF}$

Table 78. Synchronous multiplexed NOR/PSRAM read timings<sup>(1)</sup>

| Symbol               | Parameter                                       | Min                       | Max | Unit |
|----------------------|-------------------------------------------------|---------------------------|-----|------|
| $t_{w(CLK)}$         | FMC_CLK period                                  | $2T_{fmc\_ker\_ck} - 0.5$ | -   | ns   |
| $t_{d(CLKL-NExL)}$   | FMC_CLK low to FMC_NEx low ( $x = 0..2$ )       | -                         | 1   |      |
| $t_{d(CLKH-NExH)}$   | FMC_CLK high to FMC_NEx high ( $x = 0..2$ )     | $T_{fmc\_ker\_ck} - 1$    | -   |      |
| $t_{d(CLKL-NADV_L)}$ | FMC_CLK low to FMC_NADV low                     | -                         | 1.5 |      |
| $t_{d(CLKL-NADV_H)}$ | FMC_CLK low to FMC_NADV high                    | 0.5                       | -   |      |
| $t_{d(CLKL-AV)}$     | FMC_CLK low to FMC_Ax valid ( $x = 16..25$ )    | -                         | 1   |      |
| $t_{d(CLKH-AIV)}$    | FMC_CLK high to FMC_Ax invalid ( $x = 16..25$ ) | $T_{fmc\_ker\_ck} - 1$    | -   |      |
| $t_{d(CLKL-NOEL)}$   | FMC_CLK low to FMC_NOE low                      | -                         | 1   |      |
| $t_{d(CLKH-NOEH)}$   | FMC_CLK high to FMC_NOE high                    | $T_{fmc\_ker\_ck} + 0.5$  | -   |      |
| $t_{d(CLKL-ADV)}$    | FMC_CLK low to FMC_AD[15:0] valid               | -                         | 3.5 |      |
| $t_{d(CLKL-ADIV)}$   | FMC_CLK low to FMC_AD[15:0] invalid             | 0.5                       | -   |      |
| $t_{su(ADV-CLKH)}$   | FMC_A/D[15:0] valid data before FMC_CLK high    | 3.5                       | -   |      |
| $t_h(CLKH-ADV)$      | FMC_A/D[15:0] valid data after FMC_CLK high     | 1.5                       | -   |      |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high             | 2.5                       | -   |      |
| $t_h(CLKH-NWAIT)$    | FMC_NWAIT valid after FMC_CLK high              | 1.5                       | -   |      |

1. Evaluated by characterization - Not tested in production.

Figure 39. Synchronous multiplexed PSRAM write timings

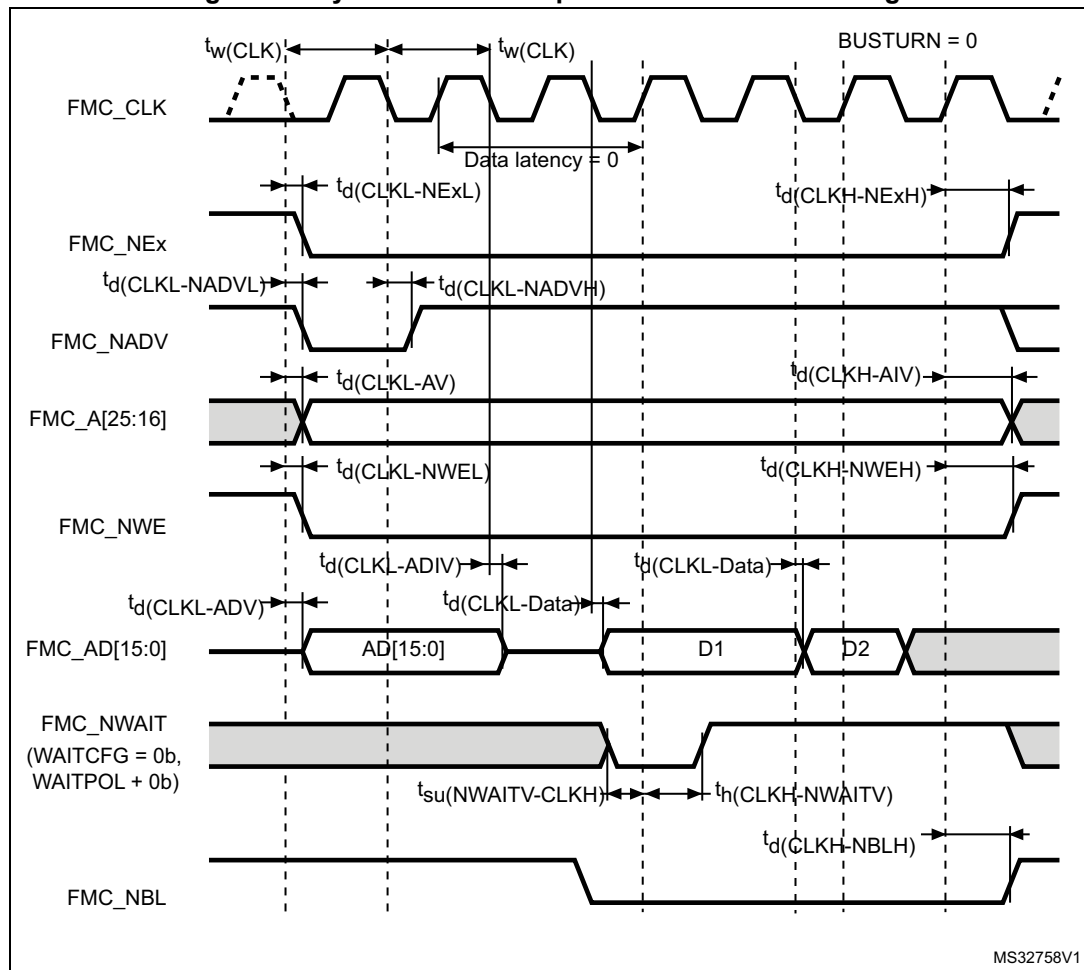
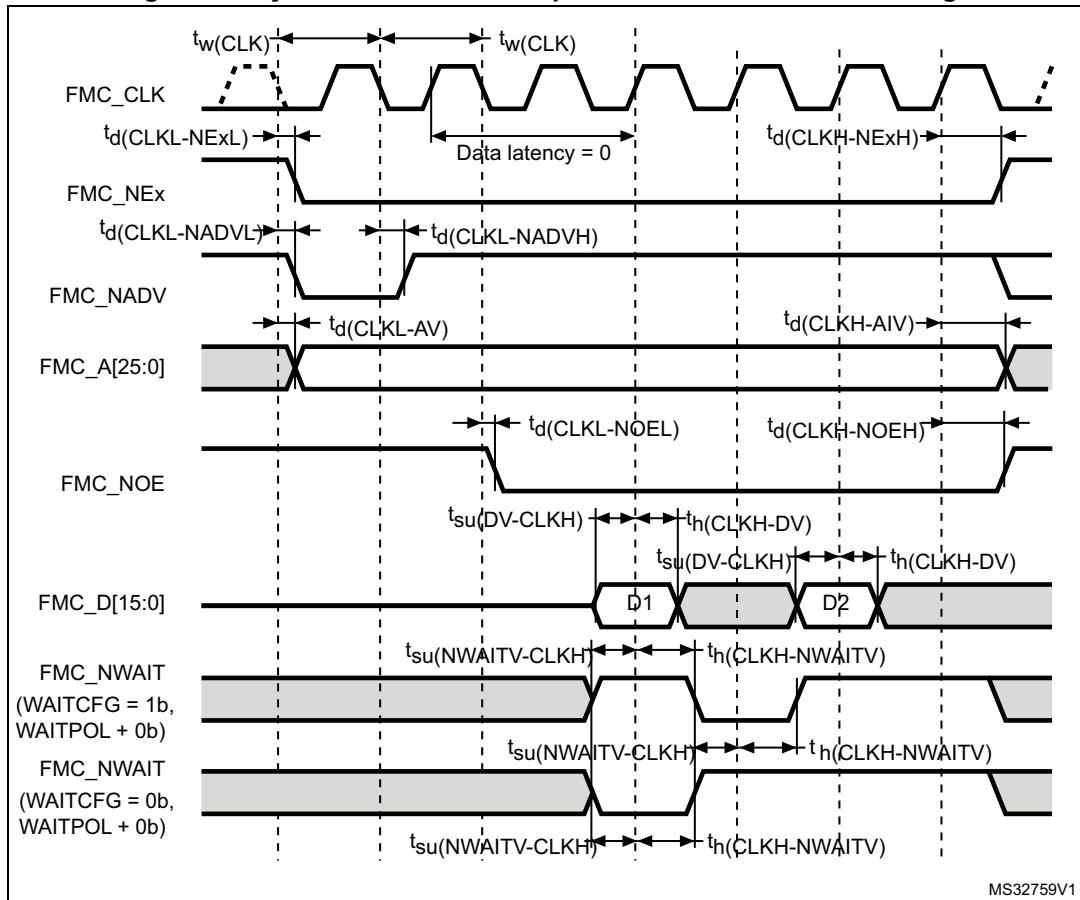


Table 79. Synchronous multiplexed PSRAM write timings<sup>(1)</sup>

| Symbol               | Parameter                                       | Min                       | Max | Unit |
|----------------------|-------------------------------------------------|---------------------------|-----|------|
| $t_{w(CLK)}$         | FMC_CLK period, $V_{DD} = 2.7$ to $3.6$ V       | $2T_{fmc\_ker\_ck} - 0.5$ | -   | ns   |
| $t_{d(CLKL-NExL)}$   | FMC_CLK low to FMC_NEx low ( $x = 0..2$ )       | -                         | 1   |      |
| $t_{d(CLKH-NExH)}$   | FMC_CLK high to FMC_NEx high ( $x = 0..2$ )     | $T_{fmc\_ker\_ck} - 1$    | -   |      |
| $t_{d(CLKL-NADV_L)}$ | FMC_CLK low to FMC_NADV low                     | -                         | 1.5 |      |
| $t_{d(CLKL-NADV_H)}$ | FMC_CLK low to FMC_NADV high                    | 0.5                       | -   |      |
| $t_{d(CLKL-AV)}$     | FMC_CLK low to FMC_Ax valid ( $x = 16..25$ )    | -                         | 1   |      |
| $t_{d(CLKH-AIV)}$    | FMC_CLK high to FMC_Ax invalid ( $x = 16..25$ ) | $T_{fmc\_ker\_ck} - 1$    | -   |      |
| $t_{d(CLKL-NWEL)}$   | FMC_CLK low to FMC_NWE low                      | -                         | 1   |      |
| $t_{d(CLKH-NWEH)}$   | FMC_CLK high to FMC_NWE high                    | $T_{fmc\_ker\_ck} + 0.5$  | -   |      |
| $t_{d(CLKL-ADV)}$    | FMC_CLK low to FMC_AD[15:0] valid               | -                         | 3.5 |      |
| $t_{d(CLKL-ADIV)}$   | FMC_CLK low to FMC_AD[15:0] invalid             | 1                         | -   |      |
| $t_{d(CLKL-DATA)}$   | FMC_A/D[15:0] valid data after FMC_CLK low      | -                         | 1   |      |
| $t_{d(CLKL-NBL_L)}$  | FMC_CLK low to FMC_NBL low                      | -                         | 1   |      |
| $t_{d(CLKH-NBL_H)}$  | FMC_CLK high to FMC_NBL high                    | $T_{fmc\_ker\_ck}$        | -   |      |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high             | 2.5                       | -   |      |
| $t_h(CLKH-NWAIT)$    | FMC_NWAIT valid after FMC_CLK high              | 1.5                       | -   |      |

1. Evaluated by characterization - Not tested in production.

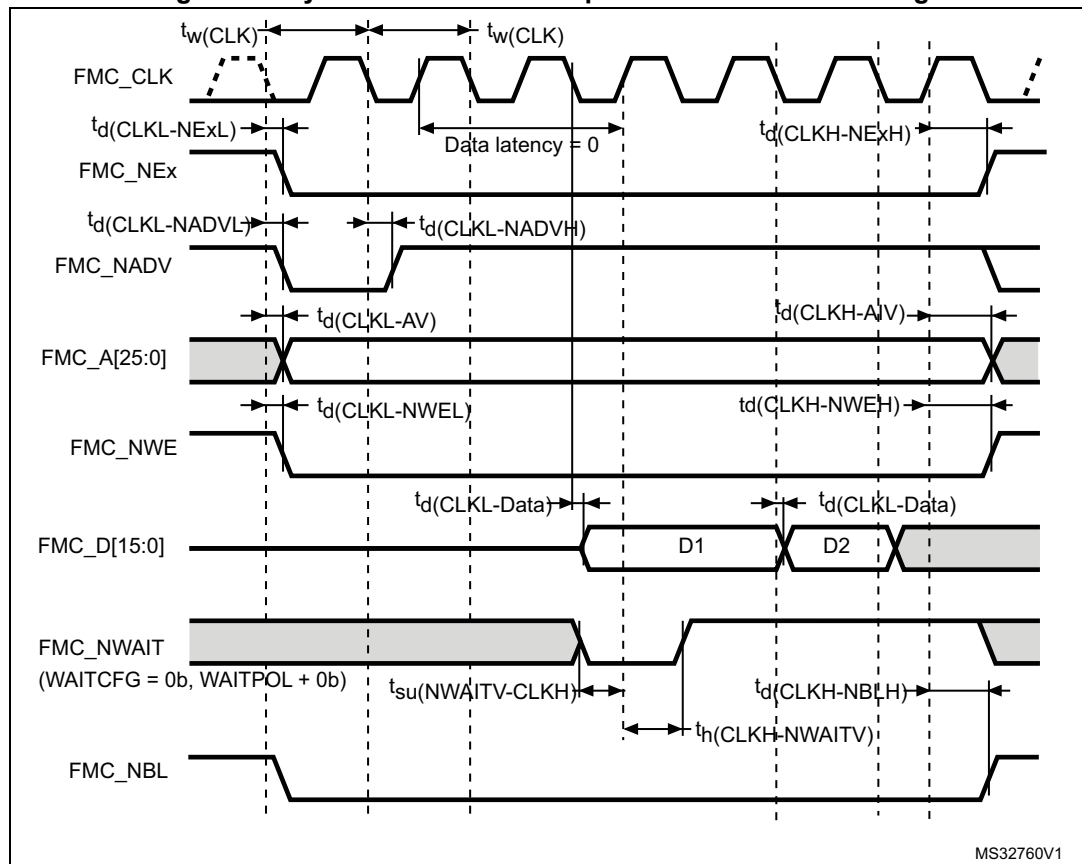
Figure 40. Synchronous non-multiplexed NOR/PSRAM read timings

Table 80. Synchronous non-multiplexed NOR/PSRAM read timings<sup>(1)</sup>

| Symbol                              | Parameter                                            | Min                              | Max | Unit |
|-------------------------------------|------------------------------------------------------|----------------------------------|-----|------|
| $t_w(\text{CLK})$                   | FMC_CLK period                                       | $2T_{\text{fmc\_ker\_ck}} - 0.5$ | -   | ns   |
| $t_{\text{d}}(\text{CLKL-NExL})$    | FMC_CLK low to FMC_NEx low ( $x = 0 \dots 2$ )       | -                                | 1   |      |
| $t_{\text{d}}(\text{CLKH-NExH})$    | FMC_CLK high to FMC_NEx high ( $x = 0 \dots 2$ )     | $T_{\text{fmc\_ker\_ck}} - 1$    | -   |      |
| $t_{\text{d}}(\text{CLKL-NADV})$    | FMC_CLK low to FMC_NADV low                          | -                                | 1.5 |      |
| $t_{\text{d}}(\text{CLKL-NADVH})$   | FMC_CLK low to FMC_NADV high                         | 0.5                              | -   |      |
| $t_{\text{d}}(\text{CLKL-AV})$      | FMC_CLK low to FMC_Ax valid ( $x = 16 \dots 25$ )    | -                                | 1   |      |
| $t_{\text{d}}(\text{CLKH-AIV})$     | FMC_CLK high to FMC_Ax invalid ( $x = 16 \dots 25$ ) | $T_{\text{fmc\_ker\_ck}} - 1$    | -   |      |
| $t_{\text{d}}(\text{CLKL-NOEL})$    | FMC_CLK low to FMC_NOE low                           | -                                | 1   |      |
| $t_{\text{d}}(\text{CLKH-NOEH})$    | FMC_CLK high to FMC_NOE high                         | $T_{\text{fmc\_ker\_ck}} + 0.5$  | -   |      |
| $t_{\text{su}}(\text{DV-CLKH})$     | FMC_D[15:0] valid data before FMC_CLK high           | 3.5                              | -   |      |
| $t_{\text{h}}(\text{CLKH-DV})$      | FMC_D[15:0] valid data after FMC_CLK high            | 1.5                              | -   |      |
| $t_{\text{su}}(\text{NWAITV-CLKH})$ | FMC_NWAIT valid before FMC_CLK high                  | 2.5                              | -   |      |
| $t_{\text{h}}(\text{CLKH-NWAITV})$  | FMC_NWAIT valid after FMC_CLK high                   | 1.5                              | -   |      |

1. Evaluated by characterization - Not tested in production.

Figure 41. Synchronous non-multiplexed PSRAM write timings

Table 81. Synchronous non-multiplexed PSRAM write timings<sup>(1)</sup>

| Symbol                       | Parameter                                            | Min                              | Max | Unit |
|------------------------------|------------------------------------------------------|----------------------------------|-----|------|
| $t_{\text{CLK}}$             | FMC_CLK period                                       | $2T_{\text{fmc\_ker\_ck}} - 0.5$ | -   | ns   |
| $t_{\text{d(CLKxL-NExL)}}$   | FMC_CLK low to FMC_NEx low ( $x = 0 \dots 2$ )       | -                                | 1   |      |
| $t_{\text{CLKH-NExH}}$       | FMC_CLK high to FMC_NEx high ( $x = 0 \dots 2$ )     | $T_{\text{fmc\_ker\_ck}} - 0.5$  | -   |      |
| $t_{\text{d(CLKxL-NADVxL)}}$ | FMC_CLK low to FMC_NADV low                          | -                                | 1.5 |      |
| $t_{\text{d(CLKxL-NADVxH)}}$ | FMC_CLK low to FMC_NADV high                         | 0.5                              | -   |      |
| $t_{\text{d(CLKxL-AV)}}$     | FMC_CLK low to FMC_Ax valid ( $x = 16 \dots 25$ )    | -                                | 1   |      |
| $t_{\text{d(CLKH-AIV)}}$     | FMC_CLK high to FMC_Ax invalid ( $x = 16 \dots 25$ ) | $T_{\text{fmc\_ker\_ck}} + 0.5$  | -   |      |
| $t_{\text{d(CLKxL-NWEL)}}$   | FMC_CLK low to FMC_NWE low                           | -                                | 1   |      |
| $t_{\text{d(CLKH-NWEH)}}$    | FMC_CLK high to FMC_NWE high                         | $T_{\text{fmc\_ker\_ck}} + 0.5$  | -   |      |
| $t_{\text{d(CLKxL-Data)}}$   | FMC_D[15:0] valid data after FMC_CLK low             | -                                | 3.5 |      |
| $t_{\text{d(CLKxL-NBL)}}$    | FMC_CLK low to FMC_NBL low                           | -                                | 1.5 |      |
| $t_{\text{d(CLKH-NBLH)}}$    | FMC_CLK high to FMC_NBL high                         | $T_{\text{fmc\_ker\_ck}} - 0.5$  | -   |      |
| $t_{\text{su(NWAIT-CLKH)}}$  | FMC_NWAIT valid before FMC_CLK high                  | 2.5                              | -   |      |
| $t_{\text{h(CLKH-NWAIT)}}$   | FMC_NWAIT valid after FMC_CLK high                   | 1.5                              | -   |      |

1. Evaluated by characterization - Not tested in production.

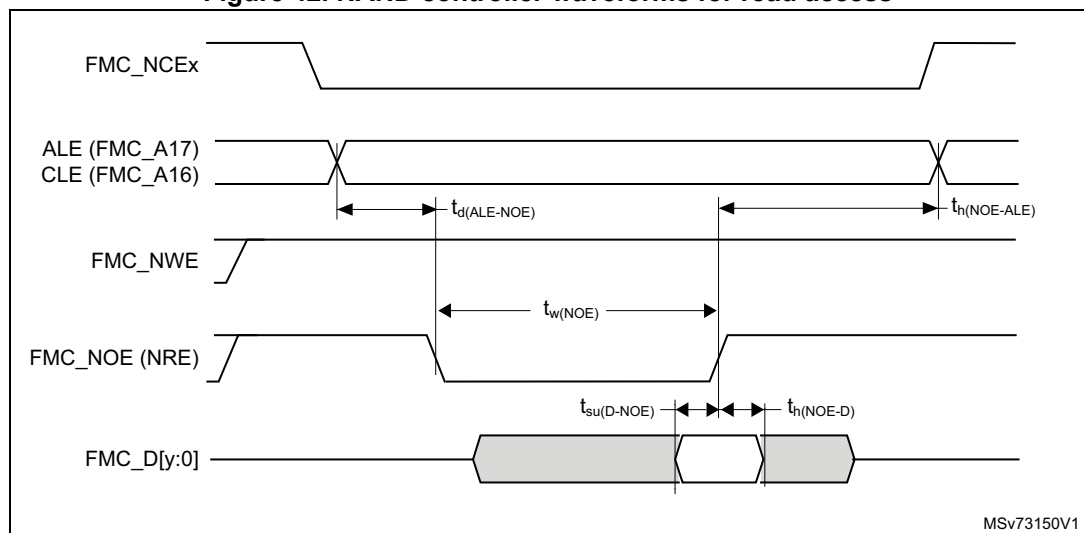
### NAND controller waveforms and timings

Figures 42 through 45 represent synchronous waveforms, tables 82 and 83 provide the corresponding timings. The results are obtained with the following FMC configuration and a capacitive load ( $C_L$ ) of 30 pF:

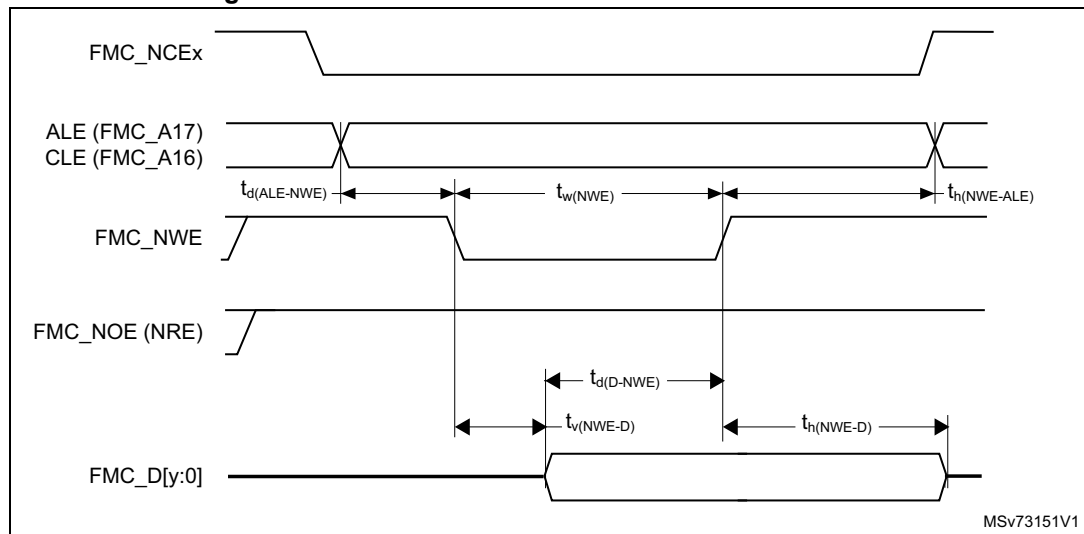
- COM.FMC\_SetupTime = 0x01
- COM.FMC\_WaitSetupTime = 0x03
- COM.FMC\_HoldSetupTime = 0x02
- COM.FMC\_HiZSetupTime = 0x01
- ATT.FMC\_SetupTime = 0x01
- ATT.FMC\_WaitSetupTime = 0x03
- ATT.FMC\_HoldSetupTime = 0x02
- ATT.FMC\_HiZSetupTime = 0x01
- Bank = FMC\_Bank\_NAND
- MemoryDataWidth = FMC\_MemoryDataWidth\_16b
- ECC = FMC\_ECC\_Enable
- ECCPageSize = FMC\_ECCPageSize\_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- Capacitive load  $C_L$  = 30 pF

In all timing tables,  $T_{fmc\_ker\_ck}$  is the HCLK clock period.

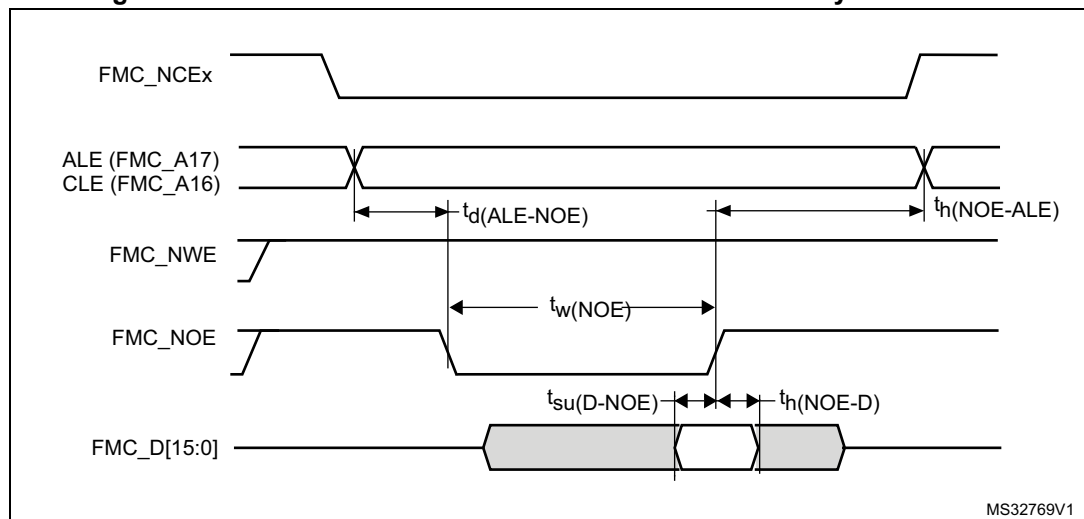
**Figure 42. NAND controller waveforms for read access**

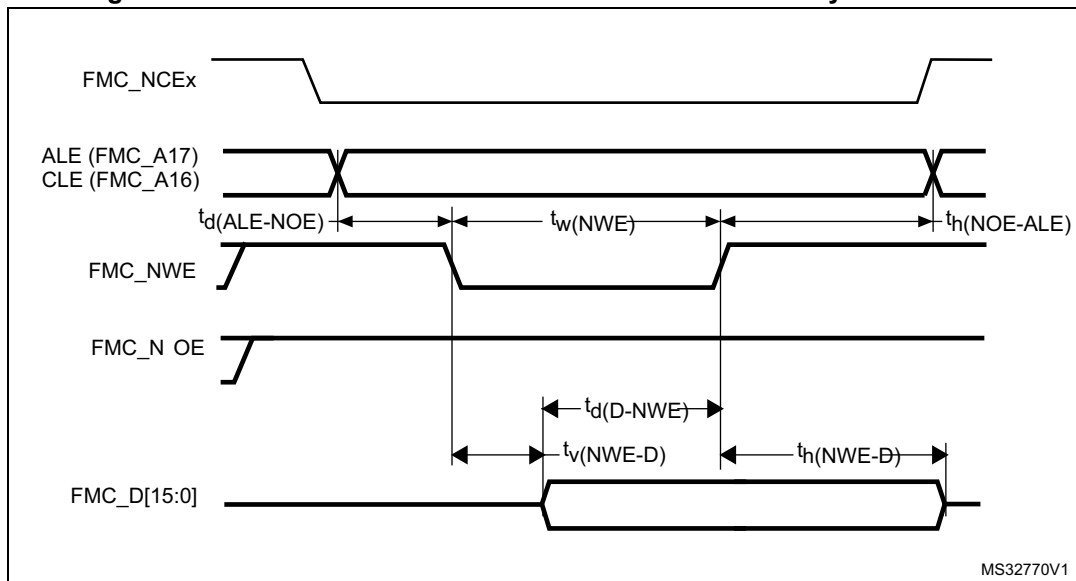


1.  $y = 7$  or  $15$ , depending upon the NAND flash memory interface.

**Figure 43. NAND controller waveforms for write access**

1.  $y = 7$  or  $15$ , depending upon the NAND flash memory interface.

**Figure 44. NAND controller waveforms for common memory read access**

**Figure 45. NAND controller waveforms for common memory write access**

MS32770V1

**Table 82. Switching characteristics for NAND flash read cycles<sup>(1)</sup>**

| Symbol          | Parameter                                  | Min                       | Max                       | Unit |
|-----------------|--------------------------------------------|---------------------------|---------------------------|------|
| $t_{w(NOE)}$    | FMC_NOE low width                          | $4T_{fmc\_ker\_ck} - 0.5$ | $4T_{fmc\_ker\_ck} + 0.5$ | ns   |
| $t_{su(D-NOE)}$ | FMC_D[15-0] valid data before FMC_NOE high | 11                        | -                         |      |
| $t_h(NOE-D)$    | FMC_D[15-0] valid data after FMC_NOE high  | 0                         | -                         |      |
| $t_d(ALE-NOE)$  | FMC_ALE valid before FMC_NOE low           | -                         | $3T_{fmc\_ker\_ck} + 0.5$ |      |
| $t_h(NOE-ALE)$  | FMC_NWE high to FMC_ALE invalid            | $4T_{fmc\_ker\_ck} - 1.5$ | -                         |      |

1. Evaluated by characterization - Not tested in production.

**Table 83. Switching characteristics for NAND flash write cycles<sup>(1)</sup>**

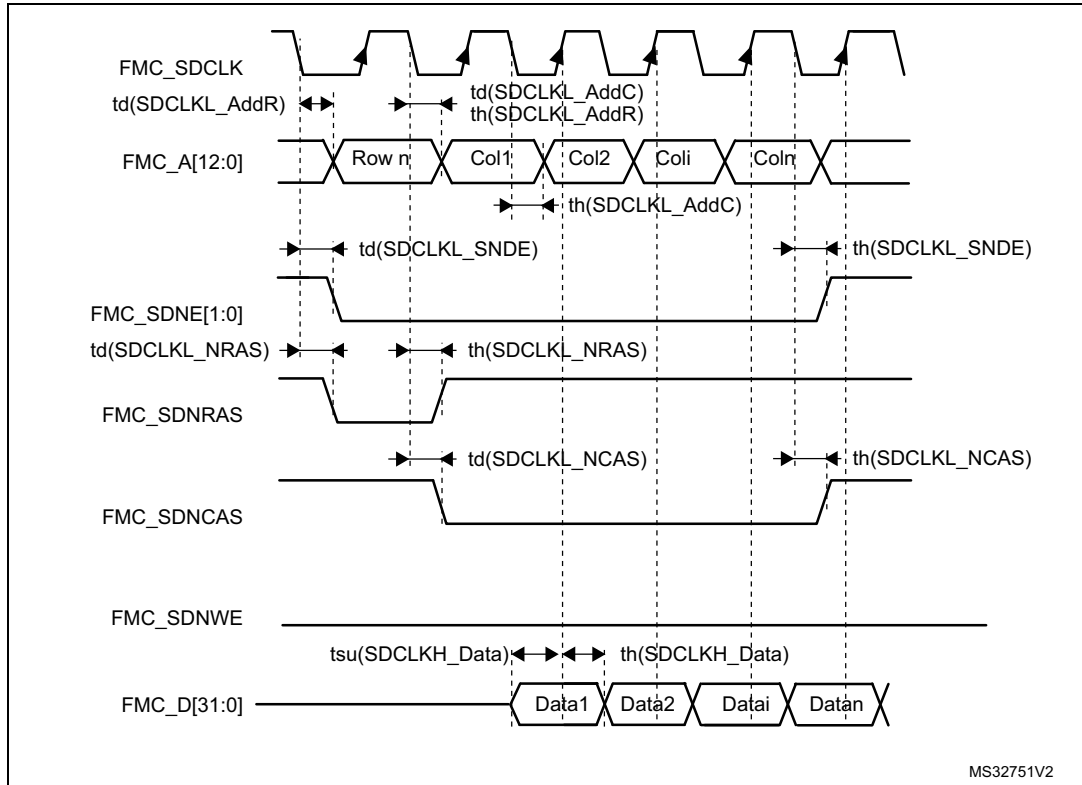
| Symbol         | Parameter                             | Min                       | Max                       | Unit |
|----------------|---------------------------------------|---------------------------|---------------------------|------|
| $t_{w(NWE)}$   | FMC_NWE low width                     | $4T_{fmc\_ker\_ck} - 0.5$ | $4T_{fmc\_ker\_ck} + 0.5$ | ns   |
| $t_v(NWE-D)$   | FMC_NWE low to FMC_D[15-0] valid      | 0                         | -                         |      |
| $t_h(NWE-D)$   | FMC_NWE high to FMC_D[15-0] invalid   | $2T_{fmc\_ker\_ck} + 0.5$ | -                         |      |
| $t_d(D-NWE)$   | FMC_D[15-0] valid before FMC_NWE high | $5T_{fmc\_ker\_ck} - 2.5$ | -                         |      |
| $t_d(ALE-NWE)$ | FMC_ALE valid before FMC_NWE low      | -                         | $3T_{fmc\_ker\_ck} + 0.5$ |      |
| $t_h(NWE-ALE)$ | FMC_NWE high to FMC_ALE invalid       | $2T_{fmc\_ker\_ck} - 1$   | -                         |      |

1. Evaluated by characterization - Not tested in production.

## SDRAM waveforms and timings

In all timing tables, the  $t_{fmc\_ker\_ck}$  is the  $f_{HCLK}$  clock period, with the following FMC\_SDCLK maximum values:

- For  $2.7\text{ V} < V_{DD} < 3.6\text{ V}$ : maximum FMC\_SDCLK = 95 MHz at 20 pF (100 MHz for  $V_{DD} > 3.0\text{ V}$ )
- For  $1.71\text{ V} < V_{DD} < 1.8\text{ V}$ : maximum FMC\_SDCLK = 95 MHz at 15 pF
- For  $1.71\text{ V} < V_{DD} < 1.8\text{ V}$ : maximum FMC\_SDCLK = 90 MHz at 20 pF

**Figure 46. SDRAM read access waveforms (CL = 1)****Table 84. SDRAM read timings<sup>(1)</sup>**

| Symbol                               | Parameter              | Min                              | Max                              | Unit |
|--------------------------------------|------------------------|----------------------------------|----------------------------------|------|
| $t_w(\text{SDCLK})$                  | FMC_SDCLK period       | $2T_{\text{fmc\_ker\_ck}} - 0.5$ | $2T_{\text{fmc\_ker\_ck}} + 0.5$ | ns   |
| $t_{\text{su}}(\text{SDCLKH\_Data})$ | Data input setup time  | 3                                | -                                |      |
| $t_h(\text{SDCLKH\_Data})$           | Data input hold time   | 0.5                              | -                                |      |
| $t_d(\text{SDCLKL\_Add})$            | Address valid time     | -                                | 1.5                              |      |
| $t_d(\text{SDCLKL\_SDNE})$           | Chip select valid time | -                                | 1.5                              |      |
| $t_h(\text{SDCLKL\_SDNE})$           | Chip select hold time  | 0                                | -                                |      |
| $t_d(\text{SDCLKL\_SDNRAS})$         | SDNRAS valid time      | -                                | 1.5                              |      |
| $t_h(\text{SDCLKL\_SDNRAS})$         | SDNRAS hold time       | 0                                | -                                |      |
| $t_d(\text{SDCLKL\_SDNCAS})$         | SDNCAS valid time      | -                                | 1                                |      |
| $t_h(\text{SDCLKL\_SDNCAS})$         | SDNCAS hold time       | 0                                | -                                |      |

1. Evaluated by characterization - Not tested in production.

Table 85. LPSDR SDRAM read timings<sup>(1)</sup>

| Symbol                 | Parameter              | Min                       | Max                       | Unit |
|------------------------|------------------------|---------------------------|---------------------------|------|
| $t_{W(SDCLK)}$         | FMC_SDCLK period       | $2T_{fmc\_ker\_ck} - 0.5$ | $2T_{fmc\_ker\_ck} + 0.5$ | ns   |
| $t_{su(SDCLKH\_Data)}$ | Data input setup time  | 3                         | -                         |      |
| $t_{h(SDCLKH\_Data)}$  | Data input hold time   | 0.5                       | -                         |      |
| $t_d(SDCLKL\_Add)$     | Address valid time     | -                         | 1.5                       |      |
| $t_d(SDCLKL\_SDNE)$    | Chip select valid time | -                         | 1.5                       |      |
| $t_h(SDCLKL\_SDNE)$    | Chip select hold time  | 0                         | -                         |      |
| $t_d(SDCLKL\_SDNRAS)$  | SDNRAS valid time      | -                         | 1.5                       |      |
| $t_h(SDCLKL\_SDNRAS)$  | SDNRAS hold time       | 0                         | -                         |      |
| $t_d(SDCLKL\_SDNCAS)$  | SDNCAS valid time      | -                         | 1                         |      |
| $t_h(SDCLKL\_SDNCAS)$  | SDNCAS hold time       | 0                         | -                         |      |

1. Evaluated by characterization - Not tested in production.

Figure 47. SDRAM write access waveforms

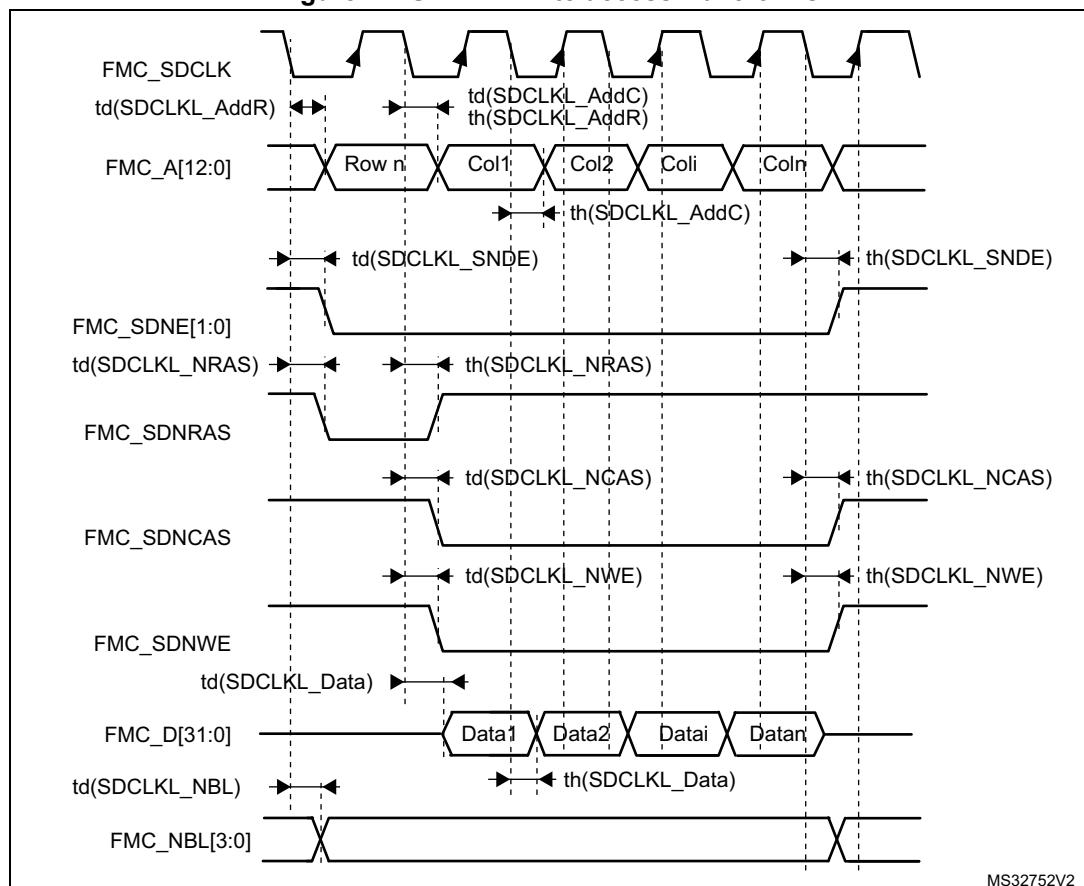


Table 86. SDRAM write timings<sup>(1)</sup>

| Symbol                       | Parameter              | Min                              | Max                              | Unit |
|------------------------------|------------------------|----------------------------------|----------------------------------|------|
| $t_w(\text{SDCLK})$          | FMC_SDCLK period       | $2T_{\text{fmc\_ker\_ck}} - 0.5$ | $2T_{\text{fmc\_ker\_ck}} + 0.5$ | ns   |
| $t_d(\text{SDCLKL\_Data})$   | Data output valid time | -                                | 1                                |      |
| $t_h(\text{SDCLKL\_Data})$   | Data output hold time  | 0                                | -                                |      |
| $t_d(\text{SDCLKL\_Add})$    | Address valid time     | -                                | 2                                |      |
| $t_d(\text{SDCLKL\_SDNWE})$  | SDNWE valid time       | -                                | 1                                |      |
| $t_h(\text{SDCLKL\_SDNWE})$  | SDNWE hold time        | 0                                | -                                |      |
| $t_d(\text{SDCLKL\_SDNE})$   | Chip select valid time | -                                | 1                                |      |
| $t_h(\text{SDCLKL\_SDNE})$   | Chip select hold time  | 0                                | -                                |      |
| $t_d(\text{SDCLKL\_SDNRAS})$ | SDNRAS valid time      | -                                | 1.5                              |      |
| $t_h(\text{SDCLKL\_SDNRAS})$ | SDNRAS hold time       | 0                                | -                                |      |
| $t_d(\text{SDCLKL\_SDNCAS})$ | SDNCAS valid time      | -                                | 1                                |      |
| $t_d(\text{SDCLKL\_SDNCAS})$ | SDNCAS hold time       | 0                                | -                                |      |

1. Evaluated by characterization - Not tested in production.

Table 87. LPSPDR SDRAM write timings<sup>(1)</sup>

| Symbol                      | Parameter              | Min                              | Max                              | Unit |
|-----------------------------|------------------------|----------------------------------|----------------------------------|------|
| $t_w(\text{SDCLK})$         | FMC_SDCLK period       | $2T_{\text{fmc\_ker\_ck}} - 0.5$ | $2T_{\text{fmc\_ker\_ck}} + 0.5$ | ns   |
| $t_d(\text{SDCLKL\_Data})$  | Data output valid time | -                                | 1                                |      |
| $t_h(\text{SDCLKL\_Data})$  | Data output hold time  | 0.                               | -                                |      |
| $t_d(\text{SDCLKL\_Add})$   | Address valid time     | -                                | 2                                |      |
| $t_d(\text{SDCLKL-SDNWE})$  | SDNWE valid time       | -                                | 1                                |      |
| $t_h(\text{SDCLKL-SDNWE})$  | SDNWE hold time        | 0                                | -                                |      |
| $t_d(\text{SDCLKL-SDNE})$   | Chip select valid time | -                                | 1.5                              |      |
| $t_h(\text{SDCLKL-SDNE})$   | Chip select hold time  | 0                                | -                                |      |
| $t_d(\text{SDCLKL-SDNRAS})$ | SDNRAS valid time      | -                                | 1.5                              |      |
| $t_h(\text{SDCLKL-SDNRAS})$ | SDNRAS hold time       | 0                                | -                                |      |
| $t_d(\text{SDCLKL-SDNCAS})$ | SDNCAS valid time      | -                                | 1                                |      |
| $t_d(\text{SDCLKL-SDNCAS})$ | SDNCAS hold time       | 0                                | -                                |      |

1. Evaluated by characterization - Not tested in production.

### 5.3.19 Octo-SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 88](#) and [Table 89](#) are derived from tests performed under the ambient temperature,  $f_{\text{HCLK}}$  frequency, and  $V_{\text{DD}}$  supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to  $\text{OSPEEDRy}[1:0] = 11$
- Measurement points are done at CMOS levels:  $0.5 V_{\text{DD}}$
- I/O compensation cell activated
- HSLV activated when  $V_{\text{DD}} \leq 2.7 \text{ V}$
- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics.

**Table 88. OCTOSPI characteristics in SDR mode<sup>(1)(2)</sup>**

| Symbol               | Parameter                              | Conditions                                                                  | Min                                              | Typ | Max <sup>(3)</sup>                               | Unit |
|----------------------|----------------------------------------|-----------------------------------------------------------------------------|--------------------------------------------------|-----|--------------------------------------------------|------|
| $F_{\text{(CLK)}}$   | Clock frequency                        | $1.71 \text{ V} < V_{\text{DD}} < 1.9 \text{ V}$ ,<br>$C_L = 15 \text{ pF}$ | -                                                | -   | 110                                              | MHz  |
|                      |                                        | $1.71 \text{ V} < V_{\text{DD}} < 3.6 \text{ V}$ ,<br>$C_L = 15 \text{ pF}$ | -                                                | -   | 150                                              |      |
| $t_{\text{w(CLKH)}}$ | Clock high and low time, even division | $\text{PRESCALER}[7:0] = n$<br>(= 0, 1, 3, 5, ..., 255)                     | $t_{\text{(CLK)}} / 2 - 0.5$                     | -   | $t_{\text{(CLK)}} / 2 + 0.5$                     | ns   |
| $t_{\text{w(CLKL)}}$ |                                        |                                                                             | $t_{\text{(CLK)}} / 2 - 0.5$                     | -   | $t_{\text{(CLK)}} / 2 + 0.5$                     |      |
| $t_{\text{w(CLKH)}}$ | Clock high and low time, odd division  | $\text{PRESCALER}[7:0] = n$<br>(= 2, 4, 6, ..., 254)                        | $(n / 2) * t_{\text{(CLK)}} / (n + 1) - 0.5$     | -   | $(n / 2) * t_{\text{(CLK)}} / (n + 1) + 0.5$     |      |
| $t_{\text{w(CLKL)}}$ |                                        |                                                                             | $(n / 2 + 1) * t_{\text{(CLK)}} / (n + 1) - 0.5$ | -   | $(n / 2 + 1) * t_{\text{(CLK)}} / (n + 1) + 0.5$ |      |
| $t_{\text{s(IN)}}$   | Data input setup time                  | -                                                                           | 4                                                | -   | -                                                |      |
| $t_{\text{h(IN)}}$   | Data input hold time                   | -                                                                           | 1                                                | -   | -                                                |      |
| $t_{\text{v(OUT)}}$  | Data output valid time                 | -                                                                           | -                                                | 0.5 | 1                                                |      |
| $t_{\text{h(OUT)}}$  | Data output hold time                  | -                                                                           | 0                                                | -   | -                                                |      |

1. All values apply to Octal- and Quad-SPI mode.
2. Evaluated by characterization - Not tested in production.
3. At VOS1 these values are degraded by up to 5%.

**Figure 48. OCTOSPI SDR read/write timing diagram**

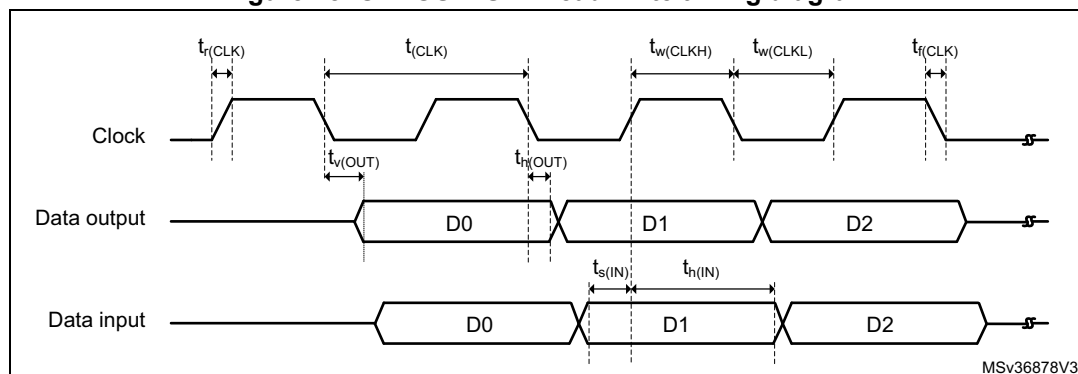


Table 89. OCTOSPI characteristics in DTR mode (no DQS)<sup>(1)(2)(3)</sup>

| Symbol                         | Parameter                       | Conditions                                                        | Min                                       | Typ                   | Max                                       | Unit |
|--------------------------------|---------------------------------|-------------------------------------------------------------------|-------------------------------------------|-----------------------|-------------------------------------------|------|
| $F_{CLK}$                      | OCTOSPI clock frequency         | $1.71\text{ V} < V_{DD} < 1.9\text{ V}$ ,<br>$C_L = 15\text{ pF}$ | -                                         | -                     | 100 <sup>(4)</sup>                        | MHz  |
|                                |                                 | $2.7\text{ V} < V_{DD} < 3.6\text{ V}$ ,<br>$C_L = 15\text{ pF}$  | -                                         | -                     | 125 <sup>(4)</sup>                        |      |
| $t_{w(CLKH)}$                  | OCTOSPI clock high and low time | PRESCALER[7:0] = n<br>(= 0, 1, 3, 5, ..., 255)                    | $t_{(CLK)} / 2 - 0.5$                     | -                     | $t_{(CLK)} / 2 + 0.5$                     | ns   |
| $t_{w(CLKL)}$                  |                                 |                                                                   | $t_{(CLK)} / 2 - 0.5$                     | -                     | $t_{(CLK)} / 2 + 0.5$                     |      |
| $t_{w(CLKH)}$                  | OCTOSPI clock high and low time | PRESCALER[7:0] = n<br>(= 2, 4, 6, 8, ..., 254)                    | $(n / 2) * t_{(CLK)} / (n + 1) - 0.5$     | -                     | $(n / 2) * t_{(CLK)} / (n + 1) + 0.5$     | ns   |
| $t_{w(CLKL)}$                  |                                 |                                                                   | $(n / 2 + 1) * t_{(CLK)} / (n + 1) - 0.5$ | -                     | $(n / 2 + 1) * t_{(CLK)} / (n + 1) + 0.5$ |      |
| $t_{v(CLK)}$                   | Clock valid time                | -                                                                 | -                                         | -                     | $t_{(CLK)} + 0.5$                         | ns   |
| $t_{sr(IN)}$ ,<br>$t_{sf(IN)}$ | Data input setup time           | -                                                                 | 4                                         | -                     | -                                         | ns   |
| $t_{hr(IN)}$ ,<br>$t_{hf(IN)}$ | Data input hold time            | -                                                                 | 1.5                                       | -                     | -                                         |      |
| $t_{vr(OUT)}$<br>$t_{vf(OUT)}$ | Data output valid time          | DHQC = 0                                                          | -                                         | 2.5                   | 3.5                                       |      |
|                                |                                 | DHQC = 1,<br>Prescaler [7:0] = 1, 2...                            | -                                         | $t_{(CLK)} / 4 + 0.5$ | $t_{(CLK)} / 4 + 1$                       |      |
| $t_{hr(OUT)}$<br>$t_{hf(OUT)}$ | Data output hold time           | DHQC = 0                                                          | 1.5                                       | -                     | -                                         |      |
|                                |                                 | DHQC = 1,<br>Prescaler [7:0] = 1, 2...                            | $t_{(CLK)} / 4 - 1$                       | -                     | -                                         |      |

1. All values apply to Octal and Quad-SPI mode.
2. Evaluated by characterization - Not tested in production.
3. Delay block bypassed.
4. DHQC must be set to reach the mentioned frequency.

Table 90. OCTOSPI characteristics in DTR mode (with DQS) / HyperBus<sup>(1)(2)</sup>

| Symbol                                       | Parameter                                    | Conditions                                                  | Min                                        | Typ                        | Max                                        | Unit |
|----------------------------------------------|----------------------------------------------|-------------------------------------------------------------|--------------------------------------------|----------------------------|--------------------------------------------|------|
| F <sub>CLK</sub>                             | OCTOSPI clock frequency                      | 1.71 V < V <sub>DD</sub> < 1.9 V,<br>C <sub>L</sub> = 15 pF | -                                          | -                          | 125 <sup>(3)(4)</sup>                      | MHz  |
|                                              |                                              | 2.7 V < V <sub>DD</sub> < 3.6 V,<br>C <sub>L</sub> = 15 pF  | -                                          | -                          | 125 <sup>(3)(5)</sup>                      |      |
| t <sub>w(CLKH)</sub>                         | OCTOSPI clock high and low time              | PRESCALER[7:0] = n<br>= (0, 1, 3, 5, ..., 255)              | t <sub>(CLK)/2</sub> - 0.5                 | -                          | t <sub>(CLK)/2</sub> + 0.5                 | ns   |
| t <sub>w(CLKL)</sub>                         |                                              |                                                             | t <sub>(CLK)/2</sub> - 0.5                 | -                          | t <sub>(CLK)/2</sub> + 0.5                 |      |
| t <sub>w(CLKH)</sub>                         | OCTOSPI clock high and low time              | PRESCALER[7:0] = n<br>= (2, 4, 6, 8, ..., 254)              | (n/2)*t <sub>(CLK)/</sub><br>(n+1) - 0.5   | -                          | (n/2)*t <sub>(CLK)/</sub><br>(n+1) + 0.5   |      |
| t <sub>w(CLKL)</sub>                         |                                              |                                                             | (n/2+1)*t <sub>(CLK)/</sub><br>(n+1) - 0.5 | -                          | (n/2+1)*t <sub>(CLK)/</sub><br>(n+1) + 0.5 |      |
| t <sub>v(CLK)</sub>                          | Clock valid time                             | -                                                           | -                                          | -                          | t <sub>(CLK)</sub> + 2                     |      |
| t <sub>h(CLK)</sub>                          | Clock hold time                              | -                                                           | t <sub>(CLK)/2</sub> - 1                   | -                          | -                                          |      |
| t <sub>ODr(CLK)</sub> <sup>(5)</sup>         | CLK, NCLK crossing level on CLK rising edge  | V <sub>DD</sub> = 1.8 V                                     | 890                                        | -                          | 1300                                       | mV   |
| t <sub>ODf(CLK)</sub> <sup>(5)</sup>         | CLK, NCLK crossing level on CLK falling edge | V <sub>DD</sub> = 1.8 V                                     | 790                                        | -                          | 1080                                       |      |
| t <sub>w(CS)</sub>                           | Chip select high time                        | -                                                           | 3 * t <sub>(CLK)</sub>                     | -                          | -                                          | ns   |
| t <sub>v(DQ)</sub>                           | Data input valid time                        | -                                                           | 3                                          | -                          | -                                          |      |
| t <sub>v(DS)</sub>                           | Data strobe input valid time                 | -                                                           | 1                                          | -                          | -                                          |      |
| t <sub>h(DS)</sub>                           | Data strobe input hold time                  | -                                                           | 0                                          | -                          | -                                          |      |
| t <sub>v(RWDS)</sub>                         | Data strobe output valid time                | -                                                           | -                                          | -                          | 3 * t <sub>(CLK)</sub>                     |      |
| t <sub>sr(DQ),</sub><br>t <sub>sf(DQ)</sub>  | Data input setup time                        | -                                                           | -0.5                                       | -                          | -                                          | ns   |
| t <sub>hr(DQ),</sub><br>t <sub>hf(DQ)</sub>  | Data input hold time                         | -                                                           | 2                                          | -                          | -                                          |      |
| t <sub>vr(OUT)</sub><br>t <sub>vf(OUT)</sub> | Data output valid time                       | DHQC = 0                                                    | -                                          | 2.5                        | 3.5                                        |      |
|                                              |                                              | DHQC = 1, all prescaler values except 0                     | -                                          | t <sub>(CLK)/4</sub> + 0.5 | t <sub>(CLK)/4</sub> + 1                   |      |
| t <sub>hr(OUT)</sub><br>t <sub>hf(OUT)</sub> | Data output hold time                        | DHQC = 0                                                    | 1.5                                        | -                          | -                                          |      |
|                                              |                                              | DHQC = 1, all prescaler values except 0                     | t <sub>(CLK)/4</sub> - 1                   | -                          | -                                          |      |

1. Evaluated by characterization - Not tested in production.
2. Delay block activated.
3. Maximum frequency value are given for a maximum RWDS to DQ skew of ± 1.0 ns.
4. DHQC must be set to reach the mentioned frequency.
5. It is recommended that PF10/PB5, PB4/PB5, and PA3/PB5 are in line with crossing specification.

Figure 49. OCTOSPI timing diagram - DTR mode

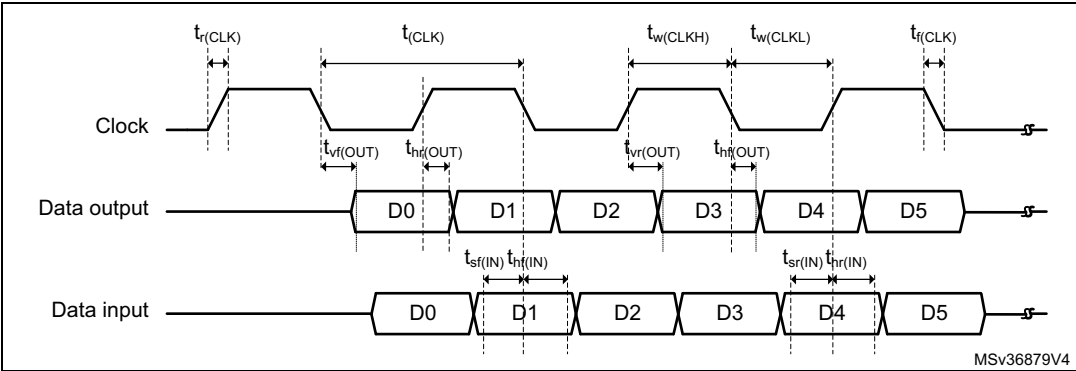


Figure 50. OCTOSPI HyperBus clock

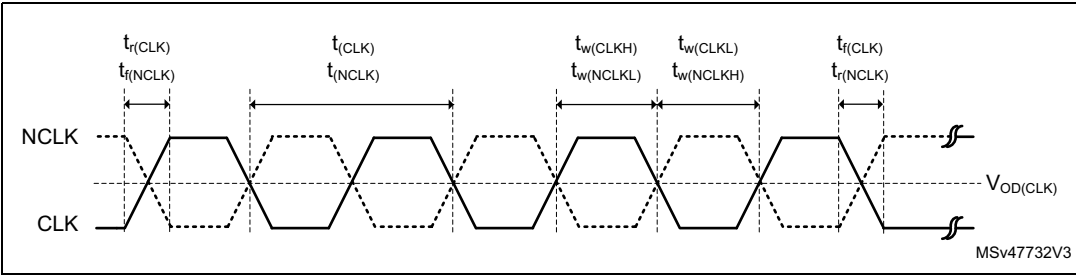


Figure 51. OCTOSPI HyperBus read

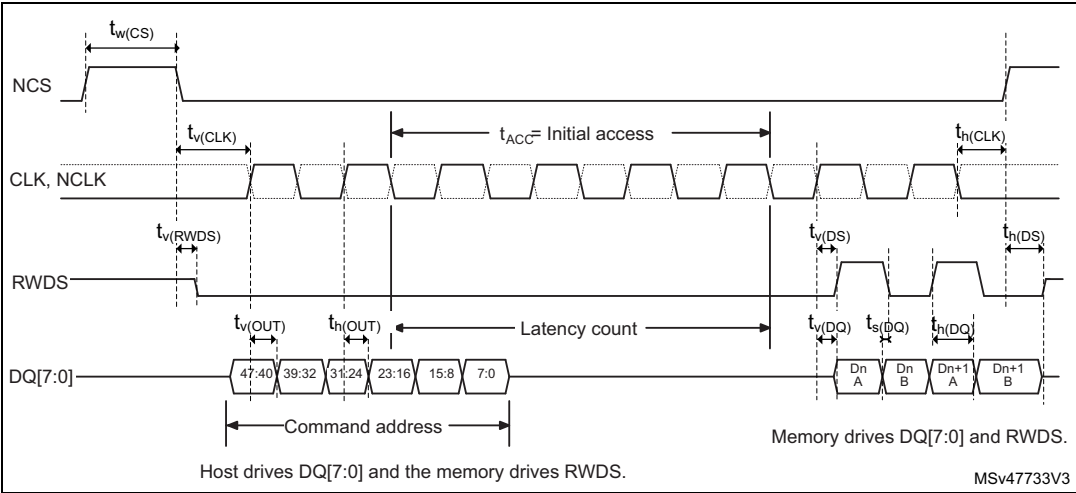
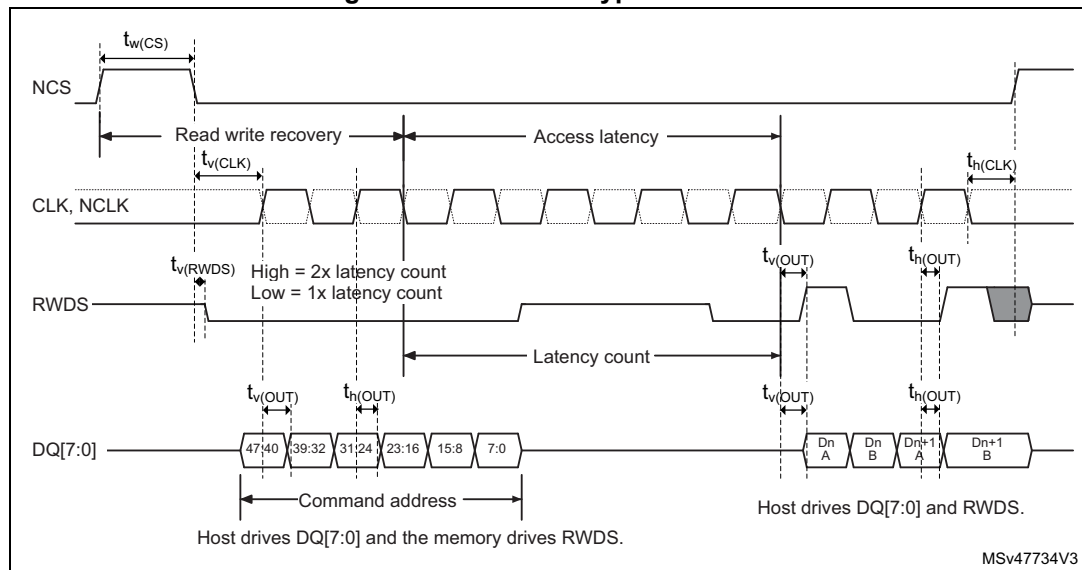


Figure 52. OCTOSPI HyperBus write



### 5.3.20 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in [Table 91](#) are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency, and  $V_{DD}$  supply voltage summarized in [Table 20](#).

Table 91. Delay block characteristics

| Symbol       | Parameter     | Conditions | Min | Typ  | Max  | Unit |
|--------------|---------------|------------|-----|------|------|------|
| $t_{init}$   | Initial delay | -          | 750 | 1100 | 1700 | ps   |
| $t_{\Delta}$ | Unit delay    | -          | 38  | 44   | 54   | ps   |

### 5.3.21 DCMI interface characteristics

Unless otherwise specified, the parameters given in [Table 92](#) are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency, and  $V_{DD}$  supply voltage summarized in [Table 20](#), with the following configuration:

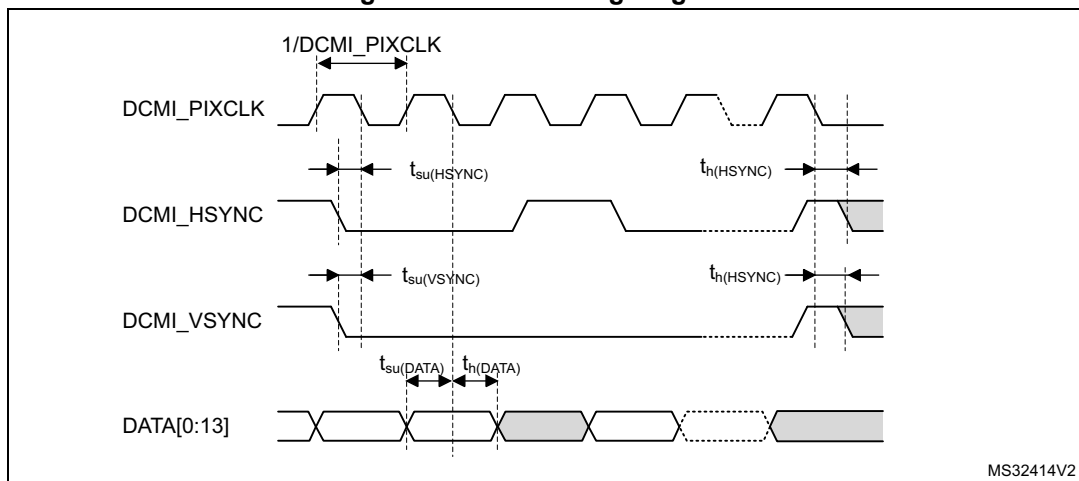
- DCMI\_PIXCLK polarity: falling
- DCMI\_VSYNC and DCMI\_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load  $C_L = 30$  pF
- Measurement points done at CMOS levels:  $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when  $V_{DD} \leq 2.7$  V
- Voltage scaling VOS0 selected

Table 92. DCMI characteristics<sup>(1)</sup>

| Symbol                         | Parameter                                   | Min | Max | Unit |
|--------------------------------|---------------------------------------------|-----|-----|------|
| -                              | Frequency ratio DCMI_PIXCLK/fHCLK           | -   | 0.4 | -    |
| DCMI_PIXCLK                    | Pixel clock input                           | -   | 100 | MHz  |
| D_PIXEL                        | Pixel clock input duty cycle                | 30  | 70  | %    |
| $t_{su}(DATA)$                 | Data input setup time                       | 2.5 | -   | ns   |
| $t_h(DATA)$                    | Data hold time                              | 2   | -   |      |
| $t_{su}(HSYNC), t_{su}(VSYNC)$ | DCMI_HSYNC and DCMI_VSYNC input setup times | 2.5 | -   |      |
| $t_h(HSYNC), t_h(VSYNC)$       | DCMI_HSYNC and DCMI_VSYNC input hold times  | 1.5 | -   |      |

1. Evaluated by characterization - Not tested in production.

Figure 53. DCMI timing diagrams



### 5.3.22 PSSI interface characteristics

Unless otherwise specified, the parameters given in [Table 92](#) and [Table 93](#) are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency, and  $V_{DD}$  supply voltage summarized in [Table 20](#) and [Section 5.3.1](#), with the following configuration:

- PSSI\_PDCK polarity: falling
- PSSI\_RDY and PSSI\_DE polarity: low
- Bus width: 16 lines
- DATA width: 32 bits
- Capacitive load  $C_L = 30$  pF
- Measurement points are done at CMOS levels:  $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when  $V_{DD} \leq 2.7$  V
- Voltage scaling VOS0 selected

**Table 93. PSSI transmit characteristics<sup>(1)</sup>**

| Symbol                 | Parameter                                   | Conditions                                    | Min | Max               | Unit |
|------------------------|---------------------------------------------|-----------------------------------------------|-----|-------------------|------|
| -                      | Frequency ratio PSSI_PDCK/f <sub>HCLK</sub> | -                                             | -   | 0.4               | -    |
| PSSI_PDCK              | PSSI clock input                            | $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  | -   | 90 <sup>(2)</sup> | MHz  |
|                        |                                             | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | -   | 86                |      |
| D <sub>pixel</sub>     | PSSI clock input duty cycle                 |                                               | 30  | 70                | %    |
| t <sub>ov</sub> (DATA) | Data output valid time                      | $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  | -   | 11                | ns   |
|                        |                                             | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | -   | 11.5              |      |
| t <sub>oh</sub> (DATA) | Data output hold time                       | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | 5.5 | -                 |      |
| t <sub>ov</sub> (DE)   | DE output valid time                        |                                               | -   | 11.5              |      |
| t <sub>oh</sub> (DE)   | DE output hold time                         |                                               | 5.5 | -                 |      |
| tsu(RDY)               | RDY input setup time                        |                                               | 0.5 | -                 |      |
| th(RDY)                | RDY input hold time                         |                                               | 0.5 | -                 |      |

1. Evaluated by characterization - Not tested in production.

2. This maximal frequency does not consider receiver setup and hold timings.

**Table 94. PSSI receive characteristics<sup>(1)</sup>**

| Symbol                 | Parameter                                   | Conditions                                    | Min | Max  | Unit |
|------------------------|---------------------------------------------|-----------------------------------------------|-----|------|------|
| -                      | Frequency ratio PSSI_PDCK/f <sub>HCLK</sub> |                                               | -   | 0.4  | -    |
| PSSI_PDCK              | PSSI clock input                            | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | -   | 100  | MHz  |
| D <sub>pixel</sub>     | PSSI clock input duty cycle                 | -                                             | 30  | 70   | %    |
| t <sub>su</sub> (DATA) | Data input setup time                       | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | 2   | -    | ns   |
| t <sub>h</sub> (DATA)  | Data input hold time                        |                                               | 2.5 | -    |      |
| t <sub>su</sub> (DE)   | DE input setup time                         |                                               | 1.5 | -    |      |
| t <sub>h</sub> (DE)    | DE input hold time                          |                                               | 2   | -    |      |
| t <sub>ov</sub> (RDY)  | RDY output valid time                       |                                               | -   | 16.5 |      |
| t <sub>oh</sub> (RDY)  | RDY output hold time                        |                                               | 5.5 | -    |      |

1. Evaluated by characterization - Not tested in production.

Figure 54. PSSI transmit timing diagram

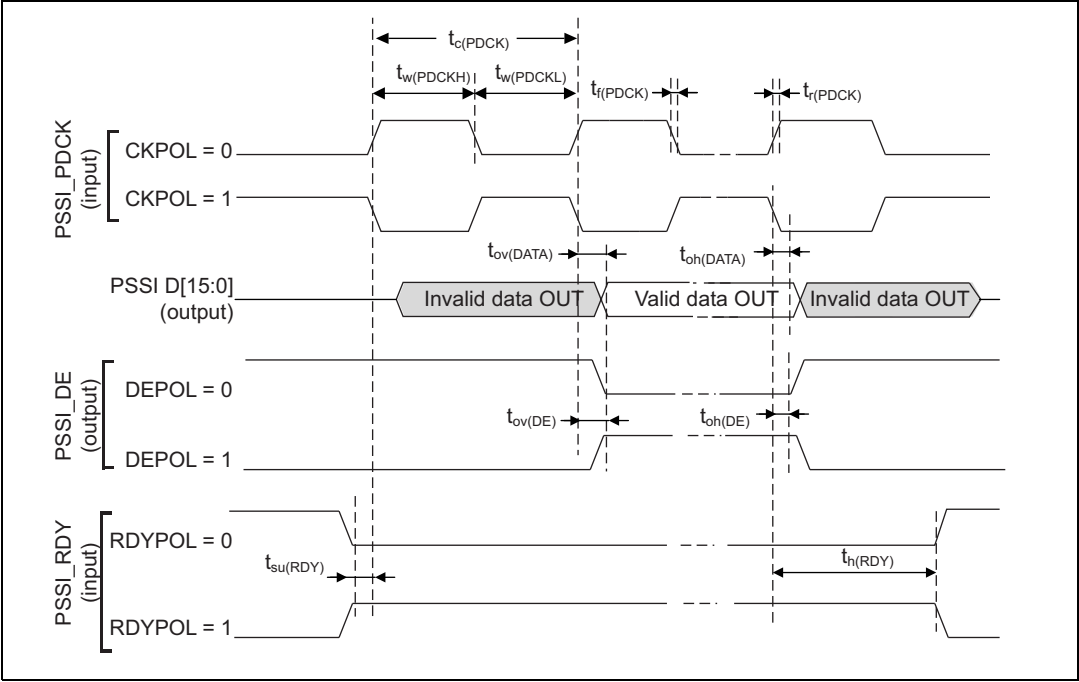
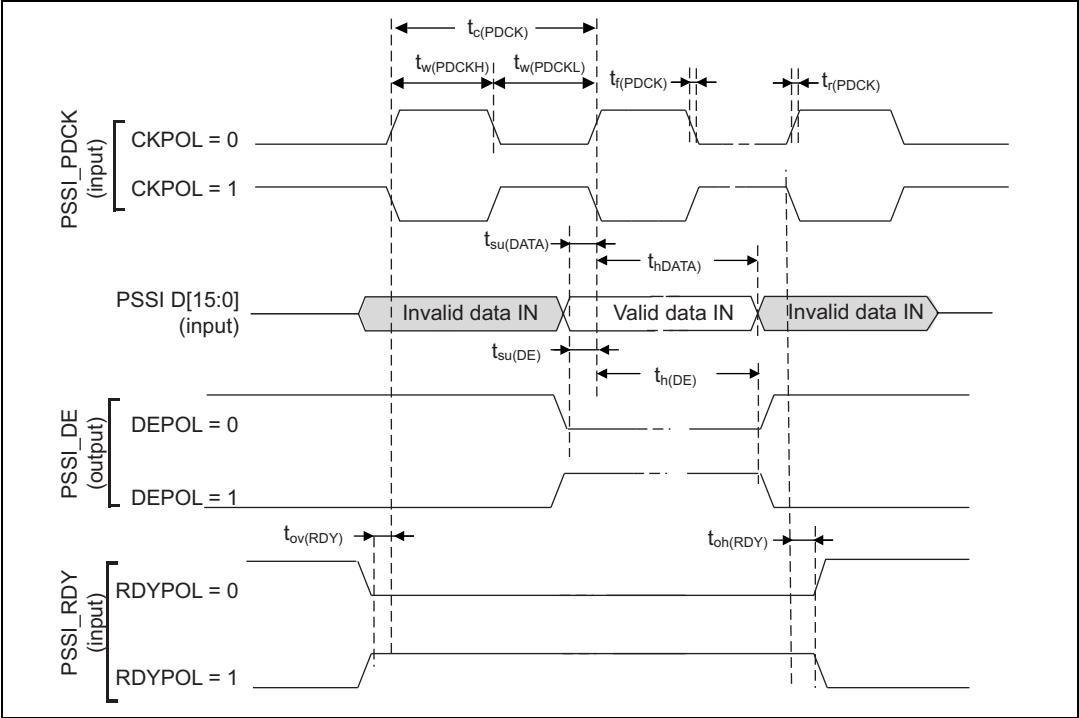


Figure 55. PSSI receive timing diagram



### 5.3.23 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 95](#) are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency, and  $V_{DDA}$  supply voltage conditions summarized in [Table 20](#).

**Table 95. 12-bit ADC characteristics<sup>(1)(2)</sup>**

| Symbol                                                                                           | Parameter                                  | Conditions                        |                              |                                |                                  |                                  | Min              | Typ                              | Max                            | Unit                             |      |                           |
|--------------------------------------------------------------------------------------------------|--------------------------------------------|-----------------------------------|------------------------------|--------------------------------|----------------------------------|----------------------------------|------------------|----------------------------------|--------------------------------|----------------------------------|------|---------------------------|
| V <sub>DDA</sub>                                                                                 | Analog supply voltage for ADC ON           | -                                 |                              |                                |                                  |                                  | 1.62             | -                                | 3.6                            | V                                |      |                           |
| V <sub>REF+</sub>                                                                                | Positive reference voltage                 | -                                 |                              |                                |                                  |                                  | 1.62             | -                                | V <sub>DDA</sub>               |                                  |      |                           |
| V <sub>REF-</sub>                                                                                | Negative reference voltage                 | -                                 |                              |                                |                                  |                                  | V <sub>SSA</sub> |                                  |                                |                                  |      |                           |
| f <sub>adc_ker_ck</sub> <sup>(3)</sup>                                                           | Clock frequency                            | 1.62 V ≤ V <sub>DDA</sub> ≤ 3.6 V |                              |                                |                                  |                                  | 1.5              | -                                | 75                             | MHz                              |      |                           |
| f <sub>S</sub> <sup>(4)</sup> with<br>R <sub>AIN</sub> = 47 Ω<br>and<br>C <sub>PCB</sub> = 22 pF | Sampling rate for fast channels (VIN[0:5]) | Resolution = 12 bits              | Continuous mode              | 1.8V ≤ V <sub>DDA</sub> ≤ 3.6V | -40°C ≤ T <sub>J</sub> ≤ 130°C   | f <sub>adc_ker_ck</sub> = 75 MHz | SMP ≈2.5         | -                                | 5.00                           | -                                | MSPS |                           |
|                                                                                                  |                                            |                                   |                              | 1.6V ≤ V <sub>DDA</sub> ≤ 3.6V |                                  |                                  |                  | f <sub>adc_ker_ck</sub> = 70 MHz | -                              | 4.66                             |      | -                         |
|                                                                                                  |                                            |                                   | Single or Discontinuous mode | 2.4V ≤ V <sub>DDA</sub> ≤ 3.6V |                                  |                                  |                  | f <sub>adc_ker_ck</sub> = 60 MHz | -                              | 4.00                             |      | -                         |
|                                                                                                  |                                            |                                   |                              | 1.6V ≤ V <sub>DDA</sub> ≤ 3.6V |                                  |                                  |                  | f <sub>adc_ker_ck</sub> = 50 MHz | -                              | 3.33                             |      | -                         |
|                                                                                                  |                                            | Resolution = 10 bits              | Continuous mode              | 1.6V ≤ V <sub>DDA</sub> ≤ 3.6V |                                  |                                  |                  | f <sub>adc_ker_ck</sub> = 75 MHz | -                              | 5.77                             |      | -                         |
|                                                                                                  |                                            |                                   |                              | 2.4V ≤ V <sub>DDA</sub> ≤ 3.6V |                                  |                                  |                  | f <sub>adc_ker_ck</sub> = 65 MHz | -                              | 5.77                             |      | -                         |
|                                                                                                  |                                            |                                   | Single or Discontinuous mode | 1.6V ≤ V <sub>DDA</sub> ≤ 3.6V |                                  |                                  |                  | f <sub>adc_ker_ck</sub> = 75 MHz | -                              | 5.00                             |      | -                         |
|                                                                                                  |                                            |                                   |                              | Resolution = 8 bits            |                                  |                                  |                  | All modes                        | 1.6V ≤ V <sub>DDA</sub> ≤ 3.6V | f <sub>adc_ker_ck</sub> = 75 MHz |      | -                         |
|                                                                                                  | Resolution = 6 bits                        | f <sub>adc_ker_ck</sub> = 75 MHz  | -                            | 8.33                           | -                                |                                  |                  |                                  |                                |                                  |      |                           |
|                                                                                                  | Sampling rate for slow channels            | Resolution = 12 bits              | All modes <sup>(5)</sup>     | 1.6V ≤ V <sub>DDA</sub> ≤ 3.6V | f <sub>adc_ker_ck</sub> = 35 MHz | -                                | 2.30             | -                                |                                |                                  |      |                           |
|                                                                                                  |                                            |                                   |                              |                                | Resolution = 10 bits             | f <sub>adc_ker_ck</sub> = 35 MHz | -                | 2.70                             | -                              |                                  |      |                           |
|                                                                                                  |                                            |                                   |                              |                                | Resolution = 8 bits              | f <sub>adc_ker_ck</sub> = 50 MHz | -                | 4.50                             | -                              |                                  |      |                           |
|                                                                                                  |                                            |                                   |                              |                                | Resolution = 6 bits              | f <sub>adc_ker_ck</sub> = 50 MHz | -                | 5.50                             | -                              |                                  |      |                           |
|                                                                                                  | t <sub>TRIG</sub>                          | External trigger period           | Resolution = 12 bits         |                                |                                  |                                  |                  | -                                | -                              | 15                               |      | 1/f <sub>adc_ker_ck</sub> |
|                                                                                                  | V <sub>AIN</sub> <sup>(2)</sup>            | Conversion voltage range          | -                            |                                |                                  |                                  |                  | 0                                | -                              | V <sub>REF+</sub>                |      | V                         |
|                                                                                                  | V <sub>CMIV</sub>                          | Common mode input voltage         | -                            |                                |                                  |                                  |                  | V <sub>REF</sub> / 2 - 10%       | V <sub>REF</sub> / 2           | V <sub>REF</sub> / 2 + 10%       |      |                           |

Table 95. 12-bit ADC characteristics<sup>(1)(2)</sup> (continued)

| Symbol              | Parameter                                                                                         | Conditions                                                           | Min             | Typ | Max   | Unit                 |
|---------------------|---------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|-----------------|-----|-------|----------------------|
| $R_{AIN}^{(6)}$     | External input impedance                                                                          | Resolution = 12 bits, $T_J = 130^{\circ}\text{C}$ (tolerance 4 LSBs) | -               | -   | 321   | $\Omega$             |
|                     |                                                                                                   | Resolution = 12 bits, $T_J = 125^{\circ}\text{C}$                    | -               | -   | 220   |                      |
|                     |                                                                                                   | Resolution = 10 bits, $T_J = 130^{\circ}\text{C}$                    | -               | -   | 1039  |                      |
|                     |                                                                                                   | Resolution = 10 bits, $T_J = 125^{\circ}\text{C}$                    | -               | -   | 2100  |                      |
|                     |                                                                                                   | Resolution = 8 bits, $T_J = 130^{\circ}\text{C}$                     | -               | -   | 6327  |                      |
|                     |                                                                                                   | Resolution = 8 bits, $T_J = 125^{\circ}\text{C}$                     | -               | -   | 12000 |                      |
|                     |                                                                                                   | Resolution = 6 bits, $T_J = 130^{\circ}\text{C}$                     | -               | -   | 47620 |                      |
|                     |                                                                                                   | Resolution = 6 bits, $T_J = 125^{\circ}\text{C}$                     | -               | -   | 80000 |                      |
| $C_{ADC}$           | Internal sample and hold capacitor                                                                | -                                                                    | -               | 3   | -     | pF                   |
| $t_{ADCVREG\_STUP}$ | LDO startup time                                                                                  | -                                                                    | -               | 5   | 10    | $\mu\text{s}$        |
| $t_{STAB}$          | Power-up time                                                                                     | LDO already started                                                  | 1               | -   | -     | Conversion cycle     |
| $t_{OFF\_CAL}$      | Offset calibration time                                                                           | -                                                                    | 1335            |     |       | $1/f_{adc\_ker\_ck}$ |
| $t_{LATR}$          | Trigger conversion latency for regular and injected channels without aborting the conversion      | CKMODE = 00                                                          | 1.5             | 2   | 2.5   |                      |
|                     |                                                                                                   | CKMODE = 01                                                          | -               | -   | 2.5   |                      |
|                     |                                                                                                   | CKMODE = 10                                                          | -               | -   | 2.5   |                      |
|                     |                                                                                                   | CKMODE = 11                                                          | -               | -   | 2.25  |                      |
| $t_{LATRINJ}$       | Trigger conversion latency for regular and injected channels when a regular conversion is aborted | CKMODE = 00                                                          | 2.5             | 3   | 3.5   |                      |
|                     |                                                                                                   | CKMODE = 01                                                          | -               | -   | 3.5   |                      |
|                     |                                                                                                   | CKMODE = 10                                                          | -               | -   | 3.5   |                      |
|                     |                                                                                                   | CKMODE = 11                                                          | -               | -   | 3.25  |                      |
| $t_S$               | Sampling time                                                                                     | -                                                                    | 2.5             | -   | 640.5 |                      |
| $t_{CONV}$          | Total conversion time (including sampling)                                                        | N-bits resolution                                                    | $t_S + 0.5 + N$ | -   | -     |                      |
| $I_{DDA\_D(ADC)}$   | Consumption on $V_{DDA}$ and $V_{REF}$ , differential mode                                        | $f_s = 5 \text{ MSPS}$                                               | -               | 600 | -     | $\mu\text{A}$        |
|                     |                                                                                                   | $f_s = 1 \text{ MSPS}$                                               | -               | 190 | -     |                      |
|                     |                                                                                                   | $f_s = 0.1 \text{ MSPS}$                                             | -               | 50  | -     |                      |
| $I_{DDA\_SE(ADC)}$  | Consumption on $V_{DDA}$ and $V_{REF}$ , single-ended mode                                        | $f_s = 5 \text{ MSPS}$                                               | -               | 500 | -     |                      |
|                     |                                                                                                   | $f_s = 1 \text{ MSPS}$                                               | -               | 150 | -     |                      |
|                     |                                                                                                   | $f_s = 0.1 \text{ MSPS}$                                             | -               | 50  | -     |                      |
| $I_{DD(ADC)}$       | Consumption on $V_{DD}$                                                                           | $f_{adc\_ker\_ck} = 75 \text{ MHz}$                                  | -               | 265 | -     |                      |
|                     |                                                                                                   | $f_{adc\_ker\_ck} = 50 \text{ MHz}$                                  | -               | 175 | -     |                      |
|                     |                                                                                                   | $f_{adc\_ker\_ck} = 25 \text{ MHz}$                                  | -               | 90  | -     |                      |
|                     |                                                                                                   | $f_{adc\_ker\_ck} = 12.5 \text{ MHz}$                                | -               | 45  | -     |                      |
|                     |                                                                                                   | $f_{adc\_ker\_ck} = 6.25 \text{ MHz}$                                | -               | 22  | -     |                      |
|                     |                                                                                                   | $f_{adc\_ker\_ck} = 3.125 \text{ MHz}$                               | -               | 11  | -     |                      |

1. Specified by design - Not tested in production.

2. The voltage booster on ADC switches must be used for  $V_{DDA} < 2.7 \text{ V}$  (embedded I/O switches).

3. This frequency is the analog ADC specification, it must respect the value in [Table 21](#).
4. These values are valid on BGA packages.
5. Depending upon the package,  $V_{REF+}$  can be internally connected to  $V_{DDA}$ , and  $V_{REF-}$  to  $V_{SSA}$ .
6. The tolerance is two LSBs for 12-, 10-, and 8-bit resolutions, if not otherwise specified.

**Table 96. Minimum sampling time versus  $R_{AIN}^{(1)(2)}$** 

| Resolution | $R_{AIN} (\Omega)$ | Minimum sampling time (s) |                             |
|------------|--------------------|---------------------------|-----------------------------|
|            |                    | Fast channel              | Slow channel <sup>(3)</sup> |
| 12 bits    | 47                 | 3.75E-08                  | 6.12E-08                    |
|            | 68                 | 3.94E-08                  | 6.25E-08                    |
|            | 100                | 4.36E-08                  | 6.51E-08                    |
|            | 150                | 5.11E-08                  | 7.00E-08                    |
|            | 220                | 6.54E-08                  | 7.86E-08                    |
|            | 330                | 8.80E-08                  | 9.57E-08                    |
|            | 470                | 1.17E-07                  | 1.23E-07                    |
|            | 680                | 1.60E-07                  | 1.65E-07                    |
| 10 bits    | 47                 | 3.19E-08                  | 5.17E-08                    |
|            | 68                 | 3.35E-08                  | 5.28E-08                    |
|            | 100                | 3.66E-08                  | 5.45E-08                    |
|            | 150                | 4.35E-08                  | 5.83E-08                    |
|            | 220                | 5.43E-08                  | 6.50E-08                    |
|            | 330                | 7.18E-08                  | 7.89E-08                    |
|            | 470                | 9.46E-08                  | 1.00E-07                    |
|            | 680                | 1.28E-07                  | 1.33E-07                    |
|            | 1000               | 1.81E-07                  | 1.83E-07                    |
|            | 1500               | 2.63E-07                  | 2.63E-07                    |
|            | 2200               | 3.79E-07                  | 3.76E-07                    |
|            | 3300               | 5.57E-07                  | 5.52E-07                    |

Table 96. Minimum sampling time versus  $R_{AIN}^{(1)(2)}$  (continued)

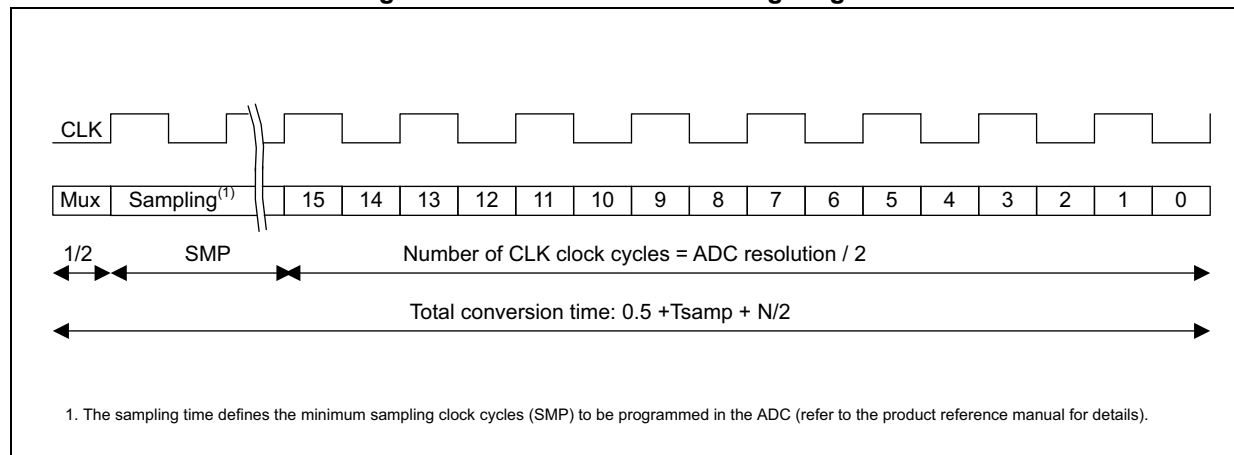
| Resolution | $R_{AIN} (\Omega)$ | Minimum sampling time (s) |                             |
|------------|--------------------|---------------------------|-----------------------------|
|            |                    | Fast channel              | Slow channel <sup>(3)</sup> |
| 8 bits     | 47                 | 2.64E-08                  | 4.17E-08                    |
|            | 68                 | 2.76E-08                  | 4.24E-08                    |
|            | 100                | 3.02E-08                  | 4.39E-08                    |
|            | 150                | 3.51E-08                  | 4.66E-08                    |
|            | 220                | 4.27E-08                  | 5.13E-08                    |
|            | 330                | 5.52E-08                  | 6.19E-08                    |
|            | 470                | 7.17E-08                  | 7.72E-08                    |
|            | 680                | 9.68E-08                  | 1.00E-07                    |
|            | 1000               | 1.34E-07                  | 1.37E-07                    |
|            | 1500               | 1.93E-07                  | 1.94E-07                    |
|            | 2200               | 2.76E-07                  | 2.74E-07                    |
|            | 3300               | 4.06E-07                  | 4.01E-07                    |
|            | 4700               | 5.73E-07                  | 5.62E-07                    |
|            | 6800               | 8.21E-07                  | 7.99E-07                    |
|            | 10000              | 1.20E-06                  | 1.17E-06                    |
|            | 15000              | 1.79E-06                  | 1.74E-06                    |
| 6 bits     | 47                 | 2.14E-08                  | 3.16E-08                    |
|            | 68                 | 2.23E-08                  | 3.21E-08                    |
|            | 100                | 2.40E-08                  | 3.31E-08                    |
|            | 150                | 2.68E-08                  | 3.52E-08                    |
|            | 220                | 3.13E-08                  | 3.87E-08                    |
|            | 330                | 3.89E-08                  | 4.51E-08                    |
|            | 470                | 4.88E-08                  | 5.39E-08                    |
|            | 680                | 6.38E-08                  | 6.79E-08                    |
|            | 1000               | 8.70E-08                  | 8.97E-08                    |
|            | 1500               | 1.23E-07                  | 1.24E-07                    |
|            | 2200               | 1.73E-07                  | 1.73E-07                    |
|            | 3300               | 2.53E-07                  | 2.49E-07                    |
|            | 4700               | 3.53E-07                  | 3.45E-07                    |
|            | 6800               | 5.04E-07                  | 4.90E-07                    |
|            | 10000              | 7.34E-07                  | 7.11E-07                    |
|            | 15000              | 1.09E-06                  | 1.05E-06                    |

1. Specified by design - Not tested in production.

2. Data valid up to 130°C, with a 22 pF PCB capacitor, and  $V_{DDA} = 1.6$  V.

3. Slow channels correspond to all ADC inputs except for the fast channels.

**Figure 56. ADC conversion timing diagram**



**Table 97. ADC accuracy<sup>(1)(2)</sup>**

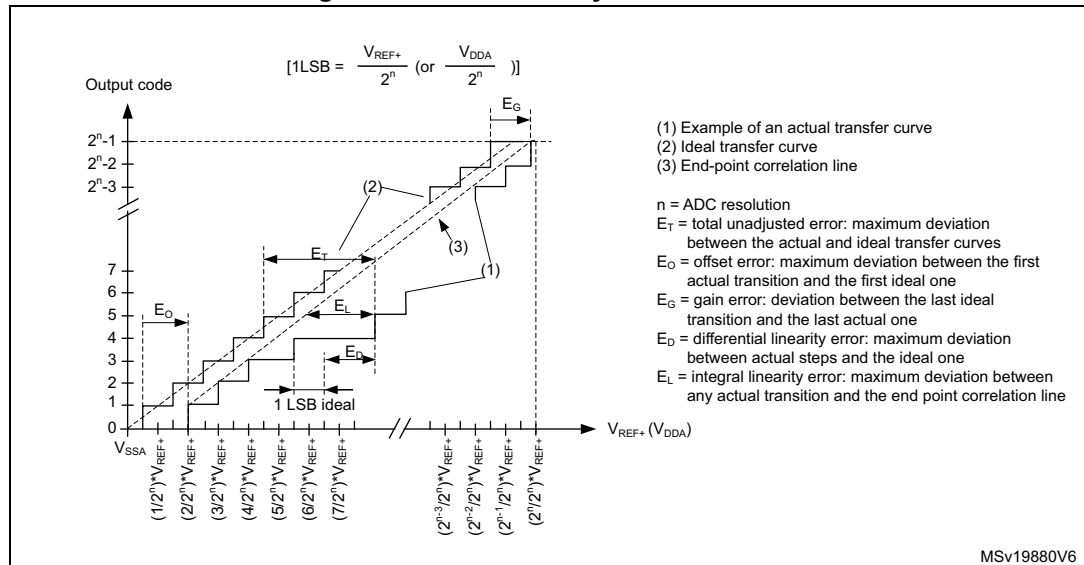
| Symbol | Parameter                            | Conditions             |              | Min | Typ   | Max   | Unit |
|--------|--------------------------------------|------------------------|--------------|-----|-------|-------|------|
| ET     | Total unadjusted error               | Fast and slow channels | Single ended | -   | ±3.5  | ±12   | LSB  |
|        |                                      |                        | Differential | -   | ±2.5  | ±7.5  |      |
| EO     | Offset error                         | -                      | Single ended | -   | ±3    | ±5.5  |      |
|        |                                      | -                      | Differential | -   | ±2    | ±3.5  |      |
| EG     | Gain error                           | -                      | Single ended | -   | ±3.5  | ±11   |      |
|        |                                      | -                      | Differential | -   | ±2.5  | ±7    |      |
| ED     | Differential linearity error         | -                      | Single ended | -   | ±0.75 | +2/-1 |      |
|        |                                      | -                      | Differential | -   | ±0.75 | +2/-1 |      |
| EL     | Integral linearity error             | Fast and slow channels | Single ended | -   | ±2    | ±6.5  |      |
|        |                                      |                        | Differential | -   | ±1    | ±4    |      |
| ENOB   | Effective number of bits             | Single ended           |              | -   | 10.8  | -     | Bits |
|        |                                      | Differential           |              | -   | 11.5  | -     |      |
| SINAD  | Signal-to-noise and distortion ratio | Single ended           |              | -   | 68    | -     | dB   |
|        |                                      | Differential           |              | -   | 71    | -     |      |
| SNR    | Signal-to-noise ratio                | Single ended           |              | -   | 70    | -     |      |
|        |                                      | Differential           |              | -   | 72    | -     |      |
| THD    | Total harmonic distortion            | Single ended           |              | -   | -70   | -     |      |
|        |                                      | Differential           |              | -   | -80   | -     |      |

1. Evaluated by characterization for BGA packages. The values for LQFP package can differ. Not tested in production.

2. ADC DC accuracy values are measured after internal calibration in continuous mode.

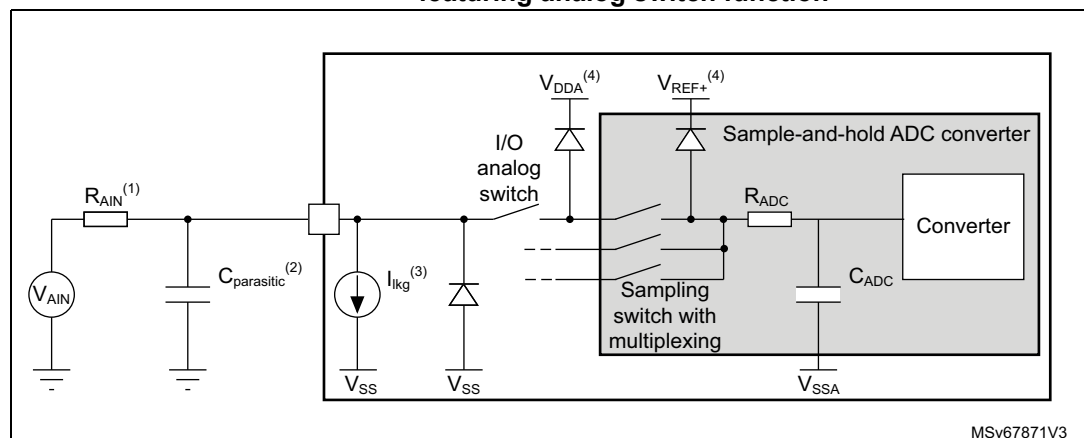
Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins, which may potentially inject negative currents.

Figure 57. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4.  $E_T$  = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
5.  $E_O$  = Offset error: deviation between the first actual transition and the first ideal one.
6.  $E_G$  = Gain error: deviation between the last ideal transition and the last actual one.
7.  $E_D$  = Differential linearity error: maximum deviation between actual steps and the ideal one.
8.  $E_L$  = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 58. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



1. Refer to [Table 95](#) for the values of  $R_{AIN}$  and  $C_{ADC}$ .
2.  $C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the

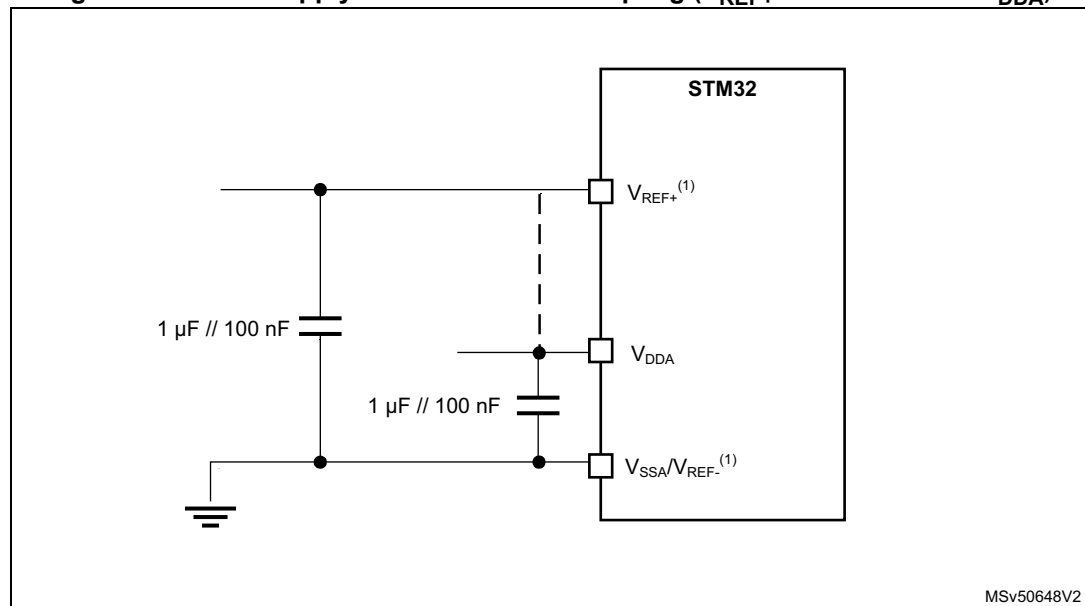
pad capacitance (refer to [Table 58](#)). A high  $C_{\text{parasitic}}$  value downgrades conversion accuracy. To remedy this,  $f_{\text{ADC}}$  should be reduced.

3. Refer to [Table 58](#) for the value of  $I_{\text{Ikg}}$ .
4. Refer to [Figure 21](#).

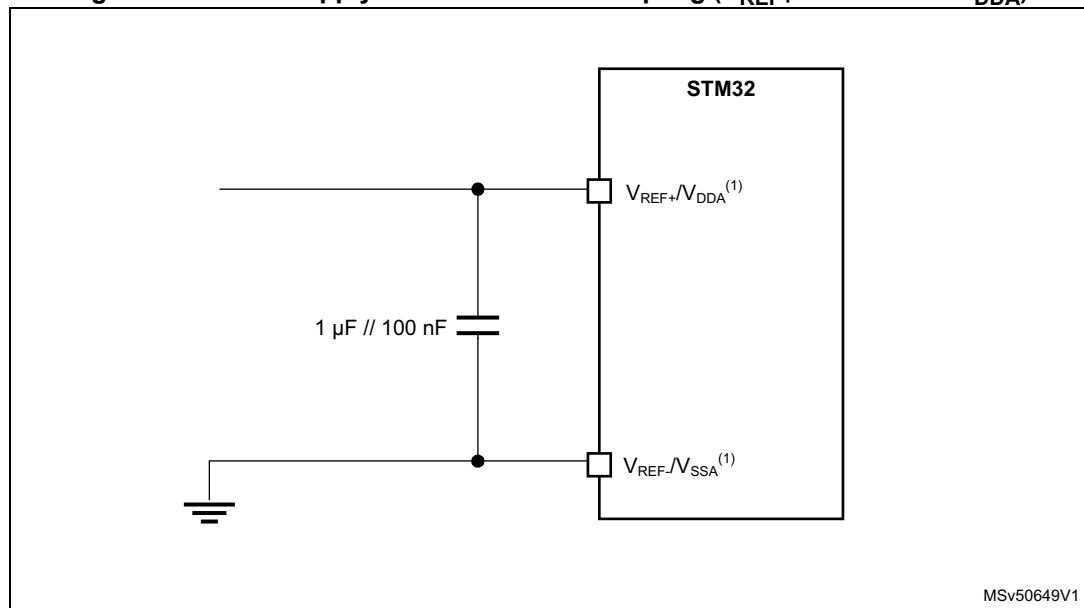
### General PCB design guidelines

It is recommended to perform power supply decoupling as shown in [Figure 59](#) or [Figure 60](#), depending on whether  $V_{\text{REF+}}$  is connected to  $V_{\text{DDA}}$  or not. The 100 nF capacitors must be ceramic (good quality), and placed as close as possible to the chip.

**Figure 59. Power supply and reference decoupling ( $V_{\text{REF+}}$  not connected to  $V_{\text{DDA}}$ )**



1.  $V_{\text{REF+}}$  input is not available on all packages (refer to [Table 14](#)),  $V_{\text{REF-}}$  is available only on UFBGA176+25, UFBGA169 with SMPS, LQFP100, UFBGA169, and UFBGA176+25 packages. When  $V_{\text{REF+}}$  is not available, it is internally connected to  $V_{\text{SSA}}$ .

Figure 60. Power supply and reference decoupling ( $V_{REF+}$  connected to  $V_{DDA}$ )

1.  $V_{REF+}$  input is not available on all packages (refer to [Table 14](#)),  $V_{REF-}$  is available only on UFBGA176+25, UFBGA169 with SMPS, LQFP100, UFBGA169, and UFBGA176+25 packages. When  $V_{REF-}$  is not available, it is internally connected to  $V_{SSA}$ . If  $V_{REF-}$  is available and connected to  $V_{DDA}$ , refer to [Figure 21](#) for more details.

### 5.3.24 DAC characteristics

Table 98. DAC characteristics<sup>(1)</sup>

| Symbol         | Parameter                                                | Conditions            | Min                     | Typ       | Max             | Unit |
|----------------|----------------------------------------------------------|-----------------------|-------------------------|-----------|-----------------|------|
| $V_{DDA}$      | Analog supply voltage                                    | -                     | 1.8                     | 3.3       | 3.6             | V    |
| $V_{REF+}$     | Positive reference voltage                               | -                     | 1.8                     | -         | $V_{DDA}$       |      |
| $V_{REF-}$     | Negative reference voltage                               | -                     | -                       | $V_{SSA}$ | -               |      |
| $R_L$          | Resistive load                                           | DAC output buffer ON  | Connected to $V_{SSA}$  | 5         | -               | kΩ   |
|                |                                                          |                       | Connected to $V_{DDA}$  | 25        | -               |      |
| $R_O$          | Output impedance                                         | DAC output buffer OFF | 10.3                    | 13        | 16              | kΩ   |
| $R_{BON}$      | Output impedance sample and hold mode, output buffer ON  | DAC output buffer ON  | $V_{DD} = 2.7\text{ V}$ | -         | -               |      |
|                |                                                          |                       | $V_{DD} = 2.0\text{ V}$ | -         | -               | kΩ   |
| $R_{BOFF}$     | Output impedance sample and hold mode, output buffer OFF | DAC output buffer OFF | $V_{DD} = 2.7\text{ V}$ | -         | -               |      |
|                |                                                          |                       | $V_{DD} = 2.0\text{ V}$ | -         | -               | kΩ   |
| $C_L$          | Capacitive load                                          | DAC output buffer OFF | -                       | -         | 50              | pF   |
| $C_{SH}$       |                                                          | Sample and hold mode  | -                       | 0.1       | 1               | µF   |
| $V_{DAC\_OUT}$ | Voltage on DAC_OUT output                                | DAC output buffer ON  | 0.2                     | -         | $V_{DDA} - 0.2$ | V    |
|                |                                                          | DAC output buffer OFF | 0                       | -         | $V_{REF+}$      |      |

Table 98. DAC characteristics<sup>(1)</sup> (continued)

| Symbol                    | Parameter                                                                                                                                                                                                                                            | Conditions                                                                               | Min                                | Typ                                                                | Max            | Unit          |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|------------------------------------|--------------------------------------------------------------------|----------------|---------------|
| $t_{\text{SETTLING}}$     | Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of $\pm 0.5\text{LSB}$ , $\pm 1\text{LSB}$ , $\pm 2\text{LSB}$ , $\pm 4\text{LSB}$ , $\pm 8\text{LSB}$ ) | Normal mode, DAC output buffer ON, $C_L \leq 50\text{ pF}$ , $R_L \geq 5\text{ k}\Omega$ | $\pm 0.5\text{ LSB}$               | -                                                                  | 2.05           | 3             |
|                           |                                                                                                                                                                                                                                                      |                                                                                          | $\pm 1\text{ LSB}$                 | -                                                                  | 1.97           | 2.87          |
|                           |                                                                                                                                                                                                                                                      |                                                                                          | $\pm 2\text{ LSB}$                 | -                                                                  | 1.67           | 2.84          |
|                           |                                                                                                                                                                                                                                                      |                                                                                          | $\pm 4\text{ LSB}$                 | -                                                                  | 1.66           | 2.78          |
|                           |                                                                                                                                                                                                                                                      |                                                                                          | $\pm 8\text{ LSB}$                 | -                                                                  | 1.65           | 2.7           |
|                           |                                                                                                                                                                                                                                                      | Normal mode, DAC output buffer OFF, $\pm 1\text{LSB}$ $C_L = 10\text{ pF}$               | -                                  | 1.7                                                                | 2              |               |
| $t_{\text{WAKEUP}}^{(2)}$ | Wake-up time from off state (setting the ENx bit in the DAC control register) until the final value of $\pm 1\text{LSB}$ is reached                                                                                                                  | Normal mode, DAC output buffer ON, $C_L \leq 50\text{ pF}$ , $R_L = 5\text{ k}\Omega$    | -                                  | 5                                                                  | 7.5            | $\mu\text{s}$ |
|                           |                                                                                                                                                                                                                                                      | Normal mode, DAC output buffer OFF, $C_L \leq 10\text{ pF}$                              | -                                  | 2                                                                  | 5              |               |
| PSRR                      | DC $V_{\text{DDA}}$ supply rejection ratio                                                                                                                                                                                                           | Normal mode, DAC output buffer ON, $C_L \leq 50\text{ pF}$ , $R_L = 5\text{ k}\Omega$    | -                                  | -80                                                                | -28            | dB            |
| $t_{\text{SAMP}}$         | Sampling time in Sample and hold mode, $C_L = 100\text{ nF}$ (code transition between the lowest and the highest input code when DAC_OUT reaches the $\pm 1\text{LSB}$ final value)                                                                  | MODE<2:0>_V12 = 100/101 (BUFFER ON)                                                      | -                                  | 0.7                                                                | 2.6            | ms            |
|                           |                                                                                                                                                                                                                                                      | MODE<2:0>_V12 = 110 (BUFFER OFF)                                                         | -                                  | 11.5                                                               | 18.7           |               |
|                           |                                                                                                                                                                                                                                                      | MODE<2:0>_V12=111 <sup>(3)</sup> (INTERNAL BUFFER OFF)                                   | -                                  | 0.3                                                                | 0.6            | $\mu\text{s}$ |
| $I_{\text{leak}}$         | Output leakage current                                                                                                                                                                                                                               | -                                                                                        | -                                  | -                                                                  | <sup>(4)</sup> | nA            |
| $C_{\text{lint}}$         | Internal sample and hold capacitor                                                                                                                                                                                                                   | -                                                                                        | 1.8                                | 2.2                                                                | 2.6            | pF            |
| $t_{\text{TRIM}}$         | Middle code offset trim time                                                                                                                                                                                                                         | Minimum time to verify each code                                                         | 50                                 | -                                                                  | -              | $\mu\text{s}$ |
| $V_{\text{offset}}$       | Middle code offset for 1 trim code step                                                                                                                                                                                                              | $V_{\text{REF}+} = 3.6\text{ V}$                                                         | -                                  | 850                                                                | -              | $\mu\text{V}$ |
|                           |                                                                                                                                                                                                                                                      | $V_{\text{REF}+} = 1.8\text{ V}$                                                         | -                                  | 425                                                                | -              |               |
| $I_{\text{DDA(DAC)}}$     | DAC quiescent consumption from $V_{\text{DDA}}$                                                                                                                                                                                                      | DAC output buffer ON                                                                     | No load, middle code (0x800)       | -                                                                  | 360            | -             |
|                           |                                                                                                                                                                                                                                                      |                                                                                          | No load, worst code (0xF1C)        | -                                                                  | 490            | -             |
|                           |                                                                                                                                                                                                                                                      | DAC output buffer OFF                                                                    | No load, middle/worst code (0x800) | -                                                                  | 20             | -             |
|                           |                                                                                                                                                                                                                                                      | Sample and hold mode, $C_{\text{SH}} = 100\text{ nF}$                                    | -                                  | $360 \cdot T_{\text{ON}} / (T_{\text{ON}} + T_{\text{OFF}})^{(5)}$ | -              |               |

Table 98. DAC characteristics<sup>(1)</sup> (continued)

| Symbol                | Parameter                              | Conditions                                                              |                                    | Min | Typ                                                                      | Max | Unit |
|-----------------------|----------------------------------------|-------------------------------------------------------------------------|------------------------------------|-----|--------------------------------------------------------------------------|-----|------|
| I <sub>DDV(DAC)</sub> | DAC consumption from V <sub>REF+</sub> | DAC output buffer ON                                                    | No load, middle code (0x800)       | -   | 170                                                                      | -   | μA   |
|                       |                                        |                                                                         | No load, worst code (0xF1C)        | -   | 170                                                                      | -   |      |
|                       |                                        | DAC output buffer OFF                                                   | No load, middle/worst code (0x800) | -   | 160                                                                      | -   |      |
|                       |                                        | Sample and hold mode, buffer ON, C <sub>SH</sub> = 100 nF (worst code)  |                                    | -   | 170*T <sub>ON</sub> /(T <sub>ON</sub> +T <sub>OFF</sub> ) <sup>(5)</sup> | -   |      |
|                       |                                        | Sample and hold mode, buffer OFF, C <sub>SH</sub> = 100 nF (worst code) |                                    | -   | 160*T <sub>ON</sub> /(T <sub>ON</sub> +T <sub>OFF</sub> ) <sup>(5)</sup> | -   |      |
|                       |                                        |                                                                         |                                    |     |                                                                          |     |      |

- Specified by design - Not tested in production, unless otherwise specified.
- In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).
- DACx\_OUT pin is not connected externally (internal connection only).
- Refer to [Table 58](#).
- T<sub>ON</sub> is the refresh phase duration, T<sub>OFF</sub> is the hold phase duration. Refer to the reference manual for more details.

Table 99. DAC accuracy<sup>(1)</sup>

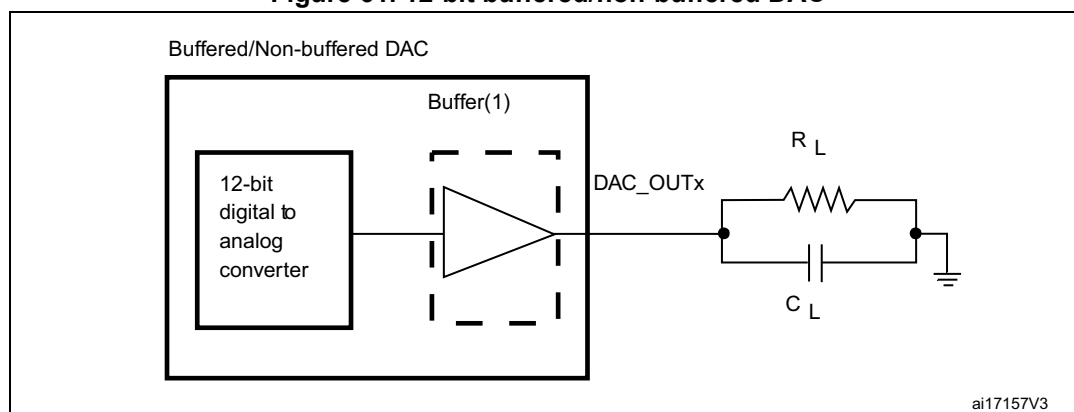
| Symbol    | Parameter                                            | Conditions                                                          |                           | Min | Typ | Max | Unit |
|-----------|------------------------------------------------------|---------------------------------------------------------------------|---------------------------|-----|-----|-----|------|
| DNL       | Differential non linearity <sup>(2)</sup>            | DAC output buffer ON                                                |                           | -2  | -   | 2   | LSB  |
|           |                                                      | DAC output buffer OFF                                               |                           | -2  | -   | 2   |      |
| -         | Monotonicity                                         | 10 bits                                                             |                           | -   | -   | -   | -    |
| INL       | Integral non linearity <sup>(3)</sup>                | DAC output buffer ON, C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ |                           | -4  | -   | 4   |      |
|           |                                                      | DAC output buffer OFF, C <sub>L</sub> ≤ 50 pF, no R <sub>L</sub>    |                           | -4  | -   | 4   |      |
| Offset    | Offset error at code 0x800 <sup>(3)</sup>            | DAC output buffer ON, C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ | V <sub>REF+</sub> = 3.6 V | -   | -   | ±12 | LSB  |
|           |                                                      |                                                                     | V <sub>REF+</sub> = 1.8 V | -   | -   | ±25 |      |
| Offset1   | Offset error at code 0x001 <sup>(4)</sup>            | DAC output buffer OFF, C <sub>L</sub> ≤ 50 pF, no R <sub>L</sub>    |                           | -   | -   | ±8  |      |
|           |                                                      |                                                                     |                           | -   | -   | ±5  |      |
| OffsetCal | Offset error at code 0x800 after factory calibration | DAC output buffer ON, C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ | V <sub>REF+</sub> = 3.6 V | -   | -   | ±5  |      |
|           |                                                      |                                                                     | V <sub>REF+</sub> = 1.8 V | -   | -   | ±7  |      |

Table 99. DAC accuracy<sup>(1)</sup> (continued)

| Symbol | Parameter                                           | Conditions                                                                               | Min | Typ   | Max      | Unit |
|--------|-----------------------------------------------------|------------------------------------------------------------------------------------------|-----|-------|----------|------|
| Gain   | Gain error <sup>(5)</sup>                           | DAC output buffer ON,<br>$C_L \leq 50$ pF, $R_L \geq 5$ k $\Omega$                       | -   | -     | $\pm 1$  | %    |
|        |                                                     | DAC output buffer OFF,<br>$C_L \leq 50$ pF, no $R_L$                                     | -   | -     | $\pm 1$  |      |
| TUE    | Total unadjusted error                              | DAC output buffer ON,<br>$C_L \leq 50$ pF, $R_L \geq 5$ k $\Omega$                       | -   | -     | $\pm 30$ | LSB  |
|        |                                                     | DAC output buffer OFF,<br>$C_L \leq 50$ pF, no $R_L$                                     |     |       | $\pm 12$ |      |
| TUECal | Total unadjusted error after calibration            | DAC output buffer ON,<br>$C_L \leq 50$ pF, $R_L \geq 5$ k $\Omega$                       | -   | -     | $\pm 23$ |      |
| SNR    | Signal-to-noise ratio <sup>(6)</sup>                | DAC output buffer ON, $C_L \leq 50$ pF,<br>$R_L \geq 5$ k $\Omega$ , 1 kHz, BW = 500 kHz | -   | 67.8  | -        | dB   |
|        |                                                     | DAC output buffer OFF, $C_L \leq 50$ pF,<br>no $R_L$ , 1 kHz, BW = 500 kHz               | -   | 67.8  | -        |      |
| THD    | Total harmonic distortion <sup>(6)</sup>            | DAC output buffer ON,<br>$C_L \leq 50$ pF, $R_L \geq 5$ k $\Omega$ , 1 kHz               | -   | -78.6 | -        |      |
|        |                                                     | DAC output buffer OFF,<br>$C_L \leq 50$ pF, no $R_L$ , 1 kHz                             | -   | -78.6 | -        |      |
| SINAD  | Signal-to-noise and distortion ratio <sup>(6)</sup> | DAC output buffer ON,<br>$C_L \leq 50$ pF, $R_L \geq 5$ k $\Omega$ , 1 kHz               | -   | 67.5  | -        |      |
|        |                                                     | DAC output buffer OFF,<br>$C_L \leq 50$ pF, no $R_L$ , 1 kHz                             | -   | 67.5  | -        |      |
| ENOB   | Effective number of bits                            | DAC output buffer ON,<br>$C_L \leq 50$ pF, $R_L \geq 5$ k $\Omega$ , 1 kHz               | -   | 10.9  | -        | bits |
|        |                                                     | DAC output buffer OFF,<br>$C_L \leq 50$ pF, no $R_L$ , 1 kHz                             | -   | 10.9  | -        |      |

1. Evaluated by characterization - Not tested in production.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFFF when the buffer is OFF, and from code giving 0.2 V and ( $V_{REF+} - 0.2$  V) when the buffer is ON.
6. Signal is -0.5 dBFS with  $F_{sampling} = 1$  MHz.

Figure 61. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly, without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

### 5.3.25 Analog temperature sensor characteristics

Table 100. Analog temperature sensor characteristics

| Symbol                   | Parameter                                                          | Min | Typ  | Max  | Unit  |
|--------------------------|--------------------------------------------------------------------|-----|------|------|-------|
| $T_L^{(1)}$              | $V_{SENSE}$ linearity with temperature (from $V_{SENSOR}$ voltage) | -   | -    | 3    | °C    |
|                          | $V_{SENSE}$ linearity with temperature (from ADC counter)          | -   | -    | 3    |       |
| Avg_Slope <sup>(2)</sup> | Average slope (from $V_{SENSOR}$ voltage)                          | -   | 2    | -    | mV/°C |
|                          | Average slope (from ADC counter)                                   | -   | 2    | -    |       |
| $V_{30}^{(3)}$           | Voltage at 30°C ± 5°C                                              | -   | 0.62 | -    | V     |
| $t_{start\_run}$         | Startup time in Run mode (buffer startup)                          | -   | -    | 25.2 | μs    |
| $t_{S\_temp}^{(1)}$      | ADC sampling time when reading the temperature                     | 9   | -    | -    |       |
| $I_{sens}^{(1)}$         | Sensor consumption                                                 | -   | 0.18 | 0.31 | μA    |
| $I_{sensbuf}^{(1)}$      | Sensor buffer consumption                                          | -   | 3.8  | 6.5  |       |

1. Specified by design - Not tested in production.
2. Evaluated by characterization - Not tested in production.
3. Measured at  $V_{DDA} = 3.3\text{ V} \pm 10\text{ mV}$ . The  $V_{30}$  ADC conversion result is stored in the TS\_CAL1 bytes.

Table 101. Temperature sensor calibration values

| Symbol  | Parameter                                                                     | Memory address            |
|---------|-------------------------------------------------------------------------------|---------------------------|
| TS_CAL1 | Temperature sensor raw data acquired value at 30°C, $V_{DDA} = 3.3\text{ V}$  | 0x08FF F814 - 0x08FF F815 |
| TS_CAL2 | Temperature sensor raw data acquired value at 130°C, $V_{DDA} = 3.3\text{ V}$ | 0x08FF F818 - 0x08FF F819 |

### 5.3.26 Digital temperature sensor characteristics

**Table 102. Digital temperature sensor characteristics<sup>(1)</sup>**

| Symbol                   | Parameter                                              | Conditions                               | Min  | Typ  | Max  | Unit  |
|--------------------------|--------------------------------------------------------|------------------------------------------|------|------|------|-------|
| $f_{DTS}^{(2)}$          | Output clock frequency                                 | -                                        | 500  | 750  | 1150 | kHz   |
| $T_{LC}^{(2)}$           | Temperature linearity coefficient                      | VOS2                                     | 1660 | 2100 | 2750 | Hz/°C |
| $T_{TOTAL\_ERROR}^{(2)}$ | Temperature offset measurement, all VOS                | $T_J = -40$ to $30^{\circ}\text{C}$      | -13  | -    | 4    | °C    |
|                          |                                                        | $T_J = 30^{\circ}\text{C}$ to $T_{Jmax}$ | -7   | -    | 2    |       |
| $T_{VDD\_CORE}$          | Additional error due to supply variation               | VOS2                                     | 0    | -    | 0    | °C    |
|                          |                                                        | VOS0, VOS1, VOS3                         | -1   | -    | 1    |       |
| $t_{TRIM}$               | Calibration time                                       | -                                        | -    | -    | 2    | ms    |
| $t_{WAKE\_UP}$           | Wake-up time from off state until DTS ready bit is set | -                                        | -    | 67   | 116  | μs    |
| $I_{DDCORE\_DTS}$        | DTS consumption on $V_{DD\_CORE}$                      | -                                        | 8.5  | 30   | 70   | μA    |

1. Specified by design - Not tested in production, unless otherwise specified.

2. Evaluated by characterization - Not tested in production.

### 5.3.27 $V_{CORE}$ monitoring characteristics

**Table 103.  $V_{CORE}$  monitoring characteristics<sup>(1)</sup>**

| Symbol          | Parameter                                             | Min | Typ | Max | Unit |
|-----------------|-------------------------------------------------------|-----|-----|-----|------|
| $T_{S\_V CORE}$ | ADC sampling time when reading the $V_{CORE}$ voltage | 1   | -   | -   | μs   |

1. Specified by design - Not tested in production.

### 5.3.28 Temperature and $V_{BAT}$ monitoring

**Table 104.  $V_{BAT}$  monitoring characteristics**

| Symbol              | Parameter                                      | Min  | Typ    | Max  | Unit |
|---------------------|------------------------------------------------|------|--------|------|------|
| R                   | Resistor bridge for $V_{BAT}$                  | -    | 4 x 26 | -    | kΩ   |
| $Q^{(1)}$           | Ratio on $V_{BAT}$ measurement                 | -    | 4      | -    | -    |
| $Er^{(2)}$          | Error on Q                                     | -10  | -      | +10  | %    |
| $t_{S\_vbat}^{(2)}$ | ADC sampling time when reading $V_{BAT}$ input | 9    | -      | -    | μs   |
| $V_{BAThigh}$       | High supply monitoring                         | 3.50 | 3.575  | 3.63 | V    |
| $V_{BATlow}$        | Low supply monitoring                          | -    | 1.36   | -    |      |
| $I_{VBATbuf}$       | Sensor buffer consumption                      | -    | 3.8    | 6.5  | μA   |

1.  $1.2\text{ V} \leq V_{BAT} \leq 3.63\text{ V}$ .

2. Specified by design - Not tested in production.

Table 105. V<sub>BAT</sub> charging characteristics

| Symbol          | Parameter                 | Conditions          | Min | Typ | Max | Unit |
|-----------------|---------------------------|---------------------|-----|-----|-----|------|
| R <sub>BC</sub> | Battery charging resistor | VBRS in PWR_CR3 = 0 | -   | 5   | -   | kΩ   |
|                 |                           | VBRS in PWR_CR3 = 1 | -   | 1.5 | -   |      |

Table 106. Temperature monitoring characteristics

| Symbol               | Parameter                   | Min | Typ | Max | Unit |
|----------------------|-----------------------------|-----|-----|-----|------|
| TEMP <sub>high</sub> | High temperature monitoring | -   | 126 | -   | °C   |
| TEMP <sub>low</sub>  | Low temperature monitoring  | -   | -37 | -   |      |

### 5.3.29 Voltage booster for analog switch

Table 107. Voltage booster for analog switch characteristics<sup>(1)</sup>

| Symbol                 | Parameter            | Conditions                       | Min  | Typ | Max | Unit |
|------------------------|----------------------|----------------------------------|------|-----|-----|------|
| V <sub>DD</sub>        | Supply voltage       | -                                | 1.71 | 2.6 | 3.6 | V    |
| t <sub>SU(BOOST)</sub> | Booster startup time | -                                | -    | -   | 50  | μs   |
| I <sub>DD(BOOST)</sub> | Booster consumption  | 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V | -    | -   | 125 | μA   |
|                        |                      | 2.7 V < V <sub>DD</sub> < 3.6 V  | -    | -   | 250 |      |

1. Evaluated by characterization - Not tested in production.

### 5.3.30 VREFBUF characteristics

Table 108. VREFBUF characteristics<sup>(1)</sup>

| Symbol                  | Parameter                       | Conditions                                      |           | Min                       | Typ    | Max                   | Unit |
|-------------------------|---------------------------------|-------------------------------------------------|-----------|---------------------------|--------|-----------------------|------|
| V <sub>DDA</sub>        | Analog supply voltage           | Normal mode at V <sub>DDA</sub> = 3.3 V         | VRS = 000 | 2.8                       | 3.3    | 3.6                   | V    |
|                         |                                 |                                                 | VRS = 001 | 2.4                       | -      | 3.6                   |      |
|                         |                                 |                                                 | VRS = 010 | 2.1                       | -      | 3.6                   |      |
|                         |                                 | Degraded mode <sup>(2)</sup>                    | VRS = 000 | 1.62                      | -      | 2.80                  |      |
|                         |                                 |                                                 | VRS = 001 | 1.62                      | -      | 2.40                  |      |
|                         |                                 |                                                 | VRS = 010 | 1.62                      | -      | 2.10                  |      |
| V <sub>REFBUF_OUT</sub> | Voltage reference buffer output | Normal mode at 30°C, I <sub>LOAD</sub> = 100 μA | VRS = 000 | 2.4980 <sup>(3)</sup>     | 2.5000 | 2.5035 <sup>(3)</sup> | V    |
|                         |                                 |                                                 | VRS = 001 | 2.046                     | 2.049  | 2.052                 |      |
|                         |                                 |                                                 | VRS = 010 | 1.801                     | 1.804  | 1.806                 |      |
|                         |                                 | Degraded mode <sup>(2)</sup>                    | VRS = 000 | V <sub>DDA</sub> - 150 mV | -      | 2.5035                |      |
|                         |                                 |                                                 | VRS = 001 |                           | -      | 2.0520                |      |
|                         |                                 |                                                 | VRS = 010 |                           | -      | 1.8060                |      |
| TRIM                    | Trim step resolution            | -                                               | -         | -                         | ±0.05  | ±0.1                  | %    |

Table 108. VREFBUF characteristics<sup>(1)</sup> (continued)

| Symbol                    | Parameter                                                                                     | Conditions                                                     |                                            | Min | Typ | Max  | Unit                  |
|---------------------------|-----------------------------------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------|-----|-----|------|-----------------------|
| $C_L$                     | Load capacitor                                                                                | -                                                              | -                                          | 0.5 | 1   | 1.50 | $\mu\text{F}$         |
| esr                       | Equivalent serial resistor of $C_L$                                                           | -                                                              | -                                          | -   | -   | 2    | $\Omega$              |
| $I_{\text{load}}$         | Static load current                                                                           | -                                                              | -                                          | -   | -   | 4    | mA                    |
| $I_{\text{line\_reg}}$    | Line regulation                                                                               | $2.8\text{ V} \leq V_{\text{DDA}} \leq 3.6\text{ V}$           | $I_{\text{load}} = 500\text{ }\mu\text{A}$ | -   | 200 | -    | ppm/V                 |
|                           |                                                                                               |                                                                | $I_{\text{load}} = 4\text{ mA}$            | -   | 100 | -    |                       |
| $I_{\text{load\_reg}}$    | Load regulation                                                                               | $500\text{ }\mu\text{A} \leq I_{\text{load}} \leq 4\text{ mA}$ | Normal mode                                | -   | 50  | -    | ppm/mA                |
| $T_{\text{coeff}}$        | Temperature coefficient                                                                       | $-40^\circ\text{C} < T_J < +130^\circ\text{C}$                 | -                                          | -   | -   | 100  | ppm/ $^\circ\text{C}$ |
| PSRR                      | Power supply rejection                                                                        | DC                                                             | -                                          | -   | 60  | -    | dB                    |
|                           |                                                                                               | 100 kHz                                                        | -                                          | -   | 40  | -    |                       |
| $t_{\text{START}}$        | Start-up time                                                                                 | $C_L = 0.5\text{ }\mu\text{F}$                                 | -                                          | -   | 300 | -    | $\mu\text{s}$         |
|                           |                                                                                               | $C_L = 1\text{ }\mu\text{F}$                                   | -                                          | -   | 500 | -    |                       |
|                           |                                                                                               | $C_L = 1.5\text{ }\mu\text{F}$                                 | -                                          | -   | 650 | -    |                       |
| $I_{\text{INRUSH}}$       | Control of maximum DC current drive on $V_{\text{REFBUF\_OUT}}$ during startup <sup>(4)</sup> | -                                                              | -                                          | -   | 8   | -    | mA                    |
| $I_{\text{DDA(VREFBUF)}}$ | Consumption from VDDA                                                                         | $I_{\text{LOAD}} = 0\text{ }\mu\text{A}$                       | -                                          | -   | 15  | 25   | $\mu\text{A}$         |
|                           |                                                                                               | $I_{\text{LOAD}} = 500\text{ }\mu\text{A}$                     | -                                          | -   | 16  | 30   |                       |
|                           |                                                                                               | $I_{\text{LOAD}} = 4\text{ mA}$                                | -                                          | -   | 32  | 50   |                       |

1. Specified by design - Not tested in production, unless otherwise specified.

2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage ( $V_{\text{DDA}}$ -drop voltage).

3. Evaluated by characterization - Not tested in production.

4. To properly control  $V_{\text{REFBUF}}$   $I_{\text{INRUSH}}$  current during the startup phase and the change of scaling,  $V_{\text{DDA}}$  voltage must be in the range of 2.1 V - 3.6 V, 2.4 V - 3.6 V, and 2.8 V - 3.6 V, respectively, for VRS = 010, 001, and 000.

### 5.3.31 Timer characteristics

The parameters given in [Table 109](#) are guaranteed by design.

Refer to [Section 5.3.15](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 109. TIMx characteristics<sup>(1)(2)</sup>

| Symbol           | Parameter                                    | Conditions <sup>(3)</sup>                                   | Min | Max                  | Unit          |
|------------------|----------------------------------------------|-------------------------------------------------------------|-----|----------------------|---------------|
| $t_{res(TIM)}$   | Timer resolution time                        | AHB/APBx prescaler = 1, 2, or 4,<br>$f_{TIMxCLK} = 250$ MHz | 1   | -                    | $t_{TIMxCLK}$ |
|                  |                                              | AHB/APBx prescaler > 4,<br>$f_{TIMxCLK} = 125$ MHz          | 1   | -                    | $t_{TIMxCLK}$ |
| $f_{EXT}$        | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK} = 250$ MHz                                     | 0   | $f_{TIMxCLK} / 2$    | MHz           |
| $Res_{TIM}$      | Timer resolution                             |                                                             | -   | 16 / 32              | bit           |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter   | -                                                           | -   | $65536 \times 65536$ | $t_{TIMxCLK}$ |

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Specified by design - Not tested in production.
3. The maximum timer frequency on APB1 or APB2 is up to 250 MHz, by setting the TIMPRE bit in the RCC\_CFGR register, if APBx prescaler is 1 or 2 or 4, then  $TIMxCLK = rcc\_hclk1$ , otherwise  $TIMxCLK = 4 \times F_{rcc\_pclkx1}$  or  $TIMxCLK = 4 \times F_{rcc\_pclkx2}$ .

### 5.3.32 Low-power timer characteristics

Table 110. LPTIMx characteristics<sup>(1)(2)</sup>

| Symbol               | Parameter                                           | Min | Max                      | Unit                 |
|----------------------|-----------------------------------------------------|-----|--------------------------|----------------------|
| $t_{res(TIM)}$       | Timer resolution time                               | 1   | -                        | $t_{lptim\_ker\_ck}$ |
| $f_{lptim\_ker\_ck}$ | Timer kernel clock                                  | 0   | 250                      | MHz                  |
| $f_{EXT}$            | Timer external clock frequency on Input1 and Input2 | 0   | $f_{lptim\_ker\_ck} / 3$ |                      |
| $Res_{TIM}$          | Timer resolution                                    | -   | 16                       | bit                  |
| $t_{MAX\_COUNT}$     | Maximum possible count                              | -   | 65535                    | $t_{lptim\_ker\_ck}$ |

1. LPTIMx is used as a general term for LPTIM1 to LPTIM6 timers.
2. Specified by design - Not tested in production.

### 5.3.33 Communication interfaces

#### I<sup>2</sup>C interface characteristics

The I<sup>2</sup>C interface meets the timings requirements of the I<sup>2</sup>C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I<sup>2</sup>C timings requirements are specified by design, not tested in production, when the I<sup>2</sup>C peripheral is properly configured (refer to the product reference manual)

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and  $V_{DD}$  is disabled, but still present. Only FT\_f I/O pins support Fm+ low level output current maximum requirement. Refer to [Section 5.3.15](#) for the I2C I/Os characteristics

All I<sup>2</sup>C SDA and SCL I/Os embed an analog filter, refer to [Table 111](#) for its characteristics.

**Table 111. I<sup>2</sup>C analog filter characteristics<sup>(1)(2)</sup>**

| Symbol   | Parameter                                                 | Min               | Max                | Unit |
|----------|-----------------------------------------------------------|-------------------|--------------------|------|
| $t_{AF}$ | Maximum pulse width of spikes suppressed by analog filter | 50 <sup>(3)</sup> | 160 <sup>(4)</sup> | ns   |

1. Evaluated by characterization - Not tested in production.

2. Measurement points are done at 50%  $V_{DD}$ .

3. Spikes with widths below  $t_{AF(min)}$  are filtered.

4. Spikes with widths above  $t_{AF(max)}$  are not filtered.

## USART interface characteristics

Unless otherwise specified, the parameters given in [Table 112](#) are derived from tests performed under the ambient temperature,  $f_{PCLKx}$  frequency, and  $V_{DD}$  supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load  $C_L$  = 30 pF
- Measurement points are done at CMOS levels: 0.5  $V_{DD}$
- I/O compensation cell activated
- VOS level set to VOS0
- HSLV activated when  $V_{DD} \leq 2.7$  V

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

**Table 112. USART characteristics<sup>(1)</sup>**

| Symbol   | Parameter             | Conditions                                                      | Min | Typ | Max                 | Unit |
|----------|-----------------------|-----------------------------------------------------------------|-----|-----|---------------------|------|
| $f_{CK}$ | USART clock frequency | Master receiver<br>$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$    | -   | -   | 31                  | MHz  |
|          |                       | Master transmitter<br>$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$ |     |     | 31/6 <sup>(2)</sup> |      |
|          |                       | Master transmitter<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$  |     |     | 31/6 <sup>(2)</sup> |      |
|          |                       | Slave receiver<br>$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$     |     |     | 83                  |      |
|          |                       | Slave transmitter<br>$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$  |     |     | 32/6 <sup>(2)</sup> |      |
|          |                       | Slave transmitter<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$   |     |     | 35/6 <sup>(2)</sup> |      |

Table 112. USART characteristics<sup>(1)</sup> (continued)

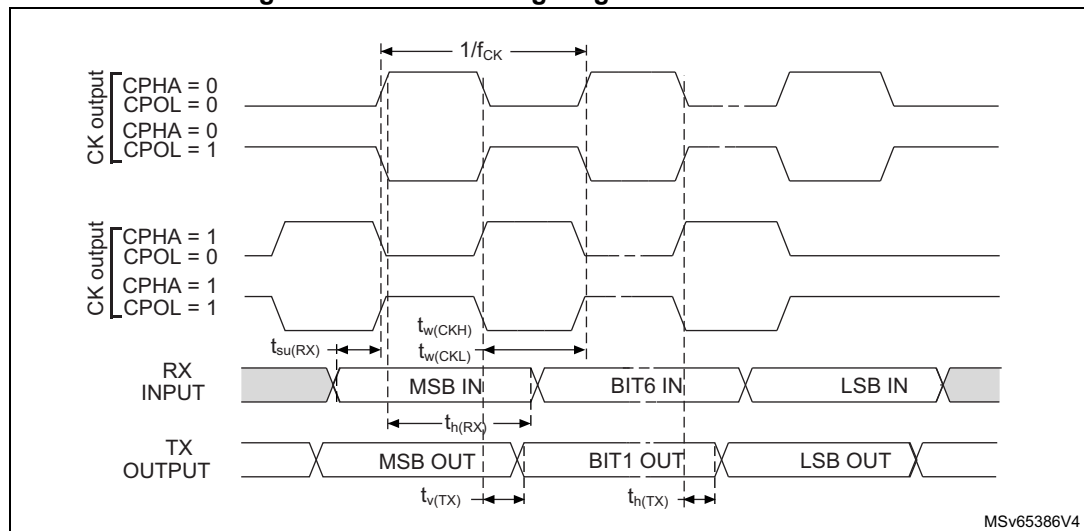
| Symbol                         | Parameter              | Conditions                                             | Min                   | Typ          | Max              | Unit |
|--------------------------------|------------------------|--------------------------------------------------------|-----------------------|--------------|------------------|------|
| $t_{su(NSS)}$                  | NSS setup time         | Slave mode                                             | $t_{ker}^{(3)} + 3.5$ | -            | -                | ns   |
| $t_{h(NSS)}$                   | NSS hold time          | Slave mode                                             | 2.5                   | -            | -                |      |
| $t_{w(SCKH)}$<br>$t_{w(SCKL)}$ | CK high and low time   | Master mode                                            | $1/f_{ck}/2 - 1$      | $1/f_{ck}/2$ | $1/f_{ck}/2 + 1$ |      |
| $t_{su(RX)}$                   | Data input setup time  | Master mode                                            | 13                    | -            | -                |      |
|                                |                        | Slave mode                                             | 3.5                   | -            | -                |      |
| $t_{h(RX)}$                    | Data input hold time   | Master mode                                            | 0.5                   | -            | -                |      |
|                                |                        | Slave mode                                             | 1.5                   | -            | -                |      |
| $t_{v(TX)}$                    | Data output valid time | Slave mode,<br>$1.71\text{ V} < V_{DD} < 3.6\text{ V}$ | -                     | 11.5         | $15.5/71^{(2)}$  | ns   |
|                                |                        | Slave mode,<br>$2.7\text{ V} < V_{DD} < 3.6\text{ V}$  | -                     |              | $14/35^{(2)}$    |      |
|                                |                        | Slave mode,<br>$1.71\text{ V} < V_{DD} < 3.6\text{ V}$ | -                     | 2.5          | $3/52^{(2)}$     |      |
|                                |                        | Slave mode,<br>$2.7\text{ V} < V_{DD} < 3.6\text{ V}$  | -                     |              | $3/22^{(2)}$     |      |
| $t_{h(TX)}$                    | Data output hold time  | Slave mode                                             | 7.5                   | -            | -                | ns   |
|                                |                        | Master mode                                            | 0                     | -            | -                |      |

1. Evaluated by characterization - Not tested in production.

2. For PB14 with OSPEEDR[1:0] = 01.

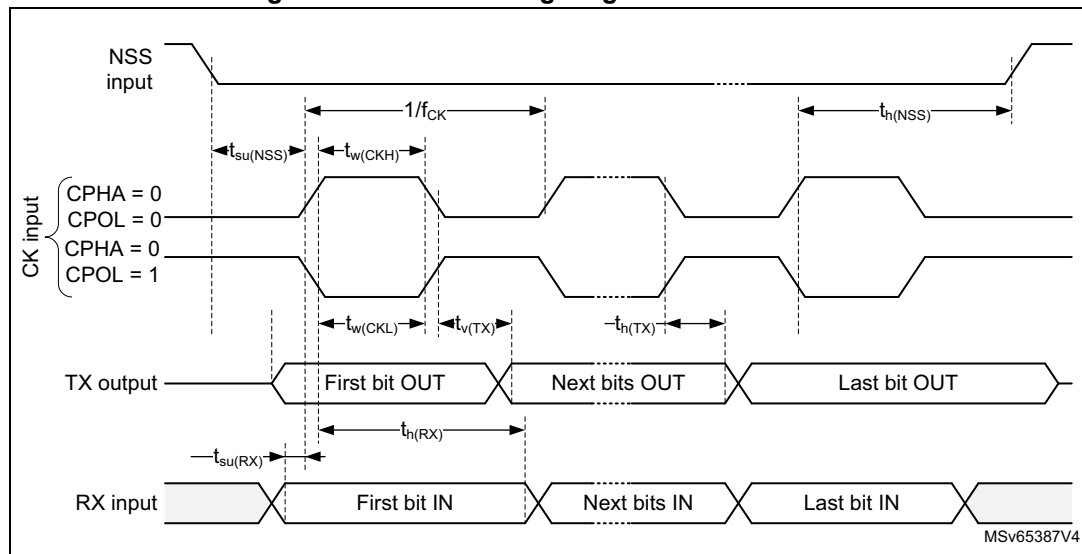
3.  $T_{ker}$  is the usart\_ker\_ck\_pres clock period.

Figure 62. USART timing diagram in Master mode



1. Measurement points are done at  $0.5V_{DD}$  and with external  $C_L = 30\text{ pF}$ .

Figure 63. USART timing diagram in Slave mode



### I3C interface characteristics

The I3C interface meets the timings requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

The parameters given in [Table 113](#) are obtained with the following configuration:

- Output speed is set to  $OSPEEDR[1:0] = 10$
- I/O compensation cell activated
- HSLV activated when  $V_{DD} \leq 2.7$  V
- VOS level set to VOS0

The timings are in line with MIPI specification, except for the ones given in [Table 113](#) and [Table 114](#). For  $t_{SU\_OD}$  and  $t_{SU\_PP}$  this can be mitigated by increasing the corresponding SCL low duration in the I3C\_TIMINGR0 register. For  $t_{SCO}$  this can be mitigated by enabling and adjusting the clock stall time both on the address ACK phase and on the data read Tbit phase in the I3C\_TIMINGR2 register. This can also be mitigated by increasing the SCL low duration in the I3C\_TIMINGR0 register. For further details, refer to AN5879.

Table 113. I3C open-drain measured timings

| Symbol       | Parameter                                  | Conditions                                             | I3C open drain mode (specification) |     | Timing measurement | Unit |
|--------------|--------------------------------------------|--------------------------------------------------------|-------------------------------------|-----|--------------------|------|
|              |                                            |                                                        | Min                                 | Max |                    |      |
| $t_{SU\_OD}$ | SDA data setup time during open drain mode | Controller<br>$1.08\text{ V} < V_{DD} < 1.32\text{ V}$ | 3                                   | -   | 23                 | ns   |
|              |                                            | Controller<br>$1.71\text{ V} < V_{DD} < 3.6\text{ V}$  | 3                                   | -   | 16.5               |      |

Table 114. I3C push-pull measured timings

| Symbol       | Parameter                               | Conditions                                                | I3C open drain mode (specification) |     | Timing measurement | Unit |
|--------------|-----------------------------------------|-----------------------------------------------------------|-------------------------------------|-----|--------------------|------|
|              |                                         |                                                           | Min                                 | Max |                    |      |
| $t_{SCO}$    | Clock in to data out for target         | Target<br>$1.08\text{ V} < V_{DDIO2} < 1.32\text{ V}$     | -                                   | 12  | 18                 | ns   |
| $t_{SU\_PP}$ | SDA signal data setup in push-pull mode | Controller<br>$1.08\text{ V} < V_{DDIO2} < 1.32\text{ V}$ | 3                                   | -   | 21                 | ns   |
|              |                                         | Controller<br>$1.71\text{ V} < V_{DDIO2} < 3.62\text{ V}$ | 3                                   | -   | 12                 |      |

### SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 115](#) are derived from tests performed under the ambient temperature,  $f_{PCLKx}$  frequency, and  $V_{DD}$  supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to  $OSPEEDRy[1:0] = 11$
- Capacitive load  $C_L = 30\text{ pF}$
- Measurement points are done at CMOS levels:  $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when  $V_{DD} \leq 2.7\text{ V}$
- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 115. SPI characteristics<sup>(1)</sup>

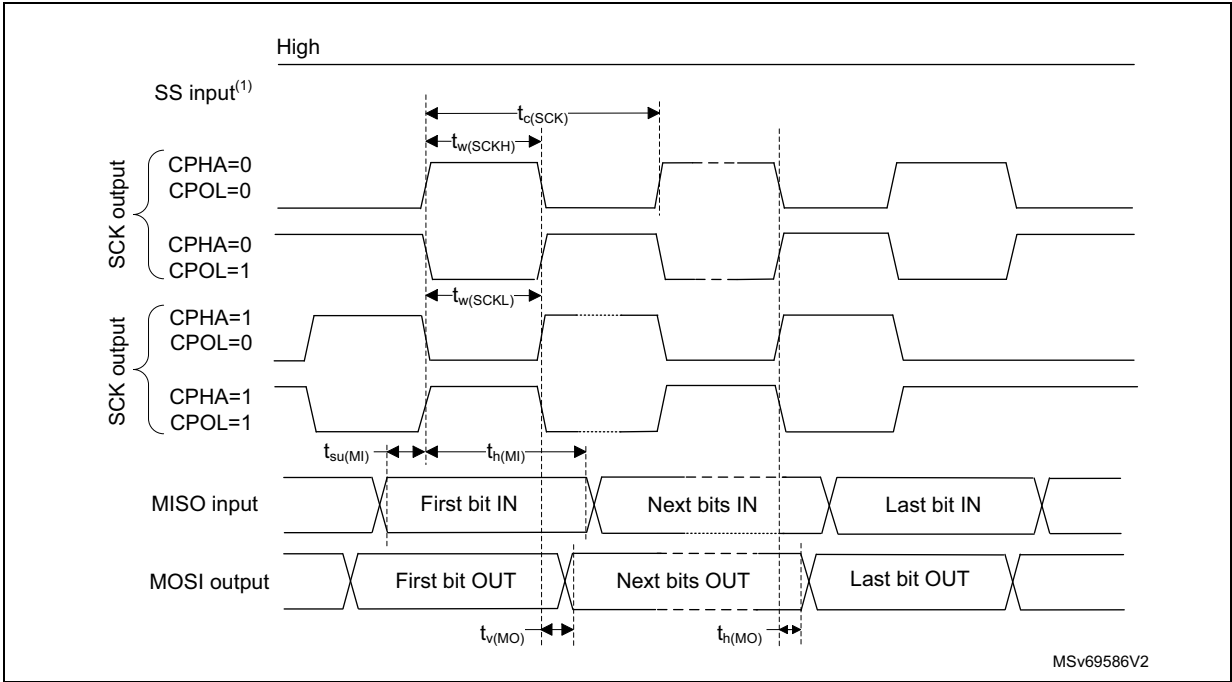
| Symbol                         | Parameter                | Conditions                                                             | Min               | Typ                   | Max                    | Unit |
|--------------------------------|--------------------------|------------------------------------------------------------------------|-------------------|-----------------------|------------------------|------|
| $f_{SCK}$<br>$1/t_{SCK}$       | SPI clock frequency      | Master receiver mode<br>$2.7\text{ V} < V_{DD} < 3.6\text{ V}$         | -                 | -                     | 135/3 <sup>(2)</sup>   | MHz  |
|                                |                          | Master receiver mode<br>$1.71\text{ V} < V_{DD} < 2.7\text{ V}$        | -                 | -                     | 120/3 <sup>(2)</sup>   |      |
|                                |                          | Master receiver mode<br>$1.08\text{ V} < V_{DDIO2} < 1.32\text{ V}$    | -                 | -                     | 50                     |      |
|                                |                          | Master transmitter mode<br>$2.7\text{ V} < V_{DD} < 3.6\text{ V}$      |                   |                       | 135/3 <sup>(2)</sup>   |      |
|                                |                          | Master transmitter mode<br>$1.71\text{ V} < V_{DD} < 3.6\text{ V}$     | -                 | -                     | 120/3 <sup>(2)</sup>   |      |
|                                |                          | Master transmitter mode<br>$1.08\text{ V} < V_{DDIO2} < 1.32\text{ V}$ |                   |                       | 50                     |      |
|                                |                          | Slave receiver mode<br>$1.71\text{ V} < V_{DD} < 3.6\text{ V}$         | -                 | -                     | 120                    |      |
|                                |                          | Slave receiver mode<br>$1.08\text{ V} < V_{DDIO2} < 1.32\text{ V}$     |                   |                       | 120                    |      |
|                                |                          | Slave transmitter mode<br>$2.7\text{ V} < V_{DD} < 3.6\text{ V}$       | -                 | -                     | 43/6 <sup>(3)</sup>    |      |
|                                |                          | Slave transmitter mode<br>$1.71\text{ V} < V_{DD} < 2.7\text{ V}$      | -                 | -                     | 41/6 <sup>(3)</sup>    |      |
|                                |                          | Slave transmitter mode<br>$1.08\text{ V} < V_{DDIO2} < 1.32\text{ V}$  | -                 | -                     | 23                     |      |
| $t_{su(NSS)}$                  | NSS setup time           | Slave mode                                                             | 3.5               | -                     | -                      | ns   |
| $t_{h(NSS)}$                   | NSS hold time            | Slave mode                                                             | 4.5               | -                     | -                      |      |
| $t_{w(SCKH)}$<br>$t_{w(SCKL)}$ | SCK high and low time    | Master mode                                                            | $(t_{SCK}/2) - 1$ | $t_{SCK}/2$           | $(t_{SCK}/2) + 1$      | ns   |
| $t_{su(MI)}$                   | Data input setup time    | Master mode                                                            | 3.5               | -                     | -                      | ns   |
| $t_{su(SI)}$                   |                          | Slave mode                                                             | 2                 | -                     | -                      |      |
| $t_{h(MI)}$                    | Data input hold time     | Master mode                                                            | 1                 | -                     | -                      |      |
| $t_{h(SI)}$                    |                          | Slave mode                                                             | 1.5               | -                     | -                      |      |
| $t_{a(SO)}$                    | Data output access time  | Slave mode                                                             | 6.5               | -                     | 15                     | ns   |
| $t_{dis(SO)}$                  | Data output disable time | Slave mode                                                             | 7.5               | -                     | 18                     |      |
| $t_{v(SO)}$                    | Data output valid time   | Slave mode,<br>$2.7\text{ V} < V_{DD} < 3.6\text{ V}$                  | -                 | 8.5/25 <sup>(3)</sup> | 11.5/33 <sup>(3)</sup> | ns   |
|                                |                          | Slave mode,<br>$1.71\text{ V} < V_{DD} < 3.6\text{ V}$                 | -                 | 10/59 <sup>(3)</sup>  | 12/76 <sup>(3)</sup>   |      |
|                                |                          | Slave mode<br>$1.08\text{ V} < V_{DDIO2} < 1.32\text{ V}$              |                   | 18                    | 21.5                   |      |
| $t_{v(MO)}$                    |                          | Master mode                                                            | -                 | 1.5                   | 2                      |      |

Table 115. SPI characteristics<sup>(1)</sup> (continued)

| Symbol      | Parameter             | Conditions                                      | Min                     | Typ | Max | Unit |
|-------------|-----------------------|-------------------------------------------------|-------------------------|-----|-----|------|
| $t_{h(SO)}$ | Data output hold time | Slave mode,<br>1.71 V < V <sub>DD</sub> < 3.6 V | 6.5/20.5 <sup>(3)</sup> | -   | -   | ns   |
| $t_{h(MO)}$ |                       | Master mode                                     | 0                       | -   | -   |      |

- 1. Evaluated by characterization - Not tested in production.
- 2. When using PB13.
- 3. When using PB14.

Figure 64. SPI timing diagram - Master mode



- 1. The SS input can be configured to active low or active high.

Figure 65. SPI timing diagram - Slave mode and CPHA = 0

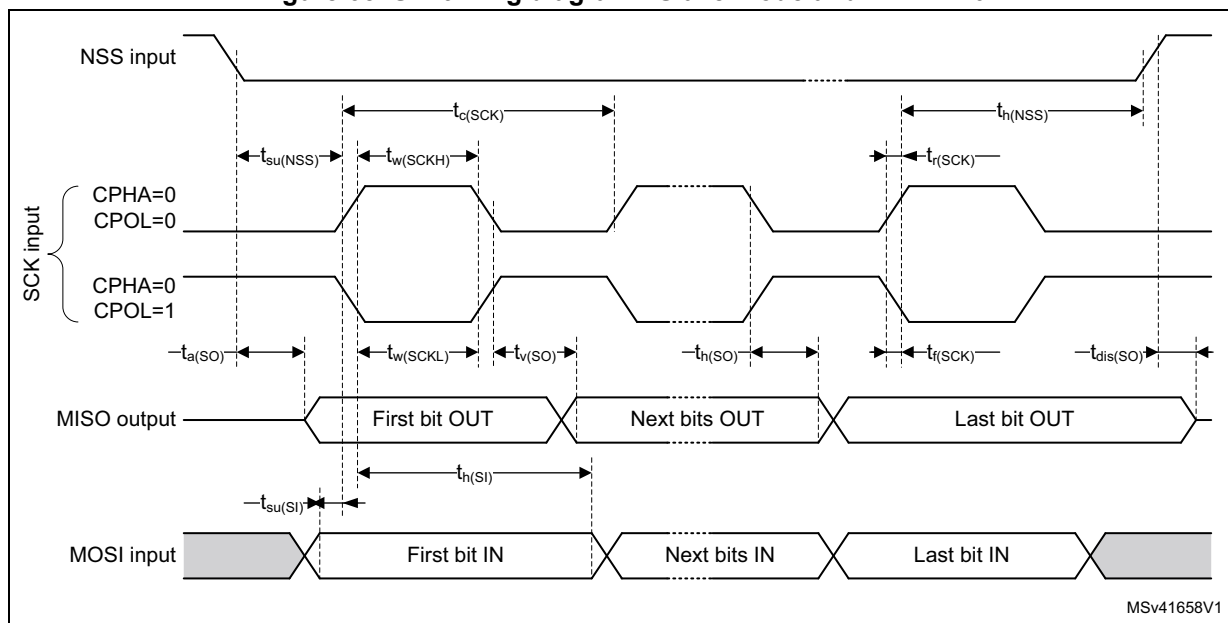
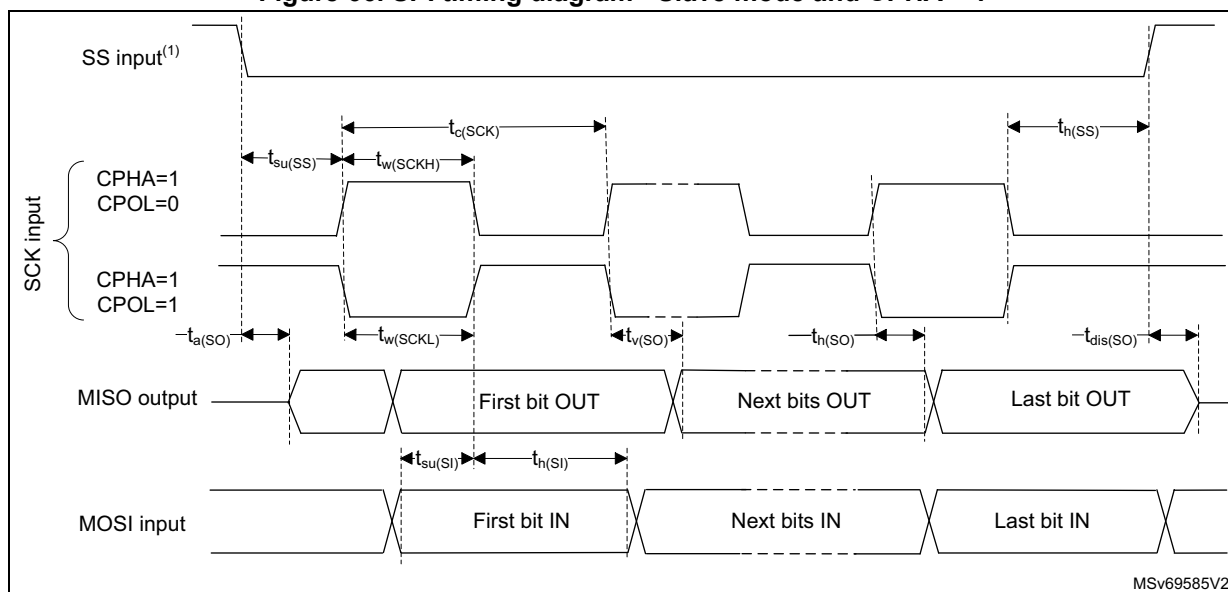


Figure 66. SPI timing diagram - Slave mode and CPHA = 1



1. The SS input can be configured to active low or active high.

## I<sup>2</sup>S interface characteristics

Unless otherwise specified, the parameters given in [Table 116](#) are derived from tests performed under the ambient temperature,  $f_{CLKx}$  frequency, and  $V_{DD}$  supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to  $OSPEEDRy[1:0] = 11$
- Capacitive load  $C_L = 30 \text{ pF}$
- Measurement points are done at CMOS levels:  $0.5 V_{DD}$
- I/O compensation cell activated

- HSLV activated when  $V_{DD} \leq 2.7$  V
- VOS level set to VOS0

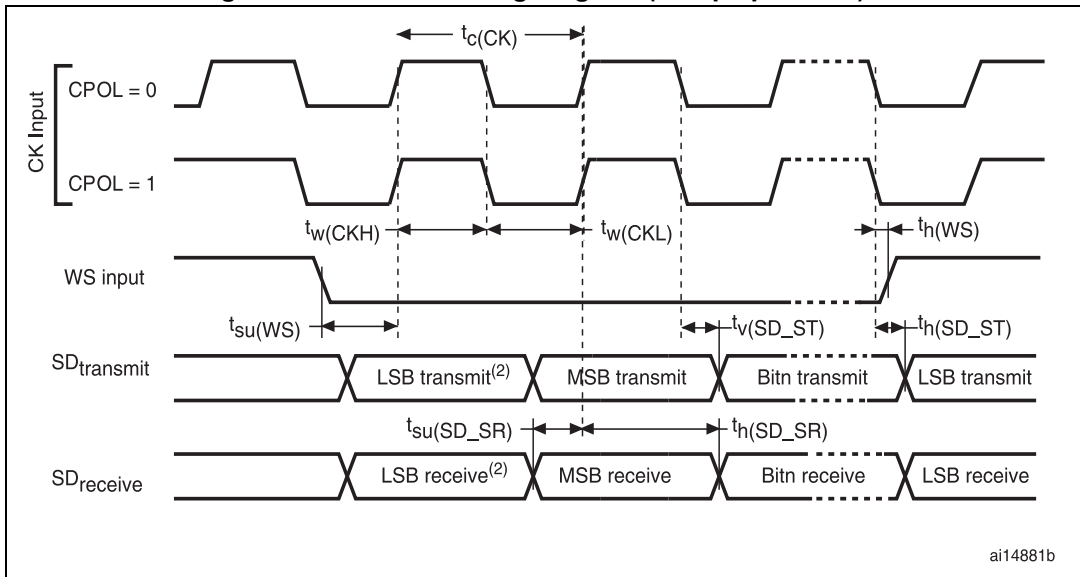
Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics (CK,SD,WS).

**Table 116. I<sup>2</sup>S dynamic characteristics<sup>(1)</sup>**

| Symbol           | Parameter                          | Conditions                             | Min | Max | Unit |
|------------------|------------------------------------|----------------------------------------|-----|-----|------|
| $f_{MCK}$        | I <sup>2</sup> S main clock output | -                                      | -   | 50  | MHz  |
| $f_{CK}$         | I <sup>2</sup> S clock output      | Master transmitter                     | -   | 50  |      |
|                  |                                    | Slave transmitter (TX)                 | -   | 21  |      |
|                  |                                    | Slave receiver (RX)                    | -   | 50  |      |
| $t_{v(WS)}$      | WS valid time                      | Master mode                            | -   | 2   | ns   |
| $t_{h(WS)}$      | WS hold time                       |                                        | 0.5 | -   |      |
| $t_{su(WS)}$     | WS setup time                      | Slave mode                             | 3   | -   |      |
| $t_{h(WS)}$      | WS hold time                       |                                        | 1.5 | -   |      |
| $t_{su(SD\_MR)}$ | Data input setup time              | Master receiver                        | 4   | -   |      |
| $t_{su(SD\_SR)}$ |                                    | Slave receiver                         | 2   | -   |      |
| $t_{h(SD\_MR)}$  | Data input hold time               | Master receiver                        | 1   | -   |      |
| $t_{h(SD\_SR)}$  |                                    | Slave receiver                         | 1.5 | -   |      |
| $t_{v(SD\_ST)}$  | Data output valid time             | Slave transmitter (after enable edge)  | -   | 14  |      |
| $t_{v(SD\_MT)}$  |                                    | Master transmitter (after enable edge) | -   | 1   |      |
| $t_{h(SD\_ST)}$  | Data output hold time              | Slave transmitter (after enable edge)  | 5.5 | -   |      |
| $t_{h(SD\_MT)}$  |                                    | Master transmitter (after enable edge) | 0   | -   |      |

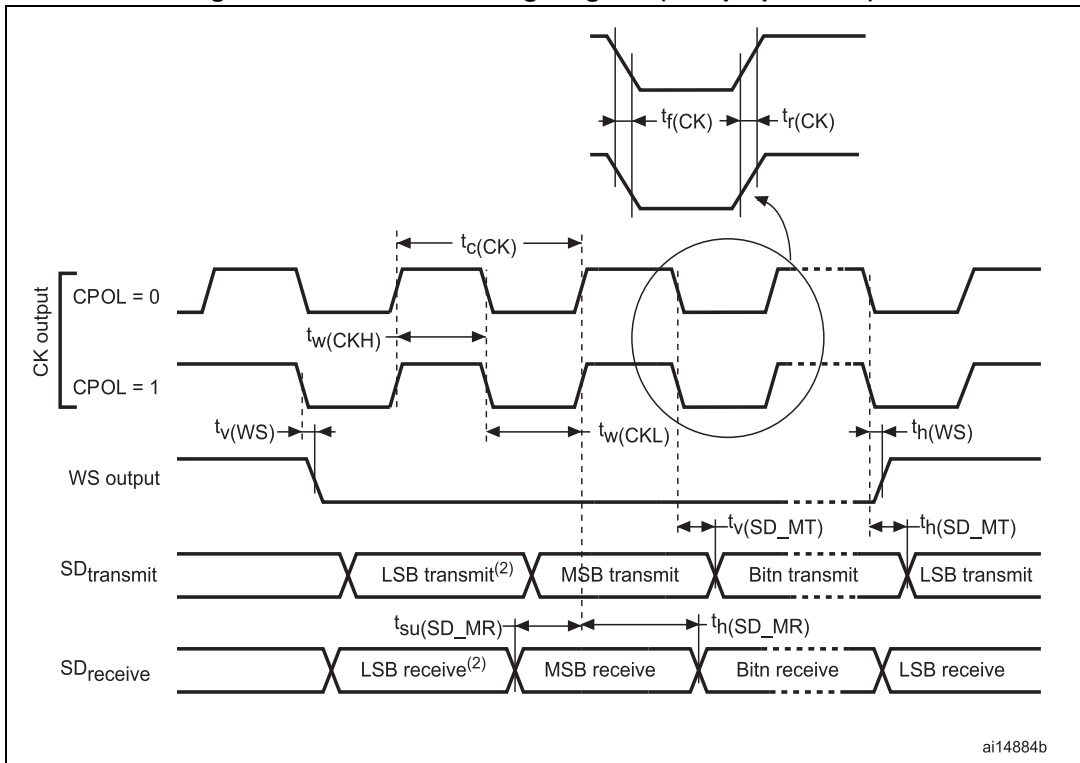
1. Evaluated by characterization - Not tested in production.

Figure 67. I<sup>2</sup>S slave timing diagram (Philips protocol)<sup>(1)</sup>



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 68. I<sup>2</sup>S master timing diagram (Philips protocol)<sup>(1)</sup>



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### USB full speed (FS) characteristics

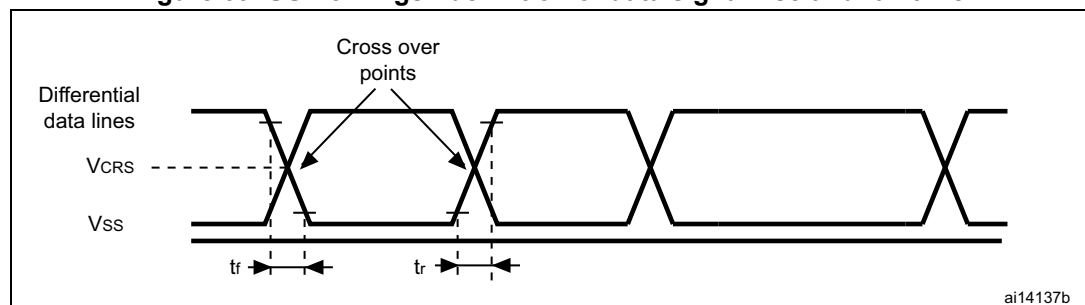
The USB interface is fully compliant with the USB specification version 2.0.

**Table 117. USB DC electrical characteristics**

| Symbol         | Parameter                                    | Conditions                                        | Min <sup>(1)</sup> | Typ  | Max <sup>(1)</sup> | Unit       |
|----------------|----------------------------------------------|---------------------------------------------------|--------------------|------|--------------------|------------|
| $V_{DD}$       | USB full speed transceiver operating voltage | -                                                 | 3.0 <sup>(2)</sup> | -    | 3.6                | V          |
| $V_{DI}^{(3)}$ | Differential input sensitivity               | Over VCM range                                    | 0.2                | -    | -                  | V          |
| $V_{CM}^{(3)}$ | Differential input common mode range         | Includes $V_{DI}$ range                           | 0.8                | -    | 2.5                |            |
| $V_{SE}^{(3)}$ | Single ended receiver input threshold        | -                                                 | 0.8                | -    | 2.0                |            |
| $V_{OL}$       | Static output level low                      | $R_L$ of 1.5 k $\Omega$ to 3.6 V <sup>(4)</sup>   | -                  | -    | 0.3                | V          |
| $V_{OH}$       | Static output level high                     | $R_L$ of 15 k $\Omega$ to $V_{SS}$ <sup>(4)</sup> | 2.8                | -    | 3.6                |            |
| $R_{PD}^{(3)}$ | Pull down resistor on PA11, PA12 (USB_DP/DM) | $V_{IN} = V_{DD}$                                 | 14.25              | -    | 24.8               | k $\Omega$ |
| $R_{PU}^{(3)}$ | Pull-up resistor on PA12 (USB_DP)            | $V_{IN} = V_{SS}$ , during idle                   | 0.9                | 1.25 | 1.575              |            |
|                | Pull-up resistor on PA12 (USB_DP)            | $V_{IN} = V_{SS}$ during reception                | 1.425              | 2.25 | 3.09               |            |

1. All the voltages are measured from the local ground potential.
2. The USB full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics, which are degraded in the 2.7-to-3.0 V  $V_{DD}$  voltage range.
3. Specified by design - Not tested in production.
4.  $R_L$  is the load connected on the USB full speed drivers.

**Figure 69. USB timings - definition of data signal rise and fall time**



**Table 118. USB startup time**

| Symbol              | Parameter                    | Max | Unit    |
|---------------------|------------------------------|-----|---------|
| $t_{STARTUP}^{(1)}$ | USB transceiver startup time | 1   | $\mu s$ |

1. Specified by design - Not tested in production.

**Table 119. USB electrical characteristics<sup>(1)</sup>**

| Driver characteristics |                                |                         |     |     |      |
|------------------------|--------------------------------|-------------------------|-----|-----|------|
| Symbol                 | Parameter                      | Conditions              | Min | Max | Unit |
| $t_{rLS}^{(2)}$        | Rise time in LS <sup>(2)</sup> | $C_L = 200$ to $600$ pF | 75  | 300 | ns   |
| $t_{fLS}^{(2)}$        | Fall time in LS <sup>(2)</sup> | $C_L = 200$ to $600$ pF | 75  | 300 |      |

Table 119. USB electrical characteristics<sup>(1)</sup> (continued)

| Driver characteristics |                                         |                       |     |     |          |
|------------------------|-----------------------------------------|-----------------------|-----|-----|----------|
| Symbol                 | Parameter                               | Conditions            | Min | Max | Unit     |
| $t_{\text{rfmLS}}$     | Rise/fall time matching in LS           | $t_r/t_f$             | 80  | 125 | %        |
| $t_{\text{rFS}}$       | Rise time in FS <sup>(2)</sup>          | $C_L = 50 \text{ pF}$ | 4   | 20  | ns       |
| $t_{\text{fFS}}$       | Fall time in FS <sup>(2)</sup>          | $C_L = 50 \text{ pF}$ | 4   | 20  |          |
| $t_{\text{rfmFS}}$     | Rise/fall time matching in FS           | $t_r/t_f$             | 90  | 111 | %        |
| $V_{\text{CRS}}$       | Output signal crossover voltage (LS/FS) | -                     | 1.3 | 2.0 | V        |
| $Z_{\text{DRV}}$       | Output driver impedance <sup>(3)</sup>  | Driving high or low   | 28  | 44  | $\Omega$ |

1. Specified by design - Not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed information, refer to USB specification - chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 120. USB BCD DC electrical characteristics<sup>(1)</sup>

| Symbol                  | Parameter                                       | Conditions | Min  | Typ | Max | Unit             |
|-------------------------|-------------------------------------------------|------------|------|-----|-----|------------------|
| $I_{\text{DD(USBBCD)}}$ | Primary detection mode consumption              | -          | -    | -   | 300 | $\mu\text{A}$    |
|                         | Secondary detection mode consumption            | -          | -    | -   | 300 |                  |
| $\text{RDAT\_LKG}$      | Data line leakage resistance                    | -          | 300  | -   | -   | $\text{k}\Omega$ |
| $\text{VDAT\_LKG}$      | Data line leakage voltage                       | -          | 0.0  | -   | 3.6 | V                |
| $\text{RDCP\_DAT}$      | Dedicated charging port resistance across D+/D- | -          | -    | -   | 200 | $\Omega$         |
| $\text{VLGC\_HI}$       | Logic high                                      | -          | 2.0  | -   | 3.6 | V                |
| $\text{VLGC\_LOW}$      | Logic low                                       | -          | -    | -   | 0.8 |                  |
| $\text{VLGC}$           | Logic threshold                                 | -          | 0.8  | -   | 2.0 |                  |
| $\text{VDAT\_REF}$      | Data detect voltage                             | -          | 0.25 | -   | 0.4 |                  |
| $\text{VDP\_SRC}$       | D+ source voltage                               | -          | 0.5  | -   | 0.7 |                  |
| $\text{VDM\_SRC}$       | D- source voltage                               | -          | 0.5  | -   | 0.7 |                  |
| $\text{IDP\_SINK}$      | D+ sink current                                 | -          | 25   | -   | 175 | $\mu\text{A}$    |
| $\text{IDM\_SINK}$      | D- sink current                                 | -          | 25   | -   | 175 |                  |

1. Specified by design - Not tested in production.

### SAI characteristics

Unless otherwise specified, the parameters given in [Table 121](#) are derived from tests performed under the ambient temperature,  $f_{\text{CLKx}}$  frequency, and  $V_{\text{DD}}$  supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to  $\text{OSPEEDRy}[1:0] = 10$
- Capacitive load  $C_L = 30 \text{ pF}$
- I/O compensation cell activated

- Measurement points are done at CMOS levels: 0.5  $V_{DD}$
- VOS level set to VOS0

Refer to [Section 5.3.15](#) for more details on the input/output alternate function characteristics (SCK, SD, WS).

**Table 121. SAI characteristics<sup>(1)</sup>**

| Symbol              | Parameter              | Conditions                                                                               | Min | Max  | Unit |
|---------------------|------------------------|------------------------------------------------------------------------------------------|-----|------|------|
| $f_{MCK}$           | SAI main clock output  | -                                                                                        | -   | 50   | MHz  |
| $f_{CK}$            | SAI clock frequency    | Master transmitter, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                         | -   | 38   |      |
|                     |                        | Master transmitter, $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                        | -   | 38   |      |
|                     |                        | Master receiver, $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                           | -   | 38   |      |
|                     |                        | Slave transmitter, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                          | -   | 34   |      |
|                     |                        | Slave transmitter, $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                         | -   | 33   |      |
|                     |                        | Slave receiver, $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                            | -   | 50   |      |
| $t_{V(FS)}$         | $F_S$ valid time       | Master mode, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                                | -   | 13   | ns   |
|                     |                        | Master mode, $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$                               | -   | 13   |      |
| $t_{su(FS)}$        | $F_S$ setup time       | Slave mode                                                                               | 3   | -    |      |
| $t_{h(FS)}$         | $F_S$ hold time        | Master mode                                                                              | 5   | -    |      |
|                     |                        | Slave mode                                                                               | 2   | -    |      |
| $t_{su(SD\_A\_MR)}$ | Data input setup time  | Master receiver                                                                          | 4   | -    |      |
| $t_{su(SD\_B\_SR)}$ |                        | Slave receiver                                                                           | 3.5 | -    |      |
| $t_{h(SD\_A\_MR)}$  | Data input hold time   | Master receiver                                                                          | 1.5 | -    |      |
| $t_{h(SD\_B\_SR)}$  |                        | Slave receiver                                                                           | 0.5 | -    |      |
| $t_{V(SD\_B\_ST)}$  | Data output valid time | Slave transmitter (after enable edge),<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$   | -   | 14.5 |      |
|                     |                        | Slave transmitter (after enable edge),<br>$1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  | -   | 15   |      |
| $t_{h(SD\_B\_ST)}$  | Data output hold time  | Slave transmitter (after enable edge)                                                    | 7   | -    |      |
| $t_{V(SD\_A\_MT)}$  | Data output valid time | Master transmitter (after enable edge),<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  | -   | 13   |      |
|                     |                        | Master transmitter (after enable edge),<br>$1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | -   | 13   |      |
| $t_{h(SD\_A\_MT)}$  | Data output hold time  | Master transmitter (after enable edge)                                                   | 5.5 | -    |      |

1. Evaluated by characterization - Not tested in production.

Figure 70. SAI master timing waveforms

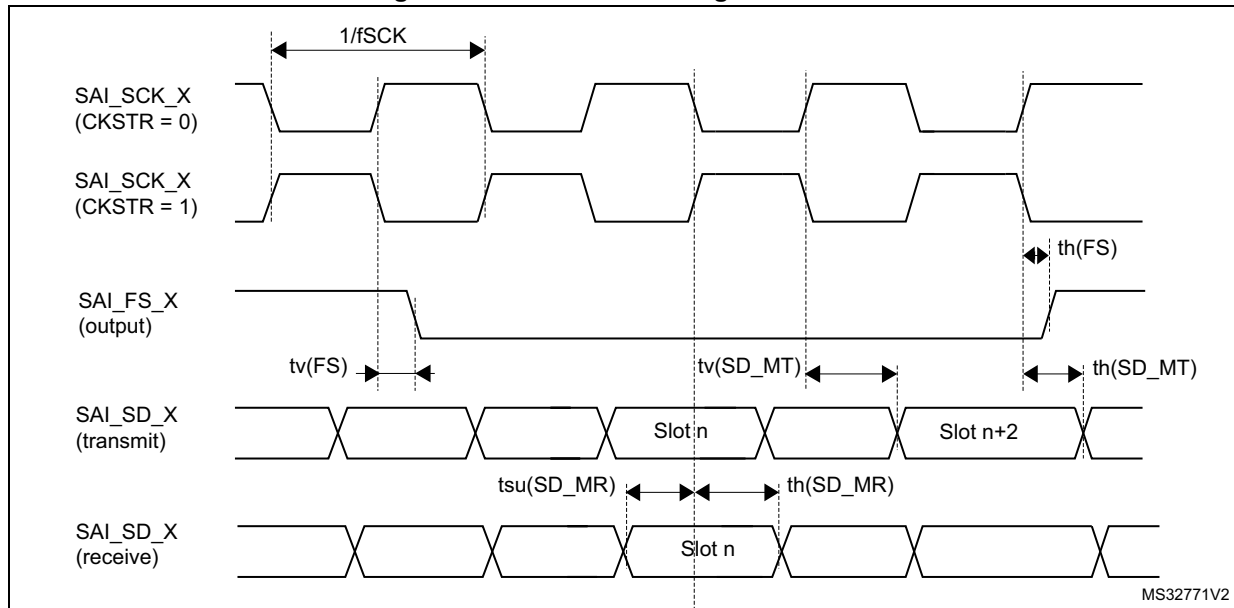
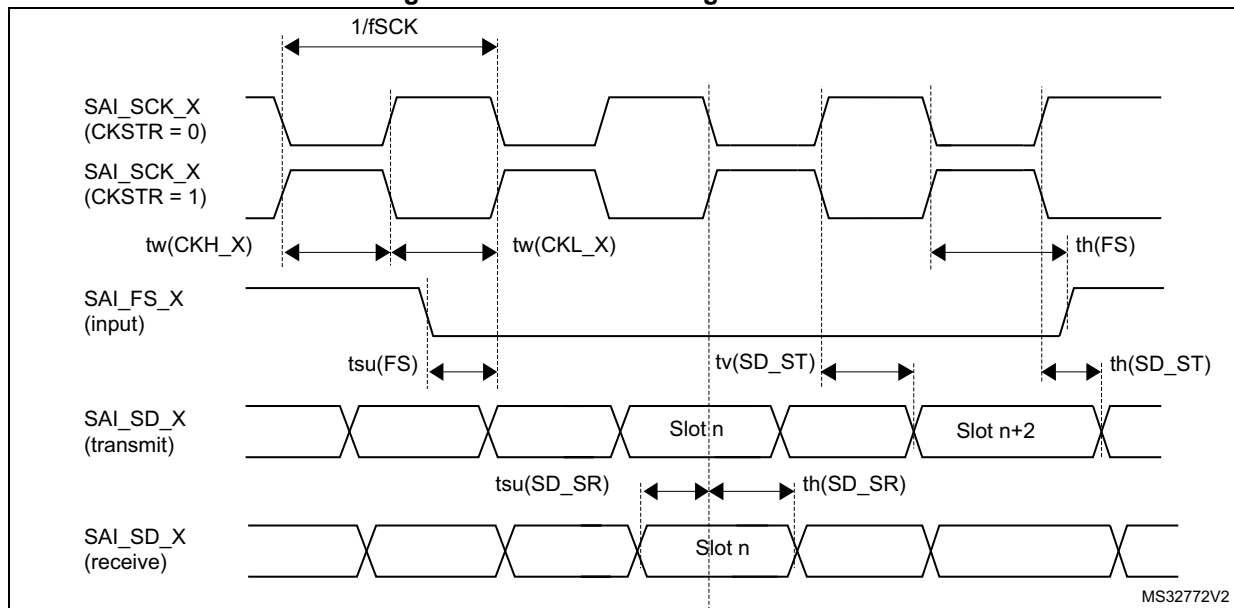


Figure 71. SAI slave timing waveforms



### SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in [Table 122](#) and [Table 123](#) are derived from tests performed under the ambient temperature,  $f_{PCLKx}$  frequency, and  $V_{DD}$  supply voltage summarized in [Table 20](#), with the following configuration:

- Output speed is set to  $OSPEEDRy[1:0] = 11$
- Capacitive load  $C_L = 30$  pF
- Measurement points are done at CMOS levels:  $0.5 V_{DD}$
- I/O compensation cell activated
- HSLV activated when  $V_{DD} \leq 2.7$  V

Refer to [Section 5.3.15](#) for more details on the input/output characteristics.

**Table 122. Dynamic characteristics: SD/MMC,  $V_{DD} = 2.7$  to  $3.6$  V<sup>(1)</sup>**

| Symbol                                                                                                         | Parameter                             | Conditions               | Min | Typ | Max                                  | Unit |
|----------------------------------------------------------------------------------------------------------------|---------------------------------------|--------------------------|-----|-----|--------------------------------------|------|
| f <sub>PP</sub>                                                                                                | Clock frequency in data transfer mode | -                        | 0   | -   | 130 <sup>(2)</sup> /6 <sup>(3)</sup> | MHz  |
| t <sub>W(CKL)</sub>                                                                                            | Clock low time                        | f <sub>PP</sub> = 52 MHz | 8.5 | 9.5 | -                                    | ns   |
| t <sub>W(CKH)</sub>                                                                                            | Clock high time                       |                          | 8.5 | 9.5 | -                                    |      |
| CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR <sup>(4)</sup> /DDR <sup>(4)</sup> mode  |                                       |                          |     |     |                                      |      |
| t <sub>ISU</sub>                                                                                               | Input setup time HS                   | -                        | 3   | -   | -                                    | ns   |
| t <sub>IH</sub>                                                                                                | Input hold time HS                    | -                        | 1   | -   | -                                    |      |
| t <sub>IDW</sub> <sup>(5)</sup>                                                                                | Input valid window (variable window)  | -                        | 4.5 | -   | -                                    |      |
| CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR <sup>(4)</sup> /DDR <sup>(4)</sup> mode |                                       |                          |     |     |                                      |      |
| t <sub>OV</sub>                                                                                                | Output valid time HS                  | -                        | -   | 5   | 5.5/38 <sup>(3)</sup>                | ns   |
| t <sub>OH</sub>                                                                                                | Output hold time HS                   | -                        | 3   | -   | -                                    |      |
| CMD, D inputs (referenced to CK) in SD default mode                                                            |                                       |                          |     |     |                                      |      |
| t <sub>ISUD</sub>                                                                                              | Input setup time SD                   | -                        | 2.5 |     | -                                    | ns   |
| t <sub>IHD</sub>                                                                                               | Input hold time SD                    | -                        | 1.5 |     | -                                    |      |
| CMD, D outputs (referenced to CK) in SD default mode                                                           |                                       |                          |     |     |                                      |      |
| t <sub>OVD</sub>                                                                                               | Output valid default time SD          | -                        | -   | 0.5 | 1/33 <sup>(3)</sup>                  | ns   |
| t <sub>OHD</sub>                                                                                               | Output hold default time SD           | -                        | 0   | -   | -                                    |      |

1. Evaluated by characterization - Not tested in production.
2.  $C_L$  applied is 20 pF.
3. When using PB13 and PB14.
4. For SD 1.8 V support, an external voltage converter is needed.
5. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

**Table 123. Dynamic characteristics: eMMC,  $V_{DD} = 1.71$  to  $1.9$  V<sup>(1)</sup>**

| Symbol                                        | Parameter                             | Conditions              | Min | Typ | Max                                  | Unit |
|-----------------------------------------------|---------------------------------------|-------------------------|-----|-----|--------------------------------------|------|
| f <sub>PP</sub>                               | Clock frequency in data transfer mode | -                       | 0   | -   | 110 <sup>(2)</sup> /6 <sup>(3)</sup> | MHz  |
| t <sub>W(CKL)</sub>                           | Clock low time                        | f <sub>PP</sub> =52 MHz | 8.5 | 9.5 | -                                    | ns   |
| t <sub>W(CKH)</sub>                           | Clock high time                       |                         | 8.5 | 9.5 | -                                    |      |
| CMD, D inputs (referenced to CK) in eMMC mode |                                       |                         |     |     |                                      |      |
| t <sub>ISU</sub>                              | Input setup time HS                   | -                       | 1.5 | -   | -                                    | ns   |
| t <sub>IH</sub>                               | Input hold time HS                    | -                       | 1.5 | -   | -                                    |      |
| t <sub>IDW</sub> <sup>(4)</sup>               | Input valid window (variable window)  | -                       | 4   | -   | -                                    |      |

Table 123. Dynamic characteristics: eMMC,  $V_{DD} = 1.71$  to  $1.9\text{ V}^{(1)}$  (continued)

| Symbol                                                | Parameter            | Conditions | Min | Typ | Max          | Unit |
|-------------------------------------------------------|----------------------|------------|-----|-----|--------------|------|
| <b>CMD, D outputs (referenced to CK) in eMMC mode</b> |                      |            |     |     |              |      |
| $t_{OV}$                                              | Output valid time HS | -          | -   | 5.5 | $6/75^{(3)}$ | ns   |
| $t_{OH}$                                              | Output hold time HS  | -          | 3   | -   | -            |      |

1. Evaluated by characterization - Not tested in production.
2.  $C_L = 20\text{ pF}$ .
3. When using PB13 and PB14.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 72. SDIO high-speed/eMMC timing

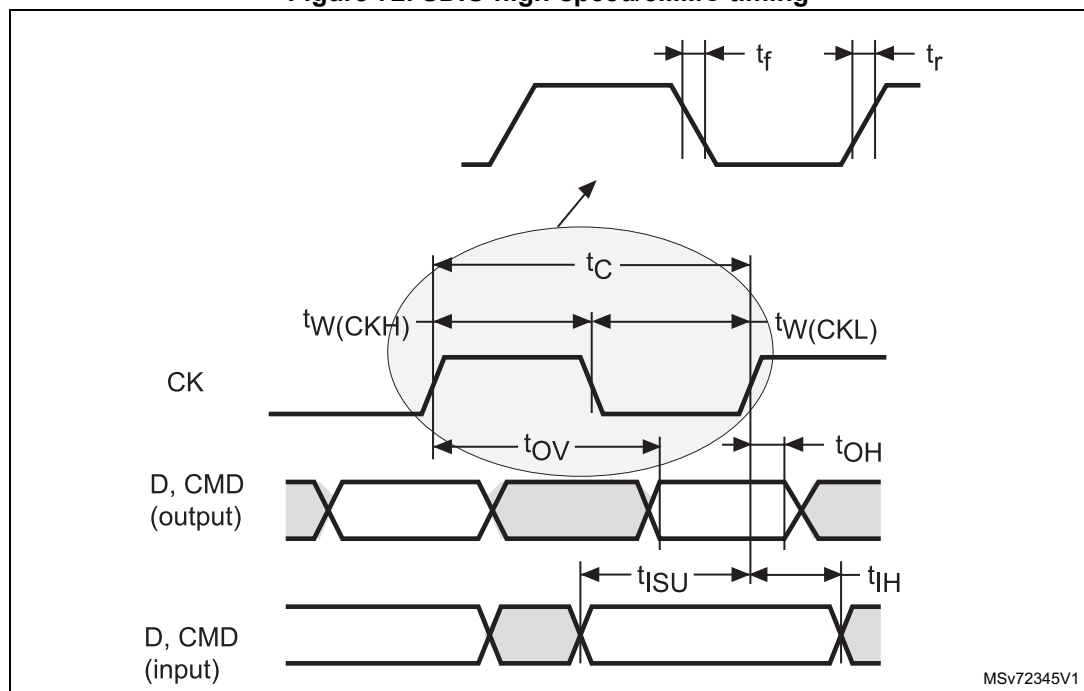


Figure 73. SD default speed timings

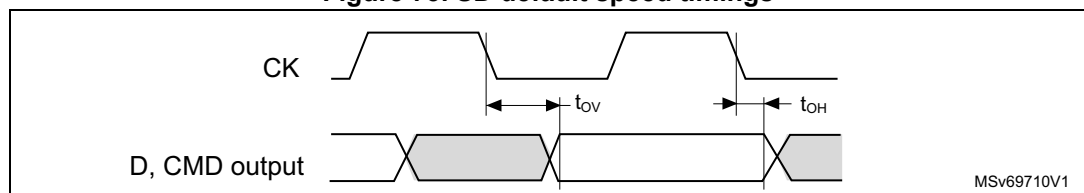
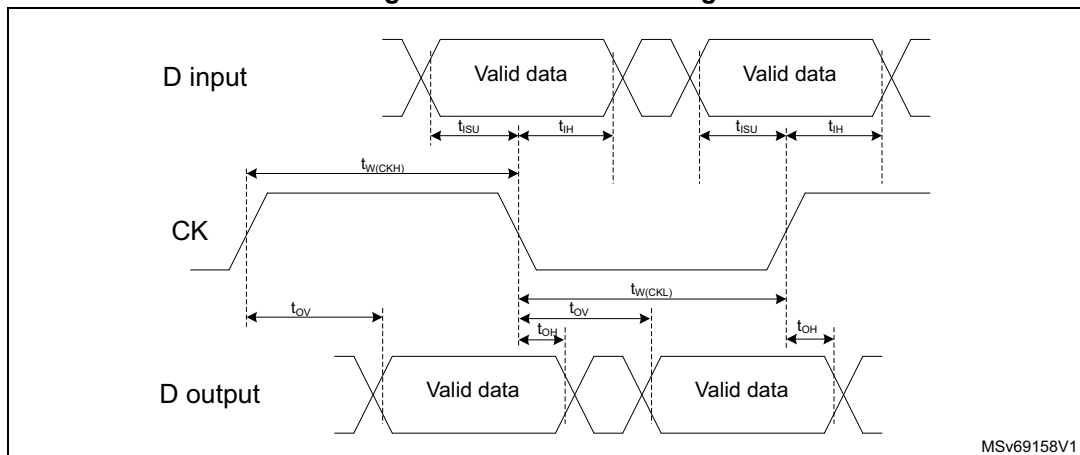


Figure 74. DDR mode timings



### Ethernet interface characteristics

Unless otherwise specified, the parameters given in [Table 124](#), [Table 125](#), and [Table 126](#) are derived from tests performed under the ambient temperature,  $f_{\text{RCC\_C\_CK}}$  frequency, and  $V_{\text{DD}}$  supply voltage conditions summarized in [Table 20](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load  $C_L = 20 \text{ pF}$
- Measurement points are done at CMOS levels:  $0.5 V_{\text{DD}}$
- I/O compensation cell activated
- HSLV activated when  $V_{\text{DD}} \leq 2.5 \text{ V}$

Refer to [Section 5.3.15](#) for more details on the input/output characteristics.

**Table 124. Dynamic characteristics: Ethernet MAC signals for SMI <sup>(1)</sup>**

| Symbol                | Parameter                | Min  | Typ | Max | Unit |
|-----------------------|--------------------------|------|-----|-----|------|
| $t_{\text{MDC}}$      | MDC cycle time (2.5 MHz) | 400  | 400 | 403 | ns   |
| $T_{\text{d(MDIO)}}$  | Write data valid time    | 0    | 0.5 | 1   |      |
| $t_{\text{su(MDIO)}}$ | Read data setup time     | 12.5 | -   | -   |      |
| $t_{\text{h(MDIO)}}$  | Read data hold time      | 0    | -   | -   |      |

1. Evaluated by characterization - Not tested in production.

**Table 125. Dynamic characteristics: Ethernet MAC signals for RMII <sup>(1)</sup>**

| Symbol               | Parameter                        | Min | Typ | Max  | Unit |
|----------------------|----------------------------------|-----|-----|------|------|
| $t_{\text{su(RXD)}}$ | Receive data setup time          | 3   | -   | -    | ns   |
| $t_{\text{ih(RXD)}}$ | Receive data hold time           | 1   | -   | -    |      |
| $t_{\text{su(CRS)}}$ | Carrier sense setup time         | 2   | -   | -    |      |
| $t_{\text{ih(CRS)}}$ | Carrier sense hold time          | 1   | -   | -    |      |
| $t_{\text{d(TXEN)}}$ | Transmit enable valid delay time | 7.5 | 9.5 | 15   |      |
| $t_{\text{d(TXD)}}$  | Transmit data valid delay time   | 7.5 | 10  | 15.5 |      |

1. Evaluated by characterization - Not tested in production.

**Table 126. Dynamic characteristics: Ethernet MAC signals for MII <sup>(1)</sup>**

| Symbol        | Parameter                        | Min | Typ  | Max  | Unit |
|---------------|----------------------------------|-----|------|------|------|
| $t_{su}(RXD)$ | Receive data setup time          | 3   | -    | -    | ns   |
| $t_{ih}(RXD)$ | Receive data hold time           | 1.5 | -    | -    |      |
| $t_{su}(DV)$  | Data valid setup time            | 2   | -    | -    |      |
| $t_{ih}(DV)$  | Data valid hold time             | 1   | -    | -    |      |
| $t_{su}(ER)$  | Error setup time                 | 3   | -    | -    |      |
| $t_{ih}(ER)$  | Error hold time                  | 1   | -    | -    |      |
| $t_d(TXEN)$   | Transmit enable valid delay time | 7.5 | 10   | 16   |      |
| $t_d(TXD)$    | Transmit data valid delay time   | 8   | 10.5 | 16.5 |      |

1. Evaluated by characterization - Not tested in production.

**Figure 75. Ethernet RMII timing diagram**

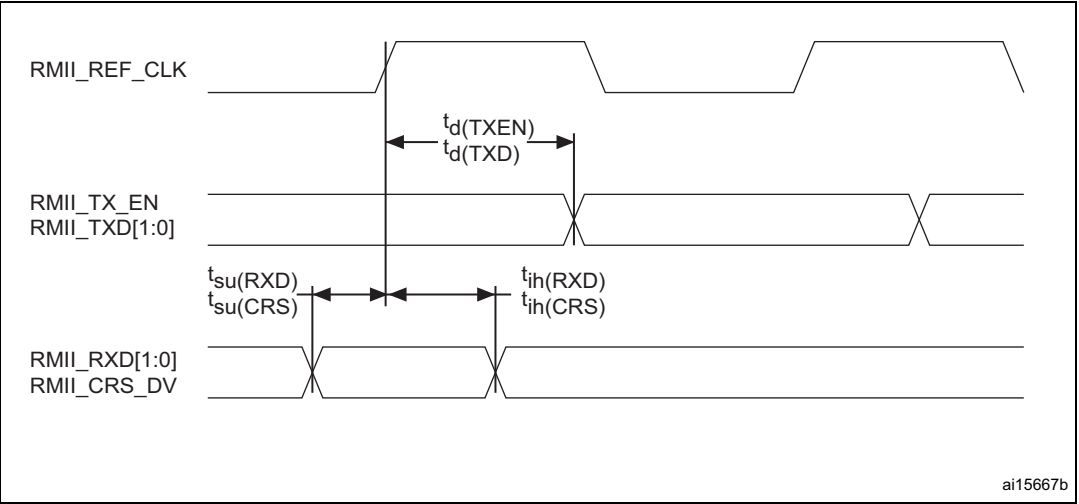


Figure 76. Ethernet MII timing diagram

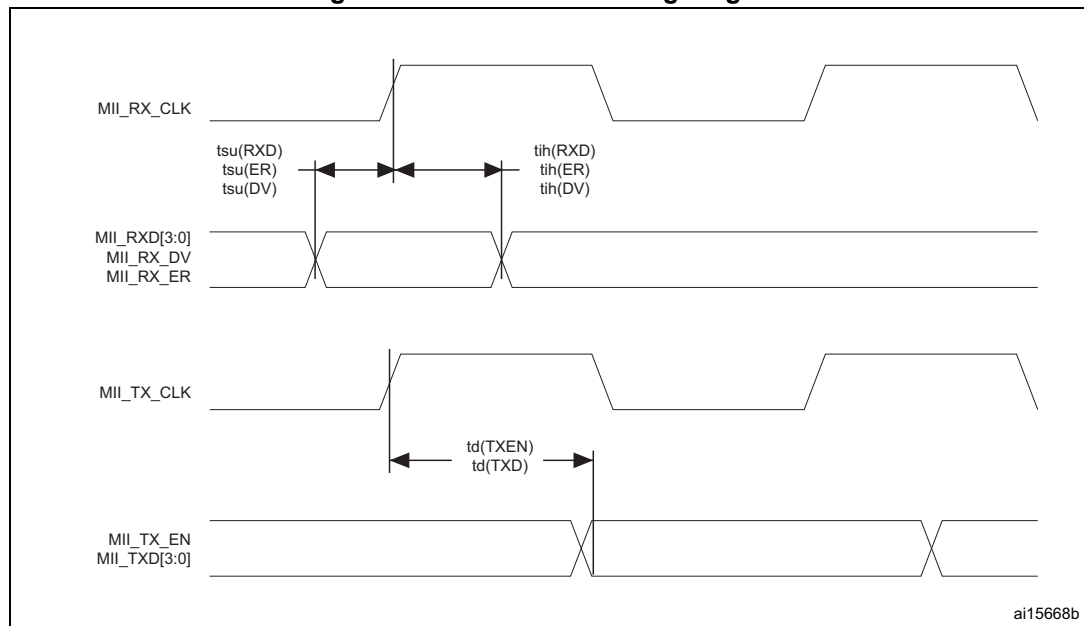
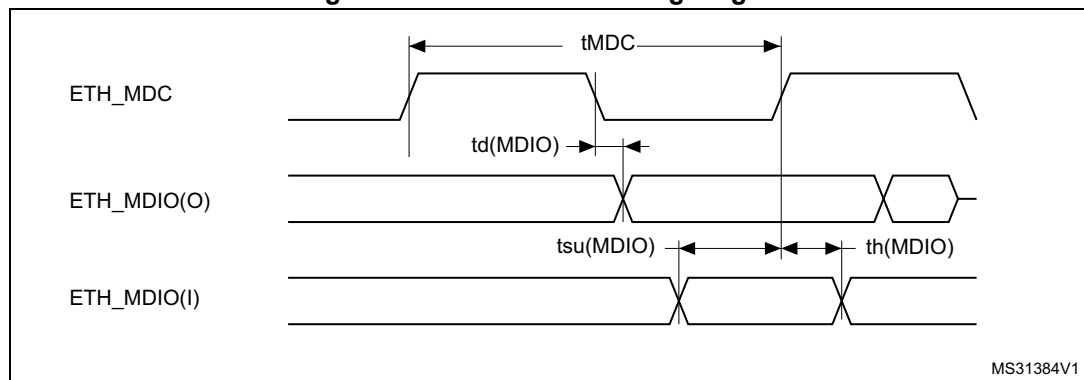


Figure 77. Ethernet SMI timing diagram



### JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in [Table 127](#) and [Table 128](#) for JTAG/SWD are derived from tests performed under the ambient temperature,  $f_{\text{rcc\_c\_ck}}$  frequency, and  $V_{\text{DD}}$  supply voltage summarized in [Table 20](#), with the following configuration:

- Output speed is set to  $\text{OSPEEDRy}[1:0] = 11$
- Capacitive load  $C_L = 30 \text{ pF}$
- HSLV activated when  $V_{\text{DD}} \leq 2.7 \text{ V}$
- Measurement points are done at CMOS levels:  $0.5 V_{\text{DD}}$

Refer to [Section 5.3.15](#) for more details on the input/output characteristics.

Table 127. Dynamic JTAG characteristics

| Symbol            | Parameter                | Conditions                              | Min | Typ | Max | Unit |
|-------------------|--------------------------|-----------------------------------------|-----|-----|-----|------|
| $F_{TCK}$         | $T_{CK}$ clock frequency | $2.7\text{ V} < V_{DD} < 3.6\text{ V}$  | -   | -   | 50  | MHz  |
| $1/t_{c(TCK)}$    |                          | $1.71\text{ V} < V_{DD} < 3.6\text{ V}$ | -   | -   | 45  |      |
| $t_{i_{su}(TMS)}$ | TMS input setup time     | -                                       | 2   | -   | -   | ns   |
| $t_{i_{h}(TMS)}$  | TMS input hold time      | -                                       | 1.5 | -   | -   |      |
| $t_{i_{su}(TDI)}$ | TDI input setup time     | -                                       | 1.5 | -   | -   |      |
| $t_{i_{h}(TDI)}$  | TDI input hold time      | -                                       | 1.5 | -   | -   |      |
| $t_{ov}(TDO)$     | TDO output valid time    | $2.7\text{ V} < V_{DD} < 3.6\text{ V}$  | -   | 8   | 10  |      |
|                   |                          | $1.71 < V_{DD} < 3.6\text{ V}$          | -   | 8   | 11  |      |
| $t_{oh}(TDO)$     | TDO output hold time     | -                                       | 6.5 | -   | -   |      |

Table 128. Dynamic SWD characteristics

| Symbol              | Parameter               | Conditions                              | Min | Typ  | Max  | Unit |
|---------------------|-------------------------|-----------------------------------------|-----|------|------|------|
| $F_{SWCLK}$         | SWCLK clock frequency   | $2.7\text{ V} < V_{DD} < 3.6\text{ V}$  | -   | -    | 80   | MHz  |
| $1/t_{c(SWCLK)}$    |                         | $1.71\text{ V} < V_{DD} < 3.6\text{ V}$ | -   | -    | 71   |      |
| $t_{i_{su}(SWDIO)}$ | SWDIO input setup time  | -                                       | 1.5 | -    | -    | ns   |
| $t_{i_{h}(SWDIO)}$  | SWDIO input hold time   | -                                       | 1.5 | -    | -    |      |
| $t_{ov}(SWDIO)$     | SWDIO output valid time | $2.7\text{ V} < V_{DD} < 3.6\text{ V}$  | -   | 10.5 | 12.5 |      |
|                     |                         | $1.71\text{ V} < V_{DD} < 3.6\text{ V}$ | -   | 10.5 | 14.0 |      |
| $t_{oh}(SWDIO)$     | SWDIO output hold time  | -                                       | 8.5 | -    | -    |      |

Figure 78. JTAG timing diagram

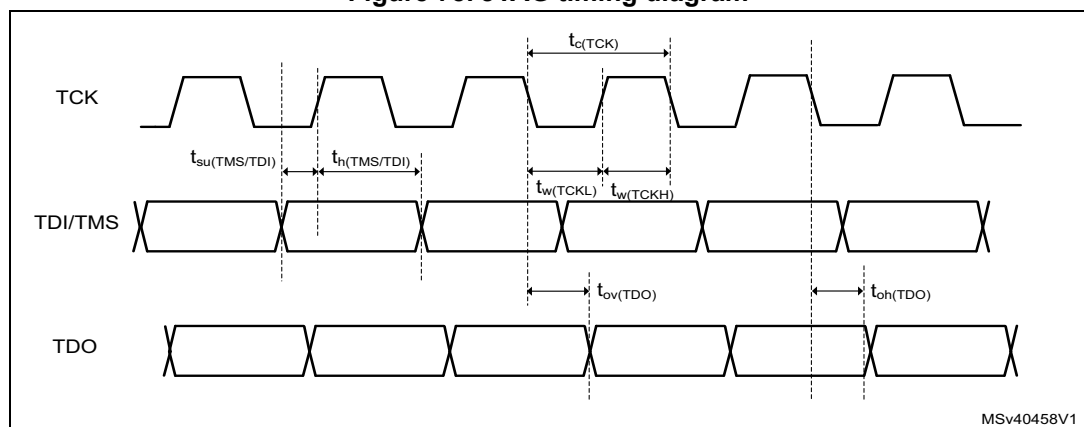
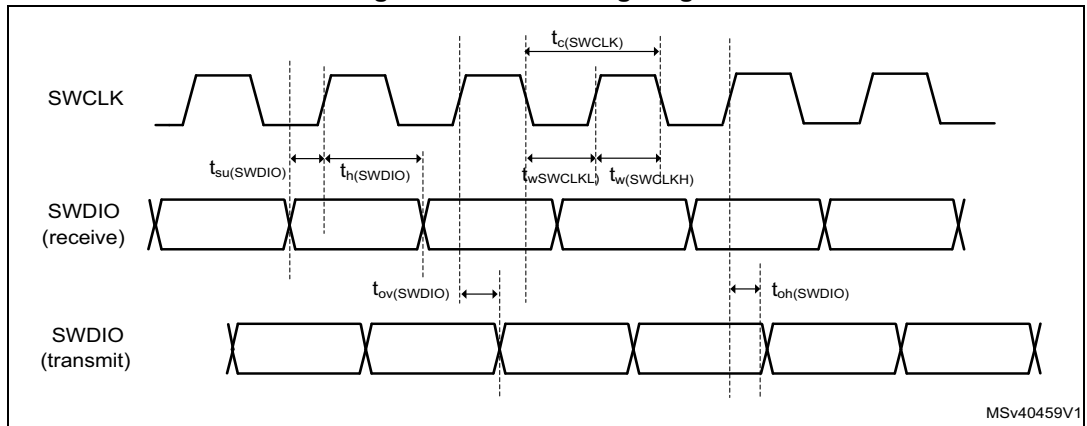


Figure 79. SWD timing diagram



## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 6.1 Device marking

Refer to “*Reference device marking schematics for STM32 microcontrollers and microprocessors*” (TN1433), available on [www.st.com](http://www.st.com), for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

## 6.2 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

*Note:* See list of notes in the notes section.

**Figure 80. LQFP64 - Outline<sup>(15)</sup>**

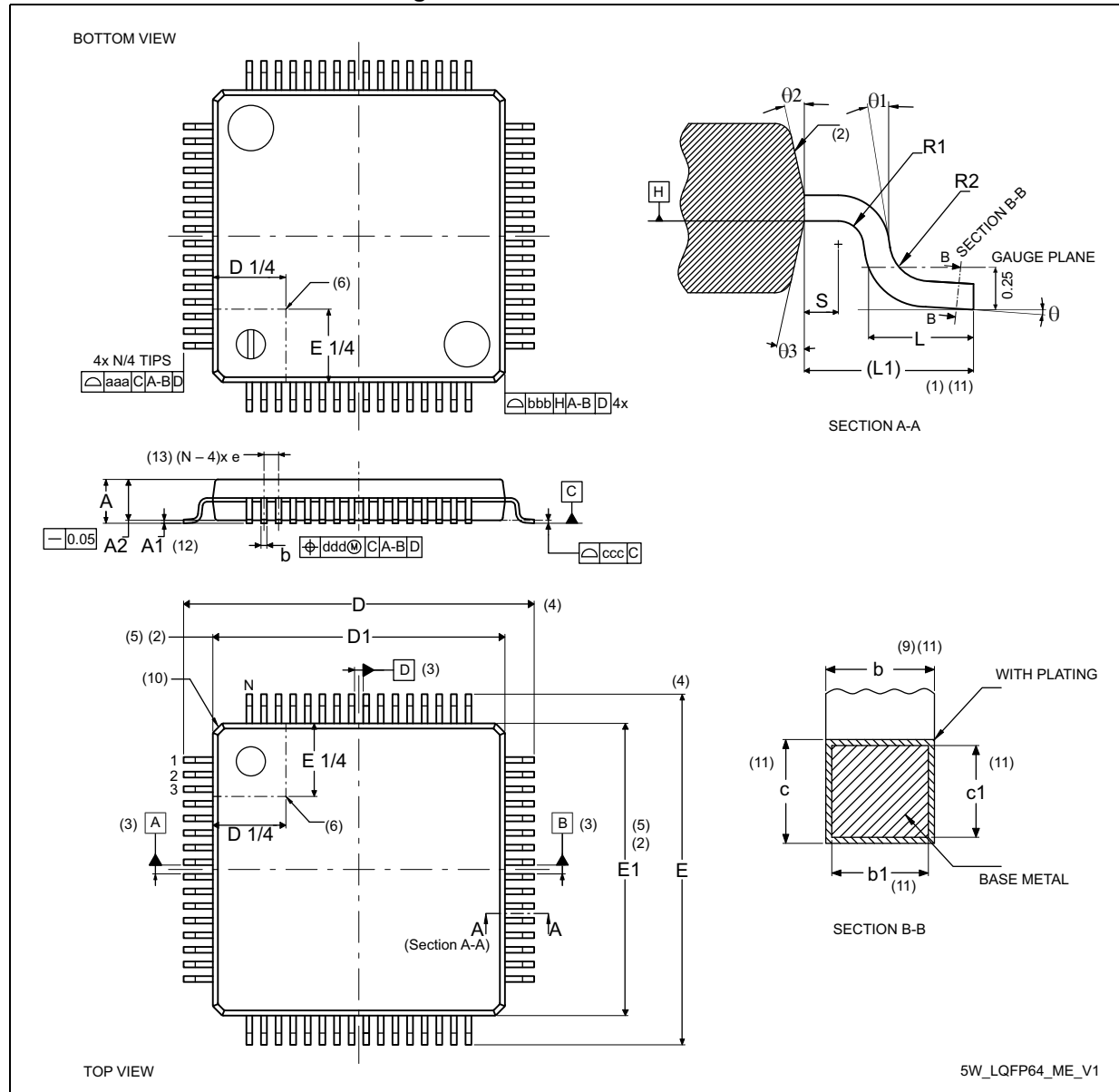
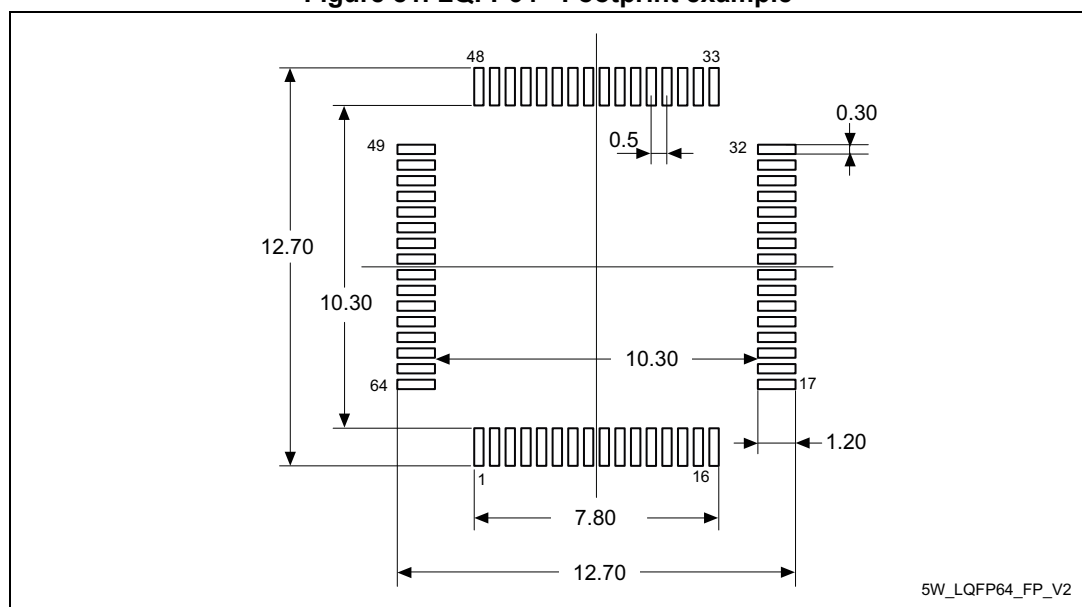


Table 129. LQFP64 - Mechanical data

| Symbol               | millimeters |      |      | inches <sup>(14)</sup> |        |        |
|----------------------|-------------|------|------|------------------------|--------|--------|
|                      | Min         | Typ  | Max  | Min                    | Typ    | Max    |
| A                    | -           | -    | 1.60 | -                      | -      | 0.0630 |
| A1 <sup>(12)</sup>   | 0.05        | -    | 0.15 | 0.0020                 | -      | 0.0059 |
| A2                   | 1.35        | 1.40 | 1.45 | 0.0531                 | 0.0551 | 0.0570 |
| b <sup>(9)(11)</sup> | 0.17        | 0.22 | 0.27 | 0.0067                 | 0.0087 | 0.0106 |
| b1 <sup>(11)</sup>   | 0.17        | 0.20 | 0.23 | 0.0067                 | 0.0079 | 0.0091 |
| c <sup>(11)</sup>    | 0.09        | -    | 0.20 | 0.0035                 | -      | 0.0079 |
| c1 <sup>(11)</sup>   | 0.09        | -    | 0.16 | 0.0035                 | -      | 0.0063 |
| D <sup>(4)</sup>     | 12.00 BSC   |      |      | 0.4724 BSC             |        |        |
| D1 <sup>(2)(5)</sup> | 10.00 BSC   |      |      | 0.3937 BSC             |        |        |
| E <sup>(4)</sup>     | 12.00 BSC   |      |      | 0.4724 BSC             |        |        |
| E1 <sup>(2)(5)</sup> | 10.00 BSC   |      |      | 0.3937 BSC             |        |        |
| e                    | 0.50 BSC    |      |      | 0.1970 BSC             |        |        |
| L                    | 0.45        | 0.60 | 0.75 | 0.0177                 | 0.0236 | 0.0295 |
| L1                   | 1.00 REF    |      |      | 0.0394 REF             |        |        |
| N <sup>(13)</sup>    | 64          |      |      |                        |        |        |
| θ                    | 0°          | 3.5° | 7°   | 0°                     | 3.5°   | 7°     |
| θ1                   | 0°          | -    | -    | 0°                     | -      | -      |
| θ2                   | 10°         | 12°  | 14°  | 10°                    | 12°    | 14°    |
| θ3                   | 10°         | 12°  | 14°  | 10°                    | 12°    | 14°    |
| R1                   | 0.08        | -    | -    | 0.0031                 | -      | -      |
| R2                   | 0.08        | -    | 0.20 | 0.0031                 | -      | 0.0079 |
| S                    | 0.20        | -    | -    | 0.0079                 | -      | -      |
| aaa <sup>(1)</sup>   | 0.20        |      |      | 0.0079                 |        |        |
| bbb <sup>(1)</sup>   | 0.20        |      |      | 0.0079                 |        |        |
| ccc <sup>(1)</sup>   | 0.08        |      |      | 0.0031                 |        |        |
| ddd <sup>(1)</sup>   | 0.08        |      |      | 0.0031                 |        |        |

**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. "N" is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

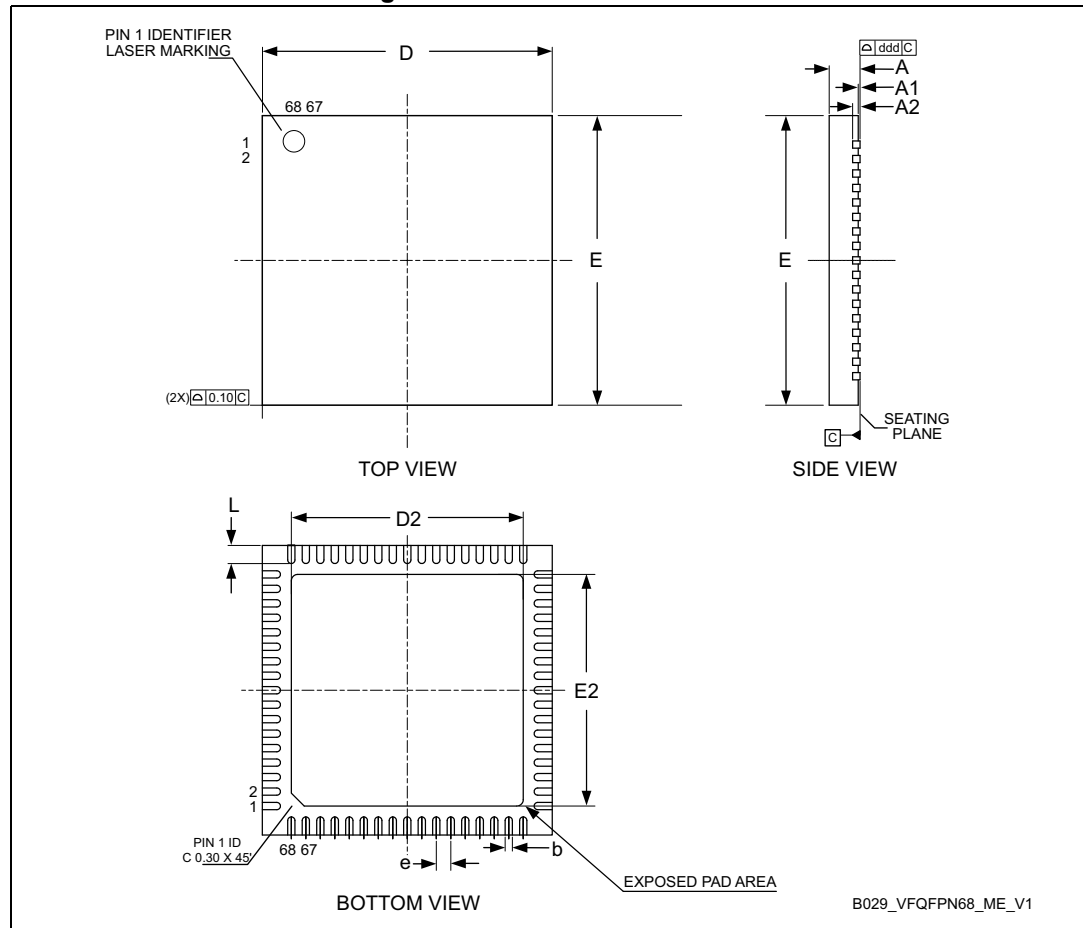
**Figure 81. LQFP64 - Footprint example**

1. Dimensions are expressed in millimeters.

### 6.3 VFQFPN68 package information (B029)

This VFQFPN is a 68 pins, 8 x 8 mm, 0.4 mm pitch, very thin fine pitch quad flat package.

**Figure 82. VFQFPN68 - Outline**



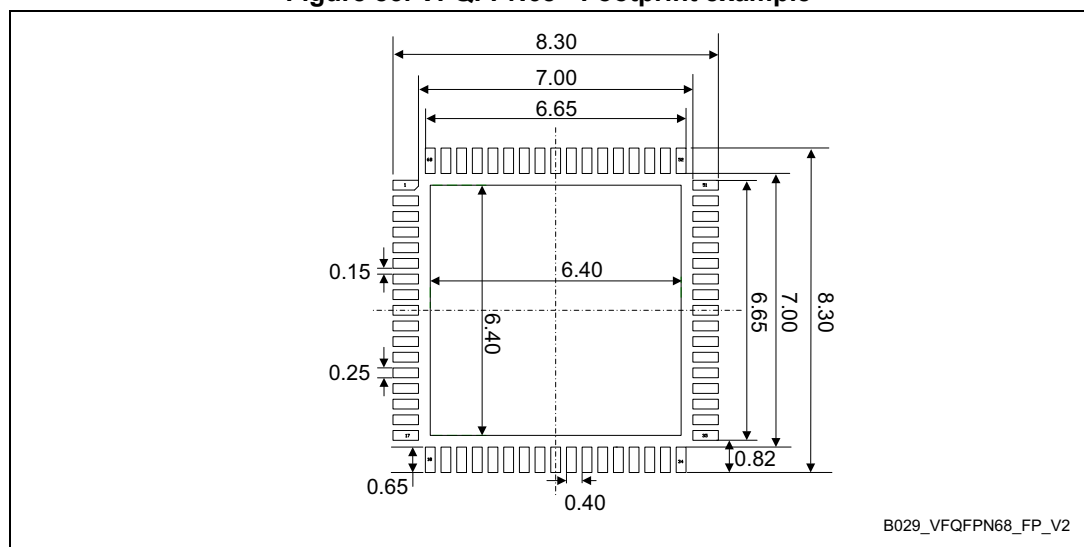
1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead. Sawed version. Very thin profile:  $0.80 < A \leq 1.00\text{mm}$ .
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

Table 130. VFQFPN68 - Mechanical data

| Symbol | millimeters |      |      | inches <sup>(1)</sup> |        |        |
|--------|-------------|------|------|-----------------------|--------|--------|
|        | Min         | Typ  | Max  | Min                   | Typ    | Max    |
| A      | 0.80        | 0.90 | 1.00 | 0.0315                | 0.0354 | 0.0394 |
| A1     | 0           | 0.02 | 0.05 | 0                     | 0.0008 | 0.0020 |
| A3     | -           | 0.20 | -    | -                     | 0.0008 | -      |
| b      | 0.15        | 0.20 | 0.25 | 0.0059                | 0.0079 | 0.0098 |
| D      | 7.85        | 8.00 | 8.15 | 0.3091                | 0.3150 | 0.3209 |
| D2     | 6.30        | 6.40 | 6.50 | 0.2480                | 0.2520 | 0.2559 |
| E      | 7.85        | 8.00 | 8.15 | 0.3091                | 0.3150 | 0.3209 |
| E2     | 6.30        | 6.40 | 6.50 | 0.2480                | 0.2520 | 0.2559 |
| e      | -           | 0.40 | -    | -                     | 0.0157 | -      |
| L      | 0.40        | 0.50 | 0.60 | 0.0157                | 0.0197 | 0.0236 |
| ddd    | -           | -    | 0.08 | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 83. VFQFPN68 - Footprint example

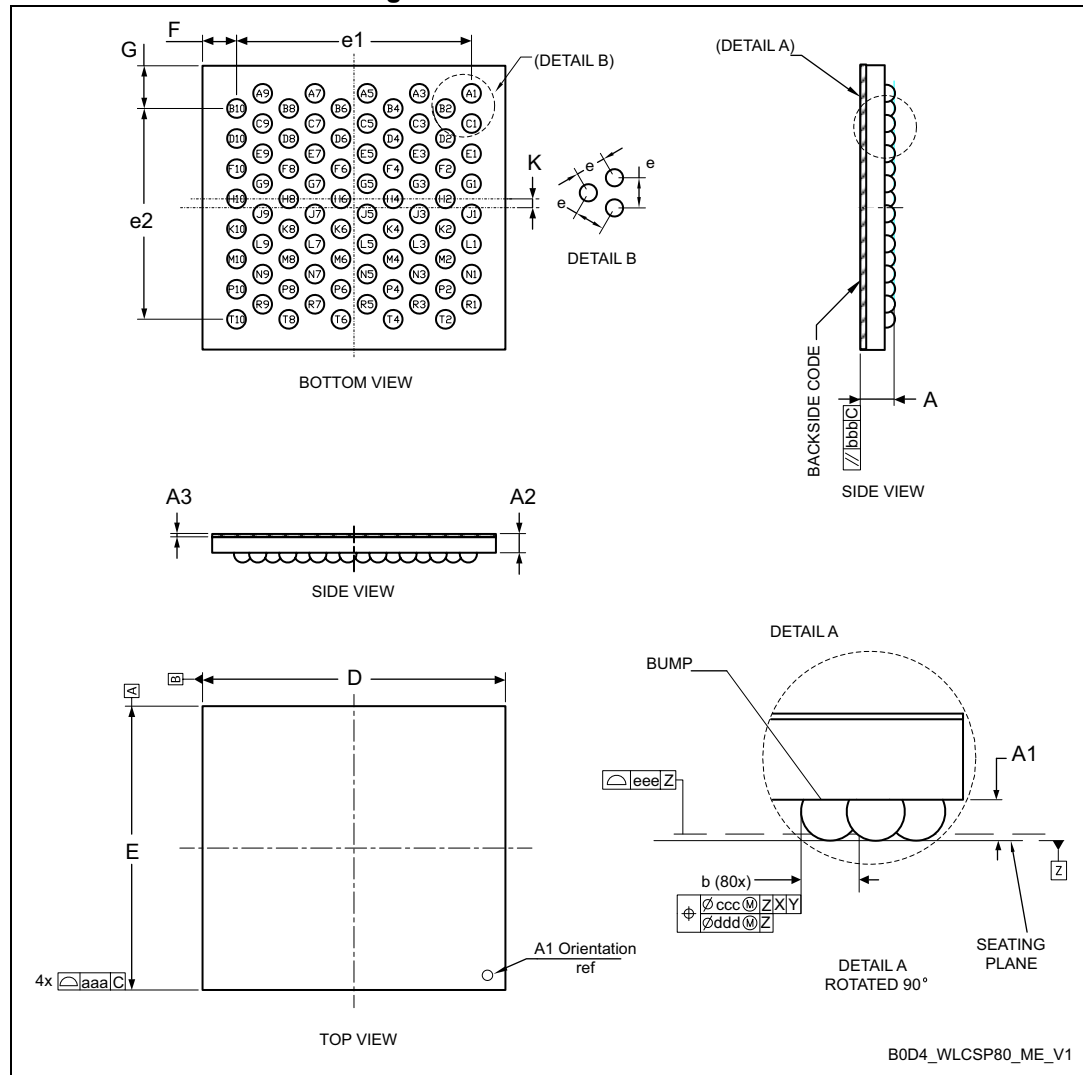


1. Dimensions are expressed in millimeters.

## 6.4 WLCSP80 package information (B0D4)

This WLCSP is a 80 ball, 3.50 x 3.27 mm, 0.35 mm pitch, wafer level chip scale package.

Figure 84. WLCSP80 - Outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.

Table 131. WLCSP80 - Mechanical data

| Symbol             | millimeters |        |      | inches <sup>(1)</sup> |        |        |
|--------------------|-------------|--------|------|-----------------------|--------|--------|
|                    | Min         | Typ    | Max  | Min                   | Typ    | Max    |
| A <sup>(2)</sup>   | -           | -      | 0.58 | -                     | -      | 0.228  |
| A1                 | -           | 0.17   | -    | -                     | 0.0067 | -      |
| A2                 | -           | 0.38   | -    | -                     | 0.0150 | -      |
| A3 <sup>(3)</sup>  | -           | 0.025  | -    | -                     | 0.0098 | -      |
| b                  | 0.22        | 0.24   | 0.27 | 0.0087                | 0.0094 | 0.0106 |
| D                  | 3.47        | 3.50   | 3.52 | 0.1366                | 0.1378 | 0.1386 |
| E                  | 3.25        | 3.27   | 3.30 | 0.1279                | 0.1287 | 0.1299 |
| e                  | -           | 0.35   | -    | -                     | 0.138  | -      |
| e1                 | -           | 2.73   | -    | -                     | 0.1075 | -      |
| e2                 | -           | 2.45   | -    | -                     | 0.0964 | -      |
| F <sup>(4)</sup>   | -           | 0.384  | -    | -                     | 0.0151 | -      |
| G <sup>(4)</sup>   | -           | 0.484  | -    | -                     | 0.0190 | -      |
| H                  | -           | 0.1025 | -    | -                     | 0.0040 | -      |
| aaa                | -           | -      | 0.10 | -                     | -      | 0.0039 |
| bbb                | -           | -      | 0.10 | -                     | -      | 0.0039 |
| ccc <sup>(5)</sup> | -           | -      | 0.10 | -                     | -      | 0.0039 |
| ddd <sup>(6)</sup> | -           | -      | 0.05 | -                     | -      | 0.0020 |
| eee                | -           | -      | 0.05 | -                     | -      | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Calculated dimensions are rounded to the 3rd decimal place
5. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.
6. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone ddd perpendicular to datum Z and located on true position as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone. Each tolerance zone ddd in the array is contained entirely in the respective zone ccc above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 85. WLCSP80 - Footprint example

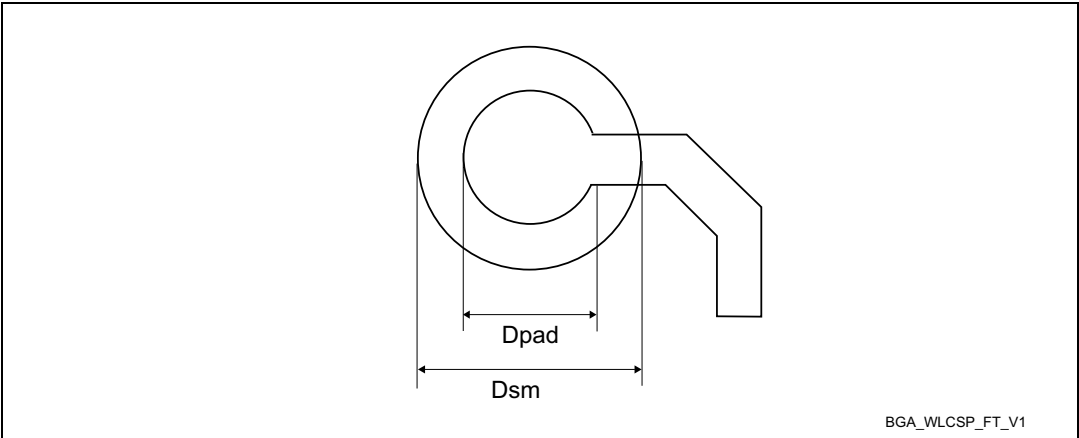


Table 132. WLCSP80 - Example of PCB design rules

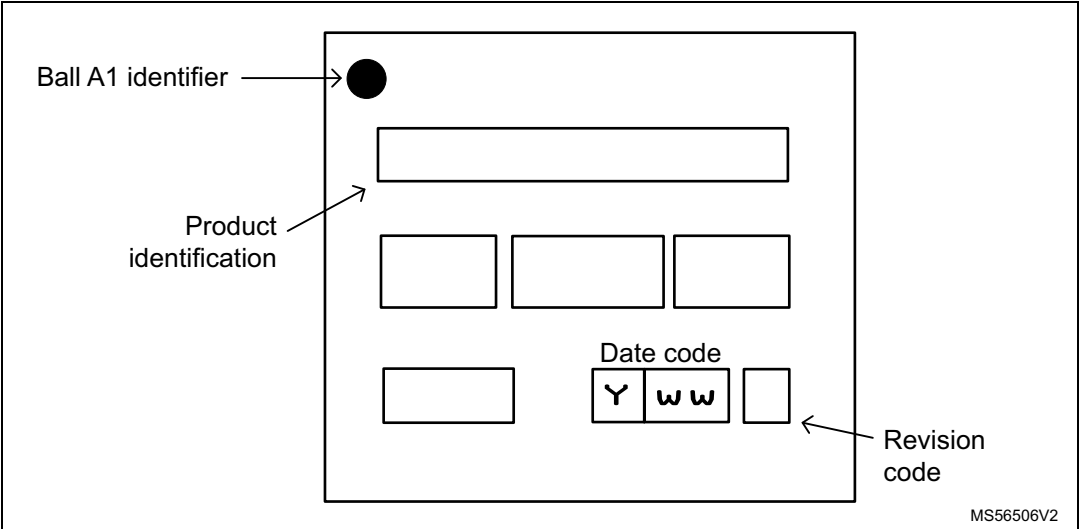
| Dimension         | Values                                                       |
|-------------------|--------------------------------------------------------------|
| Pitch             | 0.35 mm                                                      |
| Dpad              | 0.225 mm                                                     |
| Dsm               | 0.290 mm typ. (depends on soldermask registration tolerance) |
| Stencil opening   | 0.235 mm                                                     |
| Stencil thickness | 0.080 mm                                                     |

Example of device marking for WLCSP80

The following figure gives an example of the locations and orientation of the marking areas versus ball A1, and allows engineering samples to be identified.

With the device text markings oriented as in the figure, ball A1 is always located at top left.

Figure 86. WLCSP80 marking example (package top view)



## 6.5 LQFP100 package information (1L)

This LQFP is 100 lead, 14 x 14 mm low-profile quad flat package.

*Note:* See list of notes in the notes section.

**Figure 87. LQFP100 - Outline<sup>(15)</sup>**

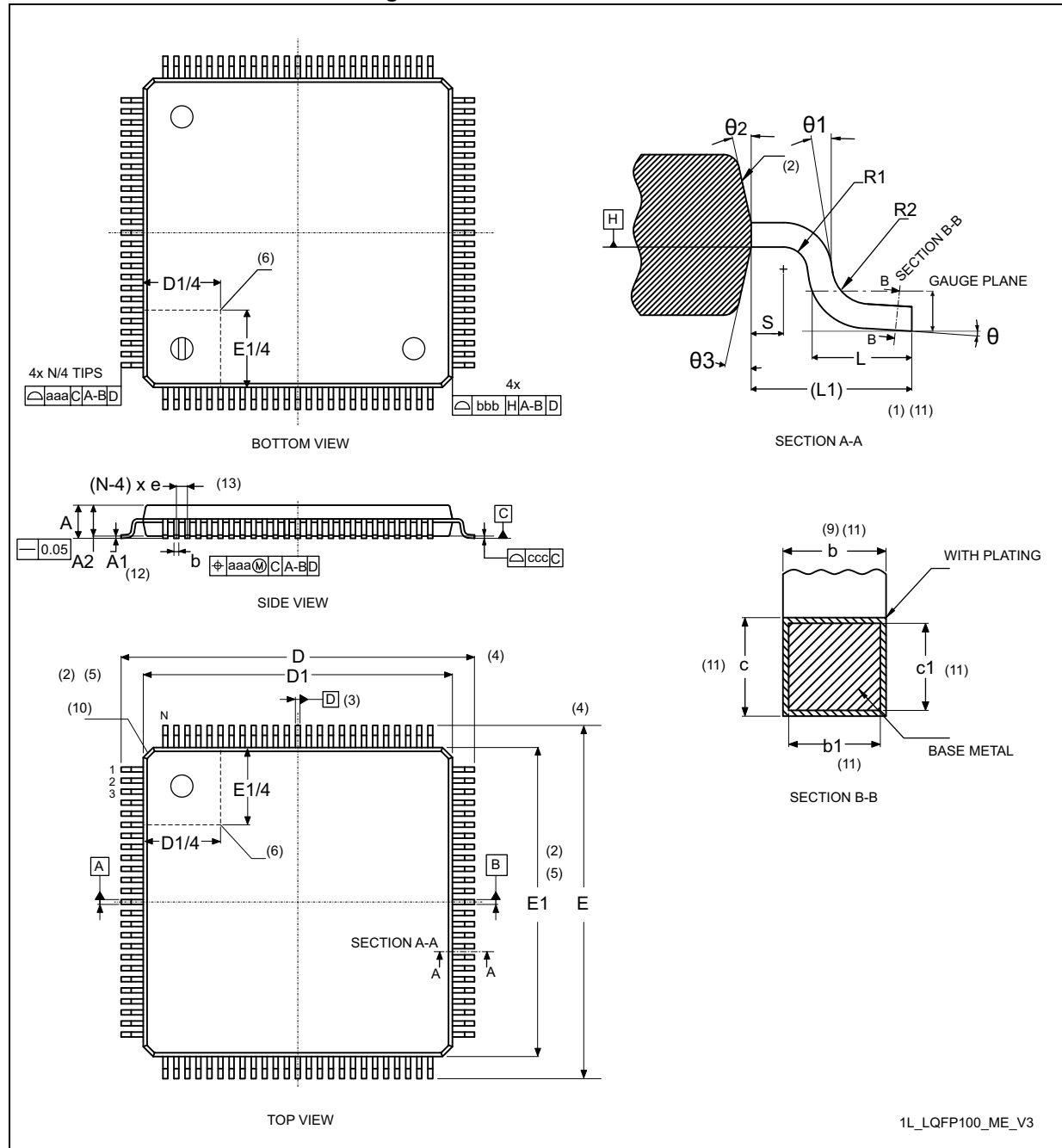
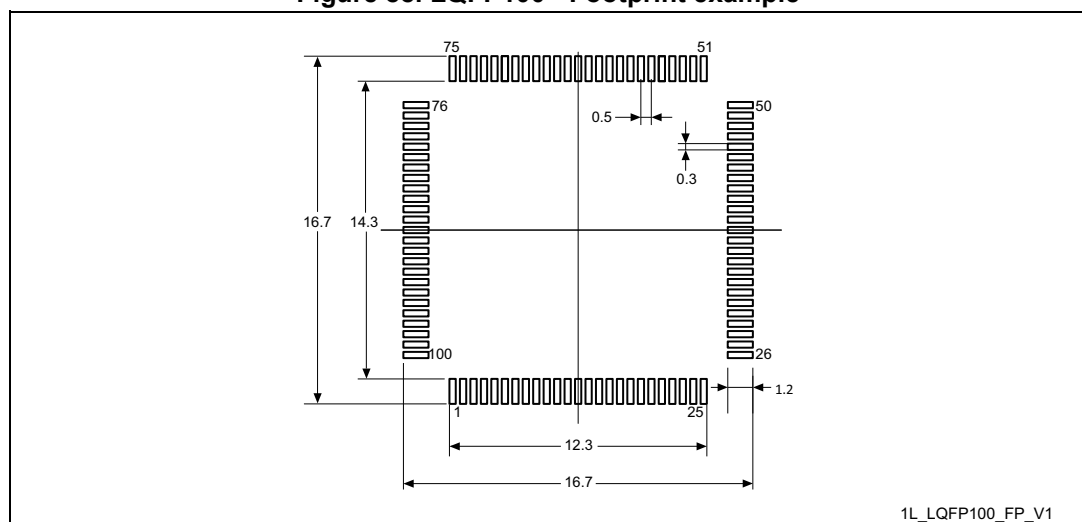


Table 133. LQFP100 - Mechanical data

| Symbol                | millimeters |      |      | inches <sup>(14)</sup> |        |        |
|-----------------------|-------------|------|------|------------------------|--------|--------|
|                       | Min         | Typ  | Max  | Min                    | Typ    | Max    |
| A                     | -           | 1.50 | 1.60 | -                      | 0.0590 | 0.0630 |
| A1 <sup>(12)</sup>    | 0.05        | -    | 0.15 | 0.0019                 | -      | 0.0059 |
| A2                    | 1.35        | 1.40 | 1.45 | 0.0531                 | 0.0551 | 0.0570 |
| b <sup>(9)(11)</sup>  | 0.17        | 0.22 | 0.27 | 0.0067                 | 0.0087 | 0.0106 |
| b1 <sup>(11)</sup>    | 0.17        | 0.20 | 0.23 | 0.0067                 | 0.0079 | 0.0090 |
| c <sup>(11)</sup>     | 0.09        | -    | 0.20 | 0.0035                 | -      | 0.0079 |
| c1 <sup>(11)</sup>    | 0.09        | -    | 0.16 | 0.0035                 | -      | 0.0063 |
| D <sup>(4)</sup>      | 16.00 BSC   |      |      | 0.6299 BSC             |        |        |
| D1 <sup>(2)(5)</sup>  | 14.00 BSC   |      |      | 0.5512 BSC             |        |        |
| E <sup>(4)</sup>      | 16.00 BSC   |      |      | 0.6299 BSC             |        |        |
| E1 <sup>(2)(5)</sup>  | 14.00 BSC   |      |      | 0.5512 BSC             |        |        |
| e                     | 0.50 BSC    |      |      | 0.0197 BSC             |        |        |
| L                     | 0.45        | 0.60 | 0.75 | 0.177                  | 0.0236 | 0.0295 |
| L1 <sup>(1)(11)</sup> | 1.00        |      |      | -                      | 0.0394 | -      |
| N <sup>(13)</sup>     | 100         |      |      |                        |        |        |
| θ                     | 0°          | 3.5° | 7°   | 0°                     | 3.5°   | 7°     |
| θ1                    | 0°          | -    | -    | 0°                     | -      | -      |
| θ2                    | 10°         | 12°  | 14°  | 10°                    | 12°    | 14°    |
| θ3                    | 10°         | 12°  | 14°  | 10°                    | 12°    | 14°    |
| R1                    | 0.08        | -    | -    | 0.0031                 | -      | -      |
| R2                    | 0.08        | -    | 0.20 | 0.0031                 | -      | 0.0079 |
| S                     | 0.20        | -    | -    | 0.0079                 | -      | -      |
| aaa <sup>(1)</sup>    | 0.20        |      |      | 0.0079                 |        |        |
| bbb <sup>(1)</sup>    | 0.20        |      |      | 0.0079                 |        |        |
| ccc <sup>(1)</sup>    | 0.08        |      |      | 0.0031                 |        |        |
| ddd <sup>(1)</sup>    | 0.08        |      |      | 0.0031                 |        |        |

**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. "N" is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

**Figure 88. LQFP100 - Footprint example**

1. Dimensions are expressed in millimeters.

## 6.6 LQFP144 package information (1A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package.

*Note:* See list of notes in the notes section.

**Figure 89. LQFP144 - Outline<sup>(15)</sup>**

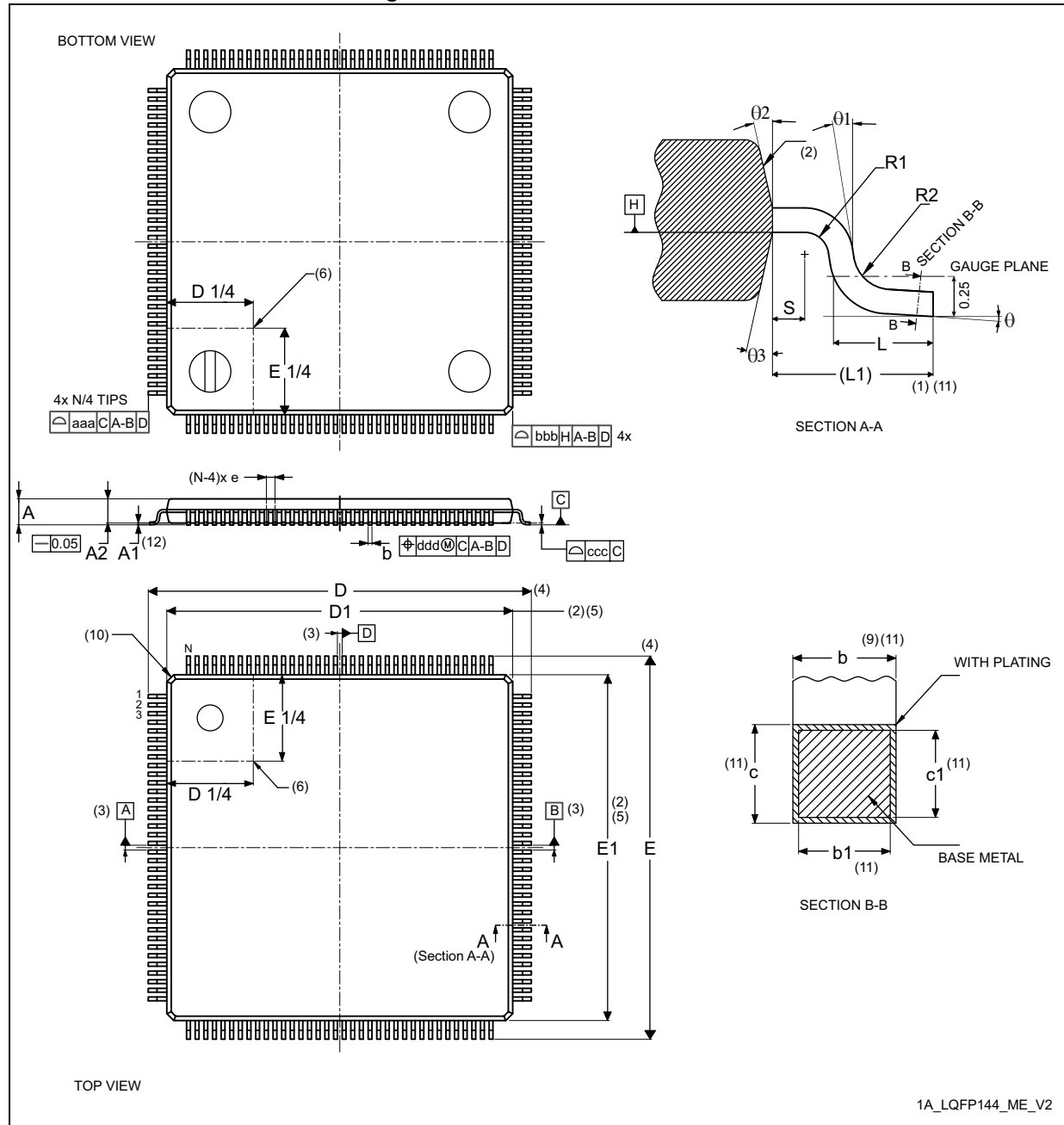


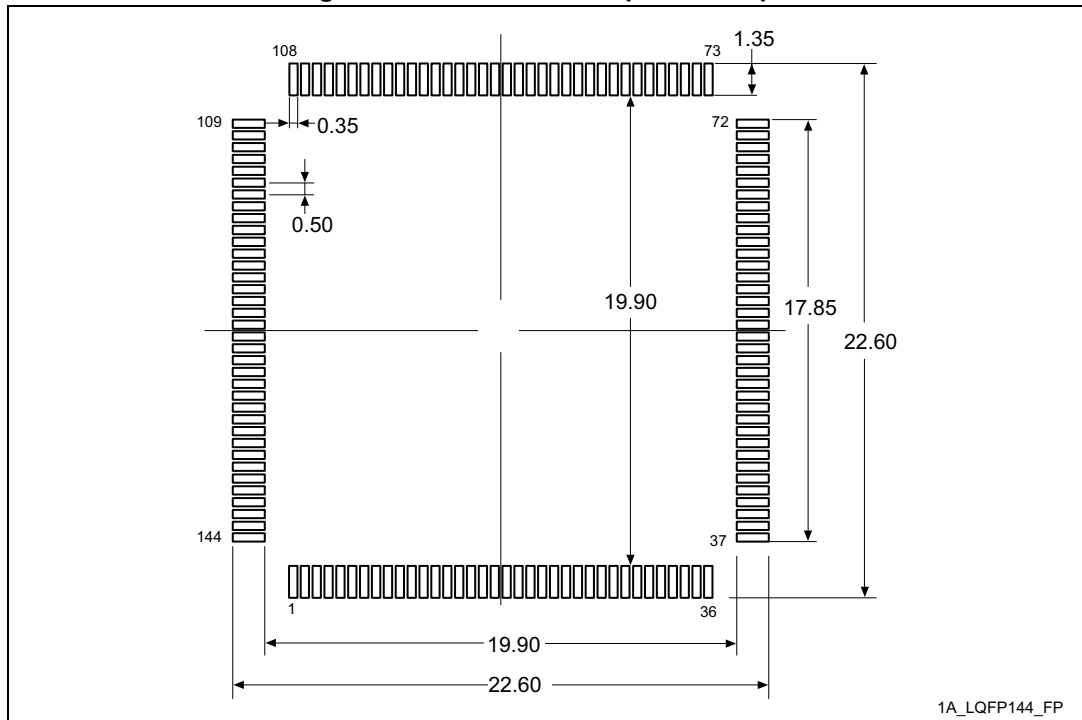
Table 134. LQFP144 - Mechanical data

| Symbol               | millimeters |      |      | inches <sup>(14)</sup> |        |        |
|----------------------|-------------|------|------|------------------------|--------|--------|
|                      | Min         | Typ  | Max  | Min                    | Typ    | Max    |
| A                    | -           | -    | 1.60 | -                      | -      | 0.0630 |
| A1 <sup>(12)</sup>   | 0.05        | -    | 0.15 | 0.0020                 | -      | 0.0059 |
| A2                   | 1.35        | 1.40 | 1.45 | 0.0531                 | 0.0551 | 0.0571 |
| b <sup>(9)(11)</sup> | 0.17        | 0.22 | 0.27 | 0.0067                 | 0.0087 | 0.0106 |
| b1 <sup>(11)</sup>   | 0.17        | 0.20 | 0.23 | 0.0067                 | 0.0079 | 0.0090 |
| c <sup>(11)</sup>    | 0.09        | -    | 0.20 | 0.0035                 | -      | 0.0079 |
| c1 <sup>(11)</sup>   | 0.09        | -    | 0.16 | 0.0035                 | -      | 0.0063 |
| D <sup>(4)</sup>     | 22.00 BSC   |      |      | 0.8661 BSC             |        |        |
| D1 <sup>(2)(5)</sup> | 20.00 BSC   |      |      | 0.7874 BSC             |        |        |
| E <sup>(4)</sup>     | 22.00 BSC   |      |      | 0.8661 BSC             |        |        |
| E1 <sup>(2)(5)</sup> | 20.00 BSC   |      |      | 0.7874 BSC             |        |        |
| e                    | 0.50 BSC    |      |      | 0.0197 BSC             |        |        |
| L                    | 0.45        | 0.60 | 0.75 | 0.0177                 | 0.0236 | 0.0295 |
| L1                   | 1.00 REF    |      |      | 0.0394 REF             |        |        |
| N <sup>(13)</sup>    | 144         |      |      |                        |        |        |
| θ                    | 0°          | 3.5° | 7°   | 0°                     | 3.5°   | 7°     |
| θ1                   | 0°          | -    | -    | 0°                     | -      | -      |
| θ2                   | 10°         | 12°  | 14°  | 10°                    | 12°    | 14°    |
| θ3                   | 10°         | 12°  | 14°  | 10°                    | 12°    | 14°    |
| R1                   | 0.08        | -    | -    | 0.0031                 | -      | -      |
| R2                   | 0.08        | -    | 0.20 | 0.0031                 | -      | 0.0079 |
| S                    | 0.20        | -    | -    | 0.0079                 | -      | -      |
| aaa                  | 0.20        |      |      | 0.0079                 |        |        |
| bbb                  | 0.20        |      |      | 0.0079                 |        |        |
| ccc                  | 0.08        |      |      | 0.0031                 |        |        |
| ddd                  | 0.08        |      |      | 0.0031                 |        |        |

**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. "N" is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 90. LQFP144 - Footprint example

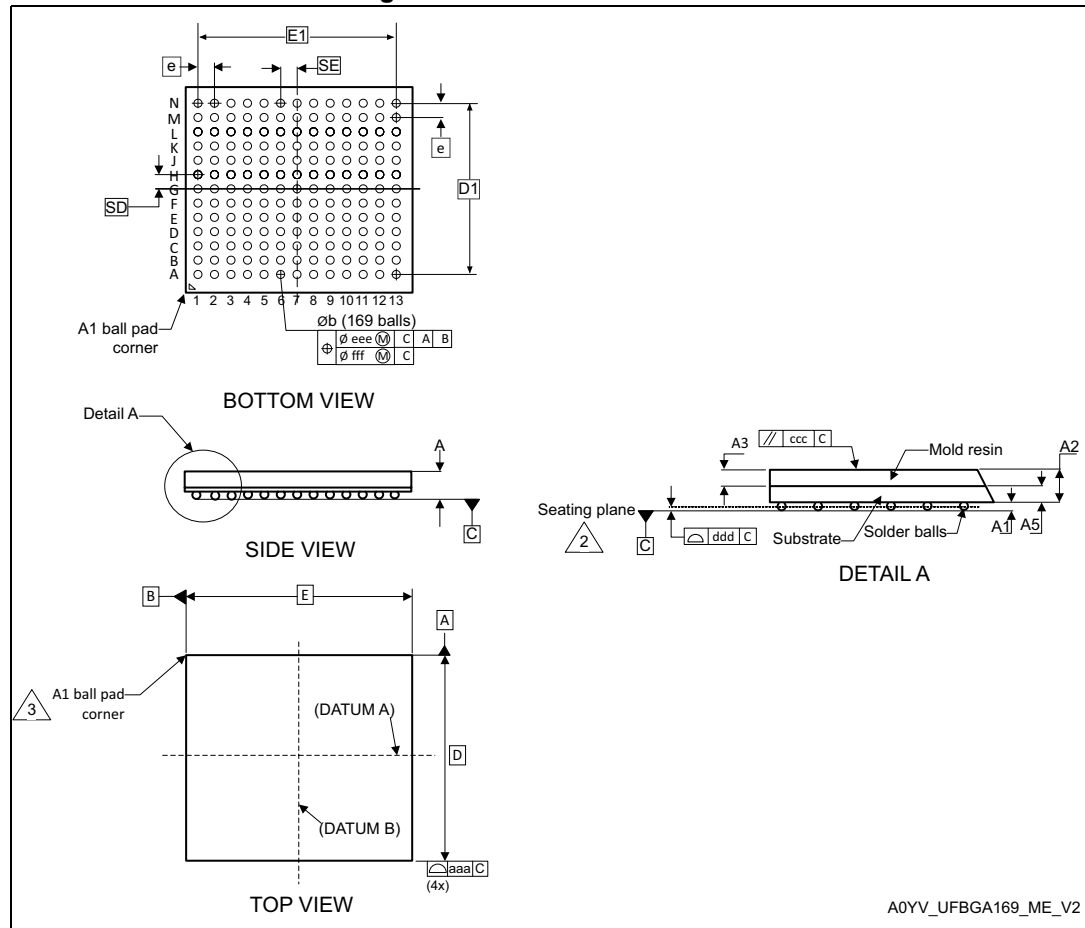


1. Dimensions are expressed in millimeters.

## 6.7 UFBGA169 package information (A0YV)

This UFBGA is a 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

**Figure 91. UFBGA169 - Outline**



1. Drawing is not to scale.
2. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
3. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguishable feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 135. UFBGA169 - Mechanical data

| Symbol               | millimeters |      |      | inches <sup>(1)</sup> |        |        |
|----------------------|-------------|------|------|-----------------------|--------|--------|
|                      | Min.        | Typ. | Max. | Min.                  | Typ.   | Max.   |
| A <sup>(2)</sup>     | -           | -    | 0.60 | -                     | -      | 0.0236 |
| A1 <sup>(3)</sup>    | 0.05        | -    | -    | 0.0020                | -      | -      |
| A2                   | -           | 0.43 | -    | -                     | 0.0169 | -      |
| b <sup>(4)</sup>     | 0.23        | 0.28 | 0.33 | 0.0091                | 0.0110 | 0.0130 |
| D <sup>(5)</sup>     | 7.00 BSC    |      |      | 0.2756 BSC            |        |        |
| D1 <sup>(5)</sup>    | 6.00 BSC    |      |      | 0.2362 BSC            |        |        |
| E <sup>(5)</sup>     | 7.00 BSC    |      |      | 0.2756 BSC            |        |        |
| E1 <sup>(5)</sup>    | 6.00 BSC    |      |      | 0.2362 BSC            |        |        |
| e <sup>(5)(6)</sup>  | 0.50 BSC    |      |      | 0.0197 BSC            |        |        |
| N <sup>(7)</sup>     | 169         |      |      |                       |        |        |
| SD <sup>(5)(8)</sup> | 0.50 BSC    |      |      | 0.0197 BSC            |        |        |
| SE <sup>(5)(8)</sup> | 0.50 BSC    |      |      | 0.0197 BSC            |        |        |
| aaa <sup>(9)</sup>   | 0.15        |      |      | 0.0059                |        |        |
| ccc <sup>(9)</sup>   | 0.20        |      |      | 0.0079                |        |        |
| ddd <sup>(9)</sup>   | 0.08        |      |      | 0.0031                |        |        |
| eee <sup>(9)</sup>   | 0.15        |      |      | 0.0059                |        |        |
| fff <sup>(9)</sup>   | 0.05        |      |      | 0.0020                |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
5. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table.
6. e represents the solder ball grid pitch.
7. N represents the total number of balls on the BGA.
8. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
9. Tolerance of form and position drawing

Figure 92. UFBGA169 - Footprint example

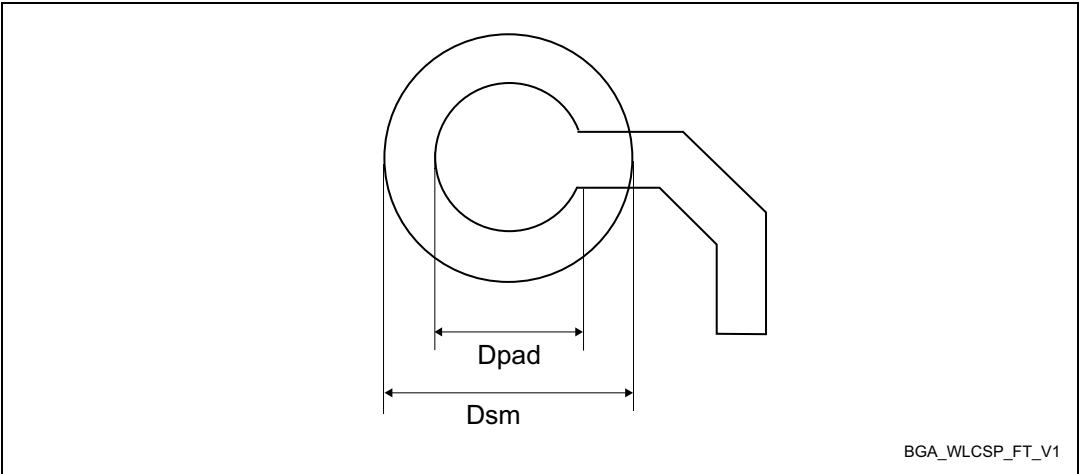


Table 136. UFBGA169 - Example of PCB design rules (0.5 mm pitch BGA)

| Dimension    | Values                                                          |
|--------------|-----------------------------------------------------------------|
| Pitch        | 0.5 mm                                                          |
| Dpad         | 0.27 mm                                                         |
| Dsm          | 0.35 mm typ. (depends on the soldermask registration tolerance) |
| Solder paste | 0.27 mm aperture diameter.                                      |

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

## 6.8 LQFP176 package information (1T)

This LQFP is a 176-pin, 24 x 24 mm, 0.5 mm pitch, low profile quad flat package.

*Note:* See list of notes in the notes section.

**Figure 93. LQFP176 - Outline<sup>(15)</sup>**

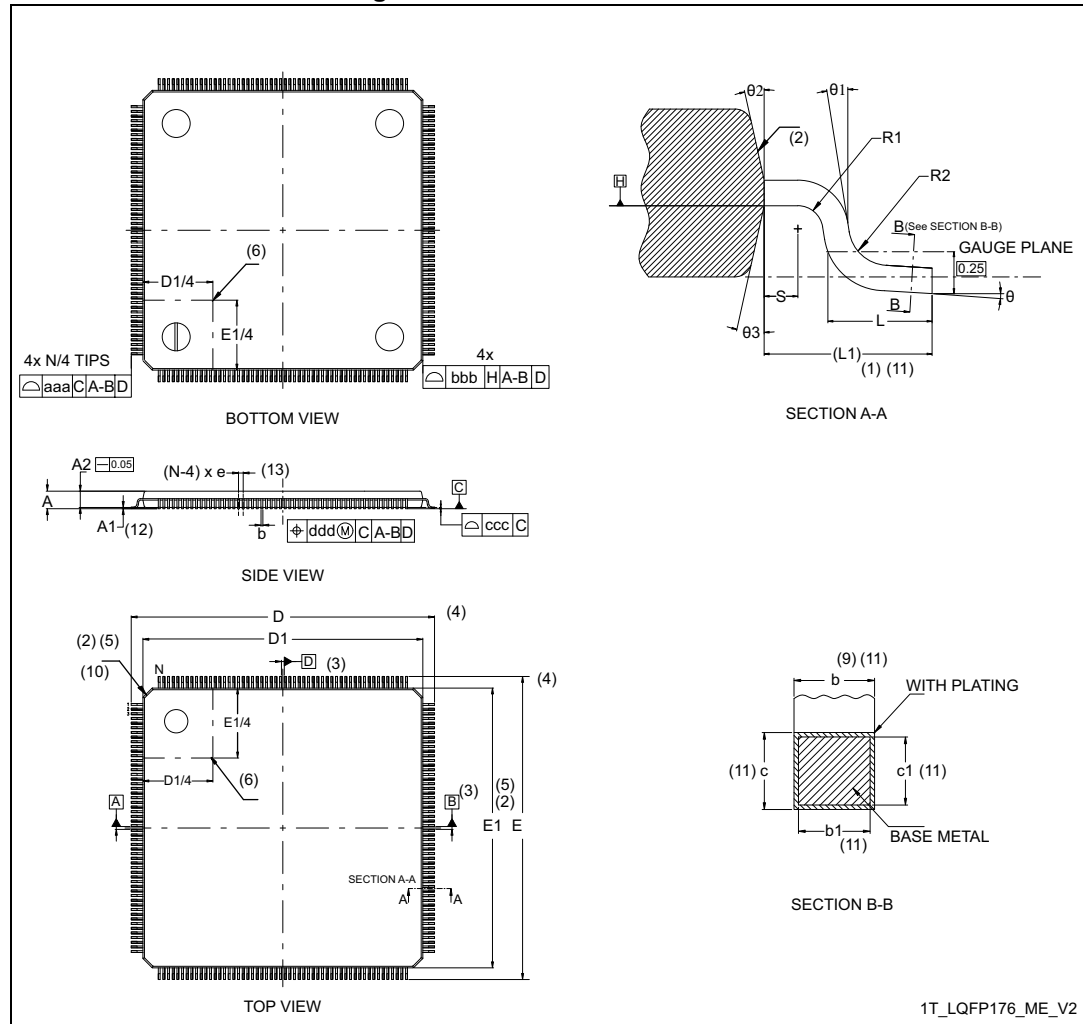


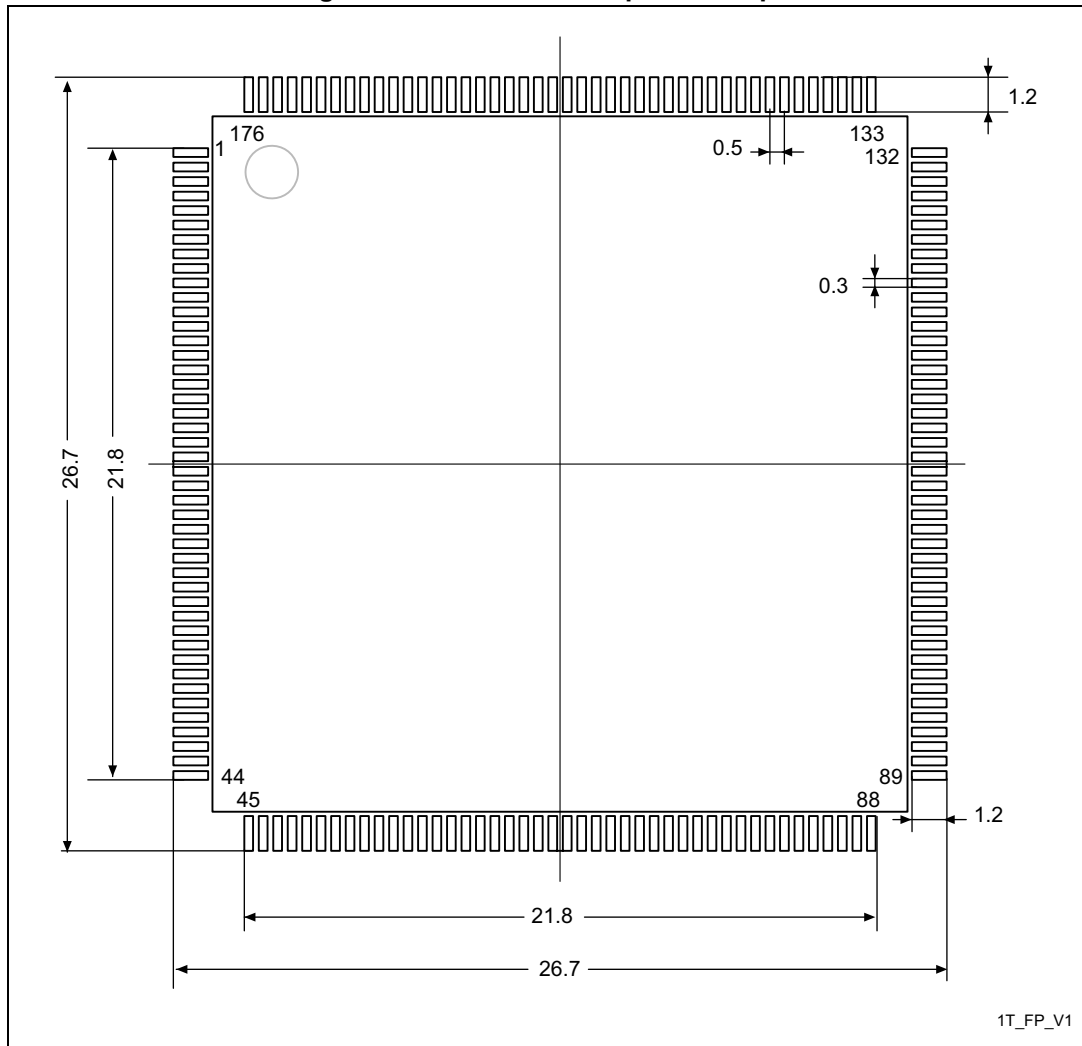
Table 137. LQFP176 - Mechanical data

| Symbol                | millimeters |       |       | inches <sup>(14)</sup> |        |        |
|-----------------------|-------------|-------|-------|------------------------|--------|--------|
|                       | Min         | Typ   | Max   | Min                    | Typ    | Max    |
| A                     | -           | -     | 1.600 | -                      | -      | 0.0630 |
| A1 <sup>(12)</sup>    | 0.050       | -     | 0.150 | 0.0020                 | -      | 0.0059 |
| A2                    | 1.350       | 1.400 | 1.450 | 0.0531                 | 0.0551 | 0.0571 |
| b <sup>(9)(11)</sup>  | 0.170       | 0.220 | 0.270 | 0.0067                 | 0.0087 | 0.0106 |
| b1 <sup>(11)</sup>    | 0.170       | 0.200 | 0.230 | 0.0067                 | 0.0079 | 0.0091 |
| c <sup>(11)</sup>     | 0.090       | -     | 0.200 | 0.0035                 | -      | 0.0079 |
| c1 <sup>(11)</sup>    | 0.090       | -     | 0.160 | 0.0035                 | -      | 0.063  |
| D <sup>(4)</sup>      | 26.000      |       |       | 1.0236                 |        |        |
| D1 <sup>(2)(5)</sup>  | 24.000      |       |       | 0.9449                 |        |        |
| E <sup>(4)</sup>      | 26.000      |       |       | 0.0197                 |        |        |
| E1 <sup>(2)(5)</sup>  | 24.000      |       |       | 0.9449                 |        |        |
| e                     | 0.500       |       |       | 0.1970                 |        |        |
| L                     | 0.450       | 0.600 | 0.750 | 0.0177                 | 0.0236 | 0.0295 |
| L1 <sup>(1)(11)</sup> | 1           |       |       | 0.0394 REF             |        |        |
| N <sup>(13)</sup>     | 176         |       |       |                        |        |        |
| θ                     | 0°          | 3.5°  | 7°    | 0°                     | 3.5°   | 7°     |
| θ1                    | 0°          | -     | -     | 0°                     | -      | -      |
| θ2                    | 10°         | 12°   | 14°   | 10°                    | 12°    | 14°    |
| θ3                    | 10°         | 12°   | 14°   | 10°                    | 12°    | 14°    |
| R1                    | 0.080       | -     | -     | 0.0031                 | -      | -      |
| R2                    | 0.080       | -     | 0.200 | 0.0031                 | -      | 0.0079 |
| S                     | 0.200       | -     | -     | 0.0079                 | -      | -      |
| aaa <sup>(1)</sup>    | 0.200       |       |       | 0.0079                 |        |        |
| bbb <sup>(1)</sup>    | 0.200       |       |       | 0.0079                 |        |        |
| ccc <sup>(1)</sup>    | 0.080       |       |       | 0.0031                 |        |        |
| ddd <sup>(1)</sup>    | 0.080       |       |       | 0.0031                 |        |        |

**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. "N" is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 94. LQFP176 - Footprint example

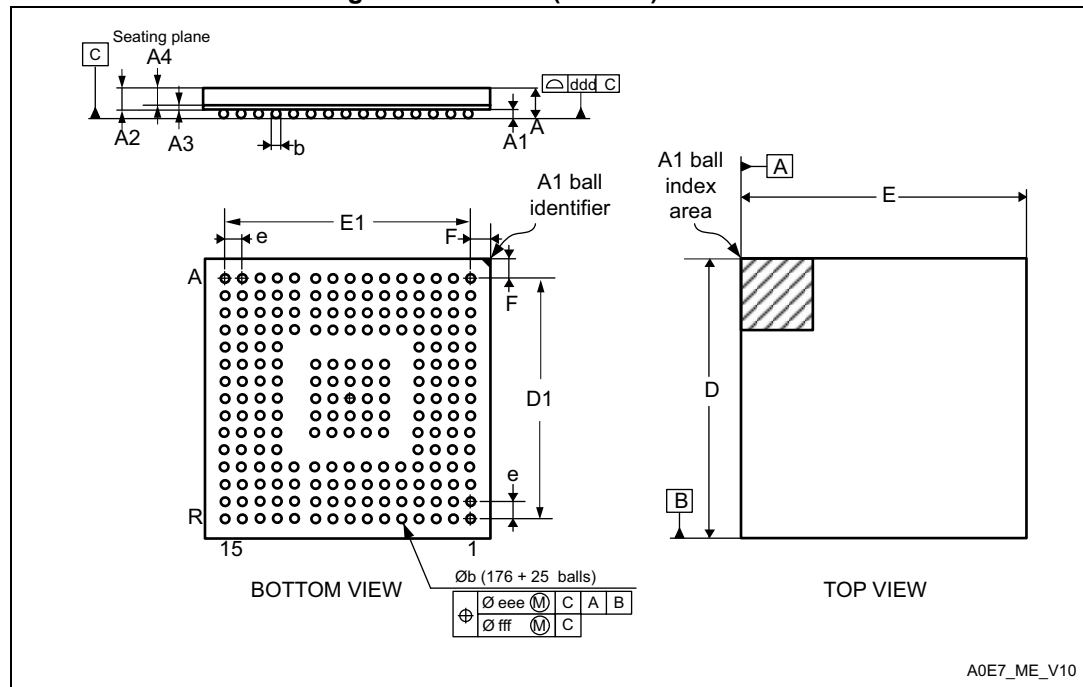


1. Dimensions are expressed in millimeters.

## 6.9 UFBGA(176+25) package information (A0E7)

This UFBGA is a 176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package.

Figure 95. UFBGA(176+25) - Outline



1. Drawing is not to scale.

Table 138. UFBGA(176+25) - Mechanical data

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min.        | Typ.   | Max.   | Min.                  | Typ.   | Max.   |
| A      | -           | -      | 0.600  | -                     | -      | 0.0236 |
| A1     | 0.050       | 0.080  | 0.110  | 0.0020                | 0.0031 | 0.0043 |
| A2     | -           | 0.450  | -      | -                     | 0.0177 | -      |
| A3     | -           | 0.130  | -      | -                     | 0.0051 | -      |
| A4     | -           | 0.320  | -      | -                     | 0.0126 | -      |
| b      | 0.240       | 0.290  | 0.340  | 0.0094                | 0.0114 | 0.0134 |
| D      | 9.850       | 10.000 | 10.150 | 0.3878                | 0.3937 | 0.3996 |
| D1     | -           | 9.100  | -      | -                     | 0.3583 | -      |
| E      | 9.850       | 10.000 | 10.150 | 0.3878                | 0.3937 | 0.3996 |
| E1     | -           | 9.100  | -      | -                     | 0.3583 | -      |
| e      | -           | 0.650  | -      | -                     | 0.0256 | -      |
| F      | -           | 0.450  | -      | -                     | 0.0177 | -      |
| ddd    | -           | -      | 0.080  | -                     | -      | 0.0031 |

Table 138. UFBGA(176+25) - Mechanical data (continued)

| Symbol | millimeters |      |       | inches <sup>(1)</sup> |      |        |
|--------|-------------|------|-------|-----------------------|------|--------|
|        | Min.        | Typ. | Max.  | Min.                  | Typ. | Max.   |
| eee    | -           | -    | 0.150 | -                     | -    | 0.0059 |
| fff    | -           | -    | 0.050 | -                     | -    | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 96. UFBGA(176+25) - Footprint example

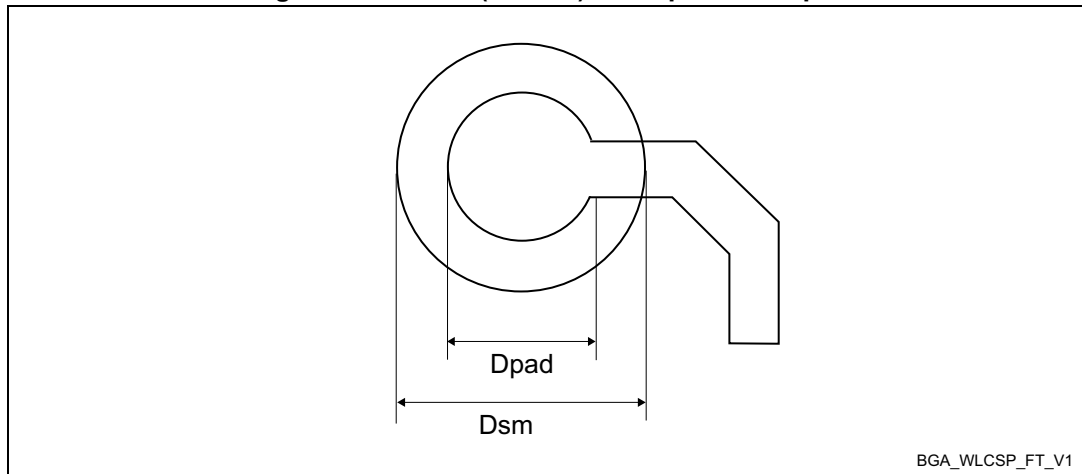


Table 139. UFBGA(176+25) - Example of PCB design rules (0.65 mm pitch BGA)

| Dimension         | Values                                                           |
|-------------------|------------------------------------------------------------------|
| Pitch             | 0.65 mm                                                          |
| Dpad              | 0.300 mm                                                         |
| Dsm               | 0.400 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening   | 0.300 mm                                                         |
| Stencil thickness | Between 0.100 mm and 0.125 mm                                    |
| Pad trace width   | 0.100 mm                                                         |

## 6.10 TFBGA225 package information (B04V)

This TFBGA is a 225-ball, 13 x 13 mm, 0.8 mm pitch, thin profile fine pitch ball grid array package.

**Note:** See list of notes in the notes section.

**Figure 97. TFBGA225 - Outline<sup>(13)</sup>**

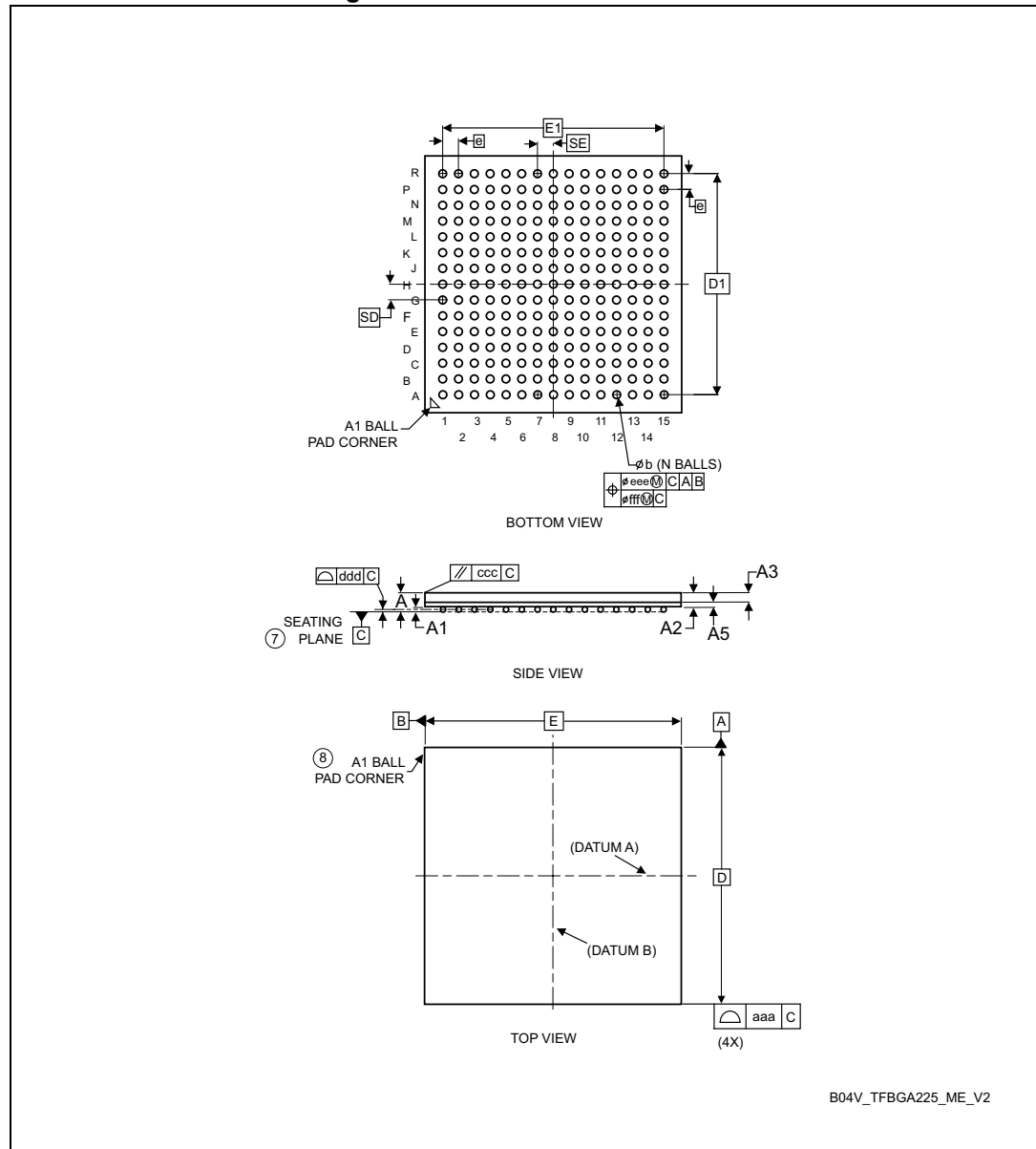


Table 140. TFBGA225 - Mechanical data

| Symbol              | millimeters <sup>(1)</sup> |      |      | inches <sup>(12)</sup> |        |        |
|---------------------|----------------------------|------|------|------------------------|--------|--------|
|                     | Min                        | Typ  | Max  | Min                    | Typ    | Max    |
| A <sup>(2)(3)</sup> | -                          | -    | 1.20 | -                      | -      | 0.0472 |
| A1 <sup>(4)</sup>   | 0.15                       | -    | -    | 0.0059                 | -      | -      |
| A2                  | -                          | 0.78 | -    | -                      | 0.0307 | -      |
| b <sup>(5)</sup>    | 0.35                       | 0.40 | 0.45 | 0.0138                 | 0.0157 | 0.0177 |
| D <sup>(6)</sup>    | 13.00 BSC                  |      |      | 0.5118 BSC             |        |        |
| D1                  | 11.20 BSC                  |      |      | 0.4409 BSC             |        |        |
| E                   | 13.00 BSC                  |      |      | 0.5118 BSC             |        |        |
| E1                  | 11.20 BSC                  |      |      | 0.4409 BSC             |        |        |
| e <sup>(9)</sup>    | 0.80 BSC                   |      |      | 0.0315 BSC             |        |        |
| N <sup>(11)</sup>   | 225                        |      |      |                        |        |        |
| SD <sup>(12)</sup>  | 0.80 BSC                   |      |      | 0.0315 BSC             |        |        |
| SE <sup>(12)</sup>  | 0.80 BSC                   |      |      | 0.0315 BSC             |        |        |
| aaa                 | 0.15                       |      |      | 0.0059                 |        |        |
| ccc                 | 0.20                       |      |      | 0.0079                 |        |        |
| ddd                 | 0.10                       |      |      | 0.0039                 |        |        |
| eee                 | 0.15                       |      |      | 0.0059                 |        |        |
| fff                 | 0.08                       |      |      | 0.0031                 |        |        |

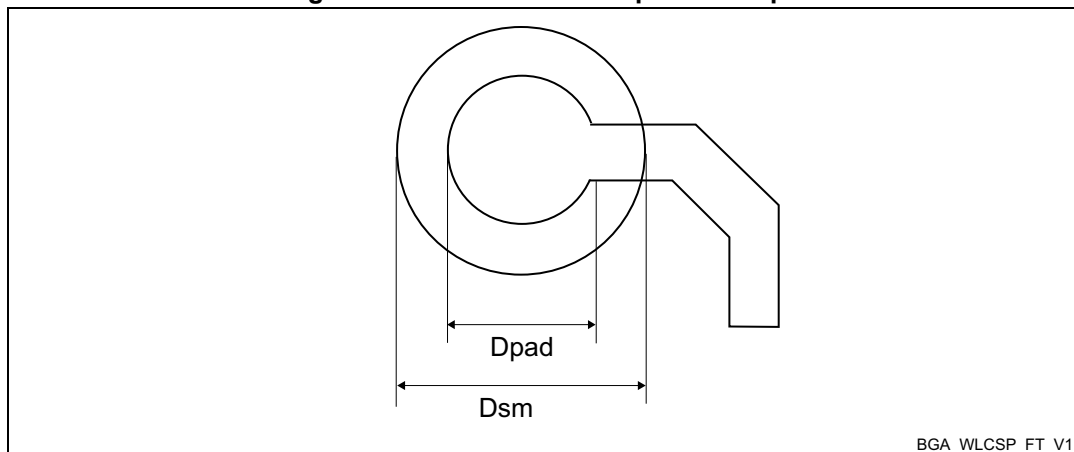
**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. TFBGA stands for Thin profile Fine pitch Ball Grid Array: 1.00mm < A ≤ 1.20mm / Fine pitch e < 1.00mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or

integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD & SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

**Figure 98. TFBGA225 - Footprint example**



**Table 141. TFBGA225 - Recommended PCB design rules (0.8 mm pitch BGA)**

| Dimension         | Recommended values |
|-------------------|--------------------|
| Pitch             | 0.8 mm             |
| Dpad              | 0.400 mm           |
| Dsm               | 0.550 mm           |
| Stencil opening   | 0.400 mm           |
| Stencil thickness | 0.125 to 0.100 mm  |

## 6.11 Package thermal characteristics

The maximum chip-junction temperature,  $T_{Jmax}$  in degrees Celsius, can be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- $T_{Amax}$  is the maximum ambient temperature in °C
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W
- $P_{Dmax}$  is the sum of  $P_{INTmax}$  and  $P_{I/Omax}$  ( $P_{Dmax} = P_{INTmax} + P_{I/Omax}$ )
- $P_{INTmax}$  is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$  represents the maximum power dissipation on output pins:

$$P_{I/Omax} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DD} - V_{OH}) \times I_{OH})$$

taking into account the actual  $V_{OL}$  /  $I_{OL}$  and  $V_{OH}$  /  $I_{OH}$  of the I/Os at low and high level in the application.

Table 142. Package thermal characteristics

| Symbol        | Definition                          | Parameter                | Value | Unit |
|---------------|-------------------------------------|--------------------------|-------|------|
| $\Theta_{JA}$ | Thermal resistance junction-ambient | LQFP64 (10 x 10 mm)      | 48.1  | °C/W |
|               |                                     | VFQFPN68 (8 x 8 mm)      | 24.2  |      |
|               |                                     | WLCSP80 (3.50 x 3.27 mm) | 47.3  |      |
|               |                                     | LQFP100 (14 x 14 mm)     | 35.9  |      |
|               |                                     | LQFP144 (20 x 20 mm)     | 37.5  |      |
|               |                                     | LQFP176 (24 x 24 mm)     | 38.3  |      |
|               |                                     | UFBGA169 (7 x 7 mm)      | 40.6  |      |
|               |                                     | UFBGA176 (10 x 10 mm)    | 39.1  |      |
|               |                                     | TFBGA225 (13 x 13 mm)    | 36.0  |      |
| $\Theta_{JB}$ | Thermal resistance junction-board   | LQFP64 (10 x 10 mm)      | 24.1  | °C/W |
|               |                                     | VFQFPN68 (8 x 8 mm)      | 9.4   |      |
|               |                                     | WLCSP80 (3.50 x 3.27 mm) | 23.0  |      |
|               |                                     | LQFP100 (14 x 14 mm)     | 21.9  |      |
|               |                                     | LQFP144 (20 x 20 mm)     | 26.3  |      |
|               |                                     | LQFP176 (24 x 24 mm)     | 28.3  |      |
|               |                                     | UFBGA169 (7 x 7 mm)      | 26.4  |      |
|               |                                     | UFBGA176 (10 x 10 mm)    | 27.0  |      |
|               |                                     | TFBGA225 (13 x 13 mm)    | 25.5  |      |
| $\Theta_{JC}$ | Thermal resistance junction-case    | LQFP64 (10 x 10 mm)      | 10.3  | °C/W |
|               |                                     | VFQFPN68 (8 x 8 mm)      | 10.8  |      |
|               |                                     | WLCSP80 (3.50 x 3.27 mm) | 2.3   |      |
|               |                                     | LQFP100 (14 x 14 mm)     | 8.5   |      |
|               |                                     | LQFP144 (20 x 20 mm)     | 8.6   |      |
|               |                                     | LQFP176 (24 x 24 mm)     | 9.1   |      |
|               |                                     | UFBGA169 (7 x 7 mm)      | 11.2  |      |
|               |                                     | UFBGA176 (10 x 10 mm)    | 10.9  |      |
|               |                                     | TFBGA225 (13 x 13 mm)    | 14.1  |      |

### 6.11.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org).
- For information on thermal management, refer to AN5036 “*Guidelines for thermal management on STM32 applications*”, available from [www.st.com](http://www.st.com).

## 7 Ordering information

|                                                             |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
|-------------------------------------------------------------|-------|---|-----|---|---|---|---|---|----|--|--|--|--|--|--|--|--|--|
| Example:                                                    | STM32 | H | 563 | V | I | T | 6 | Q | TR |  |  |  |  |  |  |  |  |  |
| Device family                                               |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| STM32 = Arm based 32-bit microcontroller                    |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Product type                                                |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| H = high performance                                        |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Device subfamily                                            |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| 562 = STM32H562xx devices without Ethernet                  |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| 563 = STM32H563xx devices                                   |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Pin count                                                   |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| R = 64 pins / 68 pins                                       |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| M = 80 pins                                                 |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| V = 100 pins                                                |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Z = 144 pins                                                |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| A = 169 balls                                               |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| I = 176 pins                                                |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| L = 225 balls                                               |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Flash memory size                                           |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| G = 1 Mbyte                                                 |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| I = 2 Mbytes                                                |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Package                                                     |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| V = VFQFPN                                                  |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| T = LQFP                                                    |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| I = UFBGA (7 x 7 mm)                                        |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| K = UFBGA (10 x 10 mm)                                      |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Y = WLCSP                                                   |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| H = TFBGA (13 x 13 mm)                                      |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Temperature range                                           |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| 6 = industrial, -40 to 85°C, available only in LDO option   |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| 7 = industrial, -40 to 105°C, available only in LDO option  |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| 3 = industrial, -40 to 125°C, available only in SMPS option |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Dedicated pinout                                            |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Q = dedicated pinout supporting SMPS step-down converter    |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| Packing                                                     |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| TR = tape and reel                                          |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |
| xxx = programmed parts                                      |       |   |     |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |

For a list of available options (such as speed or package) or for further information on any aspect of this device, contact the nearest ST sales office.

## 8 Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture ([www.psacertified.org](http://www.psacertified.org)) and/or Security Evaluation standard for IoT Platforms ([www.trustcb.com](http://www.trustcb.com)). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on [www.st.com](http://www.st.com) for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

## 9 Revision history

**Table 143. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 06-Mar-2023 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 20-Oct-2023 | 2        | <p>Updated <a href="#">Features</a> and <a href="#">Section 3.10.1: Power supply schemes</a>.<br/> Updated <a href="#">Table 2: STM32H56xxx features and peripheral counts</a>, <a href="#">Table 18: Current characteristics</a>, <a href="#">Table 20: General operating conditions</a>, tables 30 to 32, tables 34 to 35, <a href="#">Table 58: I/O static characteristics</a>, and <a href="#">Table 64: Output timing characteristics (HSLV ON)</a>.<br/> Updated <a href="#">Figure 7: WLCSP80 SMPS ballout</a>, <a href="#">Figure 42: NAND controller waveforms for read access</a>, <a href="#">Figure 43: NAND controller waveforms for write access</a>, <a href="#">Figure 64: SPI timing diagram - Master mode</a>, <a href="#">Figure 66: SPI timing diagram - Slave mode and CPHA = 1</a>, <a href="#">Figure 70: SAI master timing waveforms</a>, and <a href="#">Figure 71: SAI slave timing waveforms</a>.<br/> Added <a href="#">Section 3.32: Public key accelerator (PKA)</a>, <a href="#">Section 6.1: Device marking</a>, and <a href="#">Example of device marking for WLCSP80</a>.<br/> Minor text edits across the whole document.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 28-May-2024 | 3        | <p>Updated <a href="#">Figure 1: STM32H562xx and STM32H563xx block diagram</a>, <a href="#">Figure 6: VFQFPN68 pinout</a>, <a href="#">Figure 17: UFBGA176+25 SMPS ballout</a>, <a href="#">Figure 32: VIL/VIH for all I/Os except BOOT0</a>, and <a href="#">Figure 64: SPI timing diagram - Master mode</a>.<br/> Updated <a href="#">Table 14: STM32H562xx and STM32H563xx pin/ball definition</a>, <a href="#">Table 15: Alternate functions AF0 to AF7</a>, <a href="#">Table 21: Maximum allowed clock frequencies</a>, <a href="#">Table 23: Characteristics of SMPS step-down converter external components</a>, <a href="#">Table 30: Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-way</a>, <a href="#">Table 45: HSI oscillator characteristics</a>, tables 53 to 55, <a href="#">Table 122: Dynamic characteristics: SD/MMC, VDD = 2.7 to 3.6 V</a>, and <a href="#">Table 123: Dynamic characteristics: eMMC, VDD = 1.71 to 1.9 V</a>.<br/> Updated <a href="#">Section 3.24.1: Analog temperature sensor</a>.<br/> Added <a href="#">Section 3.25: Digital temperature sensor (DTS)</a>, <a href="#">Section 5.3.14: I/O current injection characteristics</a>, and <a href="#">USB full speed (FS) characteristics</a>.<br/> Added <a href="#">Table 60: Output voltage characteristics for FT_c I/Os</a> and <a href="#">Table 67: Output timing characteristics for FT_c I/Os (PB13/PB14)</a>.<br/> Added <a href="#">Figure 37: Asynchronous multiplexed PSRAM/NOR write waveforms</a>.<br/> Minor text edits across the whole document.</p> |

Table 143. Document revision history

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13-Dec-2024 | 4        | <p>Updated <a href="#">Features</a>, <a href="#">Section 3.28: Digital camera interface (DCMI)</a>, <a href="#">Wake-up time from low-power modes</a>, and <a href="#">Section 7: Ordering information</a>.</p> <p>Updated <a href="#">Table 2: STM32H56xxx features and peripheral counts</a>, <a href="#">Table 10: SPI features</a>, <a href="#">Table 20: General operating conditions</a>, <a href="#">Table 21: Maximum allowed clock frequencies</a>, <a href="#">Table 36: Typical and maximum current consumption in Standby mode</a>, <a href="#">Table 37: Typical and maximum current consumption in VBAT mode</a>, <a href="#">Table 40: High-speed external user clock characteristics</a>, <a href="#">Table 51: Flash memory programming</a>, <a href="#">Table 89: OCTOSPI characteristics in DTR mode (no DQS)</a>, <a href="#">Table 90: OCTOSPI characteristics in DTR mode (with DQS) / HyperBus</a>, <a href="#">Table 95: 12-bit ADC characteristics</a>, <a href="#">Table 110: LPTIMx characteristics</a>, and <a href="#">Table 135: UFBGA169 - Mechanical data</a>.</p> <p>Updated <a href="#">Figure 5: LQFP64 pinout</a> and <a href="#">Figure 91: UFBGA169 - Outline</a>.</p> <p>Minor text edits across the whole document.</p>                                                                                                                                                                                                                                           |
| 02-Jan-2025 | 5        | <p>Updated <a href="#">Table 36: Typical and maximum current consumption in Standby mode</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 27-May-2025 | 6        | <p>Introduced TFBGA225 package.</p> <p>Updated image on cover page.</p> <p>Updated <a href="#">Features</a>, <a href="#">Section 2: Description</a>, <a href="#">Section 3.5: Embedded SRAMs</a>, and <a href="#">Section 7: Ordering information</a>.</p> <p>Updated <a href="#">Table 1: Device summary</a>, <a href="#">Table 2: STM32H56xxx features and peripheral counts</a>, <a href="#">Table 6: Timer features</a>, <a href="#">Table 14: STM32H562xx and STM32H563xx pin/ball definition</a>, <a href="#">Table 20: General operating conditions</a>, <a href="#">Table 26: Embedded reference voltage</a>, <a href="#">Table 113: I3C open-drain measured timings</a>, <a href="#">Table 114: I3C push-pull measured timings</a>, <a href="#">Table 115: SPI characteristics</a>, and <a href="#">Table 142: Package thermal characteristics</a>.</p> <p>Added footnote 4 to <a href="#">Table 48: PLL characteristics (wide VCO frequency range)</a>, footnote 4 to <a href="#">Table 49: PLL characteristics (medium VCO frequency range)</a>, and footnote 1 to <a href="#">Table 104: V<sub>BAT</sub> monitoring characteristics</a>.</p> <p>Updated <a href="#">Figure 1: STM32H562xx and STM32H563xx block diagram</a> and <a href="#">Figure 86: WLCSP80 marking example (package top view)</a>.</p> <p>Added <a href="#">Figure 18: TFBGA225 ballout</a> and <a href="#">Section 6.10: TFBGA225 package information (B04V)</a>.</p> <p>Minor text edits across the whole document.</p> |

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved

