19-4207; Rev 0; 9/08

EVALUATION KIT AVAILABLE

1-to-8 I²C Bus Switches/Multiplexers with Bus Lock-Up Detection, Isolation, and Notification

General Description

The MAX7356/MAX7357/MAX7358 8-channel I²C switches/multiplexers expand the main I²C bus to any combination of 8 extended I²C buses. They enable a master on the main bus to isolate and communicate with devices or groups of devices that may otherwise have slave address conflicts. Any extended bus can be connected or disconnected by control packets from the main I²C bus writing to the main control register of these I²C switches.

The MAX7357 and MAX7358 feature an enhanced mode that includes a built-in timer used to monitor all extended buses for lock-up conditions. If the clock or data line of any of these buses is low for more than 25ms (typ), a lock condition is detected. An optional interrupt can be generated through the bidirectional $\overline{RST}$/$\overline{INT}$. The master can read the bus lock-up register to find out which extended bus is locked up. The master can also enable the MAX7357 or the MAX7358 to send a "flush-out" sequence on the faulty channel. There is an optional preconnection check that can be enabled to toggle the extended bus clock and data line low then high to ensure the downstream bus is not locked high prior to connecting it to the host bus.

The MAX7356/MAX7357/MAX7358 are transparent to signals sent and received at each channel, allowing multiple masters. Any device connected to an I²C bus can transmit and receive signals; however, only the master connected to the host side of the MAX7356/MAX7357/MAX7358 should address the device.

The MAX7356/MAX7357/MAX7358 are available in 24-pin TSSOP and TQFN packages and are specified over the extended -40°C to +85°C temperature range.

Applications

Servers
RAID
Base Stations
Control and Automation Devices
SFP Control Interface
Networking Equipment

Features

- **Bus Lock-Up Detection and Isolation (MAX7357, MAX7358)**
- **Host Notification on Detection of Lock-Up (MAX7357, MAX7358)**
- **Maintain Fault Diagnostic Information (MAX7357, MAX7358)**
- **Dual-Function $\overline{RST}$/$\overline{INT}$ Provides Lock-Up Notification and Hardware Reset (MAX7357, MAX7358)**
- **$\overline{RST}$ Input Resets I²C Interface (MAX7358)**
- **3 Address Control Inputs**
- **Low R_{ON} Switches**
- **Logic-Level Translation**
- **Low 0.1µA (typ) Standby Current**
- **Support Hot Insertion**
- **100kbps Standard-Mode or 400kbps Fast-Mode I²C Interface**
- **Address Translation Allows Multiple Device with Same ID**
- **5.5V-Tolerant Inputs**
- **2.3V to 5.5V Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7356ETG+	-40°C to +85°C	24 TQFN-EP*
MAX7356EUG+**	-40°C to +85°C	24 TSSOP
MAX7357ETG+	-40°C to +85°C	24 TQFN-EP*
MAX7357EUG+**	-40°C to +85°C	24 TSSOP
MAX7358ETG+	-40°C to +85°C	24 TQFN-EP*
MAX7358EUG+**	-40°C to +85°C	24 TSSOP

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Selector Guide

PART	ENHANCED MODE	PRECONNECTION WIGGLE TEST	POWER-UP STATE	$\overline{RST}$/$\overline{INT}$ BIDIRECTIONAL
MAX7356	No	No	Basic mode	$\overline{RST}$ only
MAX7357	Yes	Yes, enhanced mode only	Enhanced mode	Yes
MAX7358	Yes	Yes, enhanced mode only	Basic mode	Yes

Typical Operating Circuit and Pin Configurations appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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1-to-8 I²C Bus Switches/Multiplexers with Bus Lock-Up Detection, Isolation, and Notification

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
- V_{DD} ..... -0.3V to +6.0V
- All Other Pins.....-0.3V to +6.0V

Input Currents
- V_{DD} 100mA
- GND 100mA

All Input Pins.....±20mA
Output Current 25mA
Continuous Power Dissipation (T_A = +70°C)
- 24-Pin TSSOP (derate 13.9mW/°C above +70°C) 1111mW
- 24-Pin TQFN (derate 27.8mW/°C above +70°C) 2222mW

Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
- 24-Pin TSSOP.....13°C/W
- 24-Pin TQFN.....3.0°C/W

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
- 24-Pin TSSOP.....72.0°C/W
- 24-Pin TQFN.....36.0°C/W

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (3.3V SUPPLY)

(V_{DD} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C.) (Notes 2–5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{DD}			2.3		3.6	V
Supply Current	I_{DD}	V_{DD} = 3.6V; no load, f_{SCL} = 400kHz	Basic mode		30	50	µA
			Enhanced mode (MAX7357/MAX7358 only)		45	70	
Standby Current	I_{STB}	No load, V_I = V_{DD} or GND, V_{DD} = 3.6V			0.1	1	µA
Power-On Reset Voltage	V_{POR}	V_{DD} rising		0.9	1.4	2.1	V
Power-On Reset Hysteresis	V_{HYST}				0.4		V
INPUT SCL, INPUT/OUTPUT SDA							
Low-Level Input Voltage	V_{IL}					0.3 x V_{DD}	V
High-Level Input Voltage	V_{IH}			0.7 x V_{DD}			V
Low-Level Output Current	I_{OL}	V_{OL} = 0.4V		3			mA
		V_{OL} = 0.6V		6			
Input Leakage Current	I_{LH}, I_{LI}	V_{SCL} and V_{SDA} = V_{DD} or GND		-1		+1	µA
Input Capacitance	C_I	V_I = GND			15		pF
SELECT INPUTS A0 to A2, $\overline{RST}$							
Low-Level Input Voltage	V_{IL}					0.3 x V_{DD}	V
High-Level Input Voltage	V_{IH}			0.7 x V_{DD}			V
Input Leakage Current	I_{LI}	A0 to A2, and $\overline{RST}$ at V_{DD} or GND		-1		+1	µA
Input Capacitance	C_I	V_I = GND			2		pF

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ELECTRICAL CHARACTERISTICS (3.3V SUPPLY) (continued)

(V_{DD} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C.) (Notes 2–5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PASS GATE							
Switch Resistance	R_{ON}	V_{DD} = 3.0V to 3.6V, V_O = 0.4V, I_O = 15mA		5	11	30	Ω
		V_{DD} = 2.3V to 2.7V, V_O = 0.4V, I_O = 10mA		7	16	55	
Switch Output Voltage	V_{SW}	V_{SWin} = V_{DD} = 3.3V, I_{SWout} = -100µA			1.9		V
		V_{SWin} = V_{DD} = 3.0V to 3.6V, I_{SWout} = -100µA		1.6		2.8	
		V_{SWin} = V_{DD} = 2.5V, I_{SWout} = -100µA			1.5		
		V_{SWin} = V_{DD} = 2.3V to 2.7V, I_{SWout} = -100µA		1.1		2.0	
Leakage Current	I_L	V_I = V_{DD} or GND	Basic mode	-1		+1	µA
			Enhanced mode (MAX7357/MAX7358)	-2		+2	
Input/Output Capacitance	C_{IO}	V_I = GND			3		pF
OUTPUT $\overline{RST}$/$\overline{INT}$							
Low-Level Output Current	I_{OL}	V_{OL} = 0.4V (MAX7357/MAX7358)		3			mA
Leakage Current	I_{LH}, I_{LI}	$V_{\overline{RST}/\overline{INT}}$ = V_{DD} or GND		-1		+1	µA

ELECTRICAL CHARACTERISTICS (5V SUPPLY)

(V_{DD} = +4.5V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Notes 2–5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{DD}			4.5		5.5	V
Supply Current	I_{DD}	V_{DD} = 5V; no load, f_{SCL} = 400kHz	Basic mode		65	100	µA
			Enhanced mode (MAX7357/MAX7358 only)		90	130	
Standby Current	I_{STB}	No load, V_I = V_{DD} or GND, V_{DD} = 5.5V			0.2	1	µA
Power-On Reset Voltage	V_{POR}	V_{DD} rising		0.9	1.4	2.1	V
Power-On Reset Hysteresis	V_{HYST}				0.4		V
INPUT SCL, INPUT/OUTPUT SDA							
Low-Level Input Voltage	V_{IL}					0.3 x V_{DD}	V
High-Level Input Voltage	V_{IH}			0.7 x V_{DD}			V
Low-Level Output Current	I_{OL}	V_{OL} = 0.4V		3			mA
		V_{OL} = 0.6V		6			
Input Leakage Current	I_{LH}, I_{LI}	V_{SCL} = V_{SDA} = V_{DD} or GND		-1		+1	µA
Input Capacitance	C_I	V_I = GND			15		pF
SELECT INPUTS A0 TO A2, $\overline{RST}$							
Low-Level Input Voltage	V_{IL}					0.3 x V_{DD}	V
High-Level Input Voltage	V_{IH}			0.7 x V_{DD}			V
Input Leakage Current	I_{LI}	A0 to A2, and $\overline{RST}$ pins at V_{DD} or GND		-1		+1	µA

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ELECTRICAL CHARACTERISTICS (5V SUPPLY) (continued)

(V_{DD} = +4.5V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Notes 2–5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_I	V_I = GND			2		pF
PASS GATE							
Switch Resistance	R_{ON}	V_{DD} = 4.5V to 5.5V, V_O = 0.4V, I_O = 15mA		4	9	24	Ω
Switch Output Voltage	V_{SW}	V_{SWin} = V_{DD} = 5.0V, I_{SWout} = -100µA			3.6		V
		V_{SWin} = V_{DD} = 4.5V to 5.5V, I_{SWout} = -100µA		2.6		4.5	
Leakage Current	I_L	V_I = V_{DD} or GND	MAX7356	-1		+1	µA
			Enhanced mode (MAX7357/MAX7358)	-2		+2	
Input/Output Capacitance	C_{IO}	V_I = GND			3		pF
OUTPUT $\overline{RST}/\overline{INT}$							
Low-Level Output Current	I_{OL}	V_{OL} = 0.4V (MAX7357/MAX7358)		3			mA
Leakage Current	I_{LH}, I_{LI}	$V_{\overline{RST}/\overline{INT}}$ = V_{DD} or GND		-1		+1	µA

TIMING CHARACTERISTICS (STANDARD-MODE) (Figures 1, 2, 3)

(V_{DD} = 2.3V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from SDA to SD_ or SCL to SC_	t_{PD}	(Note 7)			0.3	ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		4.7			µs
Hold Time (Repeated) START Condition After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$		4.0			µs
LOW Period of the SCL Clock	t_{LOW}		4.7			µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0			µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		4.7			µs
Setup Time for a STOP Condition	$t_{SU;STO}$		4.0			µs
Data Hold Time	$t_{HD;DAT}$	(Note 8)	0		3.45	µs
Data Setup Time	$t_{SU;DAT}$		250			ns
Rise Time of Both SDA and SCL Signals	t_R				1000	ns
Fall Time of Both SDA and SCL Signals	t_F				300	ns
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spikes that Must be Suppressed by the Input Filter	t_{SP}				50	ns

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TIMING CHARACTERISTICS (STANDARD-MODE) (Figures 1, 2, 3) (continued)

(V_{DD} = 2.3V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid Time	$t_{VD;DAT}$	(High to low)			1	µs
		(Low to high)			0.6	
Data Valid Acknowledge	$t_{VD:ACK}$				1	µs
Low-Level Reset Time	$t_{WL(rst)}$			5		ns
Reset Time	t_{rst}		500			ns
Recovery to Start	$t_{REC;STA}$		0			ns

TIMING CHARACTERISTICS (FAST-MODE) (Figures 1, 2, 3)

(V_{DD} = 2.3V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from SDA to SD_ or SCL to SC_	t_{PD}	(Note 7)			0.3	ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$		0.6			µs
LOW Period of the SCL Clock	t_{LOW}		1.3			µs
HIGH Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6			µs
Setup Time for a STOP Condition	$t_{SU;STO}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$	(Note 8)	0		0.9	µs
Data Setup Time	$t_{SU;DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R		$20 + 0.1C_b$		300	ns
Fall Time of Both SDA and SCL Signals	t_F		$20 + 0.1C_b$		300	ns
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spikes that Must be Suppressed by the Input Filter	t_{SP}				50	ns
Data Valid Time	$t_{VD;DAT}$	(High to low)			1	µs
		(Low to high)			0.6	
Data Valid Acknowledge	$t_{VD;ACK}$				1	µs
Low-Level Reset Time	$t_{WL(rst)}$			5		ns
Reset Time	t_{rst}		500			ns
Recovery to START	$t_{REC;STA}$		0			ns

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TIMING CHARACTERISTICS (FAST-MODE) (Figures 1, 2, 3) (continued)

(V_{DD} = 2.3V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 6)

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications are over -40°C to +85°C and are guaranteed by design.
Note 3: Subscript SW refers to all SC_ and SD_ pins.
Note 4: V_{SWin} = Switch input voltage; I_{SWout} = Current between SD_ and SDA or SC_ and SCL. See Figure 4.
Note 5: V_I = $V_{SD_}$ or $V_{SC_}$.
Note 6: All timing is measured using 20% and 80% levels, unless otherwise noted.
Note 7: Pass gate propagation delay is calculated from the 20Ω typical R_{ON} and the 15pF load capacitance.
Note 8: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signed) to bridge the undefined region of the falling edge of SCL.

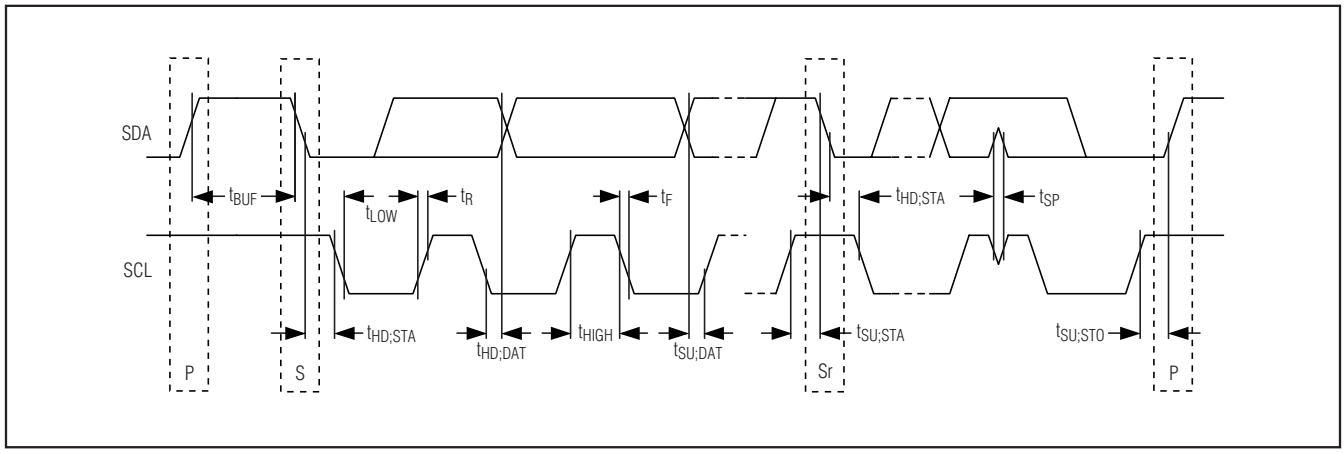


Figure 1. 2-Wire Serial-Interface Timing Diagram

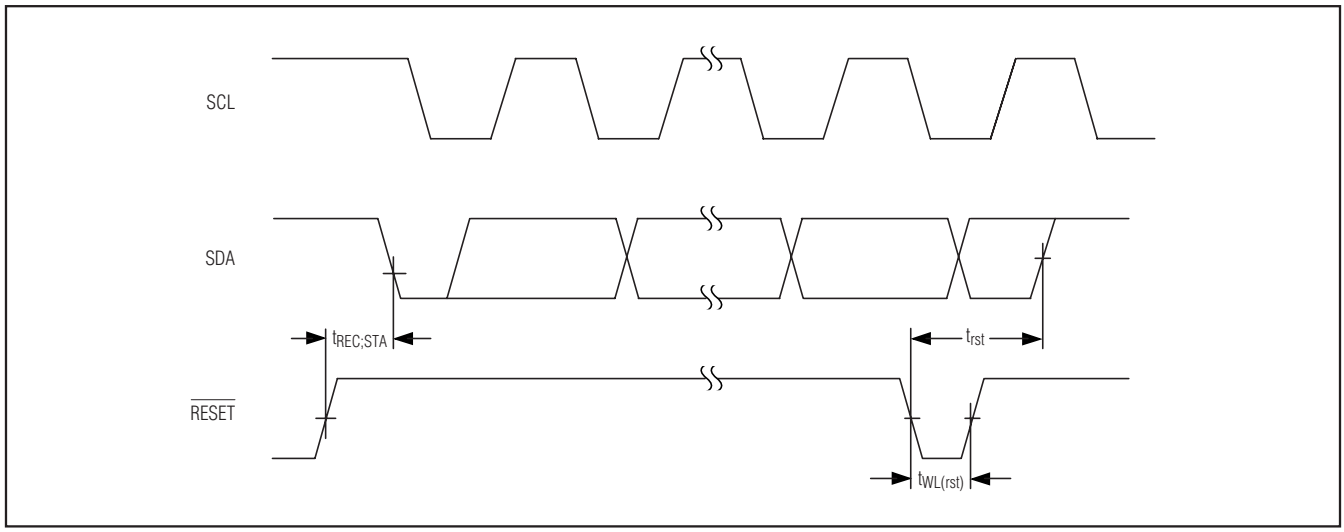


Figure 2. $\overline{RST}$ Timing Diagram

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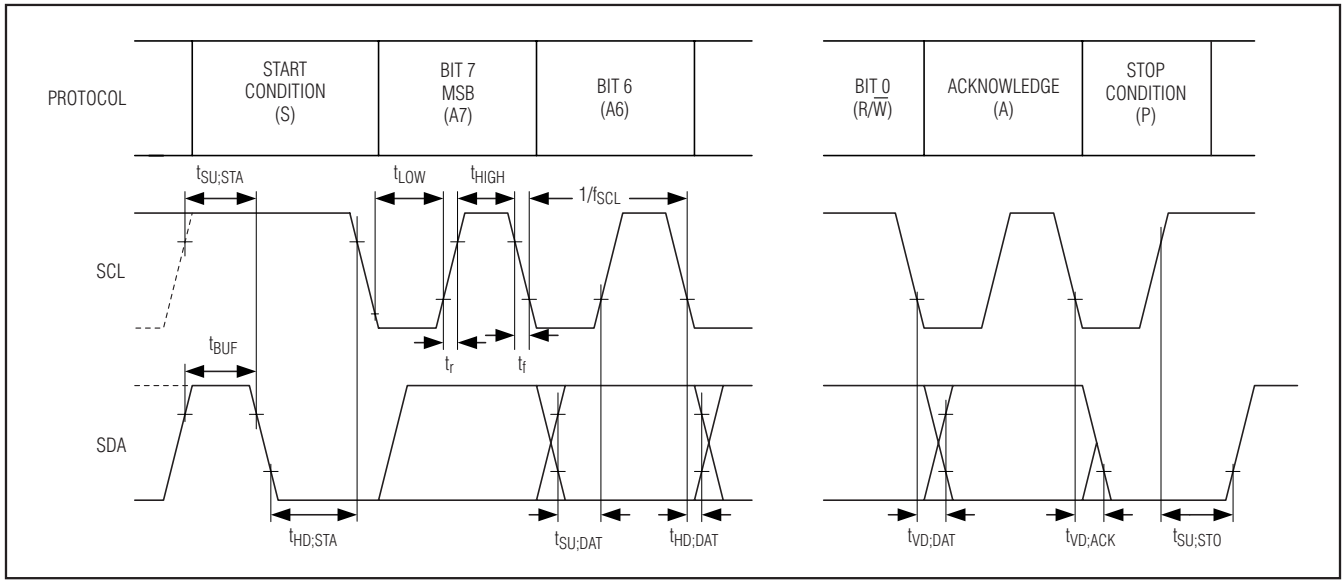


Figure 3. I²C Bus Timing Diagram

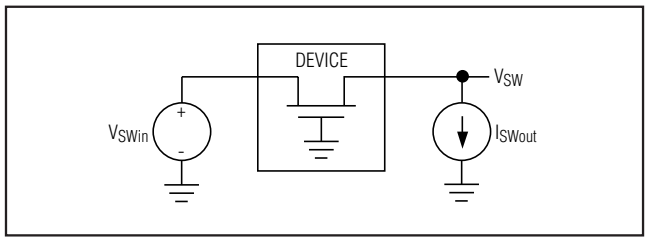
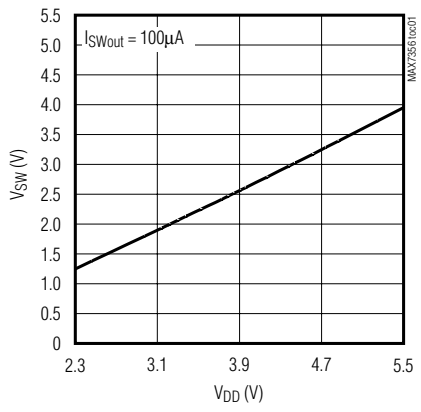


Figure 4. Switch Output Voltage and Current

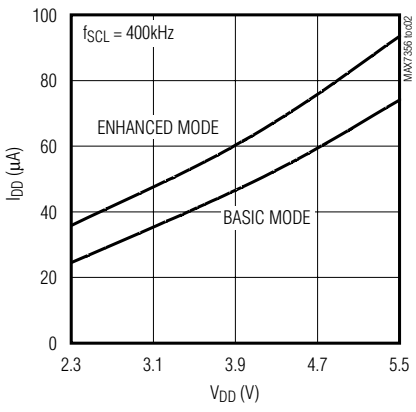
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

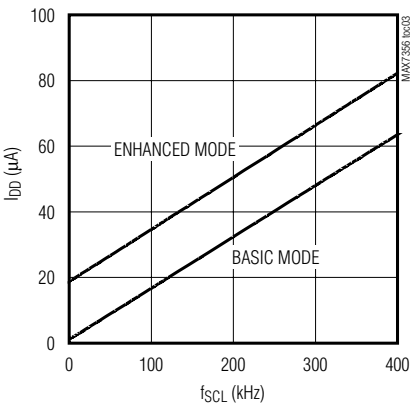
V_{SW} vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SCL FREQUENCY



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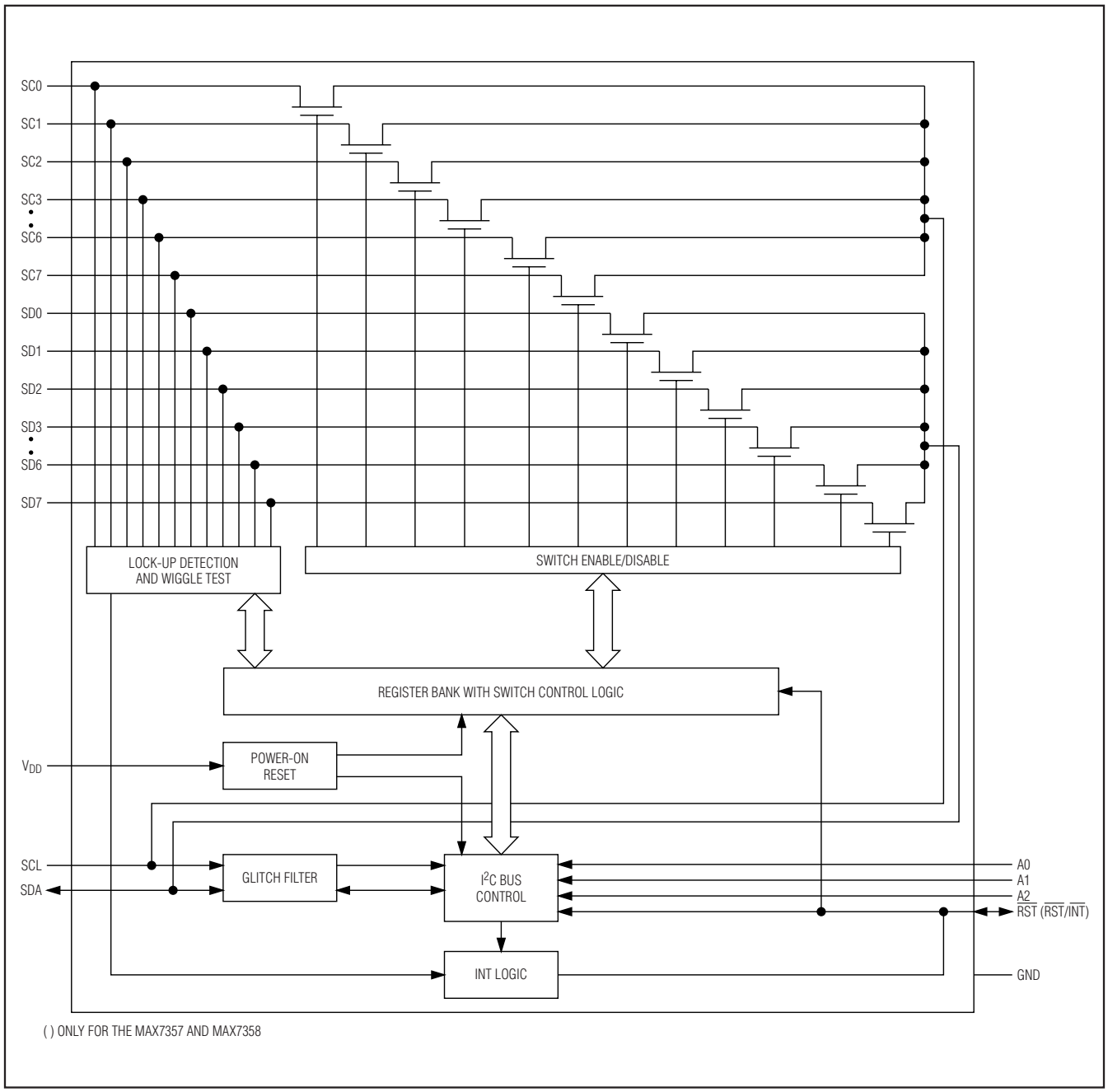
Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	4	SD0	I²C Bus0 Serial Data
2	5	SC0	I²C Bus0 Serial Clock
3	6	SD1	I²C Bus1 Serial Data
4	7	SC1	I²C Bus1 Serial Clock
5	8	SD2	I²C Bus2 Serial Data
6	9	SC2	I²C Bus2 Serial Clock
7	10	SD3	I²C Bus3 Serial Data
8	11	SC3	I²C Bus3 Serial Clock
9	12	GND	Supply Ground
10	13	SD4	I²C Bus4 Serial Data
11	14	SC4	I²C Bus4 Serial Clock
12	15	SD5	I²C Bus5 Serial Data
13	16	SC5	I²C Bus5 Serial Clock
14	17	SD6	I²C Bus6 Serial Data
15	18	SC6	I²C Bus6 Serial Clock
16	19	SD7	I²C Bus7 Serial Data
17	20	SC7	I²C Bus7 Serial Clock
18	21	A2	Device Address Bit 2
19	22	SCL	Main I²C Bus Clock
20	23	SDA	Main I²C Bus Data
21	24	V_{DD}	Supply Voltage
22	1	A0	Device Address Bit 0
23	2	A1	Device Address Bit 1
24	3	$\overline{RST}$ ($\overline{RST}$/$\overline{INT}$)	Active-Low Reset Input and Interrupt Output. $\overline{RST}$ resets the MAX7356 by a host. $\overline{RST}$/$\overline{INT}$ on the MAX7357 or MAX7358 is bidirectional. $\overline{RST}$/$\overline{INT}$ is used to reset the device by a host or by the device to send an interrupt signal to the host.
—	—	EP	Exposed Pad (TQFN Only). Connect EP to ground. Do not use EP as the only ground connection.

( ) For the MAX7357/MAX7358 only.

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Functional Diagram



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1-to-8 I²C Bus Switches/Multiplexers with Bus Lock-Up Detection, Isolation, and Notification

Detailed Description

The MAX7356/MAX7357/MAX7358 devices are 1-to-8 I²C multiplexers/switches for connecting a large number of I²C components to a single master. The circuits connect a main I²C bus to any combination of 8 extended I²C buses. They enable a master on the main bus to isolate and communicate with devices or groups of devices that may otherwise have slave address conflicts. Any extended bus can be connected or disconnected by control packets from the main I²C bus writing to the main control register of these I²C switches.

The MAX7357/MAX7358 feature a built-in timer used to monitor all extended buses, for lock-up conditions. If the data line of any of these buses is low for more than 25ms, a lock condition is detected. An optional interrupt can be generated through the bidirectional $\overline{RST}/\overline{INT}$ pin. The master can read the bus lock-up register to find out which extended bus is locked up. The master can also optionally enable the MAX7357 or MAX7358 to send a flush-out sequence on the faulty channel. There is an optional preconnection check that can be enabled, which toggles the extended bus clock and data line low then high to ensure that the downstream bus is not locked high prior to connecting it to the host bus.

The bus lock-up detection and isolation features are enabled by writing a unique series of I²C commands to the MAX7357/MAX7358.

Power-On Reset

When power is applied to V_{DD}, an internal power-on reset (POR) holds the MAX7356/MAX7357/MAX7358 in a reset state until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the MAX7356/MAX7357/MAX7358 registers and I²C state machine are initialized to their default states.

Basic Mode of Operation

The MAX7356/MAX7357/MAX7358 feature a basic mode of operation. In basic mode, the device operates solely as a collection of analog switches that enable any combination of the extended buses (SC_, SD_) to be connected to the host-side bus (SCL, SDA). Only the switch control register is accessible in basic mode of operation.

Enhanced Mode of Operation (MAX7357/MAX7358)

The MAX7357 and MAX7358 feature an enhanced mode of operation that enable features and registers that are unavailable in the basic mode of operation. When operating in enhanced mode, there are 7 registers available to the host. Features such as bus lock-up detection, preconnection fault tests, and diagnostic information are made available to the user. A special sequence of commands can switch the MAX7357 or MAX7358 from basic mode to enhanced mode, and a simple write to the configuration register can switch the devices from enhanced mode back to basic mode.

Entering Basic Mode from Enhanced Mode (MAX7357/MAX7358)

When the 7 registers of Table 2 are enabled, the MAX7357 and MAX7358 can be put into basic mode by setting bit B6 of the configuration register. When basic mode is entered, the value of all registers return to their POR value. B6 of the configuration register is also maintained to allow operation in basic mode. When in basic mode, the MAX7357 and MAX7358 can be returned to full feature mode by receiving a special sequence of commands from the host as described below.

The sequence of I²C commands for enabling the MAX7357 or MAX7358 enhanced features (bus lock-up detection, isolation, and notification) as well as access to the additional 6 registers consists of a write byte, a read byte, another write byte, and another read byte with no data bytes following any of these write or read bytes, as shown in Figure 5. A write byte consists of the 7-bit MAX7357 or MAX7358 device address followed by a 0. A read byte consists of the 7-bit MAX7357 or MAX7358 device address followed by a 1. The special sequence begins with a START condition and ends with a STOP condition. Repeated START conditions are used to interconnect these write and read bytes.

The complete special sequence of I²C commands needs to be received by the MAX7357 or MAX7358 to activate the enhanced mode.

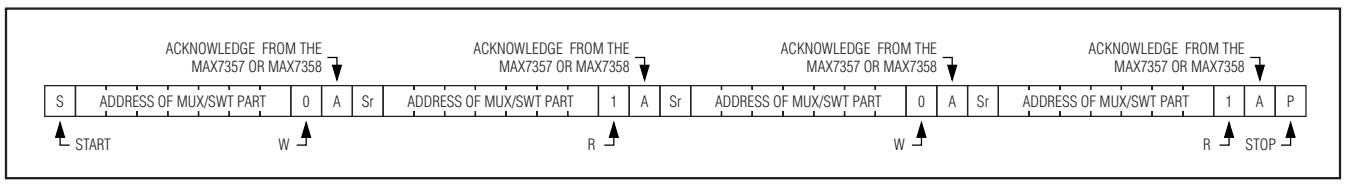


Figure 5. The Special Sequence of I²C Commands for Turning on the Full Feature

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1-to-8 I²C Bus Switches/Multiplexers with Bus Lock-Up Detection, Isolation, and Notification

Bus Lock-Up Detection, Isolation, and Notification Operation (MAX7357/MAX7358)

SDA Stuck Low

If either line of any downstream bus is low for a period exceeding 25ms between t_1 and t_2 in Figure 6, the MAX7357/MAX7358 detect a lock-up fault on that bus and takes the action configured by the user. If the lock-up is not on the main bus, SDA and SCL return to the high state at the same time. The MAX7357 or MAX7358 then identifies which SD_ or SC_ is still pulled low. If the optional interrupt function is enabled (by setting B0 of the configuration register), an active-low interrupt is generated at $\overline{RST}/\overline{INT}$.

If B4 in the configuration register is set to 1, then only faults on connected buses cause the MAX7357 or MAX7358 to disconnect all buses from each other. When this is the case, faults detected on disconnected buses set the flag in the lock-up status register, and, if enabled, notify the host of the fault, but do not disconnect the buses from one another.

B1 of the configuration register enables the flush-out sequence. If this bit is set to 1, the MAX7357 or MAX7358 attempts to send a flush-out sequence over the locked SD_ and SC_ pair (the sequence begins at t_5 in Figure 6). If the flush-out sequence is successful, the locked bus (SD_ and SC_) is released at t_6 (Figure 6). The I²C master (at SDA and SCL) reads the MAX7357 or MAX7358 lock-up status register to identify the locked-up bus. If $\overline{RST}/\overline{INT}$ is enabled as an interrupt, it is released once a read command to the lock-up indication register is received by the MAX7357 or MAX7358 (shown at t_7 in Figure 6). The $\overline{RST}/\overline{INT}$ can also be automatically released after a 1.6s delay by setting bit 2 of the configuration register.

Preconnection Wiggle Test (Stuck High Fault) (MAX7357/MAX7358)

By setting bit B7 in the configuration register to 1, a preconnection wiggle test is enabled for all downstream buses. This test only runs on the downstream bus when the bus is selected through the switch control register. Enabling this test does not affect any bus that is already connected to the host bus; however, deselecting and subsequently reselecting the bus will cause the test to occur. The test is performed when the switch control register bit (or bits if multiple buses are selected in the same I²C transaction) toggles from 0 to 1 and a stop condition is received. It consists of the MAX7357 or MAX7358 pulling the downstream clock line low, then the downstream data line low. Both lines are checked for a nominal low value, and then the clock line is released followed by the data line (**Note:** This is an I²C stop condition and is seen by any I²C devices connected to the extended bus). If either the clock or data line (or both) fail to pull low during the test, the MAX7357 or MAX7358 do not allow that downstream bus to connect to the host. If the optional interrupt notification bit is set (B0), the device notifies the host that a fault has occurred. The I²C master can then read the MAX7357 or MAX7358 registers to find out which bus or buses caused the fault. Faults detected by this test are stored in the preconnection fault register (0x06). The stuck high Fault register is cleared once this register is read, resetting the device, or disabling the preconnection test.

Device Address

The MAX7356/MAX7357/MAX7358 family of devices has selectable device addresses through three external inputs. The slave address consists of 4 fixed bits (A6–A3 set to 1110); followed by 3 pin-programmable bits (A2, A1, A0), as shown in Figure 7. The addresses A2, A1, and A0 can also be driven dynamically if required, but the values must be stable when they are expected in the address sequence.

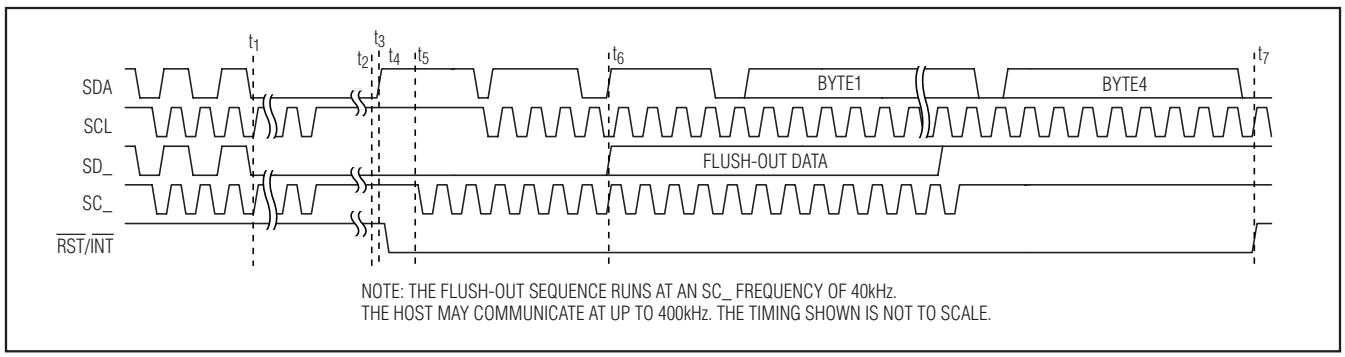


Figure 6. Bus Lock-Up Detection, Isolation, and Notification Timing Diagram

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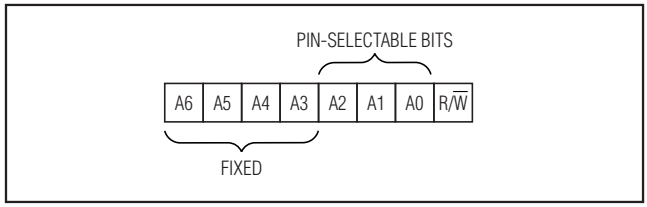


Figure 7. MAX7356/MAX7357/MAX7358 Slave Address

Available addresses depend on the hardware connections of pins A2, A1, and A0 as shown in Table 1.

The last bit following the slave address bit A0 on an I²C command defines the operation to be performed. When the last bit sets to logic 1, a read is selected while logic 0 selects a write operation.

Register Map (MAX7357/MAX7358)

The MAX7357 and MAX7358 have 7 registers (shown in Table 2) that can be accessed through the I²C bus. The MAX7357 powers up with all of these registers accessible. The initial register address counter is at 0x00. The MAX7358 powers up in basic mode with only the switch control register available. Writing to a MAX7358 changes only the contents of the switch control register. By sending a unique I²C sequence to the MAX7358, all 7 registers become available.

Register Access Protocol (MAX7356)

Only the MAX7356 device address is required to gain access to its registers. A typical I²C command to communicate with the MAX7356 starts with its device address followed directly by data bytes.

Table 1. MAX7356/MAX7357/MAX7358 Switch Multiplexer Device Address

A2 CONNECTION	A1 CONNECTION	A0 CONNECTION	A6	A5	A4	A3	A2	A1	A0
GND	GND	GND	1	1	1	0	0	0	0
GND	GND	V_{DD}	1	1	1	0	0	0	1
GND	V_{DD}	GND	1	1	1	0	0	1	0
GND	V_{DD}	V_{DD}	1	1	1	0	0	1	1
V_{DD}	GND	GND	1	1	1	0	1	0	0
V_{DD}	GND	V_{DD}	1	1	1	0	1	0	1
V_{DD}	V_{DD}	GND	1	1	1	0	1	1	0
V_{DD}	V_{DD}	V_{DD}	1	1	1	0	1	1	1

Table 2. MAX7357/MAX7358 Enhanced-Mode Register Map

REGISTER NAME	INTERNAL ADDRESS	POR DEFAULT SETTING								NEXT ADDRESS	ACCESS
		B7	B6	B5	B4	B3	B2	B1	B0		
Switch Control	0x00	0	0	0	0	0	0	0	0	0x01	R/$\overline{W}$
Configuration	0x01	0	0	0	0	0	0	0	1	0x02	R/$\overline{W}$
Flush-Out Sequence	0x02	1	1	1	1	1	1	1	1	0x00 (W) 0x03 (R)	R/$\overline{W}$
Lock-Up Indication	0x03	0	0	0	0	0	0	0	0	0x04	R
Traffic Prior to Lock-Up	0x04	0	0	0	0	0	0	0	0	0x05	R
	0x05	0	0	0	0	0	0	0	0	0x06	R
Stuck High Fault	0x06	0	0	0	0	0	0	0	0	0x00	R

Table 3. MAX7357 and MAX7358 Basic-Mode Register Map

REGISTER NAME	POR DEFAULT SETTING								ACCESS
	B7	B6	B5	B4	B3	B2	B1	B0	
Switch Control	0	0	0	0	0	0	0	0	R/$\overline{W}$

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Table 4. Switch Control Register Channel Selection

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
X	X	X	X	X	X	X	1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
X	X	X	X	X	X	1	X	Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
X	X	X	X	X	1	X	X	Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
X	X	X	X	1	X	X	X	Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
X	X	X	1	X	X	X	X	Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
X	X	1	X	X	X	X	X	Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
X	1	X	X	X	X	X	X	Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1	X	X	X	X	X	X	X	Channel 7 enabled

X = Don't care.

Only the switch control register can be accessed through an I²C write or read command. All data bytes are for the switch control register. The last data byte in an I²C write command is retained by the switch control register.

Register Access Protocol (MAX7357/MAX7358)

Only the MAX7357 or MAX7358 I²C device address is required to gain access to its registers. A typical I²C command to communicate with the MAX7357 or MAX7358 starts with its device address and is followed directly by data bytes. Internal register addresses are not used in an I²C write or read command.

For enhanced mode, all registers are accessed in sequence starting with the switch control register and follows the order defined by internal register addresses as shown in Table 2. Internal register addresses are 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, and 0x06 for switch control, configuration, flush-out sequence, lock-up indication, first and second bytes of the traffic prior to lock-up, and preconnection fault registers, respectively. When writing data to the register(s), addressing starts with address 0x00 and goes one higher in each subsequent byte and comes back to 0x00 again after 0x02 since the next four higher addressed registers are read only. Read access also starts with the internal register address 0x00 and goes one higher in each subsequent byte and comes back to 0x00 again after 0x06.

For basic mode, only the switch control register can be accessed through an I²C write or read command. All data bytes are for the switch control register. The last data byte in an I²C write command is retained by the switch control register. Incomplete bytes are ignored.

Switch Control Register

The switch control register (Figure 8) selects which channels will be connected to the main I²C bus. This register can be written and read through the main I²C bus. The POR value for the switch control register is 0x00—all switches disconnected.

A SC_/SD_ downstream pair, or channel, is selected by the contents of the switch control register. All bits of the control byte are used to determine which channel is to

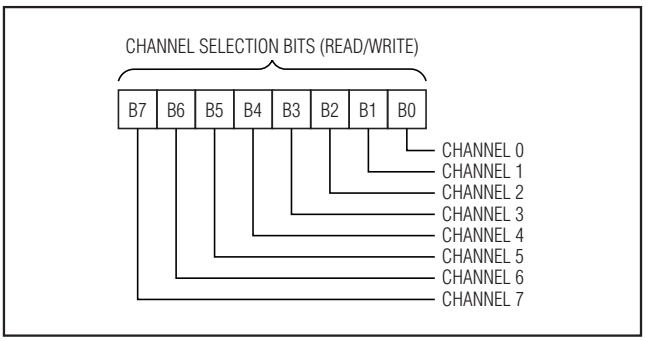


Figure 8. Switch Control Register

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Table 5. Configuration Register Definition

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Interrupt with $\overline{RST}/\overline{INT}$ disabled
X	X	X	X	X	X	X	1	Interrupt with $\overline{RST}/\overline{INT}$ enabled
X	X	X	X	X	X	0	X	Flush-out disabled
X	X	X	X	X	X	1	X	Flush-out enabled
X	X	X	X	X	0	X	X	$\overline{RST}/\overline{INT}$ released after a register read
X	X	X	X	X	1	X	X	$\overline{RST}/\overline{INT}$ released after 1.6 seconds
X	X	X	X	0	X	X	X	The lock-up register shows the current condition
X	X	X	X	1	X	X	X	The lock-up register data is not cleared until a read
X	X	X	0	X	X	X	X	Disconnect all channels on bus lock-up
X	X	X	1	X	X	X	X	Disconnect only the locked up bus
X	X	0	X	X	X	X	X	Bus lock-up detection enabled
X	X	1	X	X	X	X	X	Bus lock-up detection disabled
X	0	X	X	X	X	X	X	Enhanced mode
X	1	X	X	X	X	X	X	Basic mode enabled
0	X	X	X	X	X	X	X	Preconnect test is disabled
1	X	X	X	X	X	X	X	Preconnect test is enabled

X = Don't care.

be selected. More than one channel can be selected simultaneously. When a channel is selected, the channel becomes active immediately after a stop condition has been placed on the I²C bus. This ensures that all SC_/SD_ lines are in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Configuration Register (MAX7357/MAX7358)

B0 = $\overline{RST}/\overline{INT}$ serves as an interrupt when a bus lock-up condition is detected.

B1 = Flush-out sequence is sent automatically on locked-up channels when a lock-up condition is detected.

B2 = When B0 = 1, release the $\overline{RST}/\overline{INT}$ output after asserting for 1.6 seconds.

B3 = Data in the lock-up indication register cleared only after reading the register.

B4 = Connected channels remain connected on detection of lock-up if the lock-up condition is present only on a channel that is not connected.

B5 = Disable bus lock-up detection.

B6 = Basic mode.

B7 = Enables the preconnection wiggle test for SC_ and SD_.

Flush-Out Sequence Register (MAX7357/MAX7358)

A flush-out sequence can be sent to a particular auxiliary bus automatically after the identification of the lock-up condition. The flush-out sequence consists of 18 SC_ clock cycles. An 8-bit sequence for the SD_ to follow during the flush-out cycle can also be defined by writing to the flush-out sequence register. By default, the flush-out sequence register is all ones. The MAX7357 or MAX7358 attempt to send the one-byte sequence followed by an additional clock cycle (NACK) two times sequentially, followed by a stop condition. The effectiveness of sending the flush-out sequence depends on the behavior of the locked-up device. For an auxiliary bus with only slave devices, it is more likely that the SCL line can still be driven by the MAX7357 or MAX7358. In this case, a slave device may respond to a particular flush-out sequence. After the release of the SD_ line by a "stuck" device, the remaining sequence on the SD_ line can be used to reset itself.

Bus Lock-Up Indication Register (MAX7357/MAX7358)

The bus master can read the lock-up indication byte to identify the stuck channels. A bit set to "1" indicates that the associated channel is stuck. The indication for a given channel remains as long as the lock-up condi-

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Table 6. Lock-Up Register Channel Indication

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 no lock-up
X	X	X	X	X	X	X	1	Channel 0 lock-up
X	X	X	X	X	X	0	X	Channel 1 no lock-up
X	X	X	X	X	X	1	X	Channel 1 lock-up
X	X	X	X	X	0	X	X	Channel 2 no lock-up
X	X	X	X	X	1	X	X	Channel 2 lock-up
X	X	X	X	0	X	X	X	Channel 3 no lock-up
X	X	X	X	1	X	X	X	Channel 3 lock-up
X	X	X	0	X	X	X	X	Channel 4 no lock-up
X	X	X	1	X	X	X	X	Channel 4 lock-up
X	X	0	X	X	X	X	X	Channel 5 no lock-up
X	X	1	X	X	X	X	X	Channel 5 lock-up
X	0	X	X	X	X	X	X	Channel 6 no lock-up
X	1	X	X	X	X	X	X	Channel 6 lock-up
0	X	X	X	X	X	X	X	Channel 7 no lock-up
1	X	X	X	X	X	X	X	Channel 7 lock-up

X = Don't care.

tion exists on that channel. If the interrupt feature is selected (B0 of the configuration register is 1), however, the interrupt signal, $\overline{RST}/\overline{INT}$, deasserts (goes to high) once this bus lock-up indication register is read. If desired, setting bit B3 of the configuration register to 1 can latch the lock-up data. When B3 is set, the lock-up bits remain set (even if a channel becomes "unstuck") until the lock-up indication register is read by the master. Lock-up conditions on unconnected auxiliary buses are also detected. When this happens, operation is the same as when lock-ups are detected on connected buses, except that, if desired, bus connections may be maintained as long as any detected lock-ups are present only on unconnected channels. This option is selected using bit B4 of the configuration register. (Figure 9)

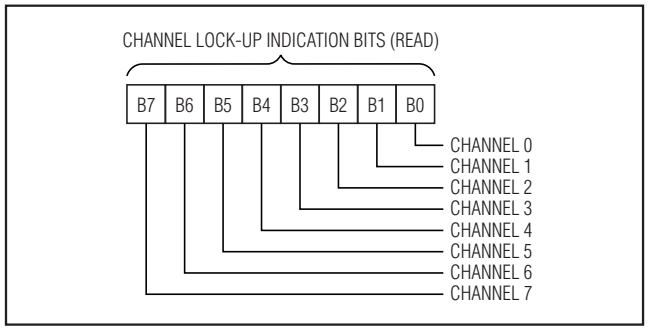


Figure 9. Lock-Up Indication Bits

Traffic Prior to Lock-Up Register (MAX7357/MAX7358)

The I²C bus traffic information per SCL clock is monitored and stored into the two-byte traffic prior to lock-up register. The first two bytes of information after a START are stored in this register. This I²C bus traffic information is frozen upon a bus lock-up detection. A host can read these two bytes of traffic information upon the reception of an interrupt signal. The contents of the traffic prior to lock-up register is released and refreshed once it is read.

The traffic prior to lock-up register can be used to identify the device address as well as the following byte involved in a bus lock-up.

When troubleshooting an I²C bus, a scope is usually used to capture traffic leading to the problem. The contents of the traffic prior to the bus fault can usually be determined by identifying a device address, a register address, or a part of this data.

Table 7 shows contents of the traffic prior to the lock-up register corresponding to a lock-up situation as demonstrated by Figure 10.

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Table 7. A Traffic Prior to Lock-Up Register Contents Example

ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0	NOTE
0x04	0	1	1	0	1	0	0	0	Write to the troubled device address
0x05	0	1	1	0	0	0	0	0	The first data byte with trailing 0's due to lock-up

Table 8. Stuck HIGH Fault Register Channel Indication

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 not stuck high
X	X	X	X	X	X	X	1	Channel 0 stuck high
X	X	X	X	X	X	0	X	Channel 1 not stuck high
X	X	X	X	X	X	1	X	Channel 1 stuck high
X	X	X	X	X	0	X	X	Channel 2 not stuck high
X	X	X	X	X	1	X	X	Channel 2 stuck high
X	X	X	X	0	X	X	X	Channel 3 not stuck high
X	X	X	X	1	X	X	X	Channel 3 stuck high
X	X	X	0	X	X	X	X	Channel 4 not stuck high
X	X	X	1	X	X	X	X	Channel 4 stuck high
X	X	0	X	X	X	X	X	Channel 5 not stuck high
X	X	1	X	X	X	X	X	Channel 5 stuck high
X	0	X	X	X	X	X	X	Channel 6 not stuck high
X	1	X	X	X	X	X	X	Channel 6 stuck high
0	X	X	X	X	X	X	X	Channel 7 not stuck high
1	X	X	X	X	X	X	X	Channel 7 stuck high

X = Don't care.

Stuck HIGH Fault Register (MAX7357/MAX7358)

Following an interrupt when bit B0 and B7 are enabled, the bus master can read the stuck high fault byte to identify stuck channels. A bit set to "1" indicates that the associated channel is stuck, and will not be allowed to be connected to the host bus. The stuck high fault register is cleared, and, if the interrupt feature is enabled, $\overline{RST}/\overline{INT}$ deasserts (goes to high) once this register is read. However, while B7 is set to one, any time a disconnected bus is selected for connection, the preconnect test runs. If the fault still exists, the fault handling sequence repeats and the faulty bus will not be allowed to connect to the host bus.

$\overline{RST}$ (MAX7356)

The $\overline{RST}$ on the MAX7356 can be used to reset the MAX7356 by a host. The $\overline{RST}$ input is an active-low signal. By asserting this signal low for a minimum of $t_{WL(rst)}$ externally, the MAX7356 resets its I²C state machine and deselects all channels. $\overline{RST}$ is overvoltage-tolerant to +6V. The $\overline{RST}$ input must be connected to V_{DD} through a pullup resistor.

$\overline{RST}/\overline{INT}$ (MAX7357/MAX7358)

The $\overline{RST}/\overline{INT}$ on the MAX7357 or MAX7358 is bidirectional. It can be used to reset the device by a host or by the device to send an interrupt signal to the host. The $\overline{RST}/\overline{INT}$ input is an active-low signal. By asserting $\overline{RST}/\overline{INT}$ low for a minimum of $t_{WL(rst)}$ externally, the device resets its registers and I²C state machine and deselects all channels. When $\overline{RST}/\overline{INT}$ is configured to notify the host of fault conditions, and while $\overline{RST}/\overline{INT}$ is being used as an output by the MAX7357 or MAX7358 (sending an interrupt to the host), it does not function as a reset input. $\overline{RST}/\overline{INT}$ is overvoltage-tolerant to +6V. $\overline{RST}/\overline{INT}$ must be connected to V_{DD} through a pullup resistor.

Interrupt Signal (MAX7357/MAX7358)

A bus lock-up-caused interrupt signal can be sent to a host through the bidirectional $\overline{RST}/\overline{INT}$ pin depending on whether or not bit B0 of the configuration register is set. Configuration register bit B2 controls how the interrupt signal is reset. When B2 = 0, the interrupt signal asserts (stays low) until the lock-up indication register is read. When B2 = 1, the interrupt signal deasserts after

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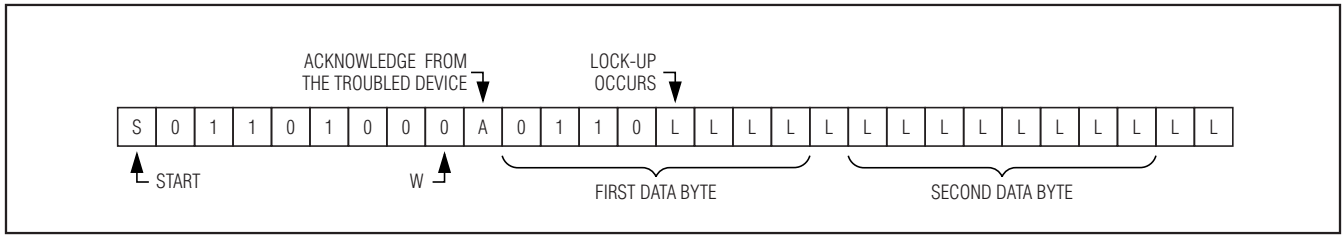


Figure 10. Bus Lock-Up During a 3-Byte Write Command

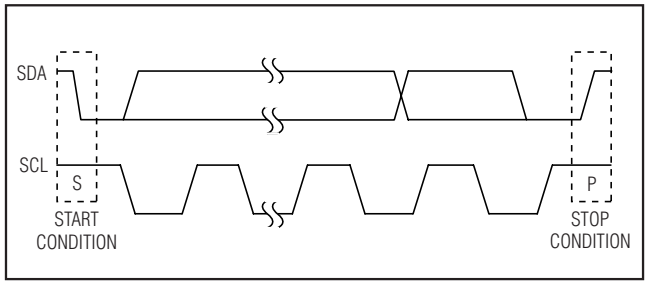


Figure 11. Start and Stop Conditions

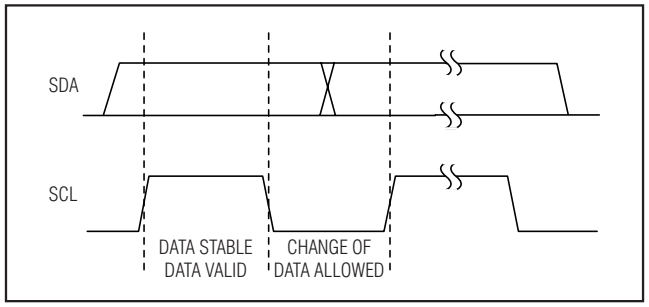


Figure 12. Bit Transfer

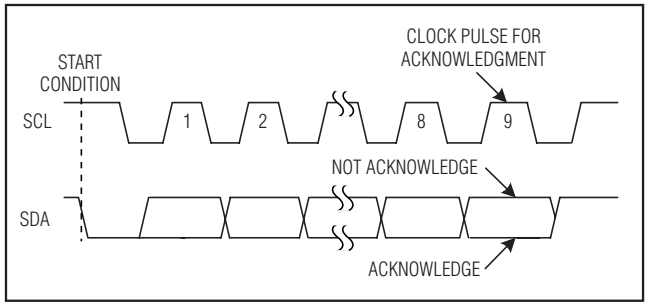


Figure 13. Acknowledge

2 seconds. The interrupt signal asserts again once a new lock-up is detected. The interrupt signal does not activate the reset function.

Serial Interface

Serial Addressing

The MAX7356/MAX7357/MAX7358 operate as a slave that sends and receives data through an I²C interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). The master initiates all data transfers to and from the MAX7357 or MAX7358 and generates the SCL clock that synchronizes the data transfer.

SDA operates as both an input and an open-drain output. A pullup resistor (4.7kΩ, typ) is required on SDA. SCL operates only as an input. A pullup resistor (4.7kΩ, typ) is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7356/MAX7357/MAX7358's 7-bit slave address plus R/$\overline{W}$ bit, and then optionally 1 or more data bytes, and finally a STOP condition (Figure 10).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. The master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 11).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 12).

Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to handshake receipt of each byte of data (Figure 13). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7356/MAX7357/MAX7358, the MAX7356/MAX7357/MAX7358 generate the acknowl-

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edge bit because the device is the recipient. When the MAX7356/MAX7357/MAX7358 are transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7356/MAX7357/MAX7358 have 7-bit-long slave addresses (Figure 6). The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, and high for a read command.

Accessing the MAX7356

A **single-byte write** to the MAX7356 sets the switch control register.

A **multibyte write** to the MAX7356 writes repeatedly to the switch control register. The last byte written determines the contents of the register.

A **single-byte read** from the MAX7356 returns the contents of the switch control register.

A **multibyte read** (2 or more bytes before the I²C STOP bit) from the MAX7356 returns the contents of the switch control register repeatedly.

Accessing the MAX7357/MAX7358 in Enhanced Mode

In enhanced mode, all 7 registers are enabled. These registers are autoincremented starting with the switch control register during each I²C transaction. When a new transaction begins, the switch control register is the first register accessed.

A **single-byte write** to the MAX7357 or MAX7358 sets the switch control register.

A **2-byte write** to the MAX7357 or MAX7358 sets the switch control and configuration registers.

A **3-byte write** to the MAX7357 or MAX7358 sets the switch control, configuration, and flush-out sequence registers.

A **multibyte write** to the MAX7357 or MAX7358 with more than three bytes sets the first three registers, then resets the pointer back to the switch control register (0x00) since the remaining registers are read only. Subsequent bytes of data, after 3 bytes, begin overwriting the first set of data starting with 0x00, 0x01, 0x02, then looping back to 0x00 again, and continuing until a STOP condition is received.

A **single-byte read** from the MAX7357 or MAX7358 returns the contents of the switch control register.

A **multibyte read** from the MAX7357 or MAX7358 returns contents of all 7 registers in sequence and repeats.

The internal register address count always begins with the switch control register, 0x00.

Accessing the MAX7357/MAX7358 in Basic Mode

In basic mode, only the switch control register is enabled.

A **single-byte write** to the MAX7357 or MAX7358 sets the switch control register.

A **multibyte write** to the MAX7357 or MAX7358 in basic mode writes repeatedly to the switch control register. The last byte written determines the contents of the register.

A **single-byte read** from the MAX7357 or MAX7358 returns the contents of the switch control register.

A **multibyte read** (2 or more bytes before the I²C STOP bit) from the MAX7357 or MAX7358 returns the contents of the switch control register repeatedly.

Writing to the MAX7356

The MAX7356's switch control register can be written by an I²C write command starting with the device address for the MAX7356 and followed by data bytes. The last data byte is stored into the switch control register.

A write to the MAX7356 starts with the master transmitting the slave address with the R/$\overline{W}$ bit set low. The MAX7356 acknowledges the slave address. The master can then issue a STOP condition after the acknowledge (Figure 14), but typically the master proceeds to transmit one or more bytes of data. The MAX7356 acknowledges these subsequent bytes of data and updates the switch control register when the master issues a STOP condition (Figure 14).

Writing to the MAX7357/MAX7358 in Enhanced Mode

The MAX7357 and MAX7358 registers can be written by an I²C write command starting with the device address for the MAX7357 or MAX7358 and followed by data bytes. The first data byte is stored into the switch control register and subsequent data bytes are stored into the subsequent registers.

A write to the MAX7357 or MAX7358 starts with the master transmitting the slave address with the R/$\overline{W}$ bit set low. The MAX7357 or MAX7358 acknowledge the slave address. The master can then issue a STOP condition after the acknowledge (Figure 15), but typically

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the master proceeds to transmit one or more bytes of data. The MAX7357 or MAX7358 acknowledge these subsequent bytes of data and update corresponding registers with each new byte until the master issues a STOP condition (Figure 15).

Writing to the MAX7357/MAX7358 in Basic Mode

The MAX7357 and MAX7358 switch control register can be written by an I²C write command starting with the device address for the MAX7357 or MAX7358 and followed by data bytes. The last data byte is stored in the switch control register.

A write to the MAX7357 or MAX7358 starts with the master transmitting the slave address with the R/$\overline{W}$ bit set low. The device acknowledges the slave address. The master can then issue a STOP condition after the acknowledge (Figure 16), but typically the master proceeds to transmit one or more bytes of data. The MAX7357 or MAX7358 acknowledge these subsequent bytes of data and update the switch control register when the master issues a STOP condition (Figure 16).

Reading from the MAX7356

A read from the MAX7356 starts with the master transmitting the slave address with the R/$\overline{W}$ bit set high. The MAX7356 acknowledges the slave address. The master can read 1 byte from the switch control register and then issue a STOP condition (Figure 17). If the master reads more than one byte, the master upon reception acknowledges each byte. All bytes return the contents of the switch control register.

Reading from the MAX7357/MAX7358 in Enhanced Mode

A read from the MAX7357 or MAX7358 starts with the master transmitting the slave address with the R/$\overline{W}$ bit set high. The device acknowledges the slave address. The master can read 1 byte from the device and then issue a STOP condition (Figure 18). In this case, the device transmits the data byte from the switch control register. Typically, the master reads 1 or 2 bytes with each byte being acknowledged by the master upon reception. The first data byte comes from the switch control register and subsequent data bytes come from the subsequent registers in order.

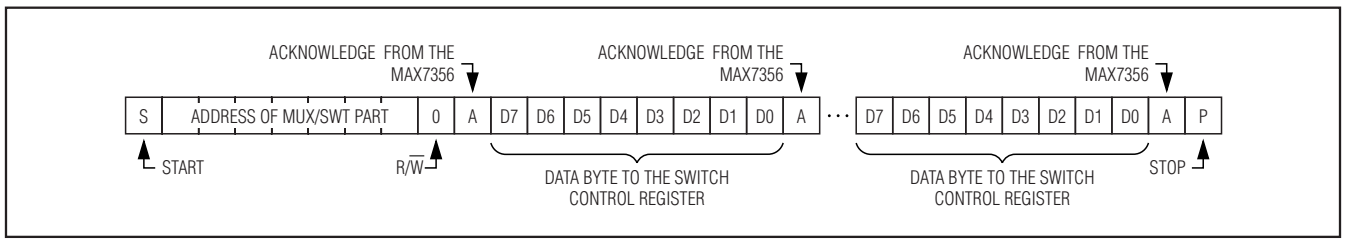


Figure 14. Writing to the MAX7356

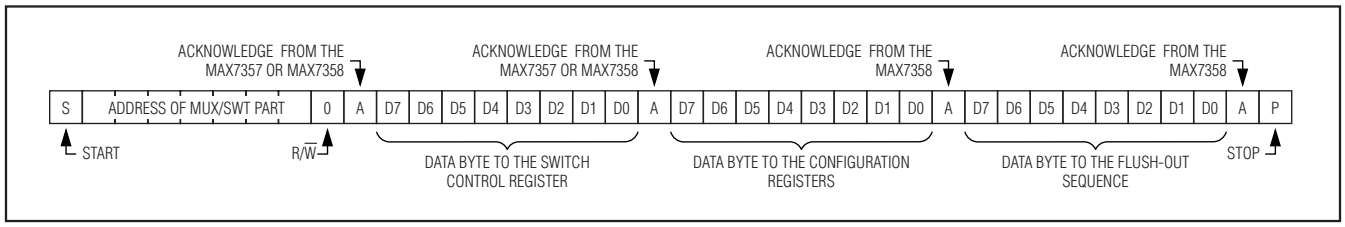


Figure 15. Writing to the MAX7357 or MAX7358 in Enhanced Mode

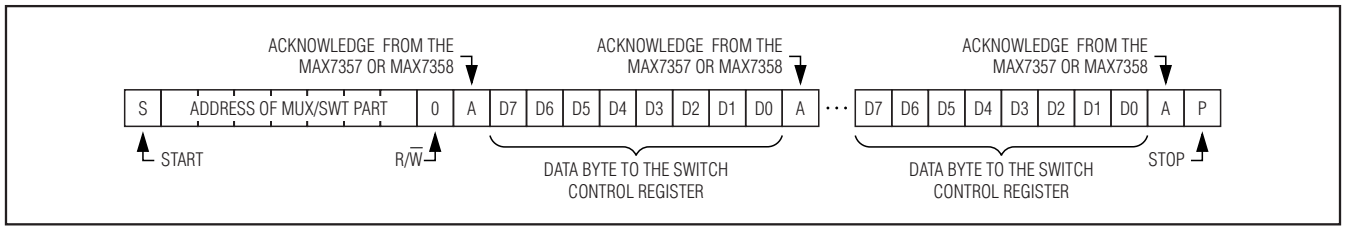


Figure 16. Writing to the MAX7357 or MAX7358 in Basic Mode

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1-to-8 I²C Bus Switches/Multiplexers with Bus Lock-Up Detection, Isolation, and Notification

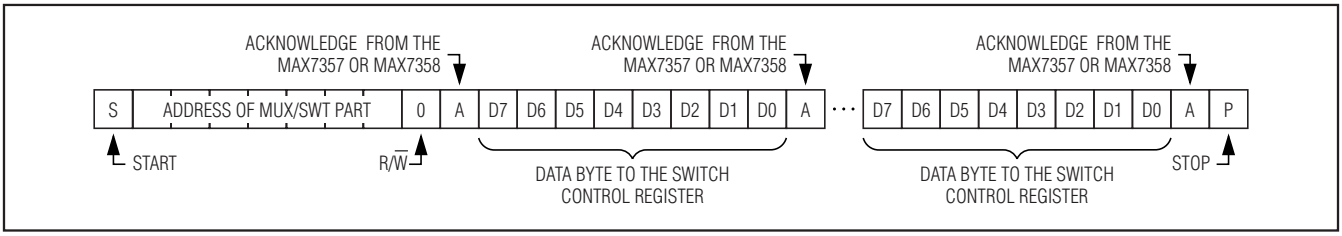


Figure 17. Reading the MAX7356

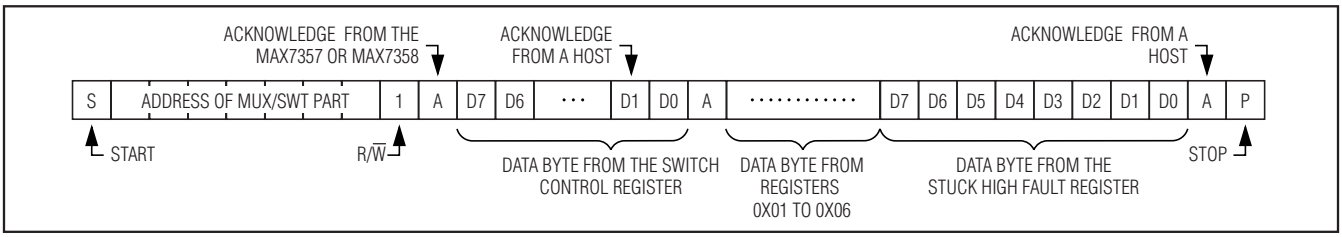


Figure 18. Reading the MAX7357 or MAX7358 in Enhanced Mode

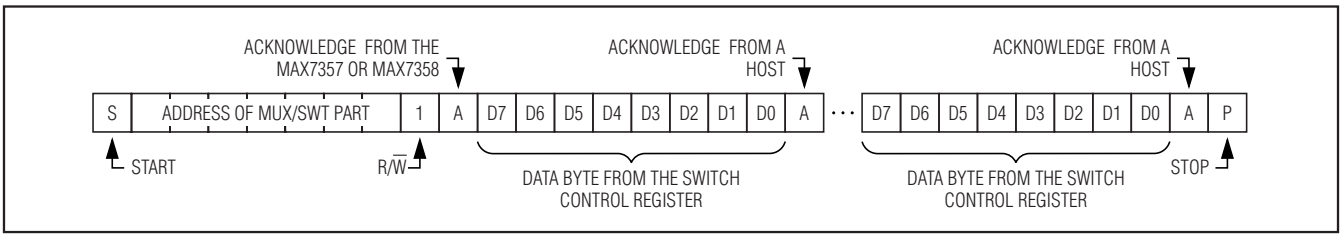


Figure 19. Reading the MAX7357 or MAX7358 in Basic Mode

Reading from the MAX7357/MAX7358 in Basic Mode

A read from the MAX7357 or MAX7358 in basic mode starts with the master transmitting the slave address with the R/$\overline{W}$ bit set high. The device acknowledges the slave address. The master can read 1 byte from the switch control register and then issue a STOP condition (Figure 19). If the master reads more than one byte, the master upon reception acknowledges each byte. All bytes return the contents of the switch control register.

Applications Information

Voltage Level Translation

The pass gates of the MAX7356/MAX7357/MAX7358 are designed so V_{DD} can be used to limit the voltage levels transferred from one bus to another. The power-supply voltage of the part should be selected to be no larger than one VGS_{ON} (0.7V, typ) above the lowest bus voltage in the system. This ensures that the analog switches do not allow current to flow from higher voltage buses to lower voltage buses.

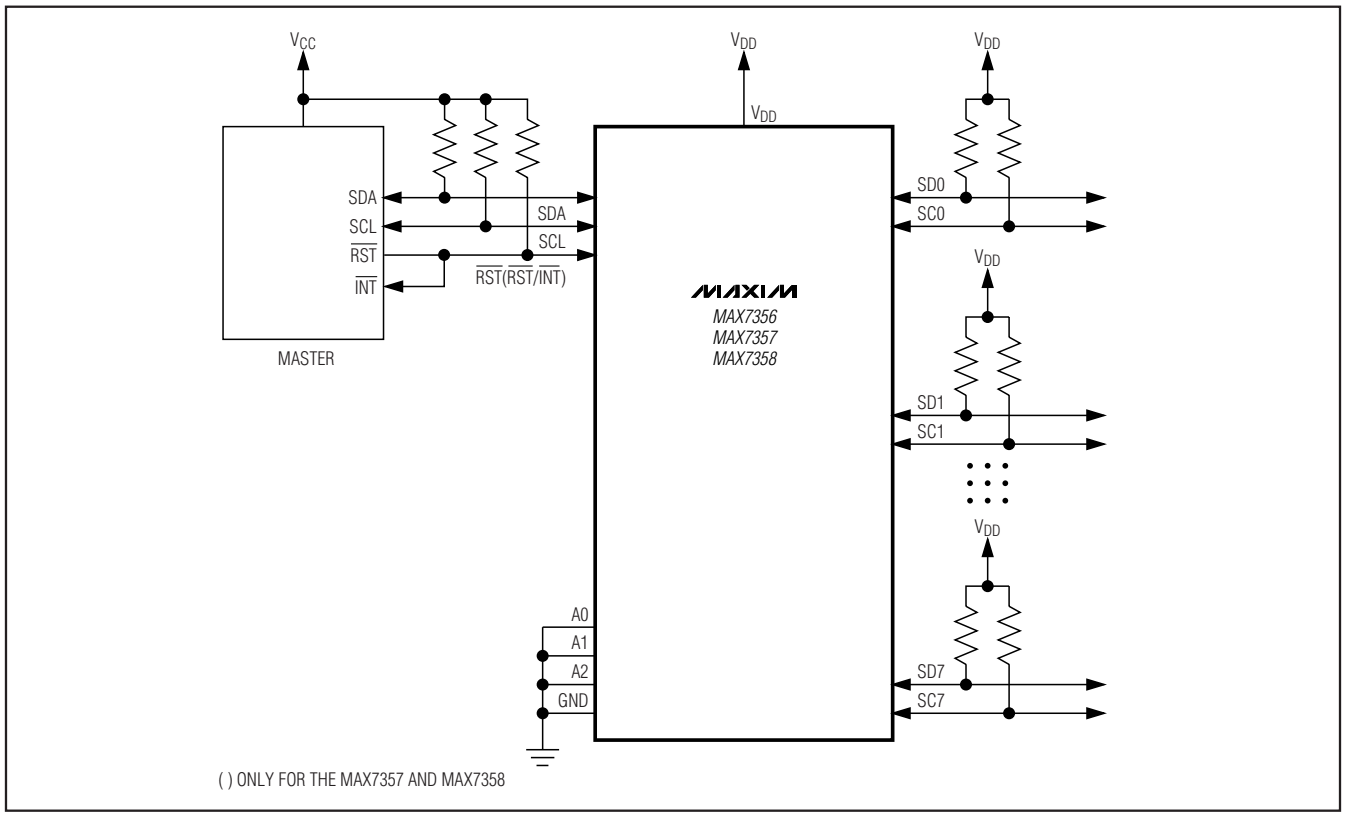
Chip Information

PROCESS: CMOS

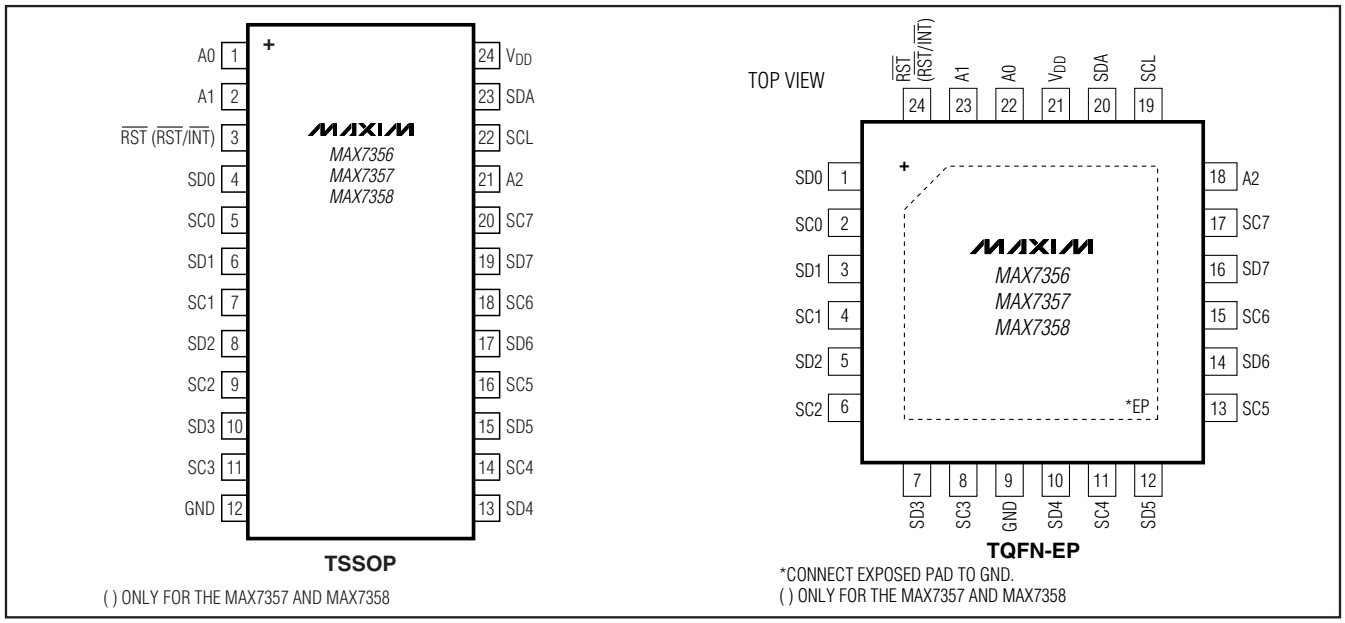
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1-to-8 I²C Bus Switches/Multiplexers with Bus Lock-Up Detection, Isolation, and Notification

Typical Operating Circuit



Pin Configurations



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Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TSSOP	U24+1	**21-0066**
24 TQFN-EP	T2444+4	**21-0139**

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