9.5V Smart Adaptive Boost High Efficiency Low Noise Large Volume Smart K Audio Amplifier

Features

- Support high power receiver stereo application
- Wide Voltage Range: 2.7V-5.5V
- High efficiency large drive ability Smart Adaptive Boost(Patented)
  - Maximum boost output voltage: 9.5V
  - Maximum output Power: 5.2W@8Ω
  - Excellent quiescent current: 5mA@3.6V
  - Overall efficiency up to 85%@0.5W
  - Overall efficiency up to 82%@1W
- Low noise：
  - 25μV (K Speaker @18dB)
  - 7μV (L Receiver @0dB)
- Speaker & receiver 2-in-1 mode application
  - LRCV receiver：0dB，En=7μV，0.14W@THD+N=1%
  - SRCV receiver：0dB，En=9μV，0.52W@THD+N=1%
- High PSRR：82dB (217Hz)
- Support 1.8V logic I^{2}C control
- Triple-Level Triple-Rate AGC algorithm to effectively eliminate noise, pure sound quality
- Selectable speaker-guard power level：0.5W~2W@8ohm, 100mW/step
- Excellent pop-click suppression
- Excellent full bandwidth EMI suppression
- FCQFN 2.0mmX3.0mmX0.55mm-20L package

Applications

- Smart phone
- Tablet PC
- Portable Audio Devices
- Notebook

General Description

AW87565 is a high efficiency, low noise, low power consumption, constant large volume Smart K audio amplifier.

AW87565 integrates AWINIC's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume.

AW87565 integrates AWINIC's proprietary Smart Adaptive Boost with efficiency up to 90%，it greatly improves efficiency at small signal, Overall efficiency up to 85% when output power is 0.5W.

AW87565 noise floor is as low as to 25μV at speaker mode, with 108dB high signal-to-noise ratio (SNR).

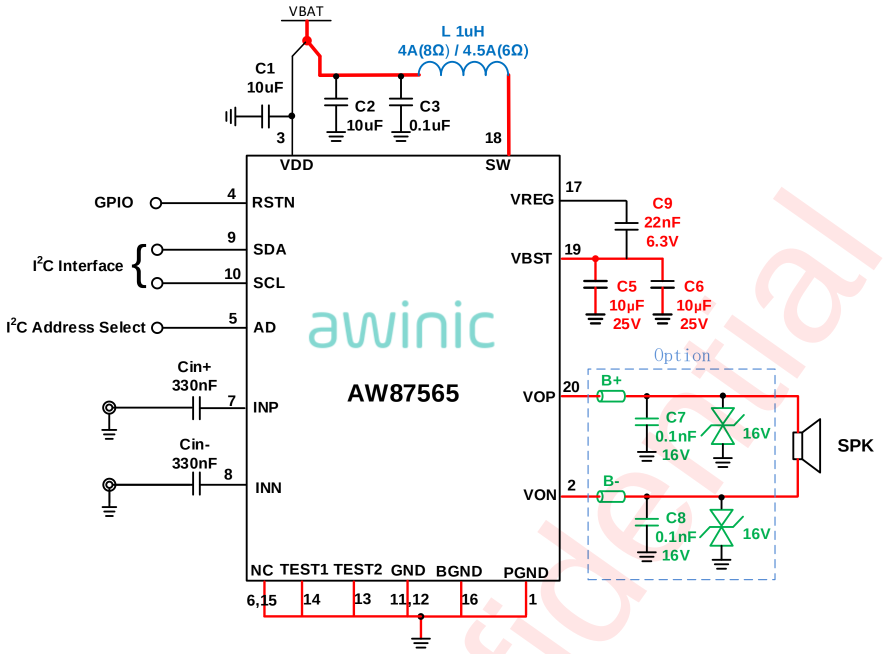
AW87565 has super volume receiver mode, it can deliver 520mW output power into an 8Ω speaker at 9μV noise.

AW87565 supports speaker and receiver 2-in-1 application. Quiescent current is 5mA when VDD is equal to 3.6V. In the receiver mode, its ultra-low noise is 7μV. Class D receiver also has high PSRR performance to completely suppress TDD-noise.

AW87565 built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip.

AW87565 is available in a FCQFN 2.0mm X3.0mm X 0.55mm-20L package.

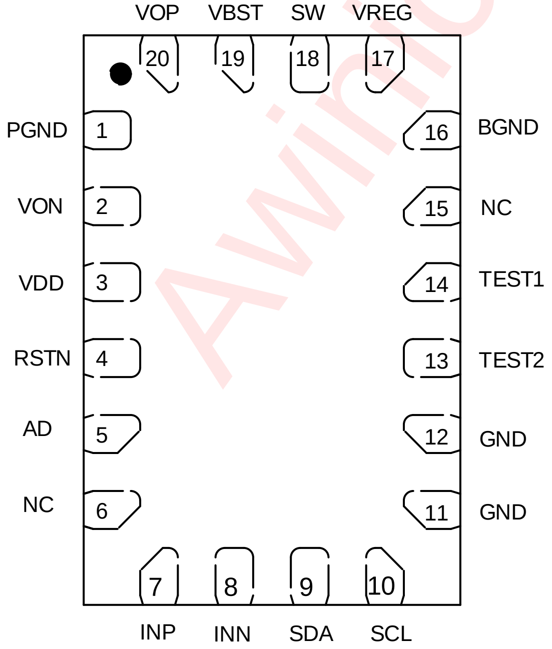
Typical Application Circuit



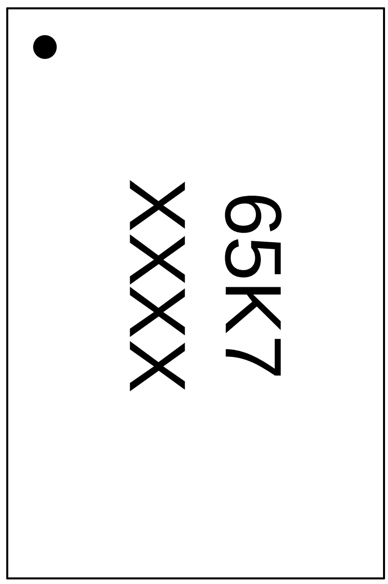
Note: Traces carry high current are marked in red in the above figure

Pin Configuration And Top Mark

AW87565FCR
(Top View)



AW87565FCR Marking
(Top View)

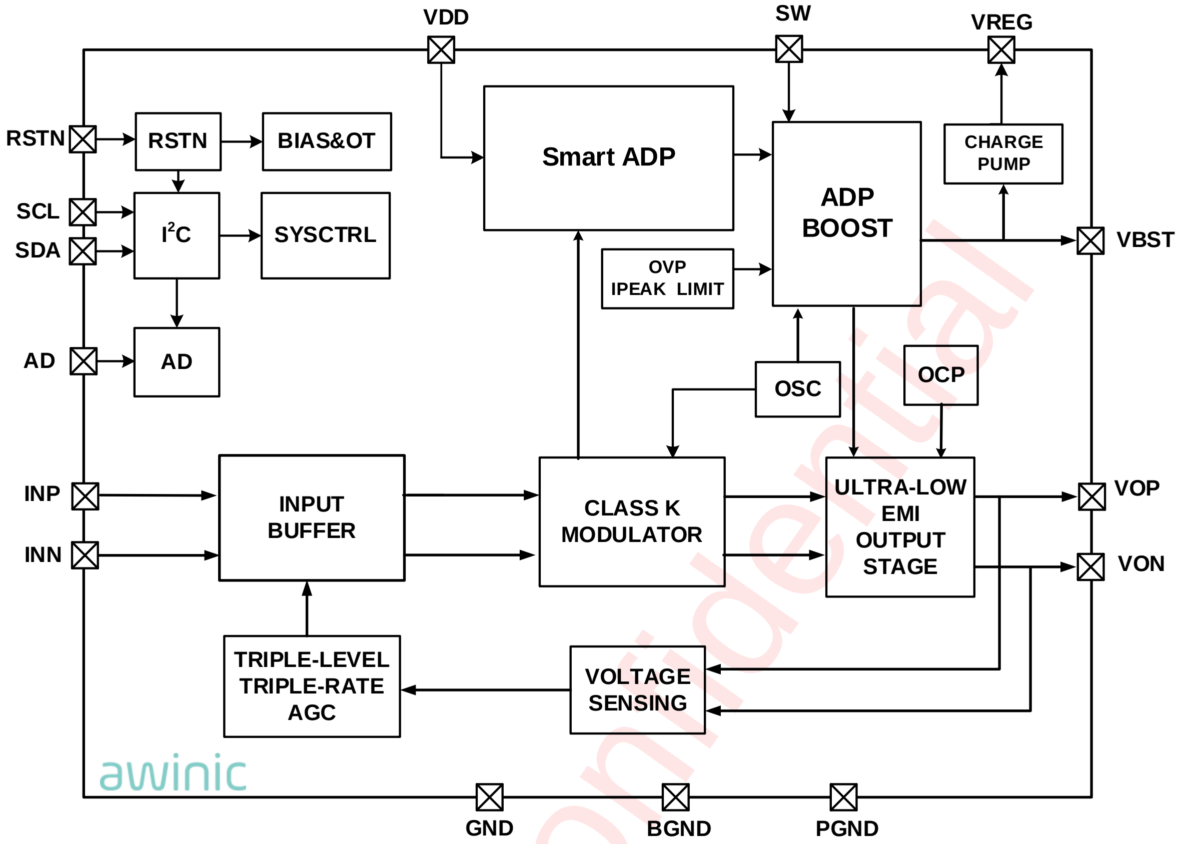


65K7 - AW87565FCR
XXXX - Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
1	PGND	Class D power ground
2	VON	Negative audio output terminal
3	VDD	Power supply
4	RSTN	Reset pin, active low reset, the internal 2MΩ pull-down resistor in chip
5	AD	I^2C address pin
6	NC	Not connect, Connect to GND in application
7	INP	Positive audio input terminal
8	INN	Negative audio input terminal
9	SDA	I^2C-bus data input/output
10	SCL	I^2C-bus clock input
11	GND	Ground
12	GND	Ground
13	TEST2	Test2 pad，connect to GND in application
14	TEST1	Test1 pad，connect to GND in application
15	NC	Not connect, Connect to GND in application
16	BGND	Boost power ground
17	VREG	Charge pump output pin
18	SW	Boost switch pin
19	VBST	Boost output pin.
20	VOP	Positive audio output terminal

Functional Block Diagram



Typical Application Circuits

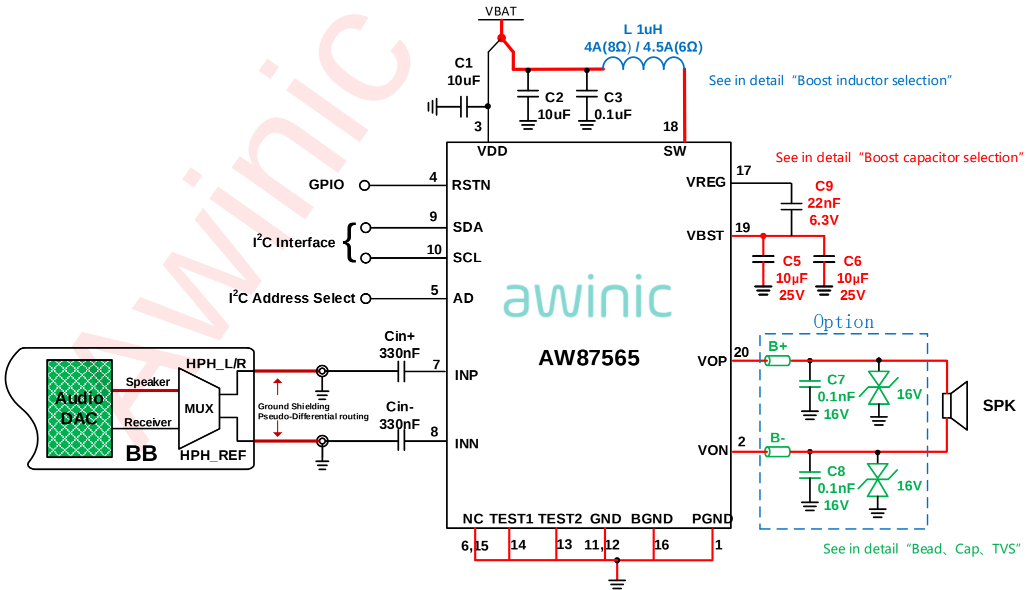


Figure 1 AW87565 Single-ended Input Mode Application Diagram(Note 1)

Note1: *When single-ended input, audio signal line from audio DAC (HPH_L or HPH_R) can arbitrarily connected to either of INN or INP input terminal. The other terminal must be connected to reference ground (HPH_REF) through input capacitor and resistor.*

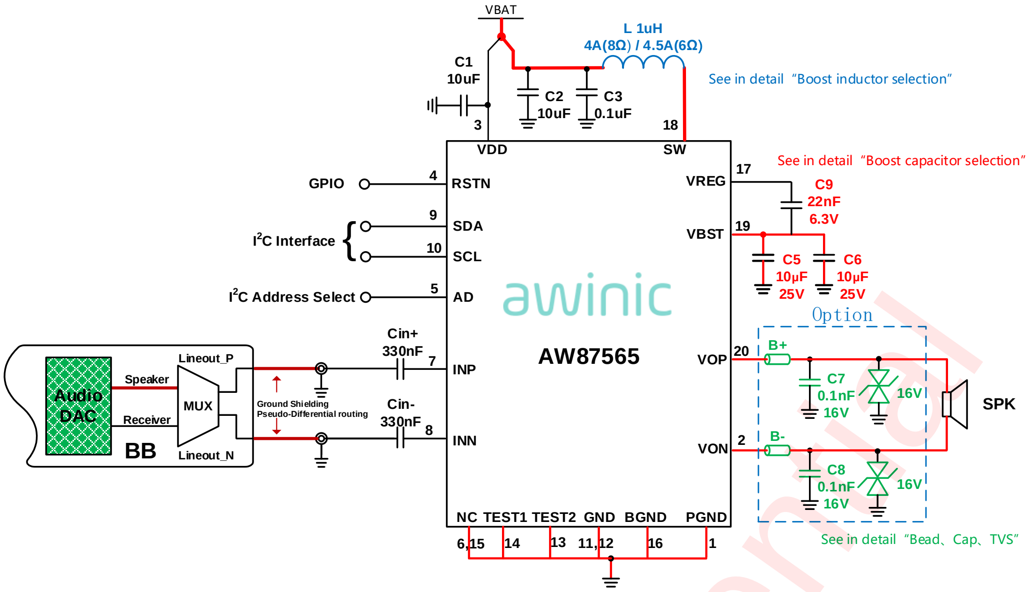


Figure 2 AW87565 Differential Input Mode Application Diagram

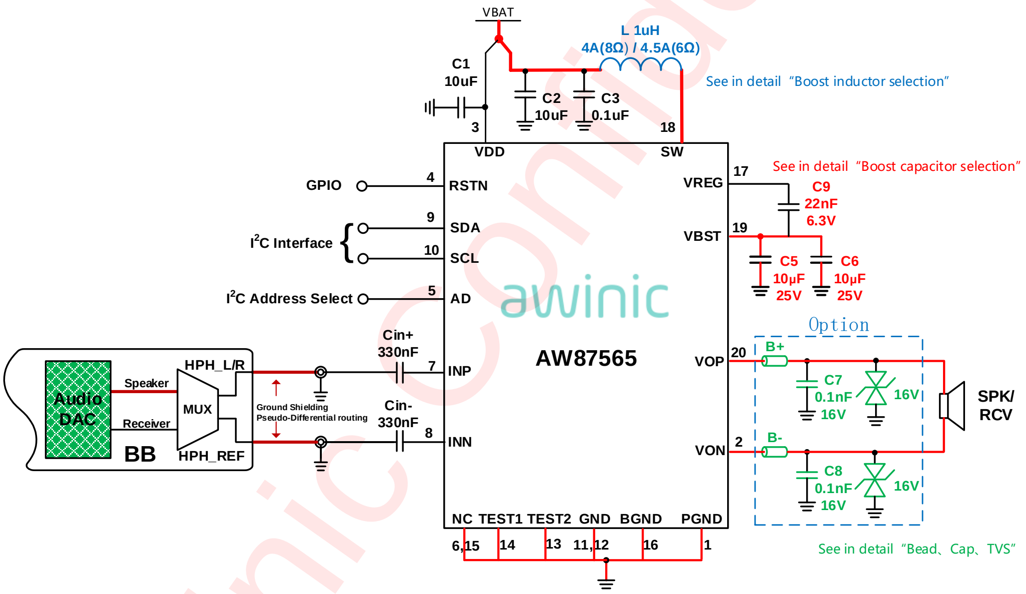


Figure 3 AW87565 Speaker & Receiver 2-in-1 Mode Application Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW87565FCR	-40°C～85°C	FCQFN 2.0mmX3.0mm X0.55mm -20L	65K7	MSL1	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE2)

Parameter	Range
Supply Voltage VDD	-0.3V to 6V
INN,INP	-0.3V to VDD+0.3V
Boost output voltage VBST	-0.3V to 11V
SW	-0.3V to VBST+2V
VOP,VON	-0.3V to VBST+0.3V
Minimum load resistance R_L	5Ω
Package Thermal Resistance $θ_{JA}$	65.66°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature（Soldering 10 Seconds）	260°C
ESD Rating (Note 3)	
HBM（human body model）	±2kV
CDM（charged-device model）	±1.5kV
Latch-up	
Test Condition：JESD78F	+IT：200mA -IT：-200mA

NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023

Test method of the charge device model: ESDA/JEDEC JS-002-2022

Electrical Characteristics

Test condition：T_A=25°C, VDD=4.2V, VBST=9.5V, R_L=8Ω+33μH, f=1kHz（unless otherwise noted）

Parameter		Test conditions	Min	Typ	Max	Units
VDD	Power supply voltage		2.7		5.5	V
UVLO	Under-voltage protection voltage			2.5		V
	Under-voltage protection hysteresis voltage			100		mV
V_{IH}	RSTN, SCL, SDA, AD high-level input voltage		1.3		VDD	V
V_{IL}	RSTN, SCL, SDA, AD low-level input voltage		0		0.45	V

Parameter		Test conditions	Min	Typ	Max	Units
I_{SD}	Shutdown current	VDD=3.6V, RSTN=0V		0.1	1	μA
T_{SD}	Over temperature protection threshold			160		°C
T_{SDR}	Over temperature protection recovery threshold			130		°C
T_{ON}	Turn-On time			45		ms
BOOST						
VBST	BOOST Output voltage	VDD=2.7V to 5.5V		9.5 (Note4)		V
OVP	OVP voltage	VDD=2.7V to 5.5V		VBST+0.5		V
	OVP hysteresis voltage	VDD=2.7V to 5.5V		500		mV
I_{L_PEAK}	Inductor peak current limit			4 (Note4)		A
F_{BST}	Boost operating frequency	VDD=2.7V to 5.5V	1.5	2	2.5	MHz
D_{MAX}	The maximum duty cycle			90		%
T_{ST}	Soft-start time	No load，C_{OUT}=22μF		2		ms
η_{boost}	Boost efficiency	VDD=4.2V, I_{load}=400mA		90		%
CLASS K MODE						
V_{OS}	Output offset voltage	No input	-6		6	mV
η_T	Total efficiency (Smart ADP BOOST+CLASS D)	VDD=4.2V, Po=0.5W, R_L=8Ω+33μH		85		%
	Total efficiency (Smart ADP BOOST+CLASS D)	VDD=4.2V, Po=1W, R_L=8Ω+33μH		82		%
I_{QK}	Speaker Quiescent current at Smart ADP MODE	VDD=3.6V, input ac grounded, R_L=8Ω+33μH		5		mA
R_{dson}	Drain-Source on-state resistance	High side MOS + Low side MOS		250		mΩ
Vinp	Recommended input signal amplitude	VDD=2.7V to 5.5V			1.45	Vp
Fosc	Modulation frequency	VDD=2.7V to 5.5V	600		1000	kHz
Pagc	TLTR AGC power	R_L=8Ω+33μH	0.72	0.8 (Note4)	0.88	W
		R_L=6Ω+33μH	0.96	1.067 (Note4)	1.17	W
PSRR	Power supply rejection ratio	VDD=4.2V, Vpp_sin=200mV, 217Hz		80		dB
		VDD=4.2V, Vpp_sin=200mV, 1kHz		78		dB
SNR	Signal-to-noise ratio	VDD=4.2V, Po=5.2W, Av=18dB ,R_L=8Ω+33μH,		108		dB

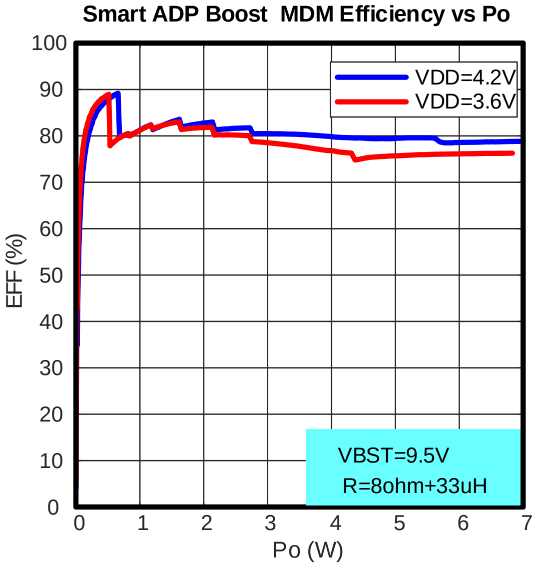
<table>
<tr><th colspan="2">Parameter</th><th colspan="2">Test conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td rowspan="3">E_N</td><td rowspan="3">Speaker Output noise</td><td>Av=24dB, LSPK mode</td><td rowspan="3">20Hz to 20kHz, input ac grounded, A-weighting</td><td></td><td>35</td><td></td><td rowspan="2">μV</td></tr>
<tr><td>Av=18dB, LSPK mode</td><td></td><td>25</td><td></td></tr>
<tr><td>Av=18dB, NSPK mode</td><td></td><td>35</td><td></td><td></td></tr>
<tr><td>Av</td><td>Speaker gain</td><td colspan="2">VDD=2.7V to 5.5V</td><td></td><td>18 (Note4)</td><td></td><td>dB</td></tr>
<tr><td rowspan="3">Rini</td><td rowspan="3">Speaker Inner input resistance</td><td colspan="2">Av=24dB, LSPK mode</td><td></td><td>2.4</td><td></td><td rowspan="3">kΩ</td></tr>
<tr><td colspan="2">Av=18dB LSPK mode</td><td></td><td>5</td><td></td></tr>
<tr><td colspan="2">Av=18dB NSPK mode</td><td></td><td>18</td><td></td></tr>
<tr><td rowspan="3">Fin</td><td>Speaker input Cut-off frequency</td><td colspan="2">Cin=330nF, Av=24dB, LSPK mode</td><td></td><td>198.6</td><td></td><td rowspan="3">Hz</td></tr>
<tr><td>Speaker input Cut-off frequency</td><td colspan="2">Cin=330nF, Av=18dB, LSPK mode</td><td></td><td>96.5</td><td></td></tr>
<tr><td>Speaker input Cut-off frequency</td><td colspan="2">Cin=100nF, Av=18dB, NSPK mode</td><td></td><td>88</td><td></td></tr>
<tr><td>THD+N</td><td>Total harmonic distortion + noise</td><td colspan="2">VDD=4.2V, Po=0.8W, RL=8Ω+33μH, f=1kHz</td><td></td><td>0.012</td><td></td><td>%</td></tr>
<tr><td rowspan="4">Po</td><td rowspan="4">Speaker Output Power</td><td colspan="2">THD+N=1%, R_L=8Ω+33μH, VDD=4.2V, VBST=9.5V, I_{L_PEAK}=4A</td><td></td><td>5.2</td><td></td><td>W</td></tr>
<tr><td colspan="2">THD+N=10%, R_L=8Ω+33μH, VDD=4.2V, VBST=9.5V, I_{L_PEAK}=4A</td><td></td><td>6.5</td><td></td><td>W</td></tr>
<tr><td colspan="2">THD+N=1%, R_L=6Ω+33μH, VDD=4.2V, VBST=9.5V, I_{L_PEAK}=4.5A</td><td></td><td>6.1</td><td></td><td>W</td></tr>
<tr><td colspan="2">THD+N=10%, R_L=6Ω+33μH, VDD=4.2V, VBST=9.5V, I_{L_PEAK}=4.5A</td><td></td><td>7.5</td><td></td><td>W</td></tr>
<tr><td colspan="8">2-in-1 Receiver MODE</td></tr>
<tr><td>I_{QD}</td><td>Receiver quiescent current（overall）</td><td colspan="2">VDD=3.6V, input ac grounded, R_L=8Ω+33μH</td><td></td><td>5</td><td></td><td>mA</td></tr>
<tr><td>η_D</td><td>SRCV efficiency</td><td colspan="2">VDD=4.2V,Po=0.95W, R_L=8Ω+33μH</td><td></td><td>90</td><td></td><td>%</td></tr>
<tr><td>Av</td><td>Gain</td><td colspan="2">VDD=2.7V to 5.5V</td><td></td><td>0 (Note4)</td><td></td><td>dB</td></tr>
<tr><td rowspan="2">Rini</td><td rowspan="2">SRCV Inner input resistance</td><td colspan="2">Av=0dB</td><td></td><td>5</td><td></td><td>kΩ</td></tr>
<tr><td colspan="2">Av=9dB</td><td></td><td>5</td><td></td><td>kΩ</td></tr>
</table>

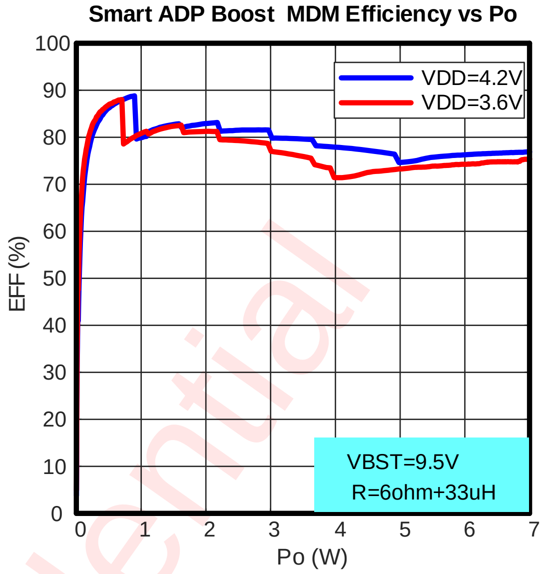
Parameter		Test conditions		Min	Typ	Max	Units
	LRCV Inner input resistance	Av=0dB			5		kΩ
	NRCV Inner input resistance	Av=0dB			48		kΩ
Fin	SRCV Inner input resistance	Cin=330nF, Av=0dB			96.5		Hz
		Cin=330nF, Av=9dB			96.5		
	LRCV Inner input resistance	Cin=330nF, Av=0dB			96.5		
	NRCV Inner input resistance	Cin=100nF, Av=0dB			33.2		
E_N	SRCV Output noise	Av=0dB	20Hz to 20kHz, input ac grounded, A-weighting		9		μV
		Av=9dB			15		μV
	LRCV Output noise	Av=0dB			7		μV
	NRCV Output noise	Av=0dB			10		μV
THD+N	Total harmonic distortion + noise	VDD=4.2V, Po=0.1W,RL=8Ω+33μH, f=1kHz, CLASS D Receiver			0.018		%
PSRR	Receiver Power supply rejection ratio	VDD=4.2V, Vp-p_sin=200mV	217Hz		82		dB
			1kHz		80		dB
Po	SRCV Output Power	THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=6/9dB, differential input			1.0		W
		THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=0dB, differential input			0.52		W
		THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=6/9dB, single-ended input			1.0		W
		THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=0dB, single-ended input			0.25		W
	LRCV Output Power	THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=0dB, differential input			0.14		W
		THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=0dB, single-ended input			0.14		W

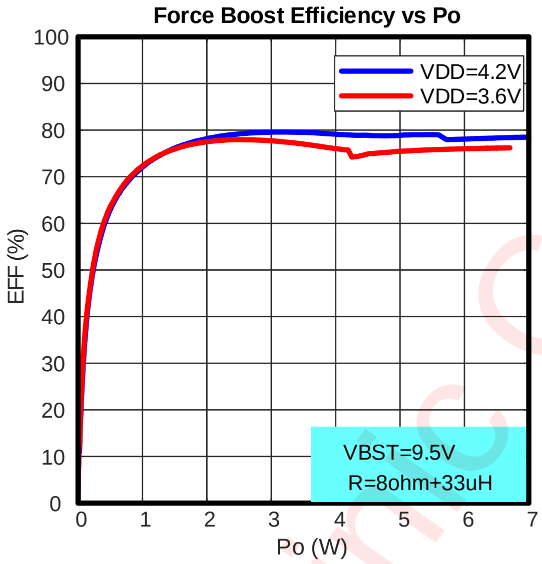
Parameter		Test conditions	Min	Typ	Max	Units
	NRCV Output Power	THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=0dB, differential input		0.52		W
		THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=0dB, single-ended input		0.25		W
Triple-Level Triple-Rate AGC						
T_{AT1}	AGC1 Attack Time			0.08 (Note4)		ms/dB
T_{AT2}	AGC2 Attack Time			0.64 (Note4)		ms/dB
T_{AT3}	AGC3 Attack Time			41 (Note4)		ms/dB
T_{RLT}	Release time			21 (Note4)		ms/dB
A_{MAX}	The maximum attenuation gain	VDD=2.7V to 5.5V		-13.5		dB

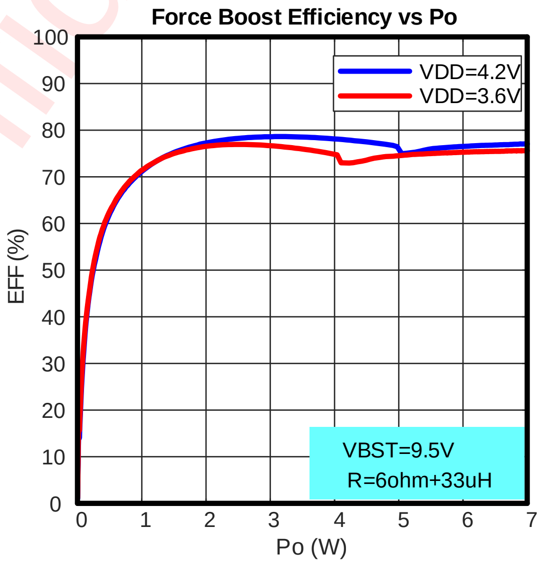
***Note 4**: Registers are adjustable; Refer to the list of registers.*

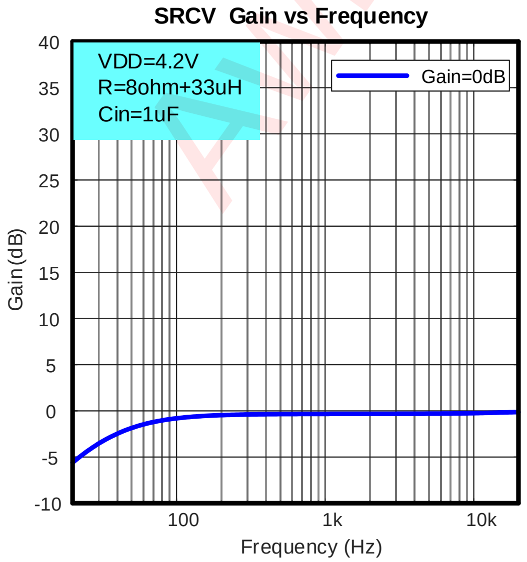
Typical Characteristics

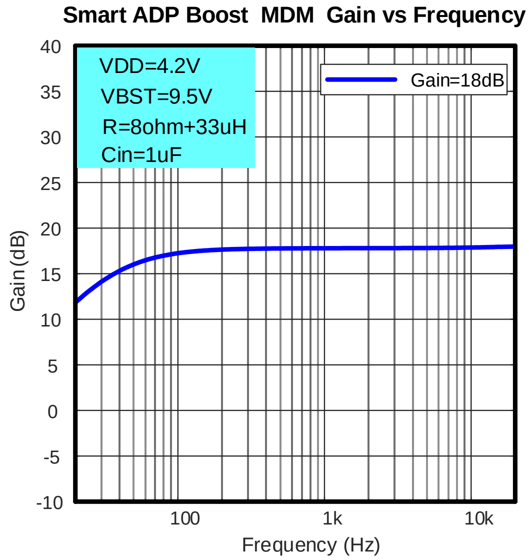




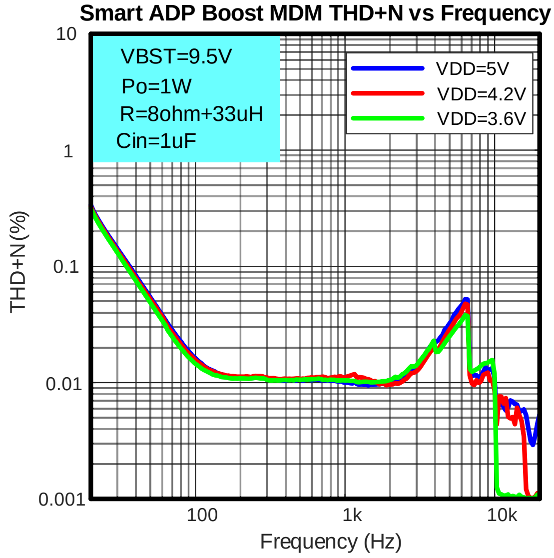




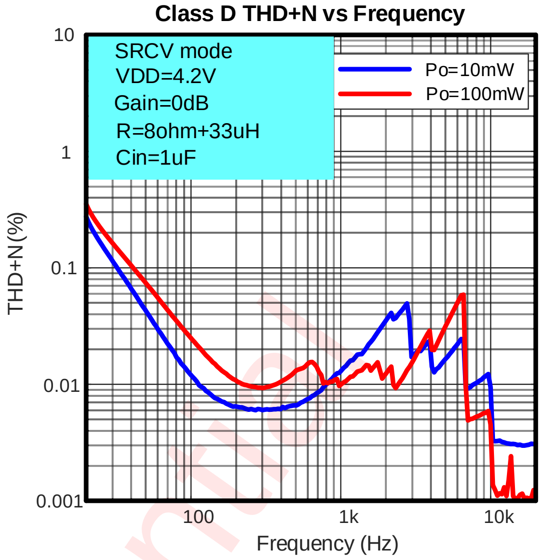




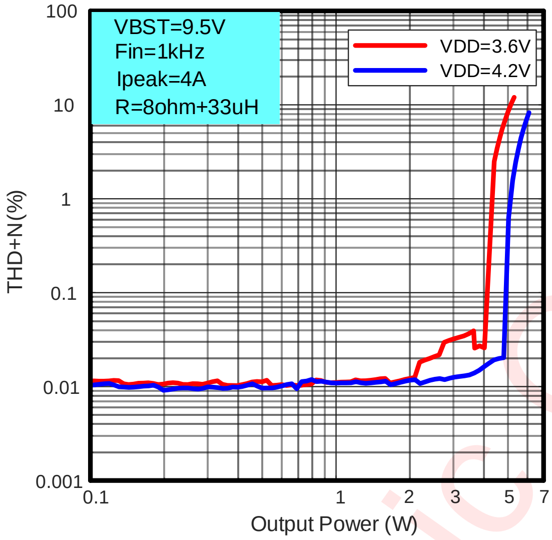
Smart ADP Boost MDM THD+N vs Frequency



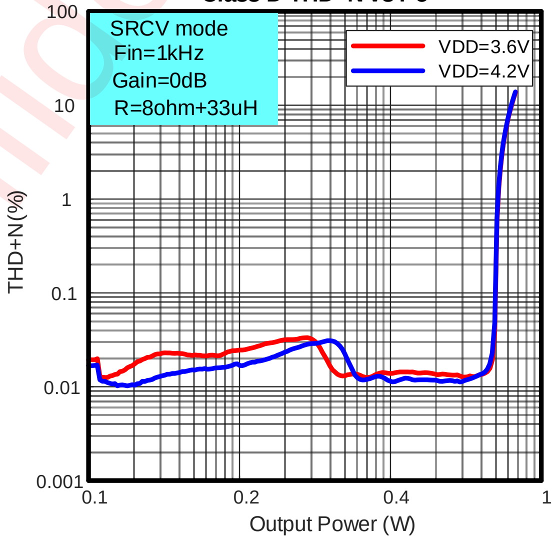
Class D THD+N vs Frequency



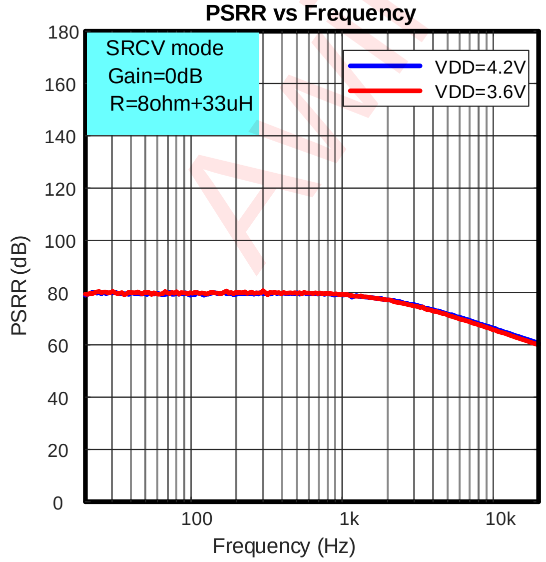
Smart ADP Boost MDM THD+N vs Po



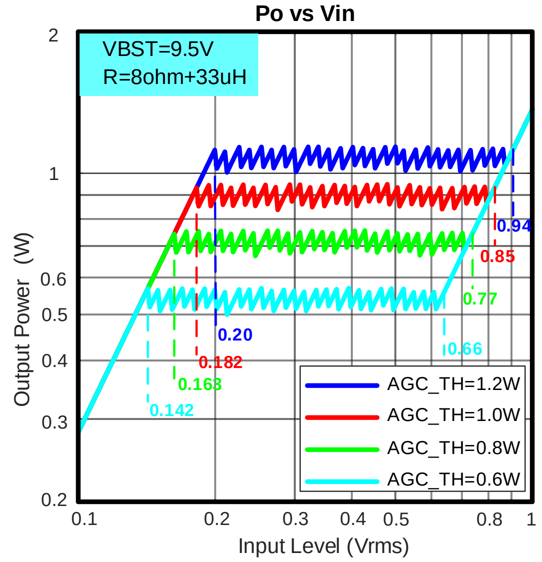
Class D THD+N vs Po



PSRR vs Frequency



Po vs Vin



Detailed Functional Description

AW87565 is a high efficiency, low noise, low power consumption, constant large volume Smart K audio amplifier.

Constant Output Power

In the mobile phone audio applications, the AGC function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually. So, it is hard to provide high quality music within the battery voltage range. AW87565 uses unique Triple-Level Triple-Rate technology, within lithium battery voltage range (3.3V~4.35V), to guarantee that output power is constant, and the output power will not drop along with the decrease of lithium battery voltage. In the process of using the phone, even if the battery voltage drops, AW87565 can still provide high quality large volume music enjoyment. The output power of AW87565 can be configured from 0.5W to 2W via I^2C, matching general speakers. Unique Triple-Level Triple-Rate AGC technology can bring high-quality music enjoyment.

Triple-Level Triple-Rate AGC Technology

AWINIC proprietary Triple-Level Triple-Rate AGC technology is designed for the protection of the high voltage power amplifier, which is divided into AGC1, AGC2 and AGC3 power levels, to obtain a large volume while maintaining excellent sound quality.

In practical applications, speaker can continuously work long hours at rated power, and also can work short-term at high power. For example, in the standard reliability of the loudspeaker experiment, the power of peak power reached around four times of the rated power. For achieving larger volume and better sound quality, speakers need to work at high power for short periods of time, in order to improve the performance of the speaker. AW87565 Triple-Level Triple-Rate AGC technology can fit the speaker better and perform better overall performance. AGC1 prevents output signal clipping by detecting output voltage in a very short time after clipping, which can effectively restrain the noise clipping; AGC2 can improve the dynamic range of the music in a relatively short period of time; AGC3 can make the speaker work under rated power, which can effectively improve the volume and protect the speaker. Triple-Level Triple-Rate AGC can obtain more excellent overall performance.

Triple-Level Triple-Rate AGC detects the peak output voltage of the power amplifier, when the output peak voltage is higher than the compression threshold voltage, the amplifier gain decreases in 0.5dB step. When the output peak voltage is lower than the release threshold voltage, the amplifier gain is recovery to the initial gain in 0.5dB step. The detailed process can be described as follows:

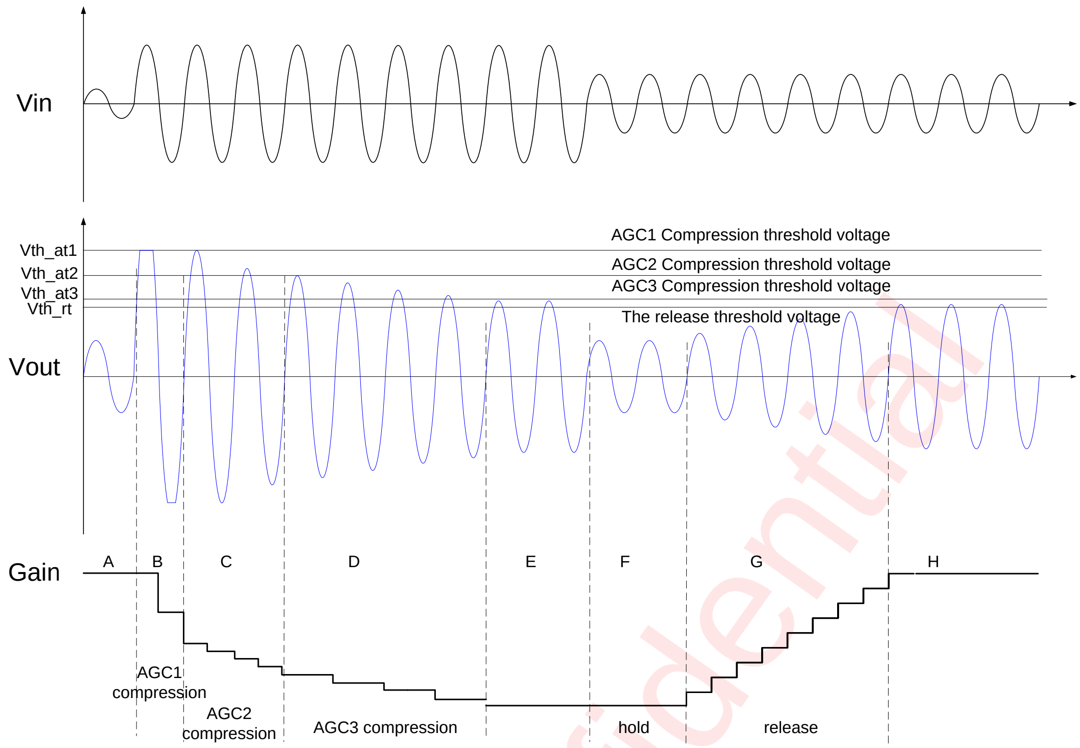


Figure 4 Triple-Level Triple-Rate AGC Operation Principle

A: Small input signal, the output voltage is lower than threshold voltage Vth of AGC, AGC don't work.

B: Input voltage becomes large. It leads to the output voltage clipping, AGC1 starts fast compression, the attack time is set through the I²C register 0x06h [2:0], when the output voltage is higher than Vth_at1, and gain register began to decrease. Gain decreases when the output signal passes through the zero. It eliminates the clipping noise as soon as possible.

C: When the output voltage is not clipping and higher than threshold voltage Vth_at2, AGC2 starts work, the attack time is set through the I²C register 0x07h [2:0], gain register begins to decrease at a certain rate. Gain register began to decrease. Gain decreases when the output signal passes through the zero. The output voltage gradually decreases to below the AGC2 attack threshold voltage Vth_at2, which can protect the speaker and enhance the sound.

D: When the output voltage is lower than the AGC2 attack threshold voltage Vth_at2 and higher than the AGC3 attack threshold voltage Vth_at3, AGC3 starts work, the attack time is set through the I²C register 0x09h [4:2], and gain register began to decrease at a certain rate. Gain decreases when the output signal passes through the zero, so the output voltage gradually decreases to below of the AGC3 attack threshold voltage Vth_at3, matching the speaker to achieve greater volume and better sound quality.

E: Triple-Level Triple-Rate AGC attack time ends, Amplifier output power is close to the speaker rated power.

F: Input voltage decreases, the output voltage becomes lower than the release threshold voltage Vth_rt, at this point, gain remains the same in the maintain time (10ms~20ms).

G: Gain increases when the time of output voltage lower than the release threshold voltage Vth_rt is longer than the holding time. The release time can be set through I²C register 0x09h [7:5].

H: Stop release when the output signal is larger than the release threshold or the gain is equal to the initial value. The output voltage remains constant.

Triple-Level Triple-Rate AGC can switch independently according to different application requirements.

Zero-Crossing Adjustment Technology

Traditional AGC doesn't contain zero adjustment technology; AGC gain changes generally at the peak, the gain variation at the peak would generate a certain transient distortion, such distortions are audibly imperceptible. Such as individual songs have a slight click.

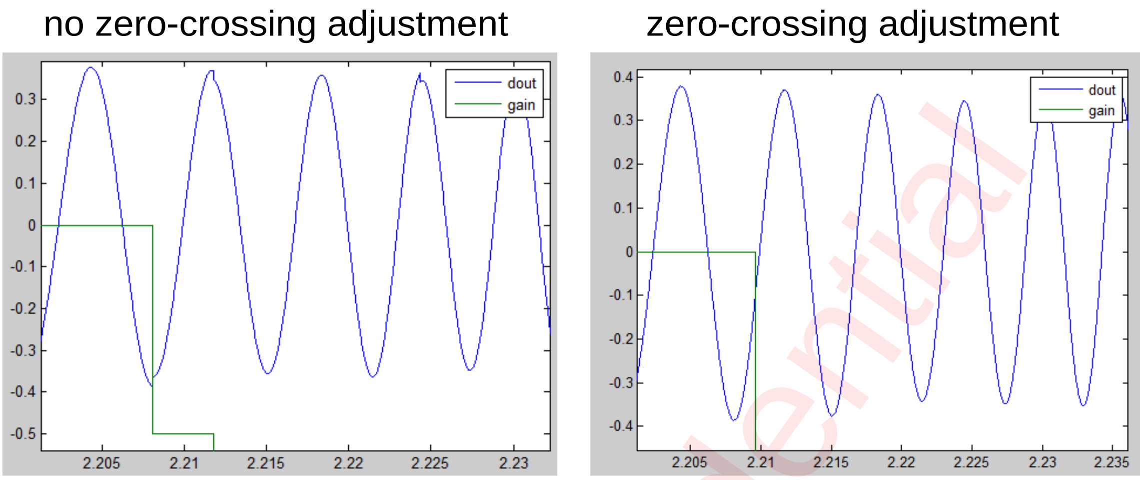


Figure 5 Zero-adjust Comparison

As shown above, when there is no zero-adjustment technology, it can be seen the obvious step change at the peak of large signal, the steps sound slightly perceived in special audio. Gain changes at zero. The steps disappear by using zero-crossing detection technology. Using zero detection technology can make the music pure and natural.

RNS (RF TDD NOISE SUPPRESSION)

TDD Noise Causes

GSM cell phones use TDMA (Time Division Multiple Access) slot sharing technology. The time is divided into periodic frames in TDMA, and each frame is subdivided into a plurality of time slots. In order to transmit signals to the base station, the signals sent from the base stations to the plurality of mobile terminals are arranged in a predetermined time slot in the transmission. In this case, each TDMA frame contains 8 time slots, the entire frame is about 4.615ms long, and each slot time is 0.577ms.

With GSM handset, the RF power amplifier will transmit once every 4.615ms (217Hz), and the signal will produce intermittent Burst current and strong electromagnetic radiation. Intermittent Burst current will form a power fluctuation of 217 Hz; High frequency (900MHz and 1800MHz) RF signals form a 217Hz RF envelope signal. 217Hz power fluctuations will be conducted through the conduction to the audio signal path, 217Hz RF envelope signal will be coupled through the radiation into the audio signal path, if the protection is not good, it will produce an audible TDD Noise, which includes the 217Hz noise And a harmonic noise signal of 217 Hz.

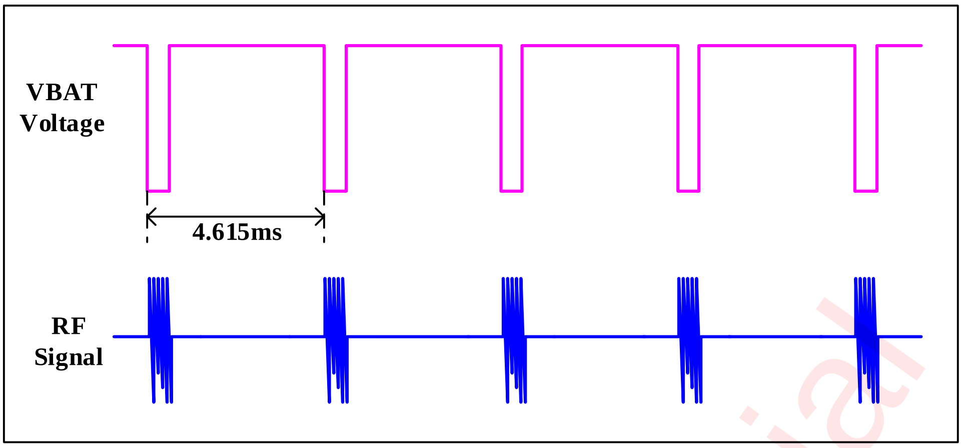


Figure 6 Schematic Diagram of Power Supply Voltage and RF Signal during GSM RF Operation

RNS fully inhibit the conduction and radiation interference by the AWINIC unique circuit architecture. Effectively improve the ability to suppress TDD Noise.

Conduction Noise Suppression

When the RF power amplifier is operating, it will draw the current from the battery by 217Hz frequency, Power supply will be introduced to 217Hz power ripple since the battery has a certain internal resistance, it will be coupled to the speaker through the audio power amplifier. The ability to suppress power fluctuations depends on the PSRR of the audio power amplifier.

$$PSRR = 20\log\left(\frac{vdd_{ac}}{vout_{ac}}\right)$$

Due to the input and output of the fully differential amplifier is perfectly symmetrical, theoretically, the effect of the power supply fluctuation on the two outputs is exactly the same, and the differential output is completely unaffected by the power supply fluctuation. In practice, due to process bias and other factors, the amplifier will have a certain mismatch, PSRR is generally better than 60dB, it shows the output relative to the power fluctuations can be reduced by 1000 times, such as 500mVp power fluctuations, the differential output of 0.5 mV, which basically can meet the application requirements.

But in practical applications, the power amplifier may encounter conduction of TDD Noise problem even if its PSRR is 60dB or 80dB, why is this? Because we also need to consider the impact of peripheral power mismatches of audio power amplifiers.

For conventional audio power amplifiers, when the input resistor Rin and the input capacitor Cin mismatch, will greatly affect the audio power amplifier PSRR indicators, in the case of 24 times the gain, PSRR will be weakened to 46dB or so if the input resistance and Capacitor with 1% mismatch. PSRR will be weakened to 28dB or so if the input resistance and input capacitance mismatch with 10% mismatch, when the power fluctuations, it is easy to produce audible TDD Noise.

In order to enhance the audio power amplifier PSRR in the input resistance and input capacitance mismatch case, AW87565 features a unique conduction noise suppression circuit, making the power amplifier to maintain a high PSRR value even in the input resistance, the input capacitance deviation of 10% or more, this greatly inhibits the generation of conducted noise.

Radiation Noise Suppression

Input traces, output traces, horn loops, and even power and ground loops are likely to be subject to RF radiation interference in the audio signal module, longer input traces and output traces similar to the antenna, especially vulnerable RF radiation effects.

The reasonable PCB layout can reduce the influence of RF radiation in the design, such as shorten the line length of input and output as much as possible; audio devices should be shielded and far away from the RF antenna, maintain the integrity of the device to audio signal pathway; to increase the small bypass capacitor RF signals in the sensitive nodes. However, in practical applications, PCB layout is difficult to fully consider the influence of RF radiation on the audio signal path, and some RF energy will still be coupled to the audio signal path to form audible TDD Noise. Therefore, AW87565 features a unique RF radiation suppression circuit, a shielding layer inside the chip, effectively prevent high frequency energy into RF chip, to ensure that the drive single of the amplifier provided to the speaker will not be affected by the antenna RF radiation, thus avoiding the antenna RF Radiation caused by TDD Noise.

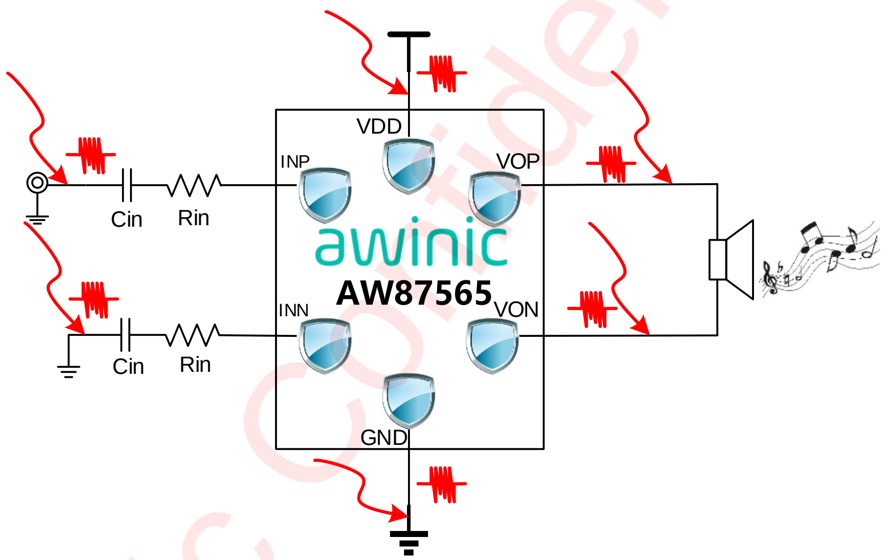


Figure 7 RF Radiation Coupling Graph

Class D Amplifier Without Filter

When the traditional Class D amplifier is in idle state of no input signal, the output will have the inverse square wave, it will directly above the load of the speaker, will form a large current power switch on the speaker, therefore we need to increase the LC filter to restore the analog audio signal at the amplifier output. The LC filter increase the cost and PCB layout area, while increase the power consumption, reduce the performance of THD+N.

The AW87565 features a Class D amplifier without a filter, eliminating the need for an output LC filter. In the idle state of no input signal, the two outputs (VOP, VON) of the amplifier are in-phase square waves and not generate idle switching currents on the speaker load. When the input signal is added to the input terminal, the duty ratio of the output is changed. The duty cycle of the VOP becomes larger and the duty cycle of the VON becomes smaller, and the difference value of the output forms the differential amplified signal on the speaker.

EEE

The AW87565 features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth, fully meet FCC Class B specification requirements.

POP-CLICK Suppression

The AW87565 features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

Automatic Recovery of Overcurrent Protection

AW87565 with automatic recovery of the output overcurrent protection function, when the overcurrent occurs, AW87565 internal protection circuit will chip off to ensure that the chip is not damaged, when the short-circuit fault is eliminated, the chip will automatically resume working without restarting.

I²C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	1.3			μs
3	t_{HIGH}	SCL High level Duration	0.6			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

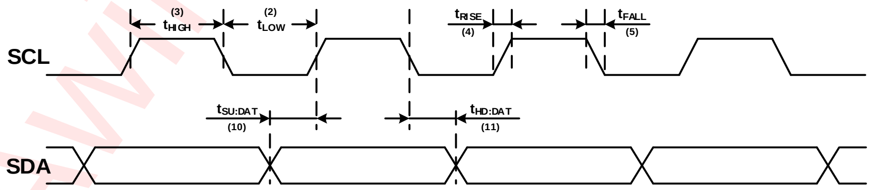


Figure 8 SCL and SDA timing relationships in the data transmission process

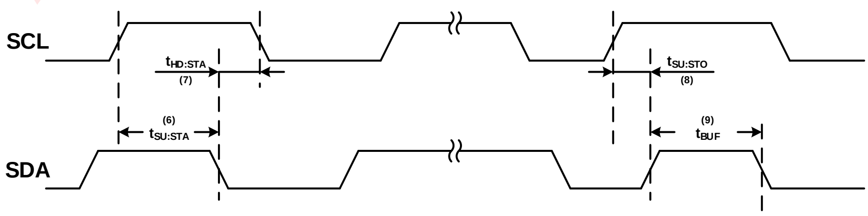


Figure 9 The Timing Relationship between START and STOP State

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. All data to start transmission and end of transmission requires the main device to issue START state and STOP status:

START state：The SCL maintain a high level, SDA from high to low level

STOP state：The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 10.

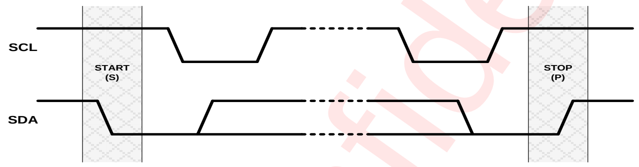


Figure 10 START and STOP State Generation Process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 11. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 12. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

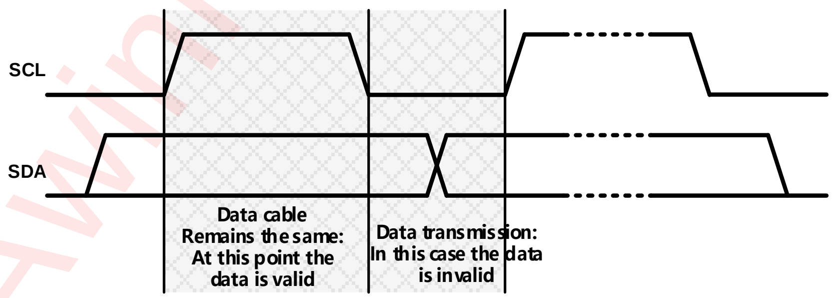


Figure 11 The Data Transfer Rules on the I2C Bus

The whole process of actual data transmission is shown in Figure 12. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

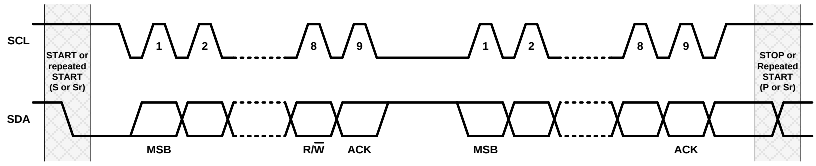


Figure 12 Data Transmission on the I²C Bus

I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW87565 as the slave device, the transmission process in accordance with the following steps, as shown in Figure 13:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW87565 register address to which the first data byte will written；

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW87565, within AW87565 each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.

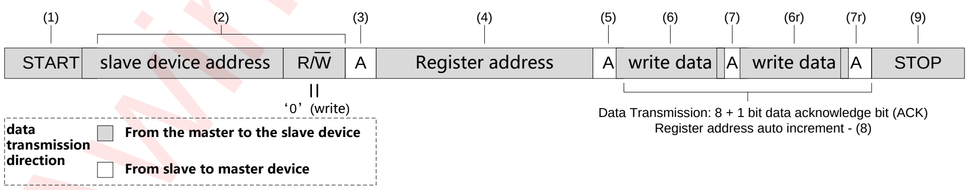


Figure 13 Writing Process (Data Transmission Direction Remains the Same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW87565 as the slave device, the transmission process carried out by following steps listed in Figure 14:

Master device asserts a start condition;

Master device transmits the 7 bits address of AW87565, and followed by a "read / write" flag ($R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device sends the 8bit address that the AW87565 register needs to read the data;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START.

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again.

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not.

The master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully.

AW87565 automatically increment register address once after the slave sent each acknowledge bit (ACK).

The master device generates the STOP state to end the data transmission.

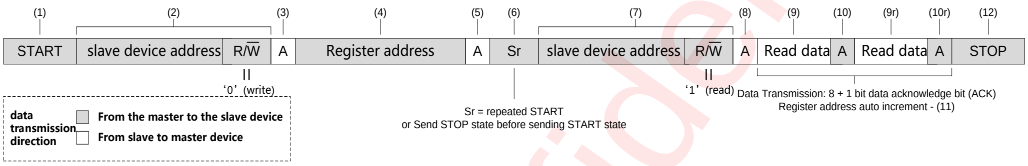


Figure 14 Reading Process (Data Transmission Direction Remains the Same)

Register Configuration

Device Address

AW87565's I²C address is 10110A2A1, as shown in Table 1, in order to avoid conflict with other I²C devices address, you can connect AD pin to GND，SCL，SDA，VDD to set the value of A2 and A1, respectively. The permitted I²C addresses are 0x58(7bit) through 0x5B (7-bit). The address information is as shown in Table 2.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	1	1	0	A2	A1	R/W

Table1 AW87565 Address Byte

AD pin	A2	A1	I²C address (7-bit)
Connects to GND	0	0	0x58
Connects to SCL	0	1	0x59
Connects to SDA	1	0	0x5A
Connects to VDD	1	1	0x5B

Table 2 AW87565 Address selection

Register List

Write AA to the 00 register of the AW87565 to reset the register

ADDR	NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	ID	IDCODE								0xC2
0x01	SYSCTRL	IIC_WEN		EN_SW	-	EN_BOOST	EN_PA	-	-	0x1C
0x02	BSTOVR	-	-		BST_VOUT					0x31
0x03	PEAKLIMIT	-	-			BST_IPEAK				0x19
0x04	ADPSET	-	-	ADP_BOOST_MODE			SET_BOOST_VTH2			0xD4
0x05	PAG	-	-		-	-	PA_GAIN			0xC5
0x06	AGC1PA	PD_AGC1	AGC1_OUTPUT_LEVEL				AGC1_ATT_TIME			0x49
0x07	AGC2PA	-	AGC2_OUTPUT_POWER				AGC2_ATT_TIME			0x1A
0x08	AGC3PA	-	-	-	PD_AGC3	AGC3_OUTPUT_POWER				0x23
0x09	AGC3P	AGC3_REL_TIME			AGC3_ATT_TIME			-		0x4E
0x17	OFFTIME	-	-	-	-	-	BST_OUT_VTH0			0x41
0x59	SYSST	UVLO_S	-	BST_OVP_S	BST_OVP2_S	BST_SCP_S	PA_OC_S	OT160_S	ADP_BOOST_S	0xBE
0x60	SYSINT	UVLO_I	-	BST_OVP_I	BST_OVP2_I	BST_SCP_I	PA_OC_I	OT160_I	ADP_BOOST_I	0xBE

Any register address which is not shown and all reserved bits are reserved for debugging and testing purposes. Changing their values may affect the normal function of the power amplifier; Reading them will get any possible values. The following lists specific information about all visible registers, including default values and programmable ranges.

Register Detailed Description

SYSST REGISTER (ADDRESS: 0x59 Default:0xBE)

Bit	Name	R/W	Description
7	UVLO_S	RO	Chip under voltage lock out detected
			0: normal operation
			1: vbat under voltage
6	Reserved	RO	Not used
5	BST_OVP_S	RO	Boost over voltage protection detected
			0: normal operation
			1: boost over voltage protection
4	BST_OVP2_S	RO	Boost heavy load protection detected
			0: normal operation
			1: boost heavy load protection detected
3	BST_SCP_S	RO	Boost short circuit detected
			0: normal operation
			1: boost short circuit protection detected
2	PA_OC_S	RO	PA over current protection detected
			0: normal operation
			1: PA over current protection detected

1	OT160_S	RO	PA segment over tempreture protection detected
			0: normal operation
			1: PA over tempreture protection detected
0	ADP_BOOST_S	RO	ADP BOOST detected
			0: direct mode
			1: boost mode

SYSINT REGISTER (ADDRESS: 0x60 Default:0xBE)

Bit	Name	R/W	Description
7	UVLO_I	R	Chip under voltage lock out detected
			0: normal operation
			1: vbat under voltage
6	Reserved	RO	Not used
5	BST_OVP_I	R	Boost over voltage protection detected
			0: normal operation
			1: boost over voltage protection
4	BST_OVP2_I	R	Boost heavy load protection detected
			0: normal operation
			1: boost heavy load protection detected
3	BST_SCP_I	R	Boost short circuit detected
			0: normal operation
			1: boost short circuit protection detected
2	PA_OC_I	R	PA over current protection detected
			0: normal operation
			1: PA over current protection detected
1	OT160_I	R	PA segment over tempreture protection detected
			0: normal operation
			1: PA over tempreture protection detected
0	ADP_BOOST_I	R	ADP BOOST detected
			0: direct mode
			1: boost mode

CHIP ID REGISTER (ADDRESS: 0x00 Default:0xC2)

I^2C Bit	Name	R/W	Default	Description
7:0	IDCODE	R	0XC2	Chip ID will be returned after read.

SYSTEM CONTROL (SYSCTRL) REGISTER (ADDRESS: 0x01 Default:0x1C)

Bit	Symbol	R/W	Description	Default
7:6	IIC_WEN	RW	IIC write enable：	00
			10: enable IIC	
			Others: disable	
5	EN_SW	RW	Chip software enable	0
			0: Disable	
			1: Enable	
4	Reserved	RW	Not used	1
3	EN_BOOST	RW	Boost Enable.	1
			0: Disable	
			1: Enable	
2	EN_PA	RW	Class D PA Enable.	1
			0: Disable	
			1: Enable	
1:0	Reserved	RW	Not used	00

BOOST OUTPUT VOLTAGE (BSTOVR) REGISTER (ADDRESS: 0x02 Default:0x31)

Bit	Symbol	R/W	Description		Default
7:5	Reserved	RW	Not used		001
4:0	BST_VOUT	RW	BOOST output voltage set：		10001
			00110: 6.25V	01101: 8.0V	
			00111: 6.5V	01110: 8.25V	
			01000: 6.75V	01111: 8.5V	
			01001: 7.0V	10000: 8.75V	
			01010: 7.25V	10001: 9.0V	
			01011: 7.5V	10010:9.25V	
			01100: 7.75V	10011:9.5V	
			Others: Reserved and Unused		

BOOST CONTROL (PEAKLIMIT) REGISTER (ADDRESS: 0x03 Default:0x19)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Not used	0001
3:0	BST_IPEAK	RW	Boost peak current limiter threshold	1001
			0000: 1.75A	
			0001: 2.0A	
			0010: 2.25A	
			0011: 2.5A	
			0100: 2.75A	

			0101: 3.0A	
			0110: 3.25A	
			0111: 3.5A	
			1000: 3.75A	
			1001: 4.0A	
			1010: 4.25A	
			1011: 4.5A	
			1100: 4.75A	
			Others: Reserved and Unused	

ADP MODE SET(ADPSET) REGISTER (ADDRESS: 0x04 Default:0xD4)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	11
5:3	ADP_BOOST_MODE	RW	Mode control	010
			000: RCV	
			001: force boost	
			010: MD1(OSB_OSD)	
			011: MD2(TSB_TSD)	
			111: MDM(MSB_MSD)	
			Others: Reserved and Unused	
2:0	SET_BOOST_VTH2	RW	Boost threshold Po2	100
			000: 1.2W	
			001: 1.4W	
			010: 1.6W	
			011: 1.8W	
			100: 2.0W	
			101: 2.2W	
			110: 2.4W	
			111: 2.6W	

CLASSD GAIN CONTROL(PAG) REGISTER (ADDRESS: 0x05 Default:0xC5)

Bit	Symbol	R/W	Description		Default
7:3	Reserved	RW	Not used		11000
2:0	PA_GAIN	RW	PA Input Signal Gain		101
			000:0dB		
			001: 3dB		
			010: 6dB		
			011: 9dB	RCV_MODE=1	
			011: 12dB	RCV_MODE=0	

			100: 15dB	
			101: 18dB	
			110: 21dB	
			111: 24dB	

AGC1 CONTROL REGISTER (ADDRESS: 0x06 Default:0x49)

Bit	Symbol	R/W	Description	Default
7	PD_AGC1	RW	Disable fastest level AGC 0: Enable 1: Disable	0
6:3	AGC1_OUTPUT_LEVEL	RW	AGC1 output Level. 0000: 6V 0001: 5.2V 0010: 5.4V 0011: 5.6V 0100: 5.8V 0101: Reserved 0110: 6.2V 0111: 6.4V 1000: 6.6V 1001: 6.8V 1010: 7V 1011: 7.2V 1100: 7.4V 1101: 7.6V 1110: 7.8V 1111: 8V	1001
2:0	AGC1_ATT_TIME	RW	Fastest Level AGC attack time 000: 0.04ms/dB 001: 0.08ms/dB 010: 0.16ms/dB 011: 0.32ms/dB 100: 0.02ms/dB 101: 0.01ms/dB 110: 0.005ms/dB 111: 0.005ms/dB	001

CLASS D AGC2 OUTPUT POWER (AGC2) REGISTER (ADDRESS: 0x07 Default:0x1A)

Bit	Symbol	R/W	Description		Default
7	Reserved	RW	Not used		0
6:3	AGC2_OUTPUT_POWER	RW	AGC2 output Power Level.		0011
			0000: 1.0W@8 ohm	0000: 1.33W@6 ohm	
			0001: 1.2W@8 ohm	0001: 1.60W@6 ohm	
			0010: 1.4W@8 ohm	0010: 1.87W@6 ohm	
			0011: 1.6W@8 ohm	0011: 2.13W@6 ohm	

			0100: 1.8W@8 ohm	0100: 2.4W@6 ohm	
			0101: 2.0W@8 ohm	0101: 2.67W@6 ohm	
			0110: 2.2W@8 ohm	0110: 2.93@6 ohm	
			0111: 2.4W@8 ohm	0111: 3.2W@6 ohm	
			1000: 2.6W@8 ohm	1000: 3.47W@6 ohm	
			1001: 2.8W@8 ohm	1001: 3.73W@6 ohm	
			1010: 3.0W@8 ohm	1010: 4.0W@6 ohm	
			1011: AGC2 OFF	1011: AGC2 OFF	
			Others: Reserved and Unused		
2:0	AGC2_ATT_TIME	RW	AGC2 total attack time. 000: 0.16ms/dB 001: 0.32ms/dB 010: 0.64ms/dB 011: 2.56ms/dB 100: 10.24ms/dB 101: 40.96ms/dB 110: 82ms/dB 111: 164ms/dB		010

CLASS D AGC3 PARAMETER (AGC3) REGISTER (ADDRESS: 0x08 Default:0x23)

Bit	Symbol	R/W	Description		Default
7:5	Reserved	RW	Not used		001
4	PD_AGC3	RW	Disable AGC3 0: Enable 1: Disable		0
3:0	AGC3_OUTPUT_POWER	RW	Speaker Protection output Power Level.		0011
			0000: 0.5W@8 ohm	0000: 0.67W@6 ohm	
			0001: 0.6W@8 ohm	0001: 0.8W@6 ohm	
			0010: 0.7W@8 ohm	0010: 0.93W@6 ohm	
			0011: 0.8W@8 ohm	0011: 1.07W@6 ohm	
			0100: 0.9W@8 ohm	0100: 1.20W@6 ohm	
			0101: 1.0W@8 ohm	0101: 1.33W@6 ohm	
			0110: 1.1W@8 ohm	0110: 1.47W@6 ohm	
			0111: 1.2W@8 ohm	0111: 1.6W@6 ohm	
			1000: 1.3W@8 ohm	1000: 1.73W@6 ohm	
			1001: 1.4W@8 ohm	1001: 1.87W@6 ohm	
			1010: 1.5W@8 ohm	1010: 2.0W@6 ohm	
			1011: 1.6W@8 ohm	1011: 2.13W@6 ohm	

			1100: 1.7W@8 ohm	1100: 2.27W@6 ohm	
			1101: 1.8W@8 ohm	1101: 2.4W@6 ohm	
			1110: 1.9W@8 ohm	1110: 2.53W@6 ohm	
			1111: 2.0W@8 ohm	1111: 2.67W@6 ohm	

CLASS D AGC3 OUTPUT POWER (AGC3) REGISTER (ADDRESS: 0x09 Default:0x4E)

Bit	Symbol	R/W	Description	Default
7:5	AGC3_REL_TIME	RW	Total 13.5dB release time. 000: 5.12ms/dB 001: 10.24ms/dB 010: 20.48ms/dB 011: 40.96ms/dB 100: 81.92ms/dB 101: 163.84ms/dB 110: 327.68ms/dB 111: 655.36ms/dB	010
4:2	AGC3_ATT_TIME	RW	Total 13.5dbB attack time. 000: 1.28ms/dB 001: 2.56ms/dB 010: 10.24ms/dB 011: 40.96ms/dB 100: 82ms/dB 101: 164ms/dB 110: 328ms/dB 111: 656ms/dB	011
1:0	Reserved	RW	Not used	10

ADP MD2 SET REGISTER (ADDRESS: 0x17 Default:0x41)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RW	Not used	01000
2:0	BST_OUT_VTH0	RW	fist step voltage of two step boost mode 000: 6.5V 001: 6.75V 010: 7.0V 011: 7.25V 100: 7.5V 101: 7.75V 110: 8.0V 111: 8.25V	001

APPLICATION INFORMATION

EXTERNAL COMPONENTS

BOOST INDUCTOR SELECTION

Selecting inductor needs to consider Inductance, size, magnetic shielding, saturation current and temperature current.

a) Inductance

Inductance value is limited by the boost converter's internal loop compensation. In order to ensure phase margin sufficient under all operating conditions, recommended 1μH inductor.

b) Size

For a certain value of inductor, the smaller the size, the greater the parasitic series resistance of the inductor DCR, the higher the loss, corresponds to the lower efficiency.

c) Magnetic shielding

Magnetic shielding can effectively prevent the inductance of the electromagnetic radiation interference. It is much better to choose inductance with magnetic shielding in the application of EMI sensitive environment.

d) Saturation current and temperature rise of current

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, on the one hand, since the magnetic core begins to saturate, inductance value will decline; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. In general, the current value is defined as the saturation current I_{SAT} when the inductance value drops to 70%; the current value is defined as temperature rise current I_{RMS} when inductance temperature rise 40°C.

For particular applications, need to calculate the maximum I_{L_PEAK} and I_{L_RMS}, which is a basis of selecting the inductor. When VDD = 4.2V, VBST=9.5V, R_L = 8Ω，amplifier R_{DSON} = 250mΩ, when THD = 1% (the maximum power without distortion), the output power is calculated as follows:

$$P_{OUT} = \frac{\left(V_{OUT} \times \frac{R_L}{R_L + R_{DSON}}\right)^2}{2 \times R_L} = \frac{\left(9.5 \times \frac{8}{8+0.25}\right)^2}{2 \times 8} = 5.2W$$

In such a large output power, the overall efficiency of the power amplifier is typically 80%, in order to calculate the maximum average current $I_{MAX\_AVG\_VDD}$ and maximum peak current $I_{MAX\_PEAK\_VDD}$ drawn from VDD:

$$I_{MAX\_AVG\_VDD} = \frac{P_{OUT}}{V_{DD} \times \eta} = \frac{5.2}{4.2 \times 0.8} A = 1.55A$$

$$I_{MAX\_PEAK\_VDD} = 2 \times I_{MAX\_AVG\_VDD} = 3.1A$$

If inductor DCR is 50mΩ, the inductor power loss at this time is:

$$P_{DCR,LOSS} = 1.5 \cdot I^2_{MAX\_AVG\_VDD} \cdot DCR = 1.5 \times 1.55^2 \times 0.05W = 180mW$$

Wherein the coefficient 1.5 is the square of the ratio of the sine wave current RMS value and average value (there is no consideration of the impact of the inductor ripple, the actual DCR loss will be even greater). If the loss which is resulting from DCR is less than 1% at maximum efficiency (P_{OUT} = 2.5W, η = 80%), then:

$$I_{AVG\_VDD} = \frac{P_{OUT}}{V_{DD} \times \eta} = \frac{2.5}{4.2 \times 0.8} = 0.74A$$

$$DCR = \frac{P_{DCR,LOSS}}{1.5 \cdot I^2_{AVG\_VDD}} \le 0.01 \times \frac{P_{OUT}}{1.5 \cdot I^2_{AVG\_VDD} \cdot \eta} = \frac{0.01 \times 2.5}{1.5 \times 0.74^2 \times 0.8} \Omega = 38m\Omega$$

According to the working principle of the Boost, we can calculate the size of the inductor current ripple ΔI_L:

$$\Delta I_L = \frac{V_{DD} \times (V_{OUT} - V_{DD})}{V_{OUT} \times f \times L} = \frac{4.2 \times (9.5 - 4.2)}{9.5 \times 2 \times 10^6 \times 1 \times 10^{-6}} A = 1.17A$$

Thus, the maximum peak inductor current I_{L_PEAK} and maximum effective inductor current I_{L_RMS} is:

$$I_{L\_PEAK} = I_{MAX\_PEAK\_VDD} + \frac{\Delta I_L}{2} = 3.1A + \frac{1.17}{2} A = 3.69A$$

$$I_{L\_RMS} = \sqrt{I^2_{MAX\_PEAK\_VDD} + \frac{\Delta I_L^2}{12}} = \sqrt{3.1^2 + \frac{1.17^2}{12}} A = 3.12A$$

From the above calculation results:

1) For typical DCR about 38mΩ inductance, the efficiency loss caused by around1.5%;
2) In practice, the maximum output power of the amplifier is likely to reach 5.2W in an instant, so the selected inductor saturation current I_{SAT} requires more than the maximum inductor peak current I_{L_PEAK};
3) In some cases, if the I_{L_PEAK} calculated according to the above method is greater than the set of input inductor current limit value I_{LIMIT}, shows the power amplifier is restricted by inductance input current limit, the actual maximum output power is less than the calculated value, the measured value shall prevail, and I_{SAT} need greater than the set current limiting value I_{LIMIT}, and cannot be less than 3.1A;
4) For example, under different conditions, the typical method of selecting I_{SAT} in the following table:

VDD(V)	VBST(V)	R_L(Ω)	I_{LIMIT}(A)	Efficiency(η) (%)	P_O(W)	I_{L_PEAK}(A)	Inductor saturation current I_{SAT} minimum value (A)
4.2	9.5	8	4	80	5.2	3.69	4.0
4.2	9.5	6	4.5	75	6.1	4.45	4.5

5) As the result of the action of AGC，amplifier will not work long hours at maximum power without distortion, the actual average inductor current is far less than the maximum inductor current effective I_{L_RMS}, so when selecting the inductor, the inductor temperature rise current is not usually a limiting factor;
6) Inductor Selection example: the inductor package size is 252012, inductance value is 1μH, DCR Typical value is 47mΩ, the typical saturation current I_{SAT} is 4.2A, the typical temperature rise current I_{RMS} is 3.0A, suitable for VDD=4.2V, VBST=9.5V, speaker impedance R_L=8Ω, inductor input current limit I_{LIMIT}= 4A. If you choose I_{SAT} or I_{RMS} of the inductance is too small, it is possible to cause the chip don't work properly, or the temperature of the inductance is too high.

Inductance value	size	DCR（Ω）	I_{SAT}（A）	I_{RMS}（A）
1uH	2.5×2.0×1.2mm	0.047	4.2	3.0

CAPACITOR SELECTION

BOOST CAPACITOR SELECTION

The output capacitor of charge pump is usually within the range 0.1μF~47μF, It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically BaTiO3), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

a) temperature stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive. X5R capacitance change within ±15% in temperature range of 55°C to 85°C, X7R capacitance change within ±15% in temperature range of -55°C~125°C. The output capacitance of the AW87565's charge pump recommends X5R ceramic capacitors.

b) Voltage Stability

Class II type capacitor has poor voltage stability ——Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take for TDK C series X5R for example, its pressure voltage value is 16V or 25V, the package size is 0805, 1206 or 0603, the capacitance value is 10μF. The capacitor's voltage stability of different types of capacitor is as shown below:

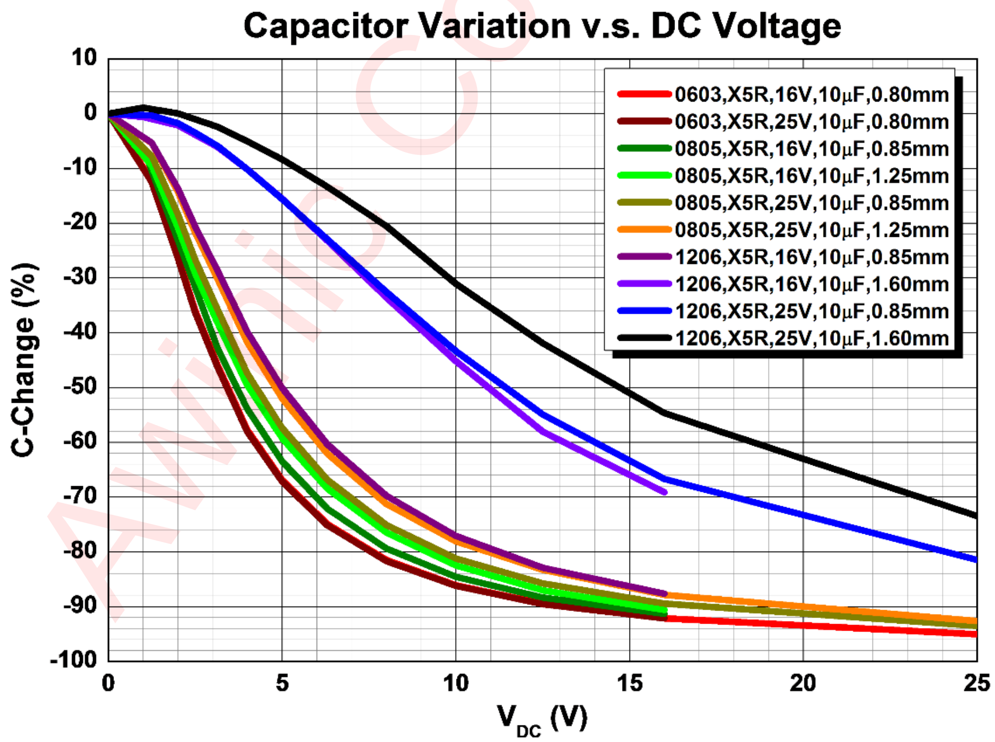


Figure 15 Different Types of Capacitive Voltage Stability

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. The higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of smaller package size (0603) capacitor change affected by the pressure value is very small.

In AW87565 typical applications, it is necessary to ensure the output value of the VBST capacitor ≥3.6μF when VBST=9.5V.

Take the following capacitances as the Boost of the output capacitor for example:

value	material	size (mm^3)	rated voltage (V)	quantity	value@9.5V
10uF	X5R	1.60×0.80×0.80 (0603)	16	3	5.4uF
10uF	X5R	2.00×1.25×1.25 (0805)	25	2	5.4uF

As for the different manufacturers' capacitors, it's important to determine the type and quantity of the capacitors through the capacitor voltage stability data provided by the manufacturer.

INPUT CAPACITOR- C_{in} (INPUT HIGH-PASS CUTOFF FREQUENCY)

The input capacitors and input resistors form a high-pass filter to filter out the DC component of the input signal. The -3dB frequency points of the high pass filter is shown below：

$$f_H(-3dB) = \frac{1}{2\pi \times R_{intotal} \times C_{in}} (Hz)$$

The selection of a smaller Cin capacitor in the application helps to filter out 217Hz noise, which comes from the input coupling, and the smaller capacitor is advantageous to reduce the pop-click noise when the power amplifier turn on.Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise. A capacitor value deviation of 10% or better capacitance is recommended.

Take typical application as an example(Gain=18dB), the input high-pass cutoff frequency is calculated as below:

$$f_H(-3dB) = \frac{1}{2\pi \times R_{intotal} \times C_{in}} = \frac{1}{2\pi \times 5k\Omega \times 330nF} (Hz) = 96.46Hz$$

SUPPLY DECOUPLING CAPACITOR（C_S）

A good decoupling capacitor can improve the efficiency and the best performance of the power amplifier. At the same time, in order to get good high frequency transient performance, the ESR value of the capacitor should be as small as possible. In AW87565 applications, low ESR (equivalent-series-resistance) X7R or X5R ceramic capacitors are recommended. Generally, 10μF ceramic capacitors are used to bypass the VDD to the ground, and the decoupling capacitor should be placed as close to the VDD chip as possible in the layout. If you want to filter out low-frequency noise better, you need to add a 10μF or greater decoupling capacitor depending on your application. Meanwhile, a 33pF~0.1μF ceramic capacitor is placed on the pin of the power supply to filter the high frequency interference on the power supply. The capacitor should be placed as close as possible to the pin3 and inductor.

OUTPUT BEADS, CAPACITORS, TVS

Using EEE technology, in the class K mode, the AW87565 can also meet the FCC CLASS B specification requirements. It is recommended to Use ferrite chip beads and capacitors if device near the EMI sensitive circuits, there are long leads from amplifier to speaker, placed as close as possible to the output pin.

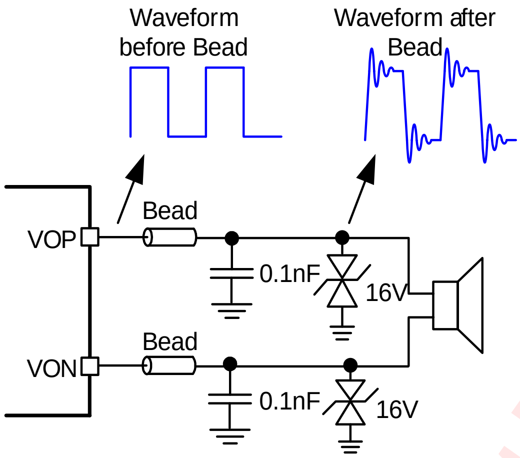


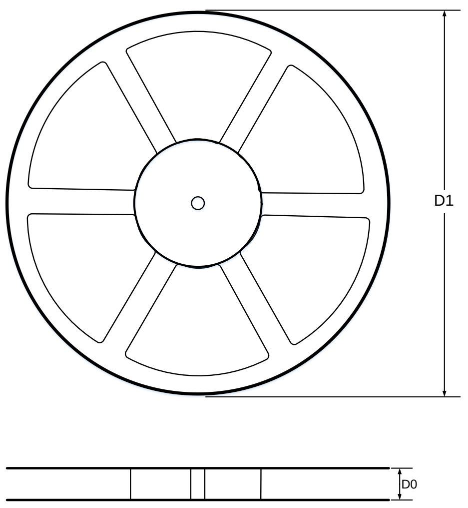
Figure 16 Ferrite Chip Bead and Capacitor

Amplifier output is a square wave signal. The voltage across the capacitor will be much larger than the VBST voltage after increasing the bead capacitor. It suggested the use of rated voltage above 16V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 16V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 16V capacitor, but quiescent current will increase.

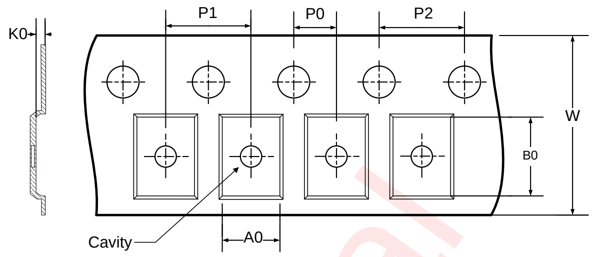
Power amplifier output PWM signals of high voltage to VBST voltage, voltage to 9.5 V, will produce some ringing after bead capacitor, resulting in higher peak voltage. Recommended choose the operating voltage of 16V TVS.

Tape And Reel Information

REEL DIMENSIONS

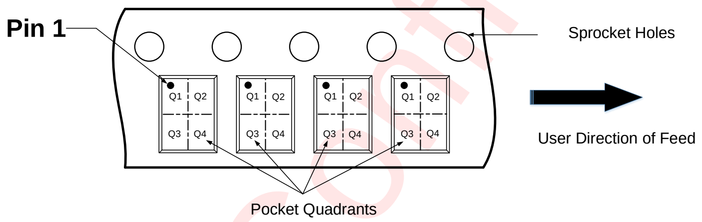


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



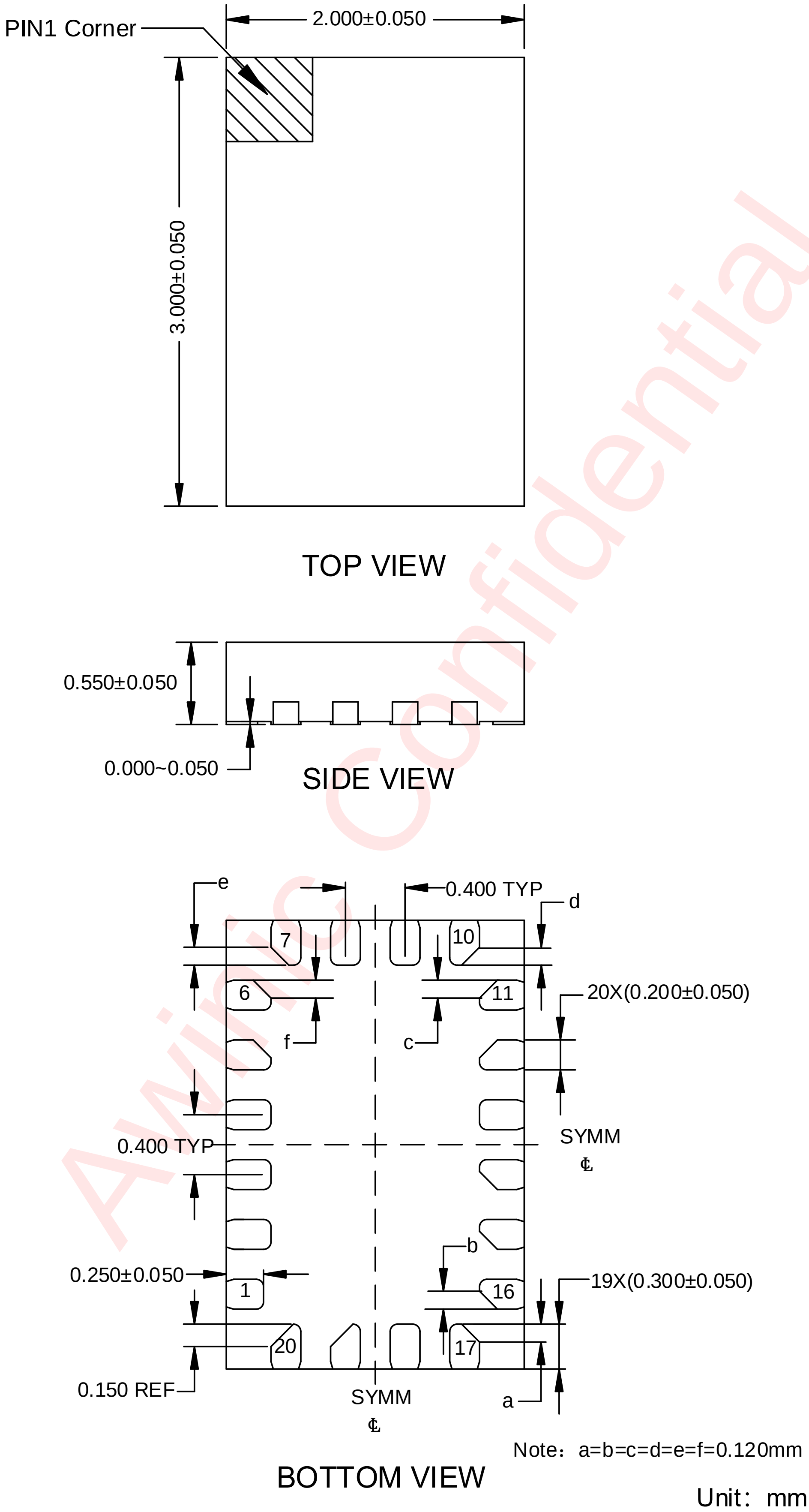
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

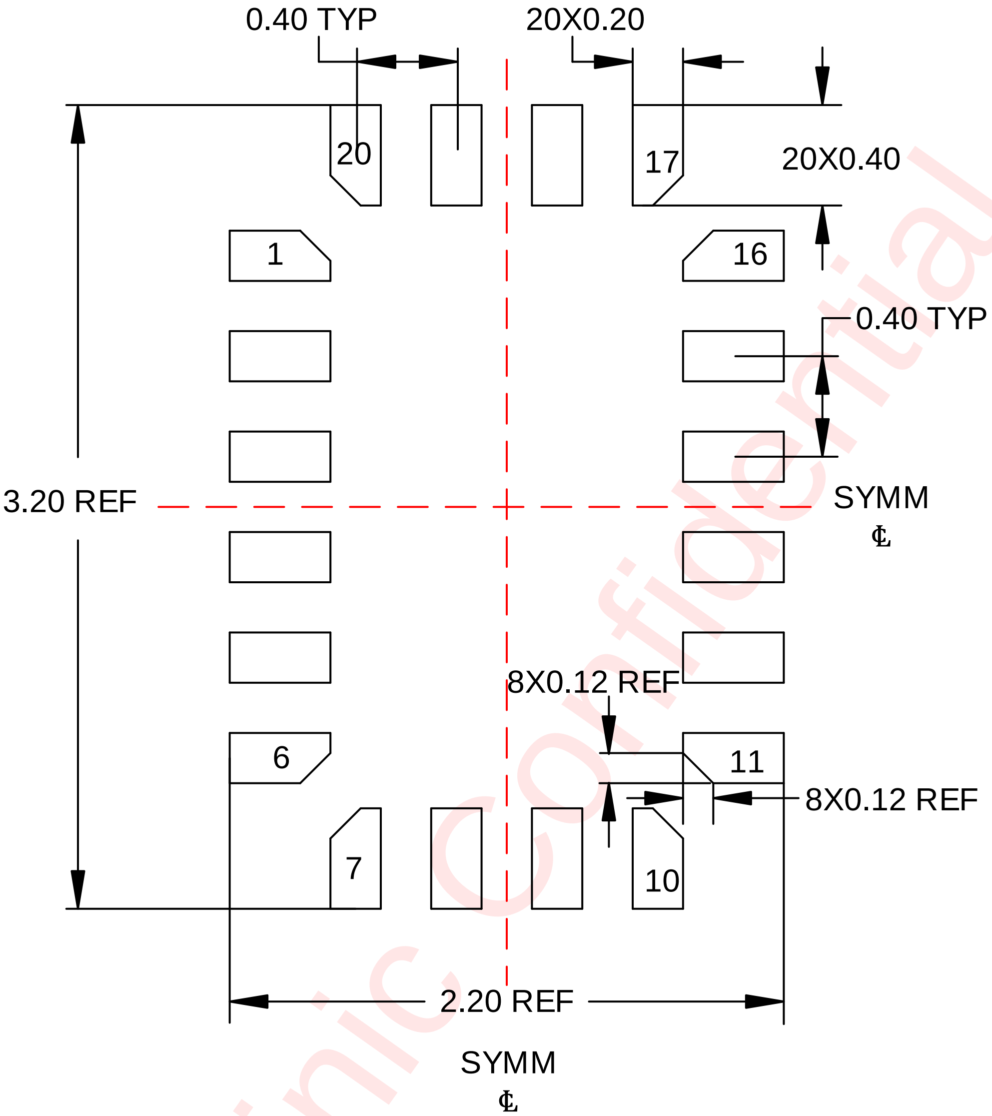
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	2.3	3.3	0.75	2	4	4	12	Q1

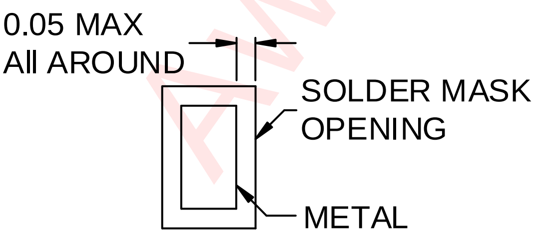
All dimensions are nominal

Package Description

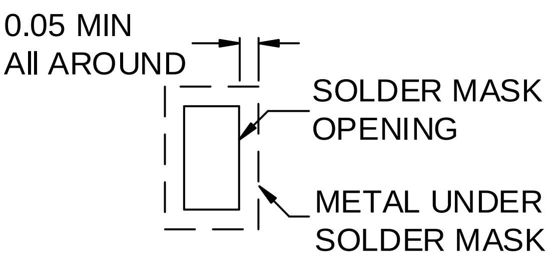


Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2023	AW87565 datasheet V1.0
V1.1	Feb. 2024	1. Add ESD Data; 2. Add Single-end Power Data; 3. Modify Ipeak Data；
V1.2	Dec. 2024	Fixed some typical characteristics.
V1.3	Mar.2025	Fixed some register information.
V1.4	Apr.2025	Add some register information.

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